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FIFO

# Modules

A diagram of a computer hardware system

Description automatically generated

**My Modules are the following:**

* FIFO\_RAM.v : Dual RAM Memory used as FIFO Memory.
* DATA\_SYNC.v: Double Flipflop Synchronizer to synchronize the Gray encoded Pointers.
* RD\_CONTRL.v: FIFO read pointer and Empty flag calculator.
* WR\_CONTRL.v: FIFO write pointer and FULL flag calculator.
* FIFO.v : The Top Module Wrapper.

# Problem

**First the FIFO Problem:**

        Reading Frequency = 40 MHz  "Reading Period = 25ns"

        Writing Frequency = 100 MHz "Writing Period = 10ns"

        Writing Data Packet size = 10 Byte

**Solution:**

        Time needed to write One Byte = 10ns

        Time needed to write the Packet = 100 ns

        number of packets to be read = 100/25 = 4 byte

        then min FIFO Depth = 10 - 4 = 6 byte

# Testbench

Testbench Idea is to send one packet of size 10 bytes and receive it from another size

A screenshot of a computer

Description automatically generated