

1. Description

1.1. Project

Project Name	IPSS
Board Name	NUCLEO-F411RE
Generated with:	STM32CubeMX 6.12.1
Date	12/11/2024

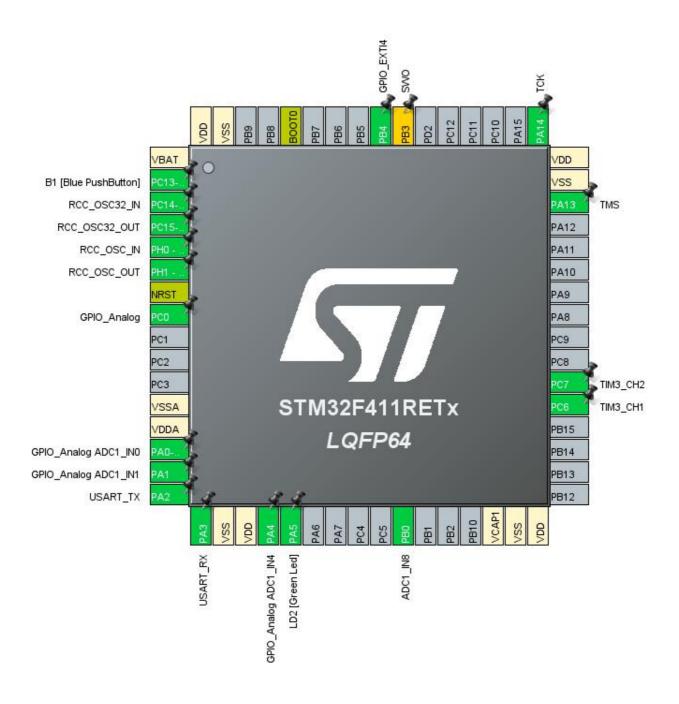
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



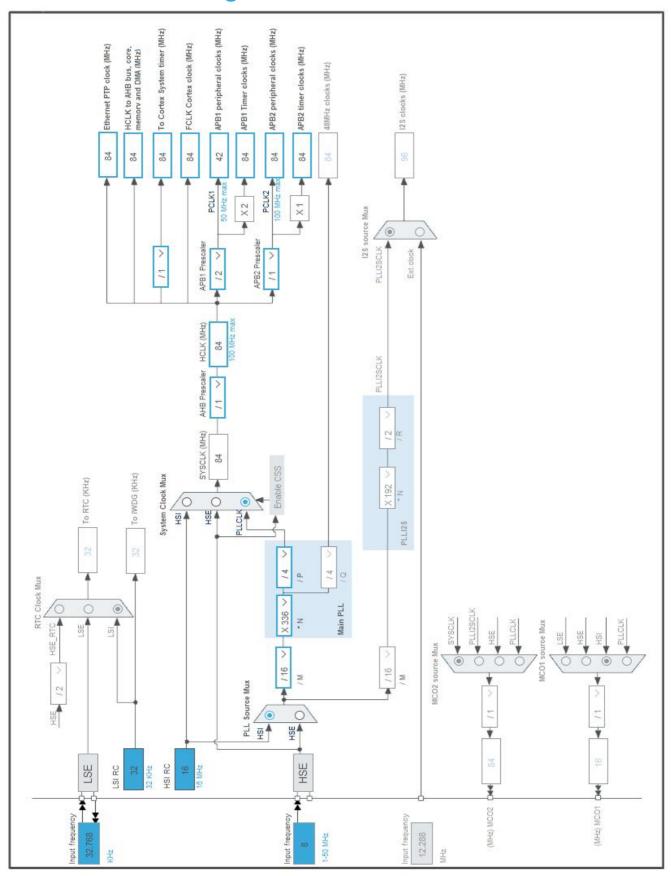
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP64	(function after		Function(s)	
201101	reset)		r directori(e)	
4	,	Dawar		
2	VBAT PC13-ANTI_TAMP	Power I/O	CDIO EVII12	P4 [Plue PuehPutten]
3			GPIO_EXTI13	B1 [Blue PushButton]
	PC14-OSC32_IN	1/0	RCC_OSC32_IN	
4	PC15-OSC32_OUT	1/0	RCC_OSC32_OUT	
5	PH0 - OSC_IN	1/0	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset	CDIO Angles	
8	PC0 *	I/O	GPIO_Analog	
12	VSSA	Power		
13	VDDA	Power	0000 4 1 4004 100	
14	PA0-WKUP	1/0	GPIO_Analog, ADC1_IN0	
15	PA1	I/O	GPIO_Analog, ADC1_IN1	
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	GPIO_Analog, ADC1_IN4	
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
26	PB0	I/O	ADC1_IN8	
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
37	PC6	I/O	TIM3_CH1	
38	PC7	I/O	TIM3_CH2	
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 **	I/O	SYS_JTDO-SWO	SWO
56	PB4	I/O	GPIO_EXTI4	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

^{*} The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated		

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411RETx
Datasheet	DS10314_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	1.7

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

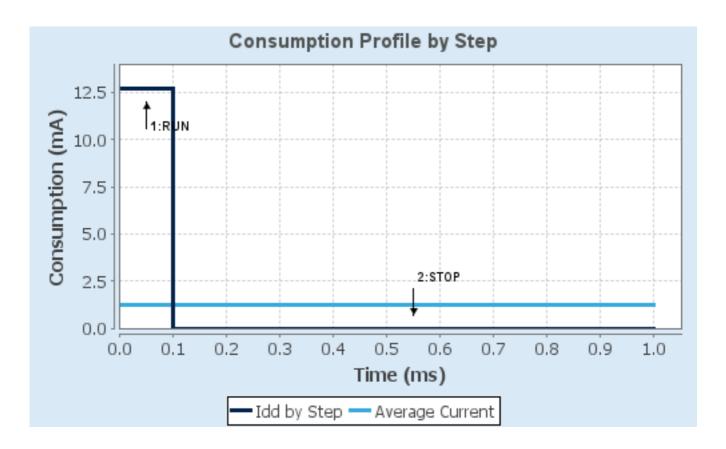
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash- PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	103.99	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19	Average DMIPS	125.0 DMIPS
	days, 6 hours	-	

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	IPSS
Project Folder	C:\Users\ajara\OneDrive\Documents\PROJET_ENIB\IPS\IPSS
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART2_UART_Init	USART2
5	MX_ADC1_Init	ADC1
6	MX_TIM3_Init	TIM3

3. Peripherals and Middlewares Configuration

3.1. ADC1 mode: IN0 mode: IN1 mode: IN4 mode: IN8

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment
Scan Conversion Mode Enabled

Continuous Conversion Mode Enabled *

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Enabled *

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 4

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel Channel 0
Sampling Time 3 Cycles
Rank 2 *

Channel 1 *

Sampling Time 3 Cycles

Rank 3 *

Channel 4 *

Sampling Time 3 Cycles
Rank 4 *

Channel 8 *

Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode

false

3.2. RCC

High Speed Clock (HSE): BYPASS Clock Source Low Speed Clock (LSE): Crystal/Ceramic Resonator

3.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

3.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

3.4. TIM3

Combined Channels: Encoder Mode

3.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
Encoder:	
Encoder Mode	Encoder Mode TI1 and TI2 *
Parameters for Channel 1	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
Parameters for Channel 2	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
3.5. USART2 Mode: Asynchronous 3.5.1. Parameter Settings: Basic Parameters:	
Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1
Advanced Parameters:	
Data Direction	Receive and Transmit
Over Sampling	16 Samples

^{*} User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	ТСК
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USART_RX
Single Mapped Signals	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
GPIO	PC13- ANTI_TAMP	ANITI TAMB	External Interrupt	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
			Mode with Falling			
			edge trigger detection			
	PC0	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	
	PA0-WKUP	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	
	PA1	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	
	PA4	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PB4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	

IPSS Project
Configuration Report

4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Medium *

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Circular *
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line4 interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
TIM3 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		

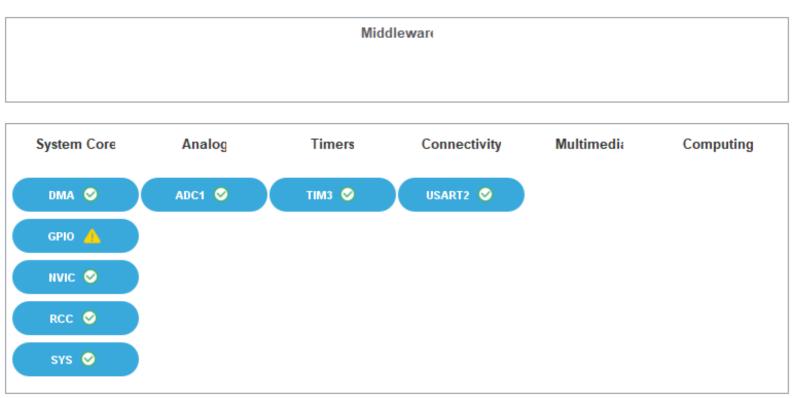
4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line4 interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true

* User modified value		

5. System Views

- 5.1. Category view
- 5.1.1. Current



6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f411_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f411_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f4-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

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