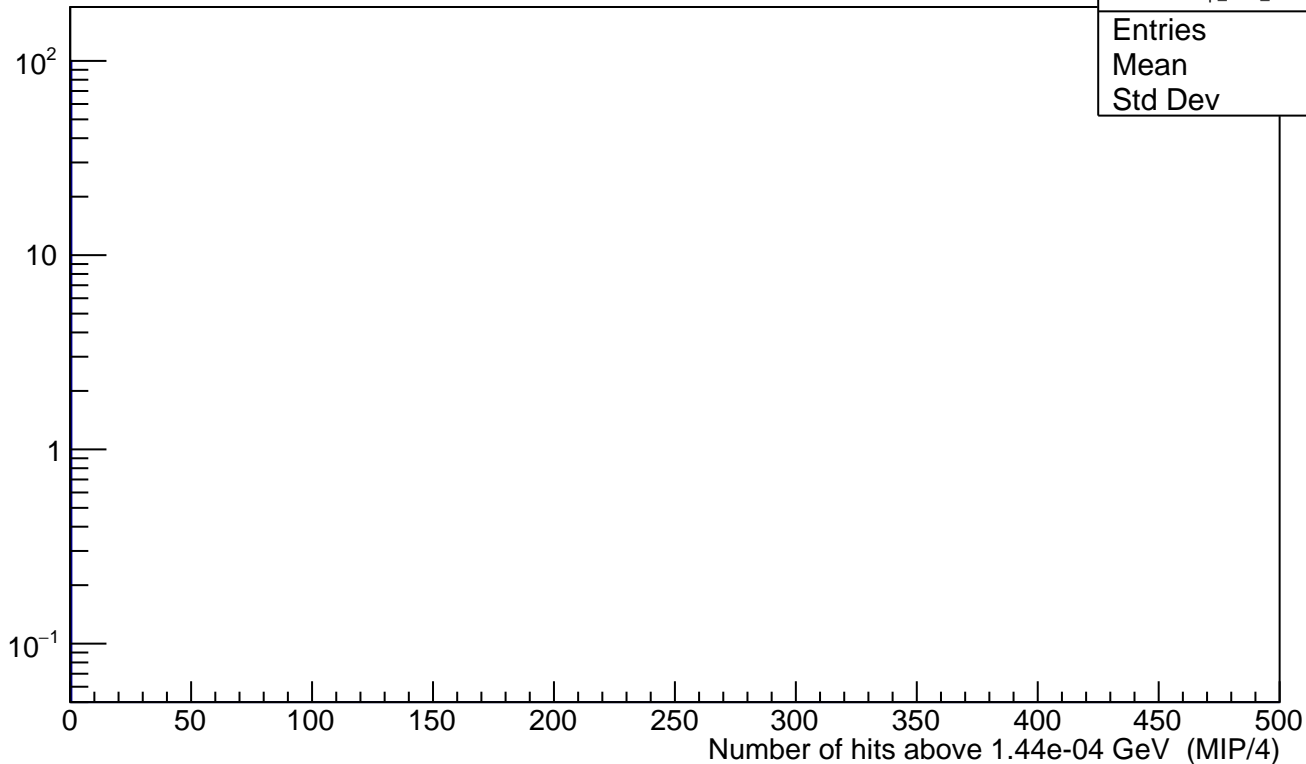


ScHCalEndcap_T0:3_L32:48

Number of Events



ScHCalEndcap_T0:3_L32:48_all_#hits	
Entries	100
Mean	0
Std Dev	0