

# Lab #3 Requirement

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## 1. Info about the requirement

The requirement is to design a 4x4 multiplier and to output the result on a 7-segment display. The design should be done using Verilog and the simulation should be done using ModelSim or Quartus. More details about the requirement can be found in the [Lab #3 Requirement](#) file.

## 2. Running the Simulation

The simulation can be run using ModelSim or Quartus. You would need to create a new project and add the [verilog files](#) to it. Then, you could simulate the design or the testbench.

## 3. Screenshots

In this section, I will show some screenshots of the simulation of the testbenches on ModelSim for the following modules:

1. [4x4 Multiplier](#)
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### 3.1. 4x4 Multiplier

When the testbench is simulated, the following waveform is generated:

+ /tb_multiplier_4x4/a	5	0	15	10	5
+ /tb_multiplier_4x4/b	10	0	15	0	15
+ /tb_multiplier_4x4/y	50	0		225	50

And the following is the output of the simulation:

#	a	b	y	expected
#	0000	0000	00000000	00000000
#	0000	1111	00000000	00000000
#	1111	0000	00000000	00000000
#	1111	1111	11100001	11100001
#	1010	0101	00110010	00110010
#	0101	1010	00110010	00110010

### 3.2. BCD Encoder

When the testbench is simulated, the following waveform is generated:

/tb_bcd/in	0	15	20	25	99	100	255	0
/tb_bcd/ones	0	5	0	5	9	0	5	0
/tb_bcd/tens	0	1	2	2	9	0	5	0
/tb_bcd/hundreds	0	0	0	0	0	1	2	0

And the following is the output of the simulation:

```
VSIM 28> run -all
# in      ones    tens    hundreds
# -----
# 0        0       0       0
# 1        1       0       0
# 2        2       0       0
# 3        3       0       0
# 9        9       0       0
# 10       0       1       0
# 15       5       1       0
# 20       0       2       0
# 25       5       2       0
# 99       9       9       0
# 100      0       0       1
# 255      5       5       2
# 0        0       0       0
```

### 3.3. Seven Segment Decoder

When the testbench is simulated, the following waveform is generated:

/tb_ssd/in	0	0	1	2	3	4	5	6	7	8	9
/tb_ssd/out	1000000	1000000	1111001	0100100	0110000	0011001	0010010	0000010	1111000	0000000	0010000

And the following is the output of the simulation:

```
# in      out      expected
# -----
# 0        1000000  1000000
# 1        1111001  1111001
# 2        0100100  0100100
# 3        0110000  0110000
# 4        0011001  0011001
# 5        0010010  0010010
# 6        0000010  0000010
# 7        1111000  1111000
# 8        0000000  0000000
# 9        0010000  0010000
```

### 3.4. Integrated Design

When the testbench is simulated, the following waveform is generated:

/tb_mult_integrated/a	15	0	1	4	2	9	10	2	15	
/tb_mult_integrated/b	15	0	1	2	3	0	1	2	5	9
/tb_mult_integrated/ss_ones	0010010	1000000				1111001	0000000	1000000	1111001	1000000
/tb_mult_integrated/ss_tens	0100100	1000000				1111001	0000000	1000000	0110000	0100100
/tb_mult_integrated/ss_hundreds	0100100	1000000						1111001	1000000	0100100

And the following is the output of the simulation:

```
VSIM 35> run -all
# a      b      a*b      ss_ones  ss_tens  ss_hundreds
# -----
# 0      0      0      1000000  1000000  1000000
# 0      1      0      1000000  1000000  1000000
# 0      2      0      1000000  1000000  1000000
# 0      3      0      1000000  1000000  1000000
# 1      0      0      1000000  1000000  1000000
# 1      1      1      1111001  1000000  1000000
# 4      2      8      0000000  1000000  1000000
# 2      5     10      1000000  1111001  1000000
# 9      9     81      1111001  0000000  1000000
# 10     10    100      1000000  1000000  1111001
# 2      15    30      1000000  0110000  1000000
# 15     2     30      1000000  0110000  1000000
# 15     15    225     0010010  0100100  0100100
```