Credit Hours System
CMPN111 Logic Design-2
Fall-2022

Cairo University
Faculty of Engineering

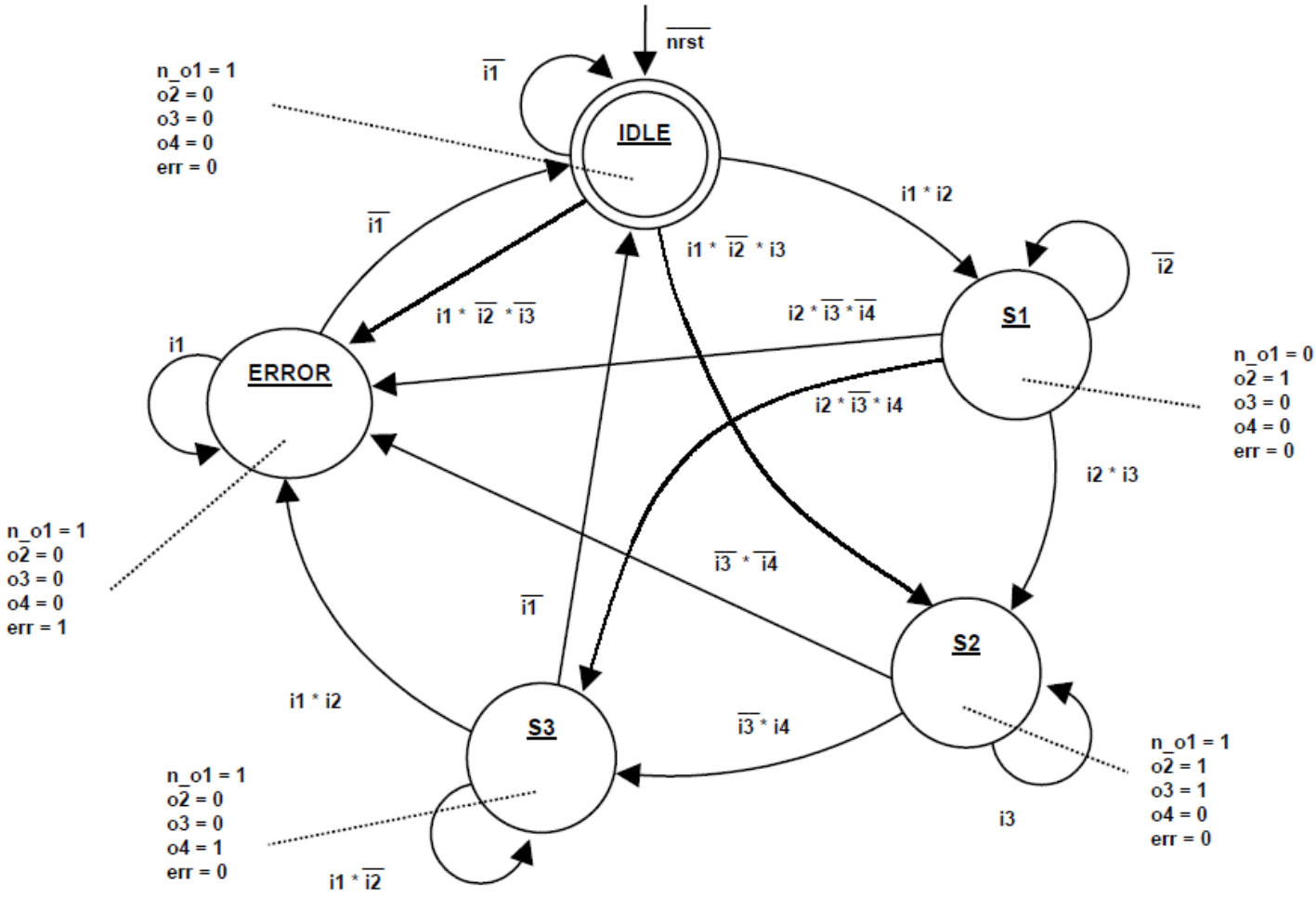
Lab Requirement 6
Finite State Machines

Finite State Machines

For this lab, you are required to implement the finite state machine(FSM) in the picture with your ID. Use Quartus and Verilog. Refer to Lab 06 slides for examples of how FSMs are implemented.

Use the testbench named with your ID to test your design.

Example FSM:



Deliverables

- Quartus project folder, compressed.