Design of 6T SRAM Cell using CMOS and Sky130 nm PDKs

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Abstract

As day by day, technology is being evolved and data science is becoming the most crucial topic of interest, more the data, more storage is needed. This paper consists of the design of a 6T SRAM cell that stores 1bit of data and also explains its READ and WRITE operation and explains the function of how it stores 1bit in a cell. This SRAM cell is designed with CMOS logic using the eSim EDA tool and SkyWater 130nm technology. The circuit diagram with its des description, waveform are given below for reference.

1. Reference Circuit Details

SRAM known as Static Random Access Memory also known as Read Write Memory has become a very crucial part of SOCs and ASIC. As the basic unit of SRAM is the SRAM cell, the need of SRAM cell is to perform stable and robust read/write operation in such a way that it consumes the least power and enhance the on-chip storage capacity. The given circuit demonstrates six transistor SRAM cell, out of which four transistors Q1, Q2, Q3, and Q4 forms a cross-coupled CMOS inverter, that itself becomes a memory. And remaining two nmos act as access transistors. These access transistors are connected to the bit line and bit line bar that are denoted by “BL & BLB”. And word line here denoted by “WL” is connected to access transistors when the word line is set on, the access transistors can be accessed and similarly when a word line is set off the content of the memory comes set to hold state as the access transistors are turned off, and as a result, the data will remain unchanged in the cell, for the write operation bit line and bit line bar acts as input lines and for reading operation these lines would act as output lines. We would design this circuit using open-source SkyWater 130nm PDKs sponsored by Google, here 130nm defines the minimum channel length of a transistor.

2. Reference Circuit

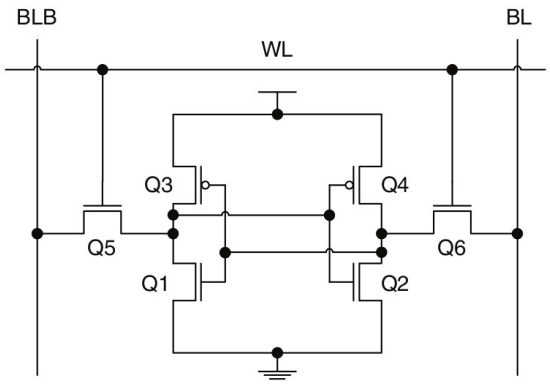

Figure 1: Reference circuit diagram[1].

3. Reference Circuit Waveforms

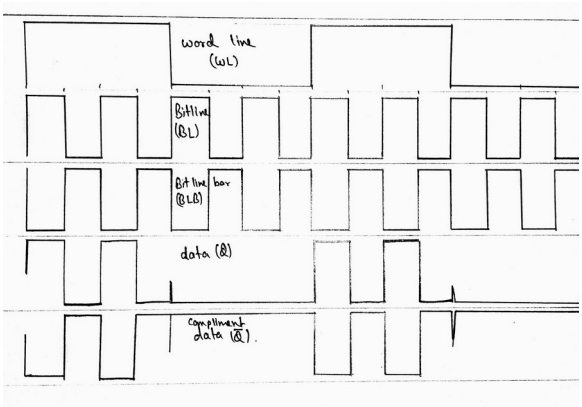

Figure 2: Reference waveform.

References

[1] Andrei Pavlov, Manoj Sachadev, CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies. https://link.springer.com/book/10.1007/978-1-4020-8363-1

[2] S.B. Lokesh1 " Design Of Read And Write Operations For 6t Sram Cell.” IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) , vol. 8, no. 1, 2018 https://www.iosrjournals.org/iosr-jvlsi.html