Digital Design and Verification

Lab Manual # 08 – Combinational Circuits using System Verilog

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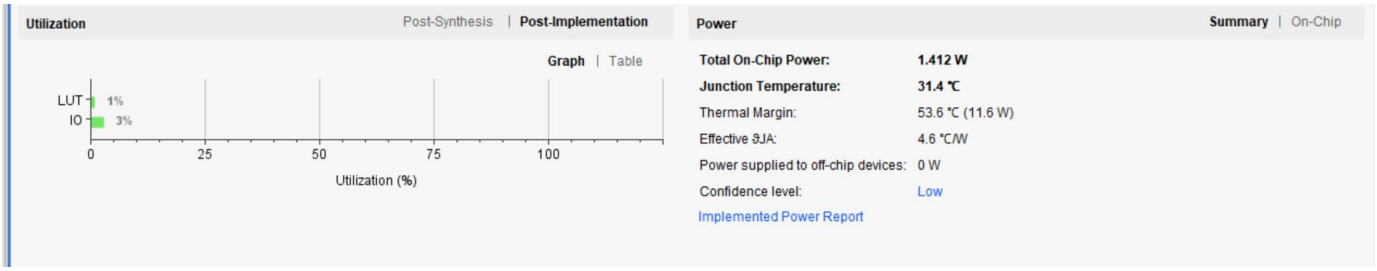
Instructor	*Hira Sohail*
Date	*30 July 2025*

1. In-Lab Tasks: (*Write your lab task & screenshots here*)

i. Task 1:

1.1

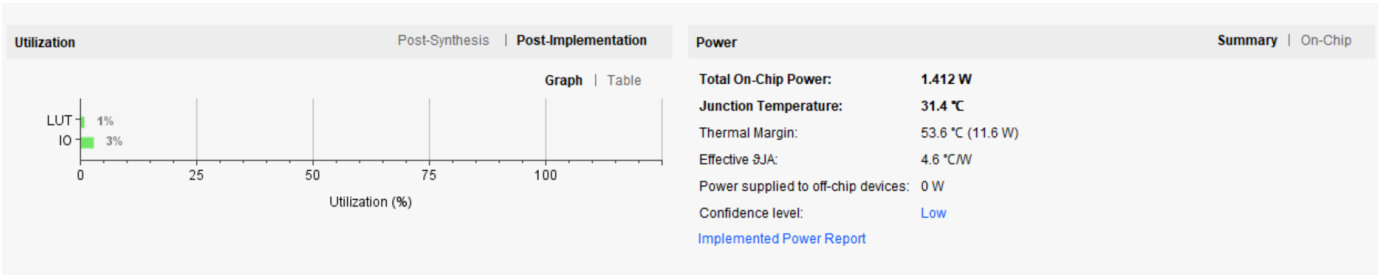
Power Report:



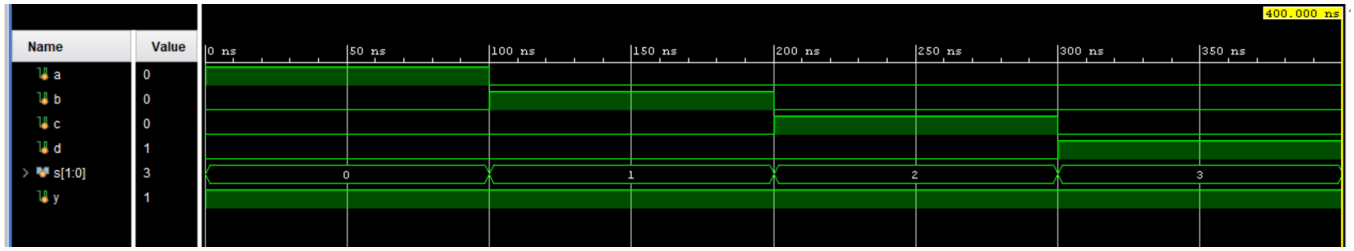
Waveform:

1.2

Power Report:

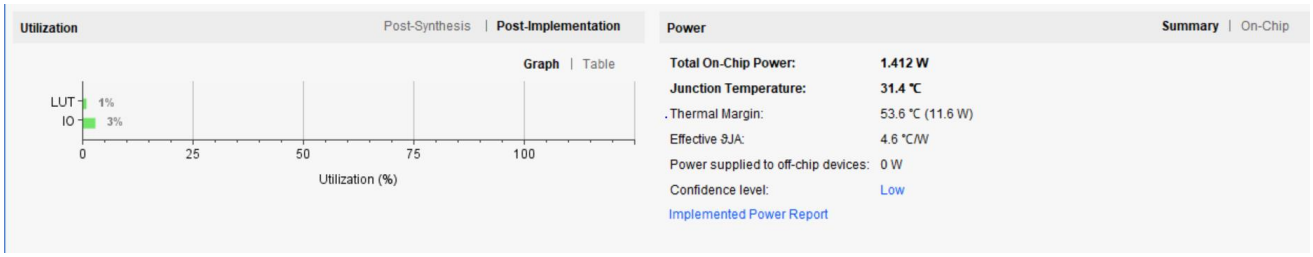


Waveform:

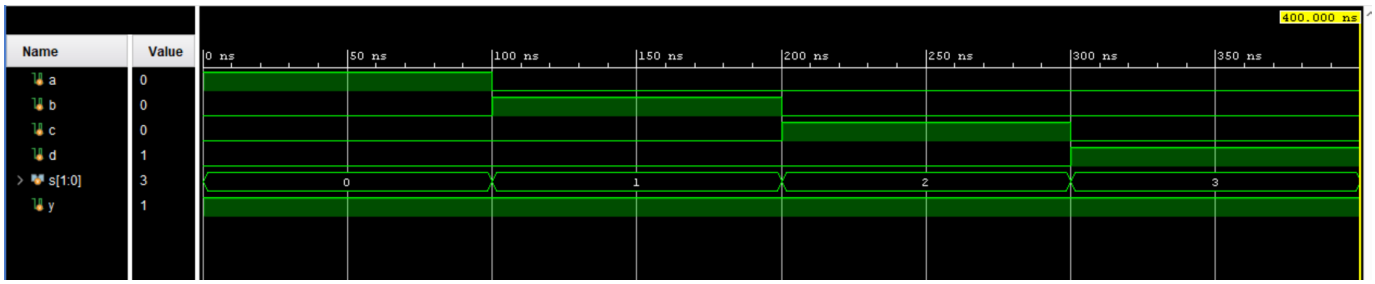


1.3

Power Report:



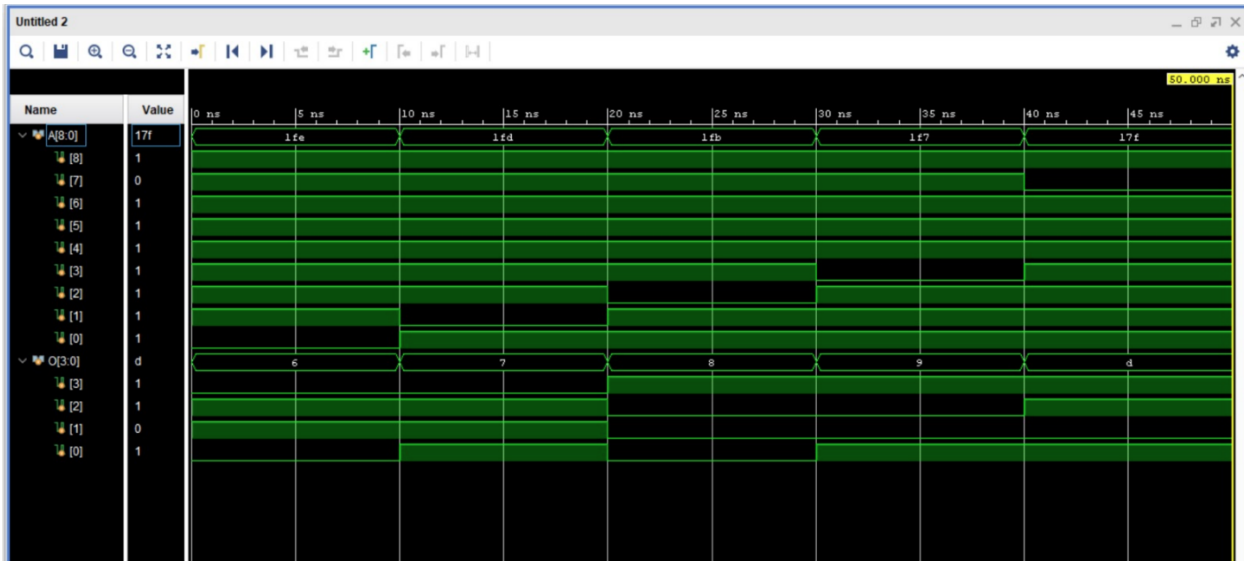
Waveform:



ii. Task 2:

Power Report:

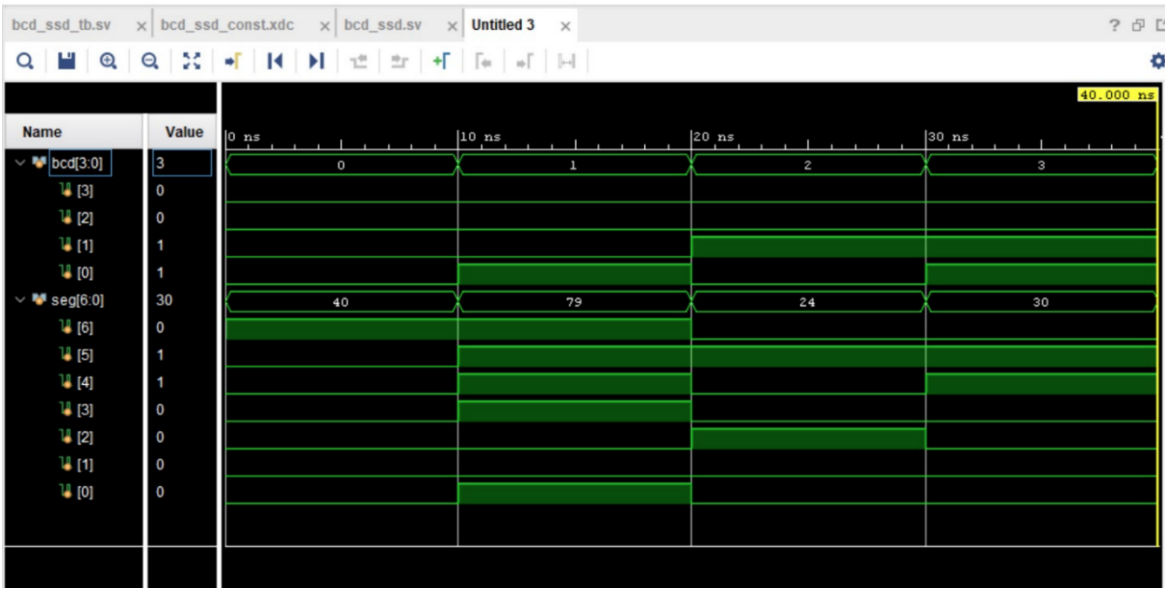
Waveform:



iii. Task 3:

Power Report:

Waveform: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bcd_ssd_const.xdc
bcd_ssd.sv
Untitled 3
40.000 ns
Name
Value
0 ns
10 ns
20 ns
30 ns
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[3]
0
[2]
0
[1]
1
[0]
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[6]
0
[5]
1
[4]
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[3]
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3
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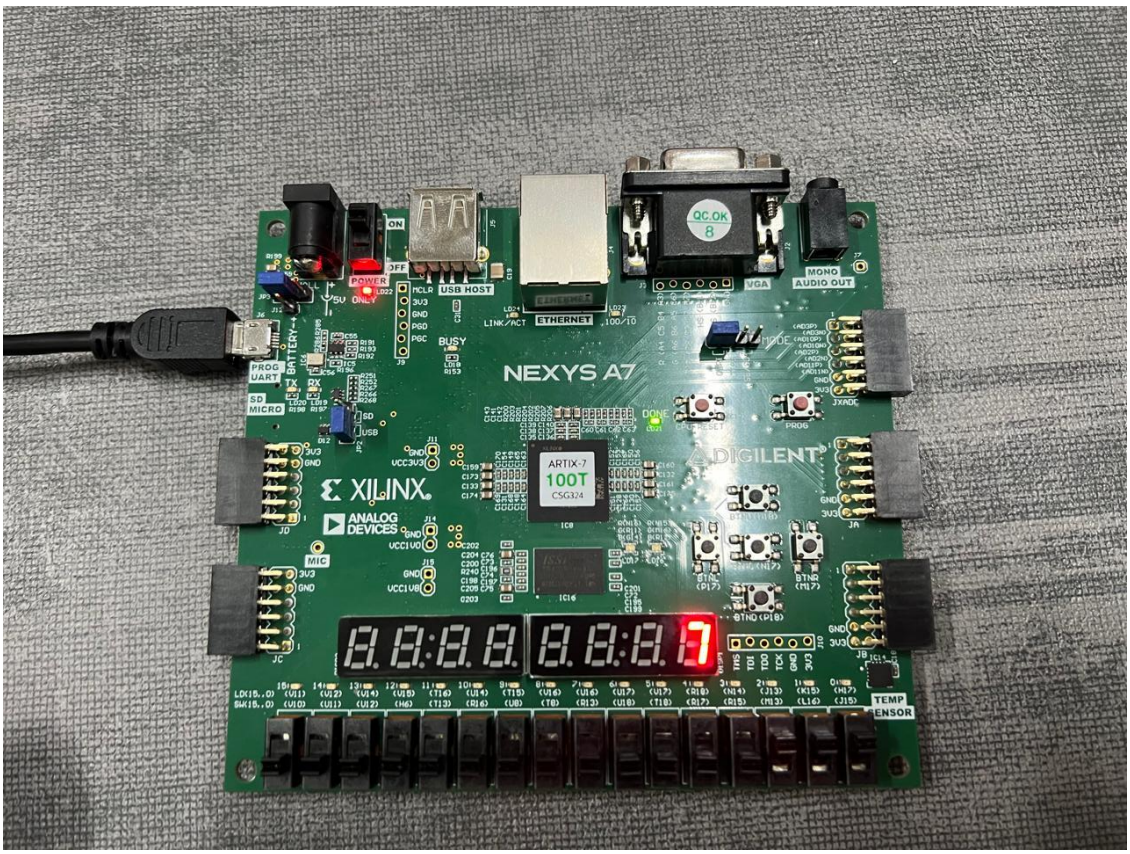
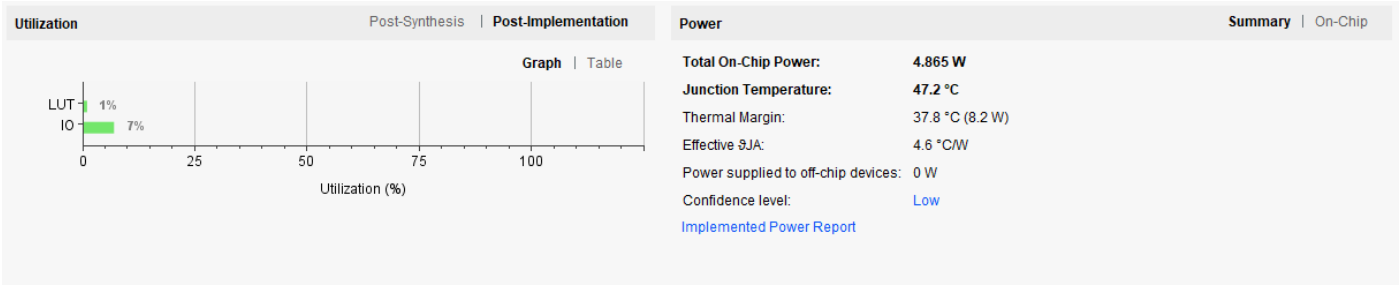
79
24
30

FPGA:

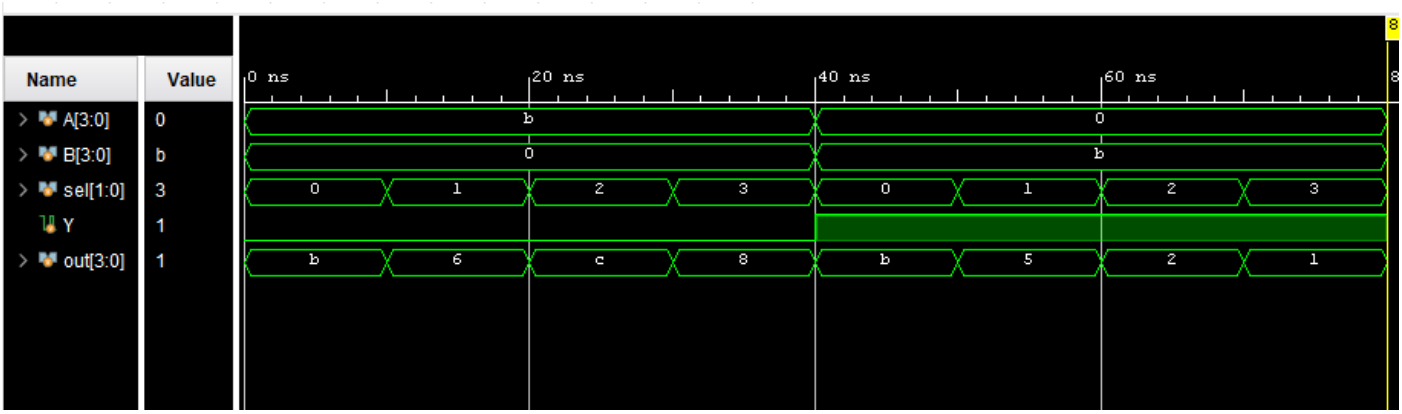

NEXYS A7
XILINX
DIGILENT
ARTIX-7
100T
ANALOG DEVICES
USB HOST
ETHERNET
VGA
MONO AUDIO OUT
TEMP SENSOR

iv. Task 4:

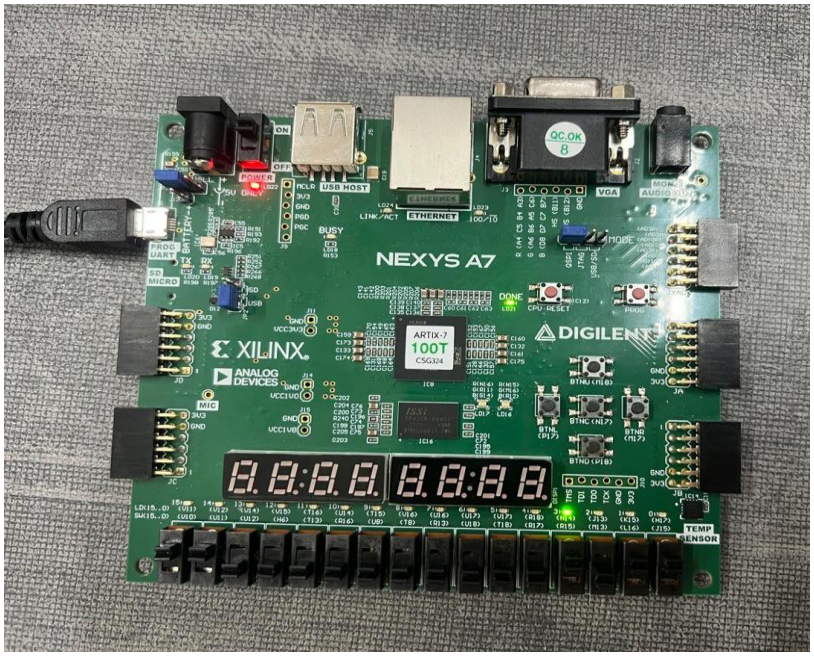
Power Report:



Waveform:

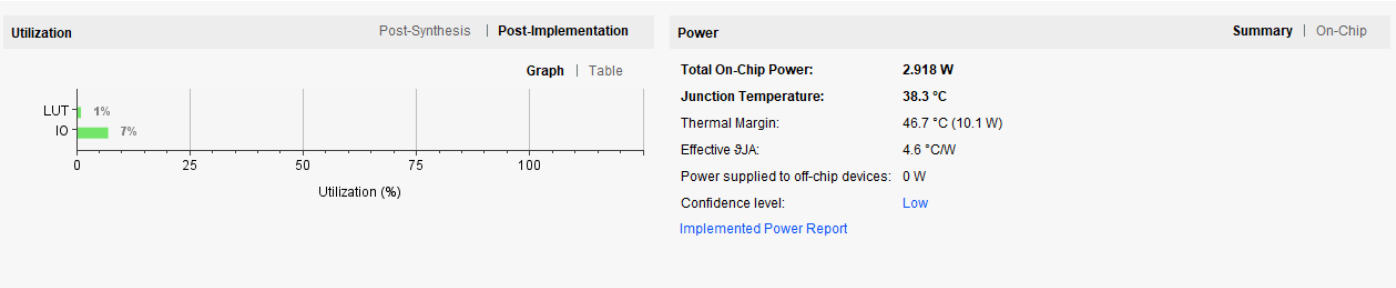


FPGA :

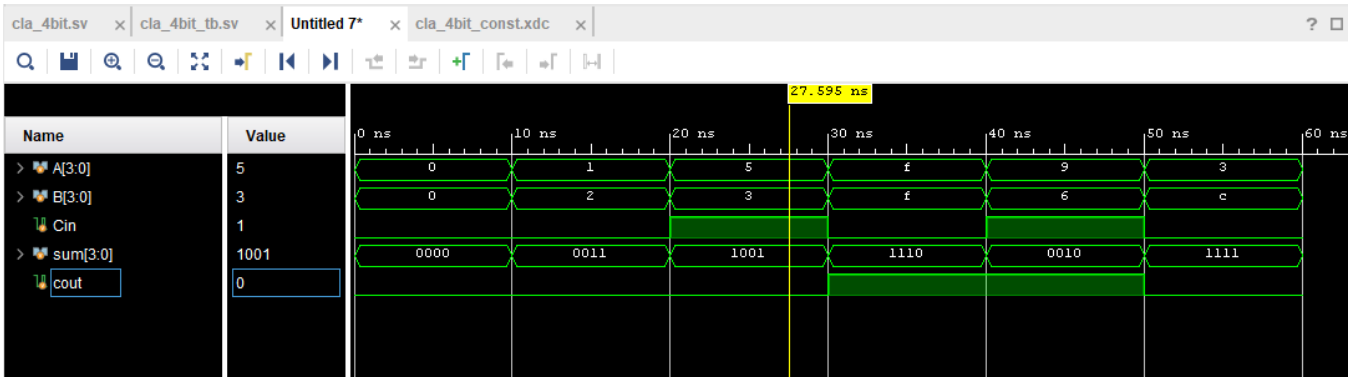


v. Task 5:

Power Report:



Waveform:



Critical Analysis:

I explored various essential digital logic components using three different modeling levels: behavioral, dataflow (gate-level), and structural. Starting with a 4x1 multiplexer, I implemented and understood how logic can be expressed differently based on the abstraction level. I then designed BCD to 7-segment decoder, decimal to BCD converter, a 4-bit barrel shifter using left shifts, and finally, the carry look-ahead adder logic. This lab significantly improved my understanding of combinational logic design, modular coding, and simulation in SystemVerilog.