



NUST CHIP DESIGN CENTRE

Digital Design Verification Training DLD

Task: 4-bit ALU

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| <u>Name</u> | <i><u>Khalil Rehman</u></i> |
| <u>Instructor</u> | <i><u>Hira Sohail</u></i> |
| <u>Date</u> | <i><u>30 July 2025</u></i> |

1. In-Lab Tasks:

i. Task 1:

SV file attached

ii. Task 2:

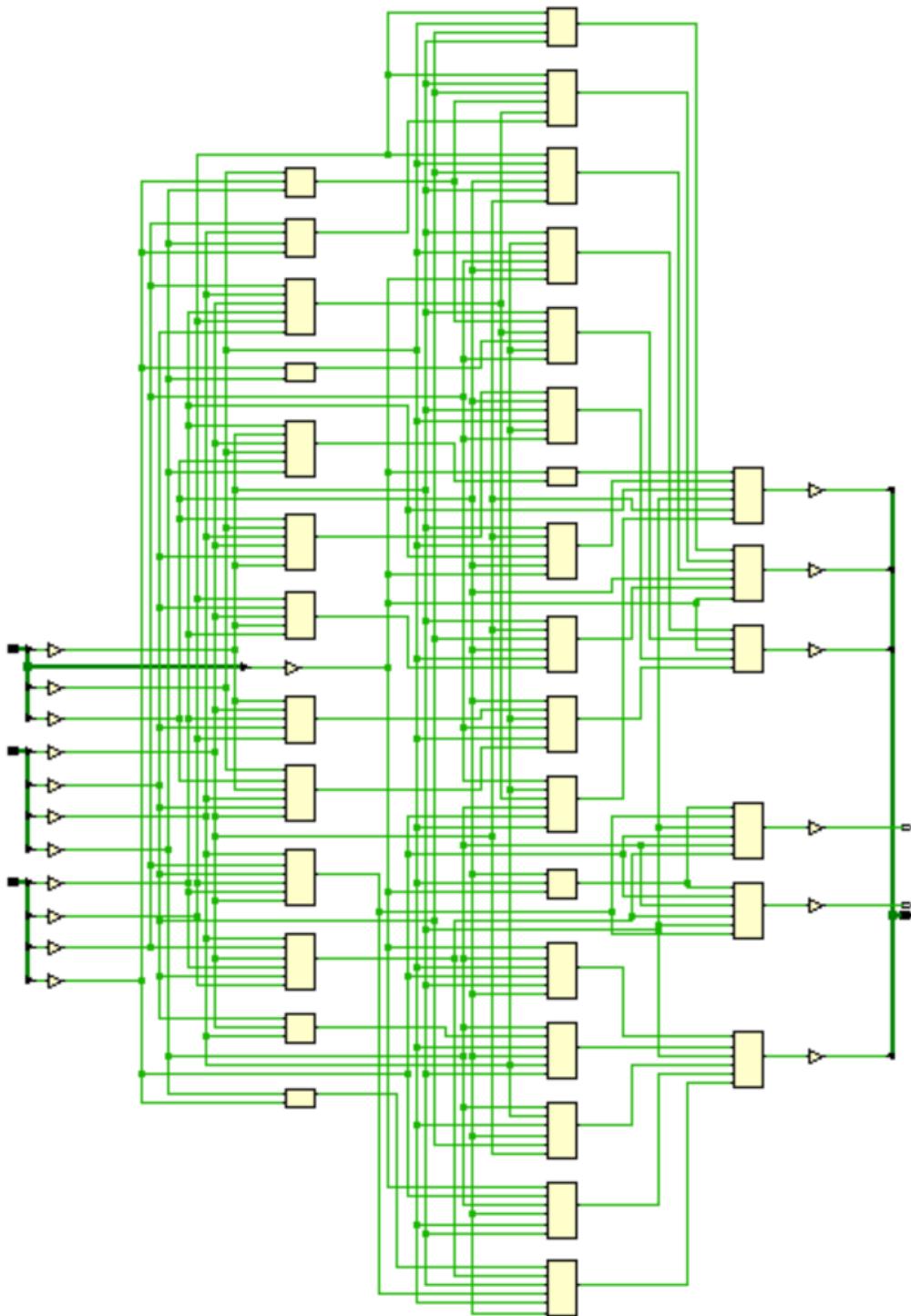
Testbench file attached

iii. Task 3:

Attached

iv. Task 4:

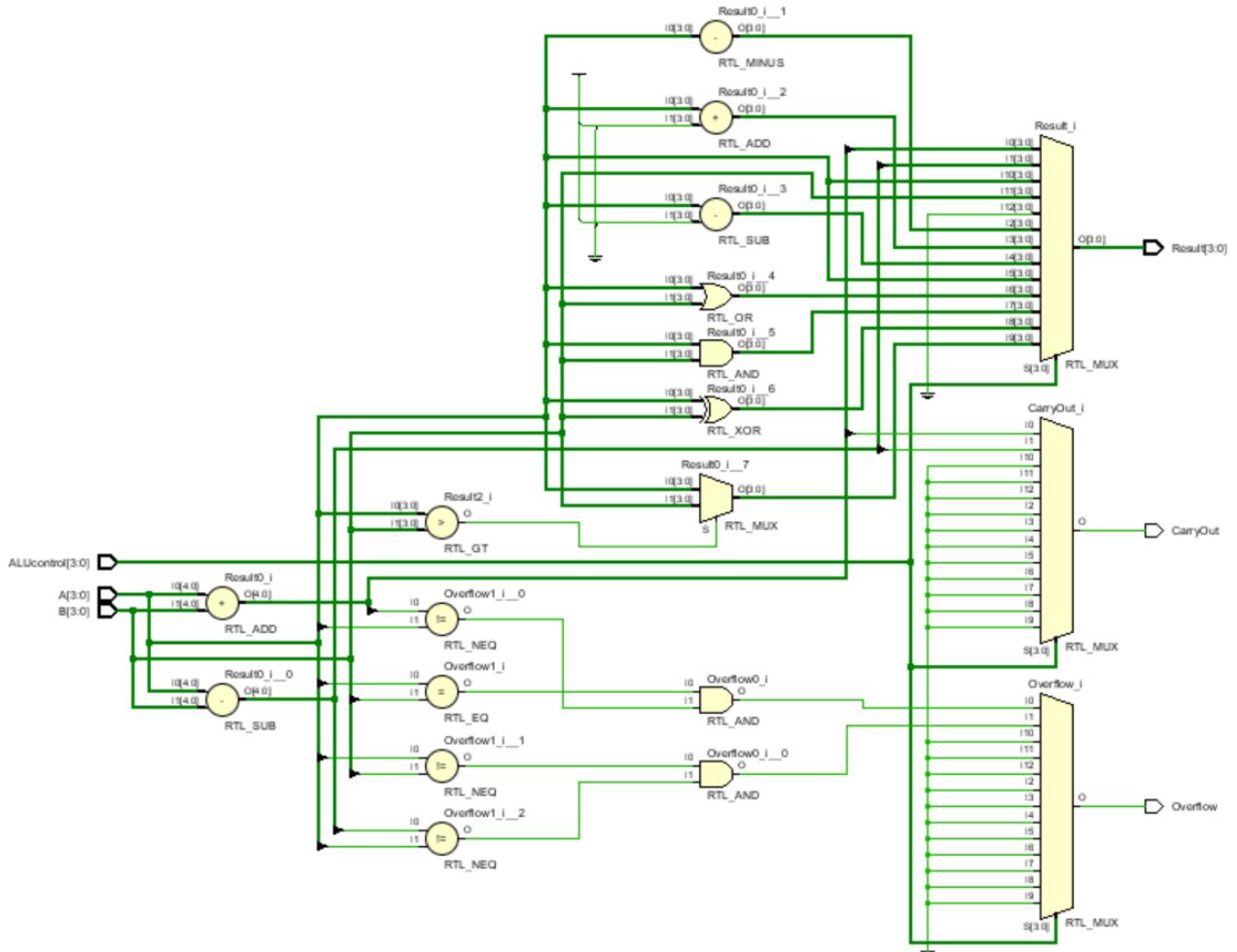
Attached



C / C++ Programming

v. Task 5:

RTL Diagram



vi. Task 6:

Power Report

| Utilization | Post-Synthesis | Post-Implementation | Power | Summary | On-Chip |
|--|----------------------|---|--------------------------|---------|---------|
| <p>LUT Utilization: 1% (Post-Synthesis), 9% (Post-Implementation)</p> <p>IO Utilization: 10% (Post-Synthesis), 10% (Post-Implementation)</p> | <p>Graph Table</p> | <p>Total On-Chip Power: 2.403 W</p> <p>Junction Temperature: 36.0 °C</p> <p>Thermal Margin: 49.0 °C (10.6 W)</p> <p>Effective θJA: 4.6 °C/W</p> <p>Power supplied to off-chip devices: 0 W</p> <p>Confidence level: Low</p> <p>Implemented Power Report</p> | <p>Summary On-Chip</p> | | |