Digital Design Verification

Lab Manual # 09 – Sequential Circuits using System Verilog (Counters / Digital clocks)

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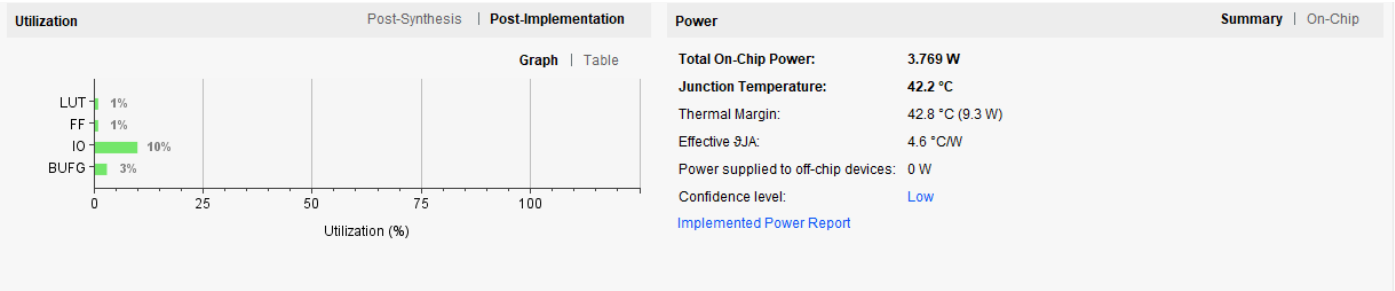
Instructor	*Hira Sohail*
Date	*31 July 2025*

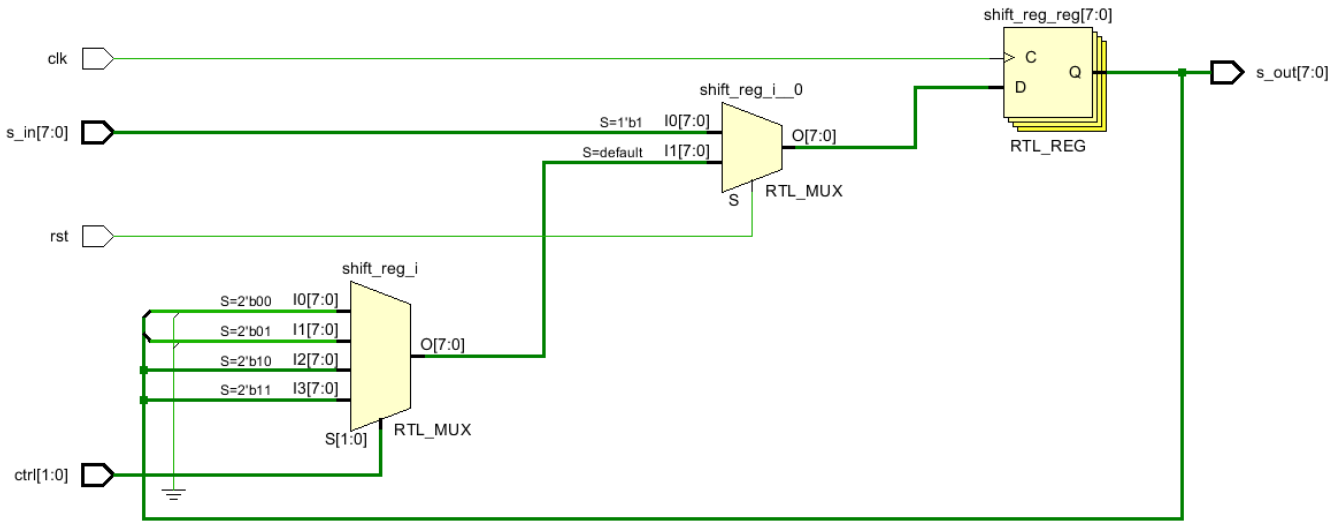
1. In-Lab Tasks: (*Write your lab task & screenshots here*)

i. Task 1:

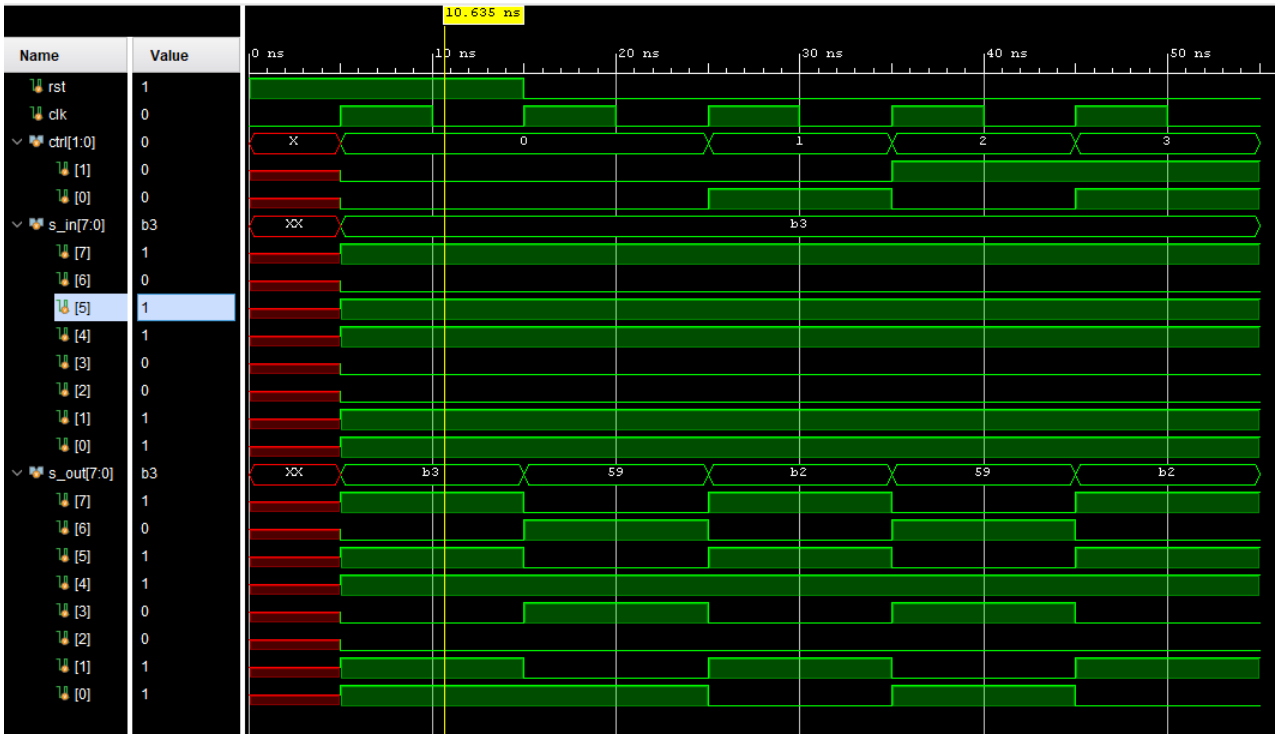
Power Report:



Schematic Diagram:

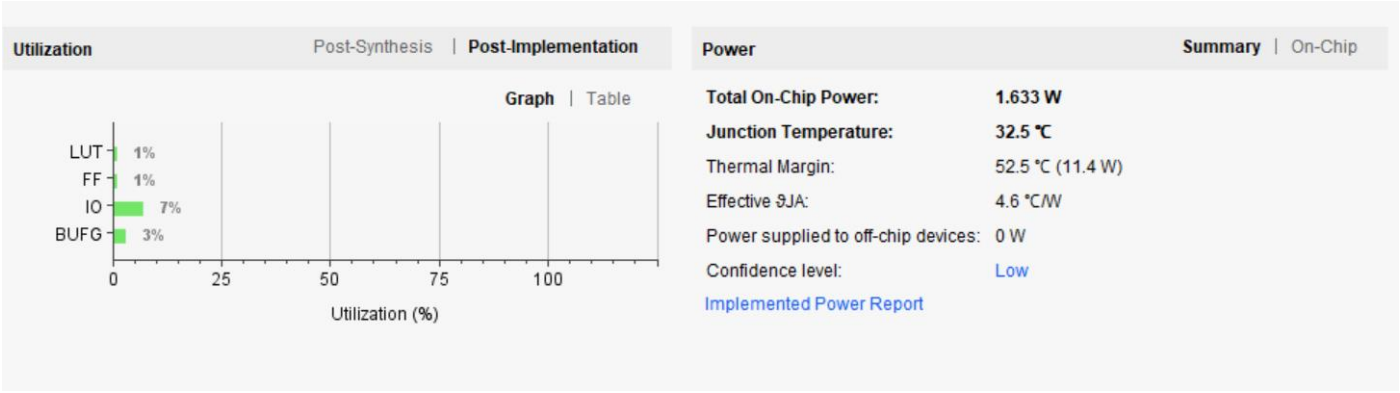


Waveform:



ii. Task 2:

Power Report:



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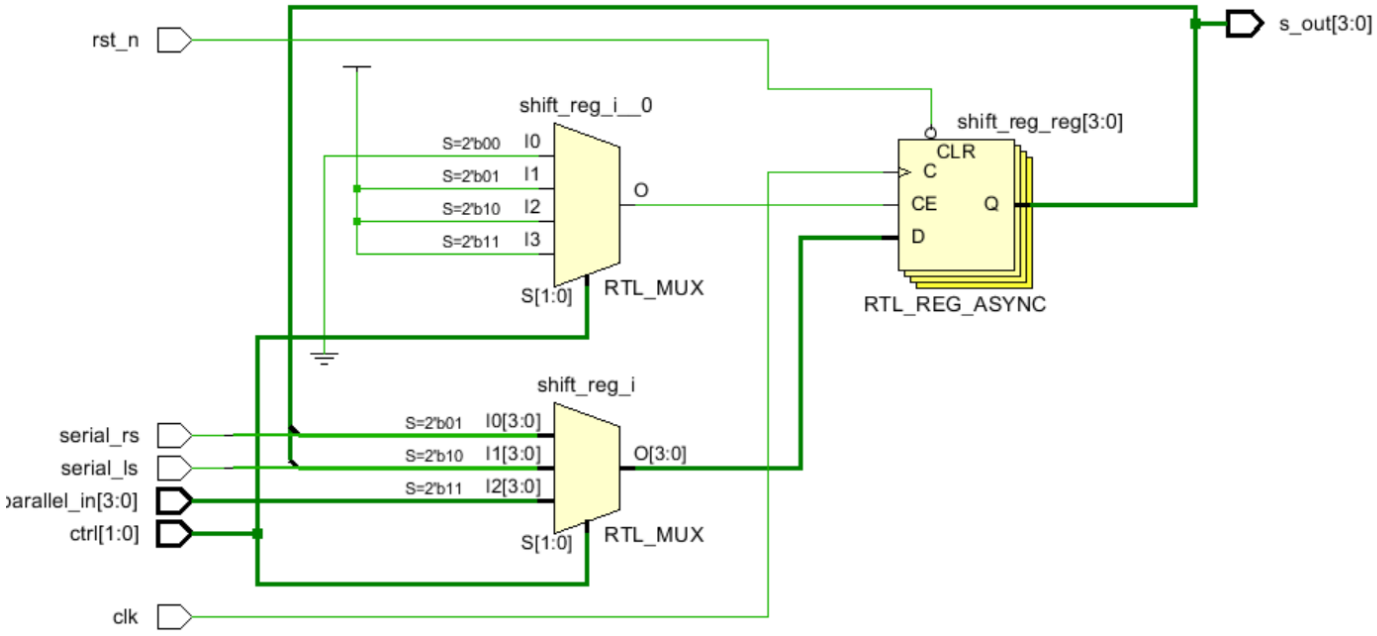

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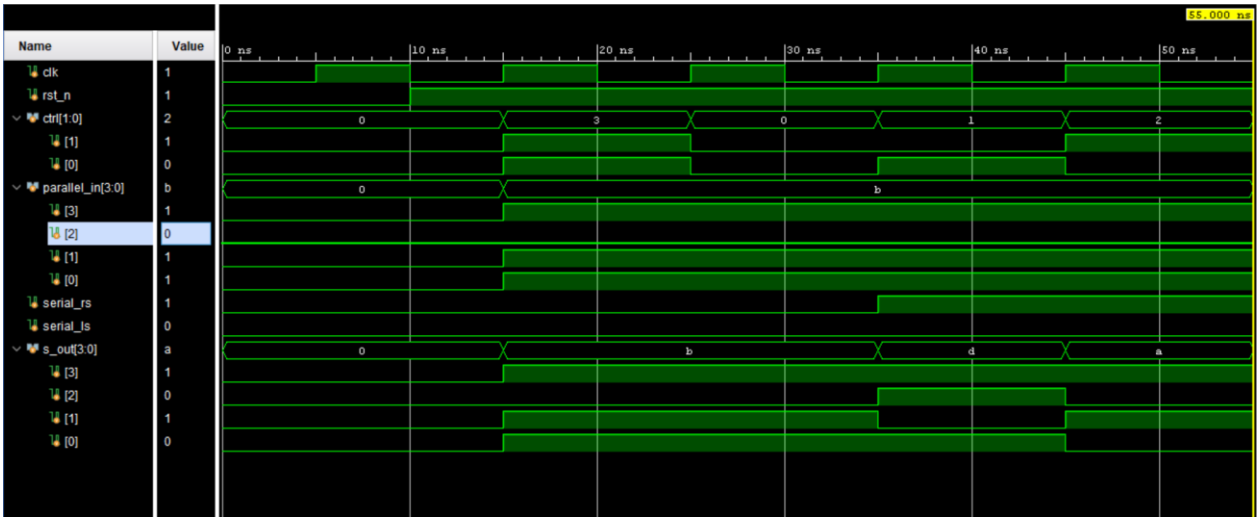
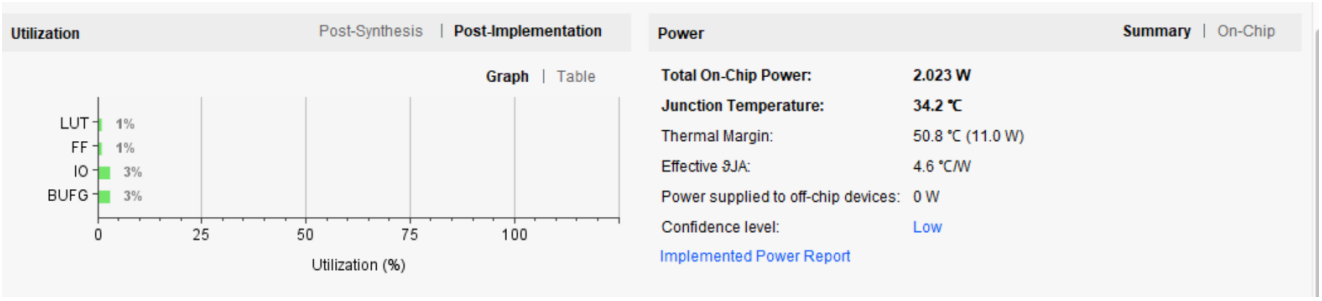


iii. Task 3:

Power Report:



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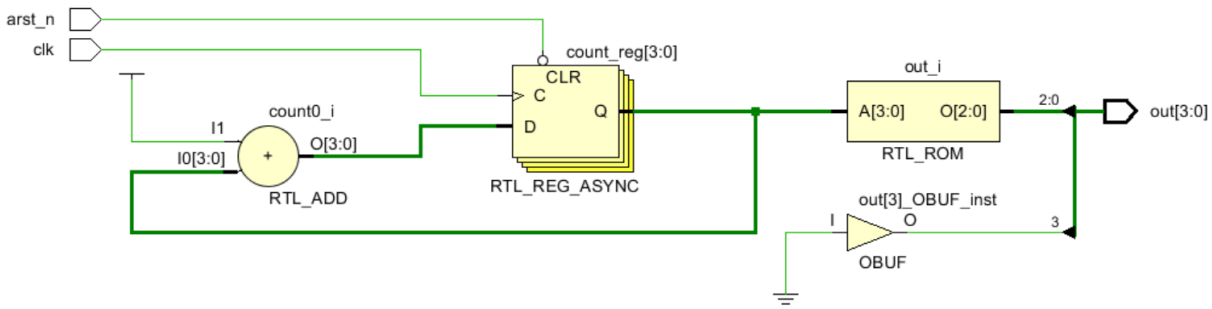
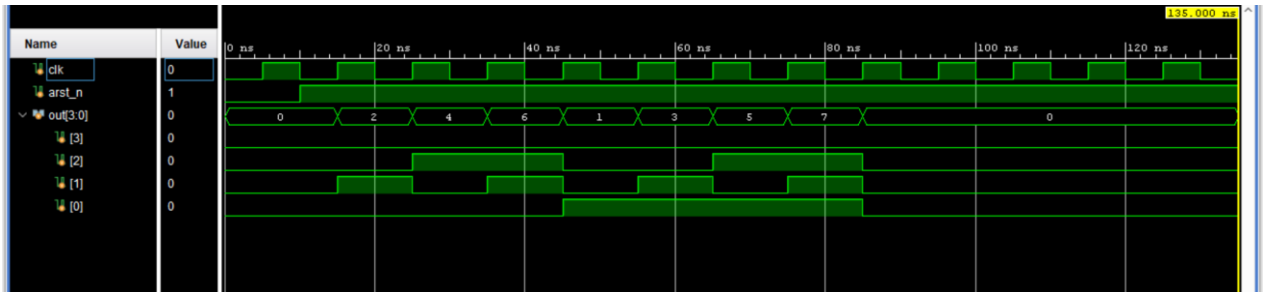


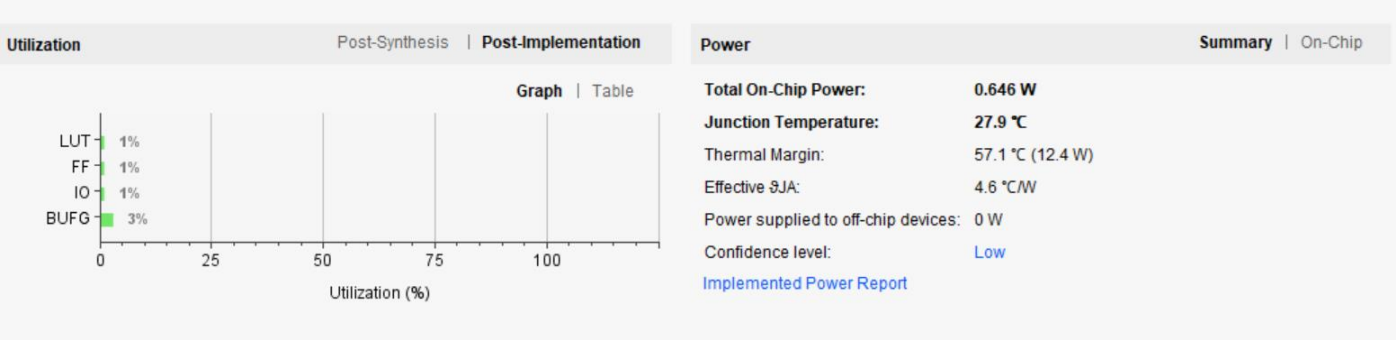
Waveform:



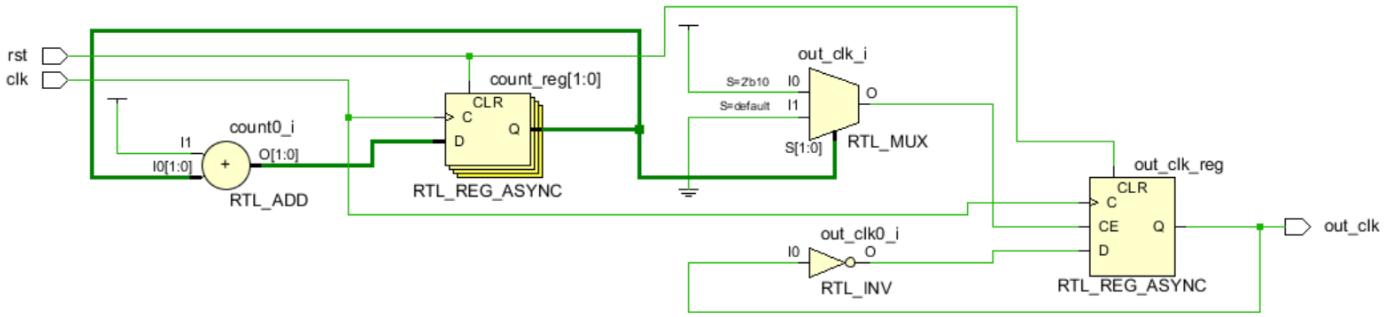
iv. Task 4:

4.1

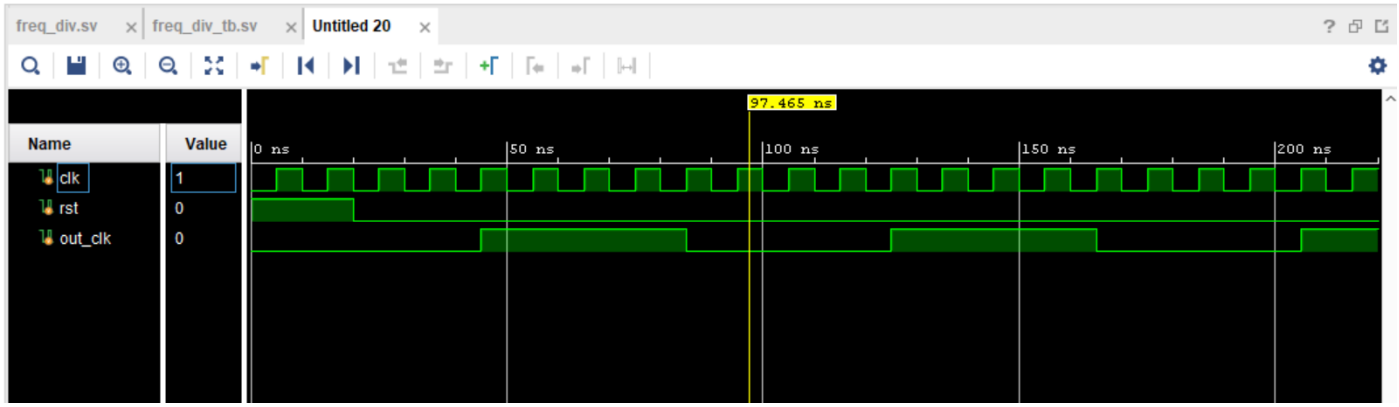
Power Report:



Schematic Diagram:



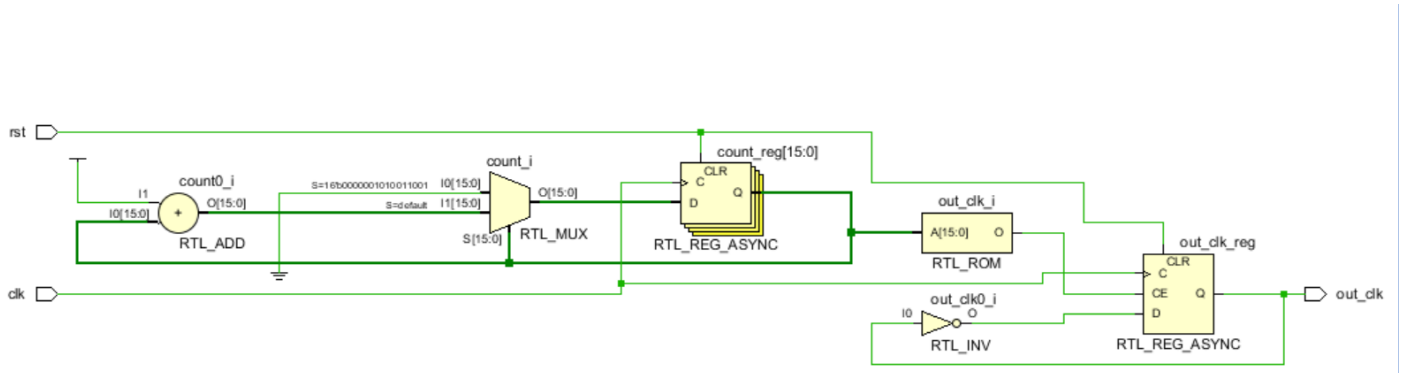
Waveform:



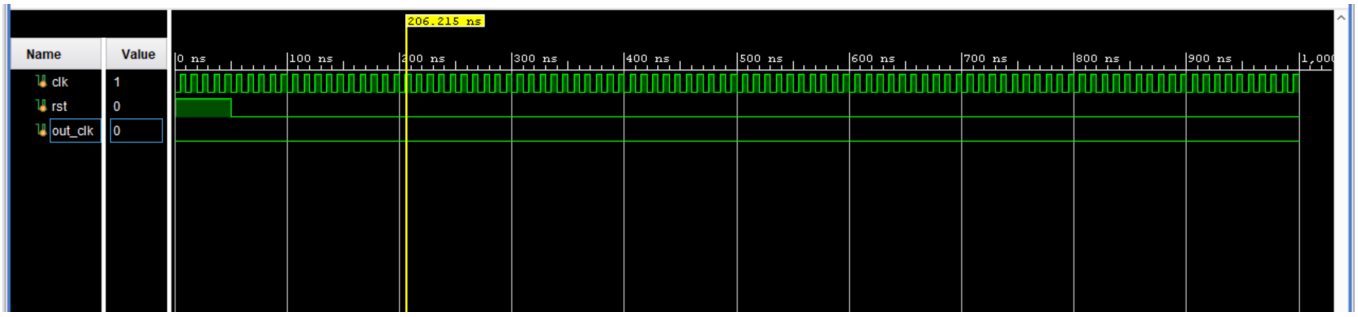
4.2

Power Report:

Schematic Diagram:



Waveform:



v. Task 5: