NUST CHIP DESIGN CENTRE

Digital Logic Design

Lab # 12
SPI Protocol Implementation

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1. In-Lab Tasks:

The objective of our project was to design and implement a complete control and monitoring system for the ADAR1000 beamforming IC using the SPI protocol. The system was intended to allow beam parameter configuration and on-chip sensor readback, enabling flexible beam control and health monitoring. To accomplish this, we assigned the work among three members, each responsible for a specific module: SPI Master, Data Management & Memory Interface, and Sensor Data Acquisition as mentioned in the manual given. By using a modular approach, we ensured that each component could be developed and tested independently before system integration.

We began by studying the ADAR1000 datasheet to understand its SPI interface, register map, beam RAM structure, and sensor readback features. Based on the system requirements, we defined clear module responsibilities:

Member 1 (Khalil Rehman): SPI Master Module

The SPI Master controller was successfully designed and implemented in Systemverilog, supporting all four SPI modes (Modes 0–3) through configurable CPOL (clock polarity) and CPHA (clock phase) parameters. The module features a 4-wire interface (SCLK, MOSI, MISO, CS#) with a finite state machine (IDLE, ENABLE, DATA, DONE) to manage transactions. It handles 24-bit transfers (8-bit command + 16-bit address) with precise clock generation, shift registers for serialization (MOSI), and deserialization (MISO), while ensuring proper chip-select timing. The design was verified via simulation, with basic functionality confirmed across all SPI modes, though minor synchronization issues were observed during high-speed operation which require further troubleshooting to fully meet ADAR1000 timing requirements.

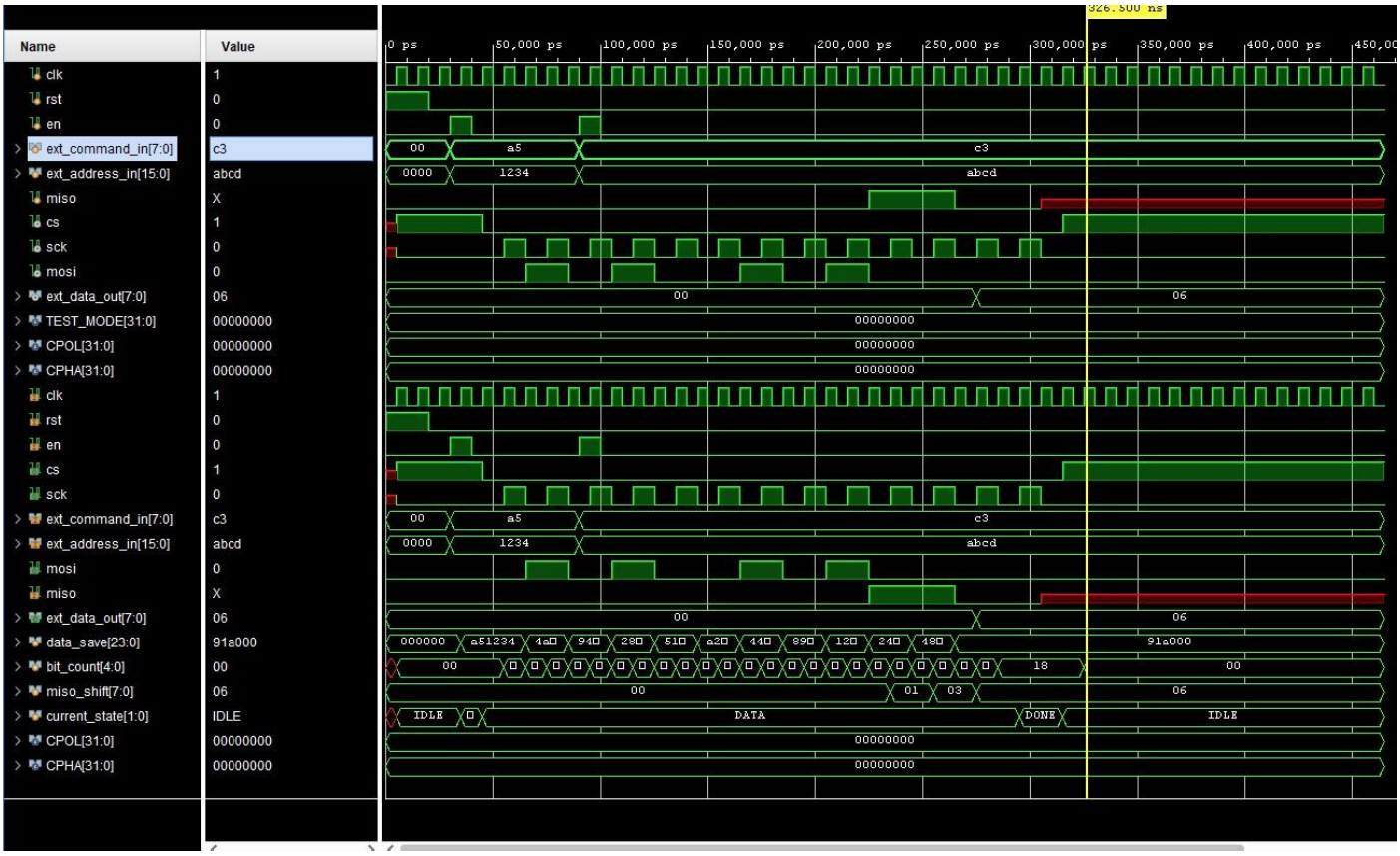
Member 2 (Momna Majeed): Sensor Data Acquisition Module

We implemented a Sensor Data Acquisition module dedicated to retrieving on-chip sensor readings from the ADAR1000. This module used the SPI Master's handshake interface to request sequential reads from specific ADAR1000 registers, including the temperature readback register and the four RF detector ADC registers (DET1 through DET4). An internal finite state machine managed the process by issuing one read command at a time, waiting for the SPI Master to signal completion, and then storing the returned data in dedicated registers. The raw temperature ADC value was immediately processed using the conversion formula from the ADAR1000 datasheet to produce a signed temperature output in centi-degrees Celsius, eliminating the need for floating-point operations in hardware. The raw detector values were preserved in their 8-bit form for later calibration or power level calculation. Once all readings were complete, the module asserted a data_ready signal for one clock cycle to notify the rest of the system that valid sensor data was available.

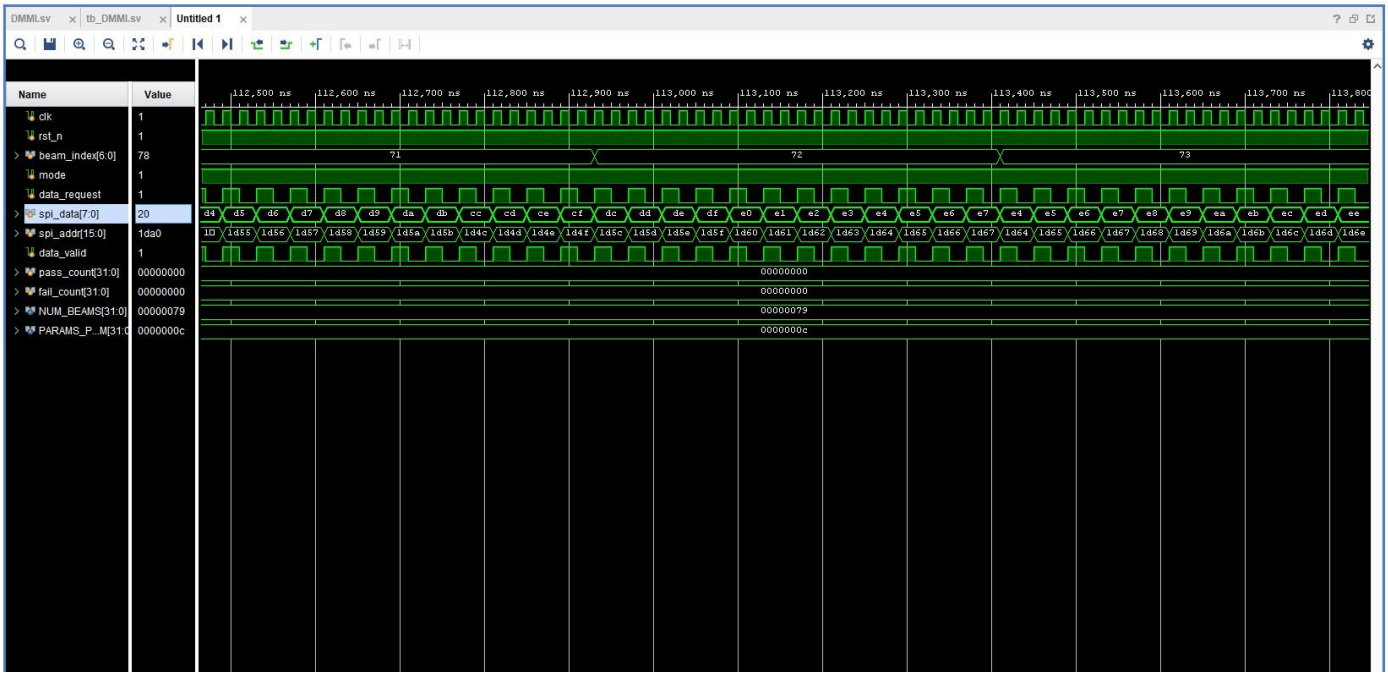
Member 3 (Sameer Awais): Data Management & Memory Interface

We developed a Data Management & Memory Interface module responsible for storing and supplying beamforming parameters to the SPI Master for programming the ADAR1000's beam RAM. The module contained a dual-mode memory structure with hardcoded parameter sets for both transmit (TX) and receive (RX) modes, covering all beams and all relevant per-channel parameters such as gain, I-phase, and Q-phase. At startup, the memory was initialized with default beam tables derived from the project's configuration plan. When triggered by a request from the SPI Master, the module calculated the correct memory index based on the requested beam number, mode selection, and parameter index, and then returned the corresponding data byte. Address mapping was implemented in accordance with the ADAR1000 beam RAM addressing scheme, ensuring correct parameter placement during writes. The handshake interface allowed the SPI Master to retrieve one parameter byte at a time, synchronizing the transfer to avoid timing hazards and ensuring each parameter was delivered in the correct sequence for beam configuration.

Simulation:



Master Controller Simulation



Data Management and Memory Interface

2. Critical Analysis:

We have successfully designed and implemented the key modules for the SPI-based ADAR1000 control system, dividing the work into three coordinated components:

SPI Master Module: Developed to communicate with the ADAR1000.

Data Management Module: Implemented to store and provide beamforming parameters.

Sensor Data Acquisition Module: Built to read and process on-chip RF detector and temperature sensor outputs.

Each module has been individually verified through simulation. Currently, we are working on integrating all modules to validate full system functionality. Once integration is complete, we will conduct comprehensive testing to ensure seamless operation of the ADAR1000 control and monitoring system.