Digital Design Verification

Lab Manual # 09 – Sequential Circuits using System Verilog (Counters / Digital clocks)

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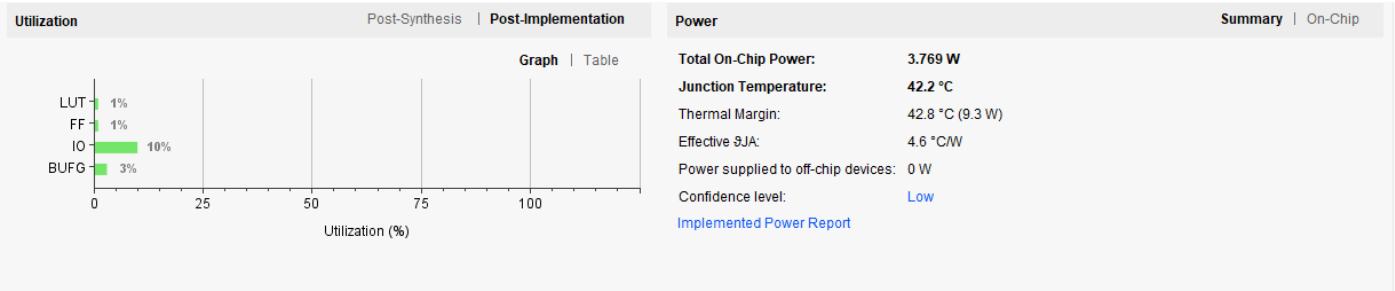
Instructor	*Hira Sohail*
Date	*31 July 2025*

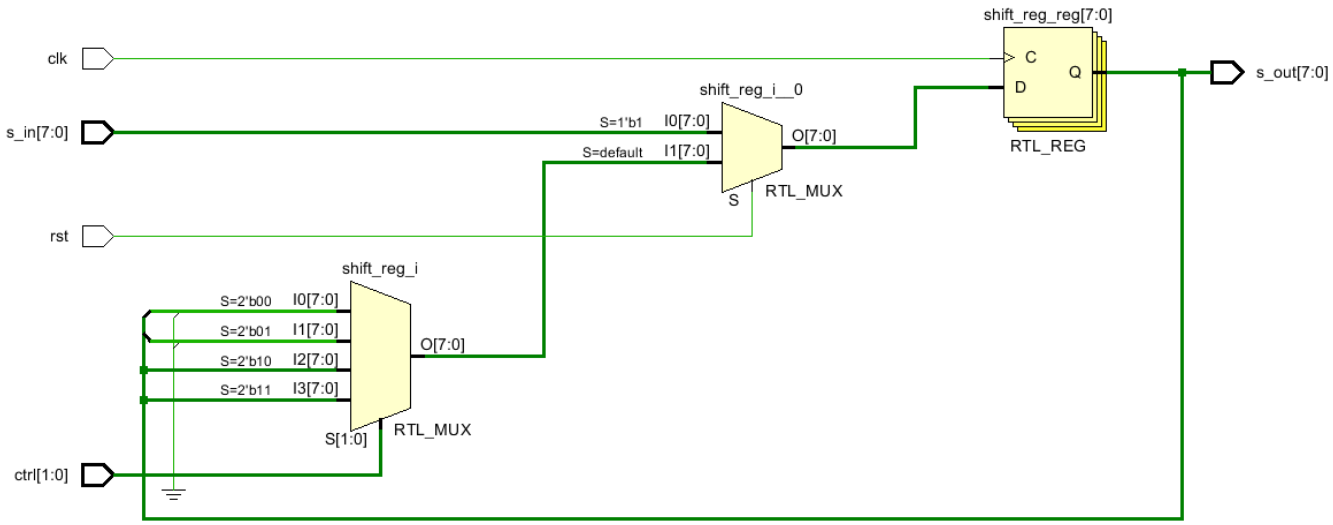
1. In-Lab Tasks: (*Write your lab task & screenshots here*)

i. Task 1:

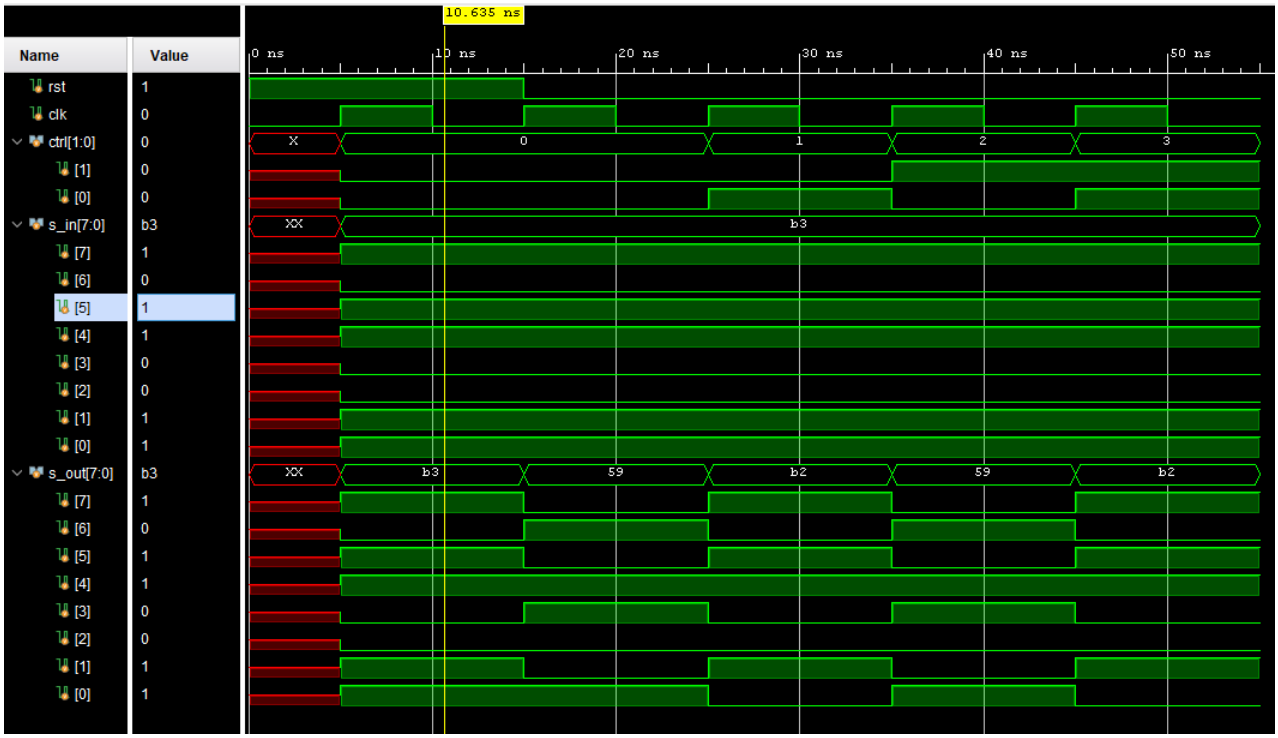
Power Report:



Schematic Diagram:

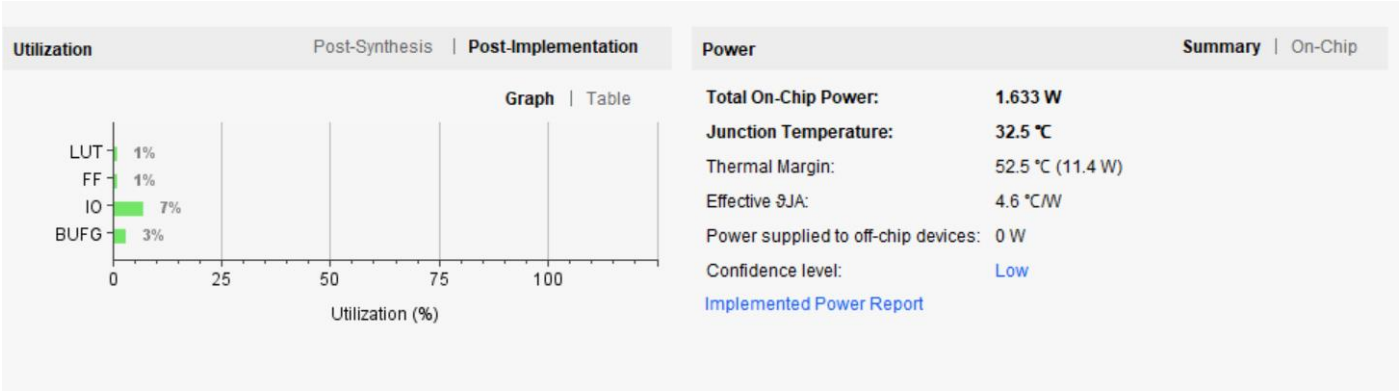


Waveform:

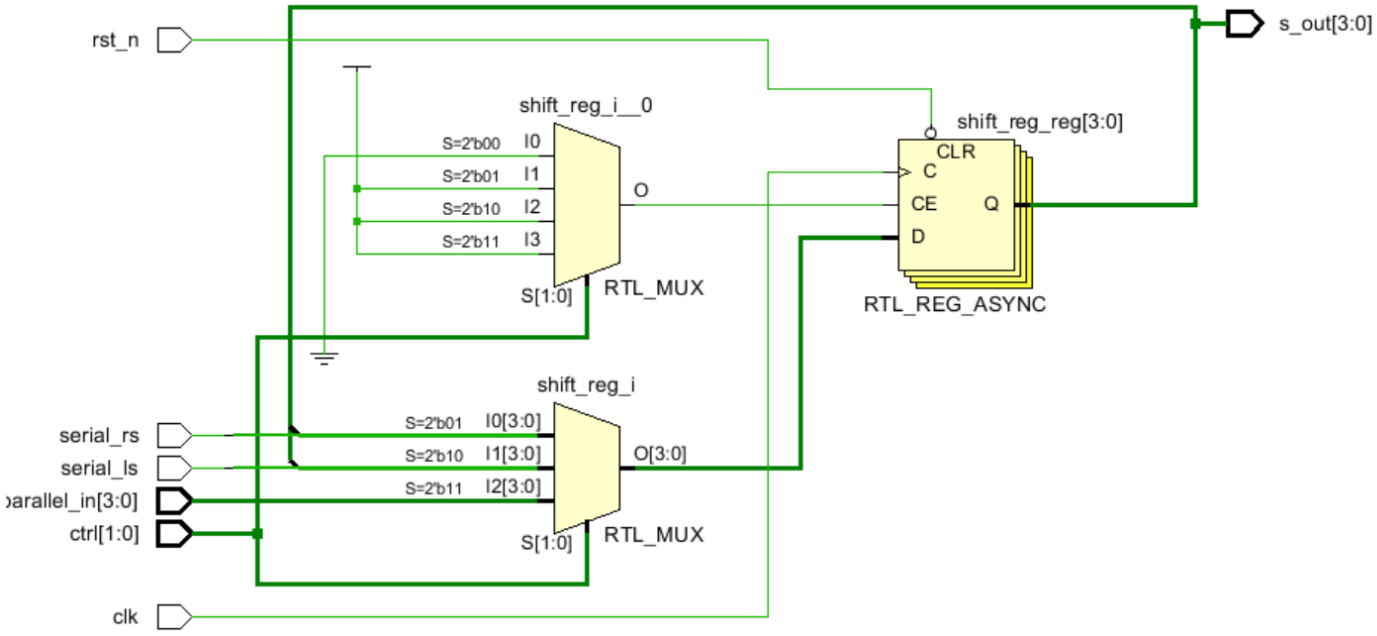


ii. Task 2:

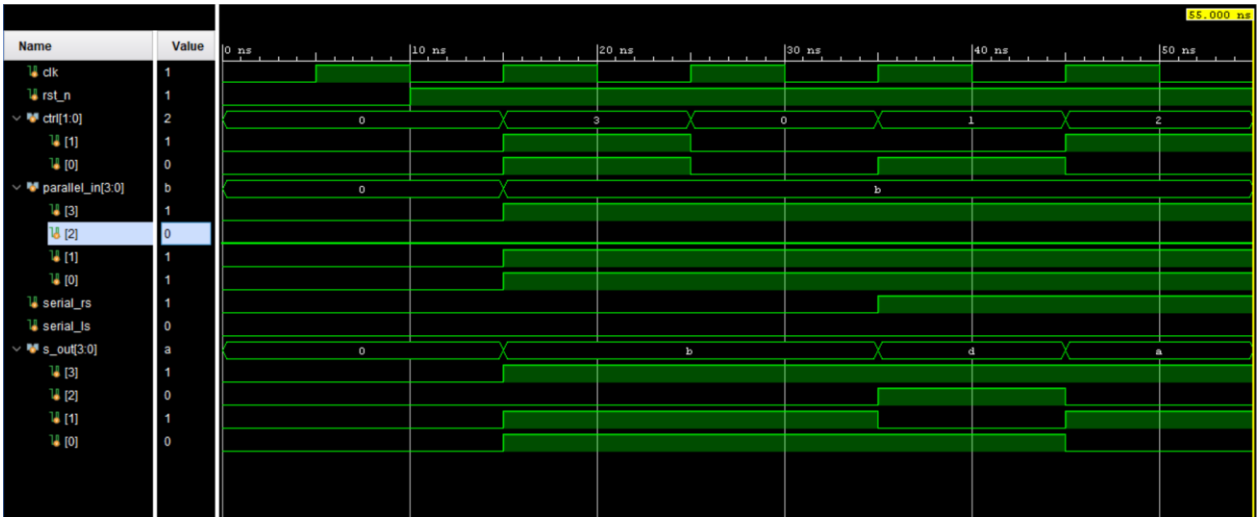
Power Report:



Schematic Diagram:

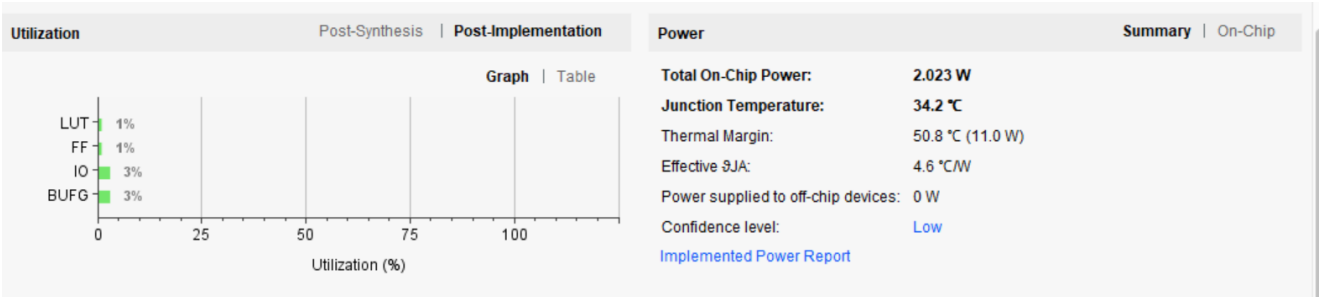


Waveform:

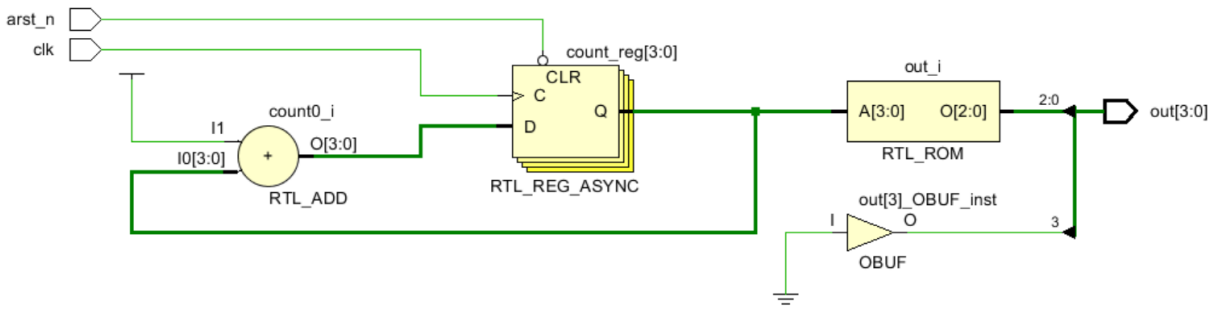


iii. Task 3:

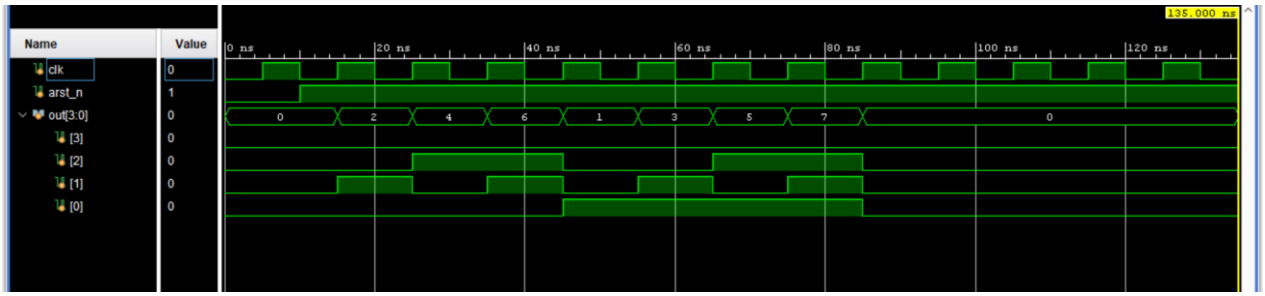
Power Report:



Schematic Diagram:



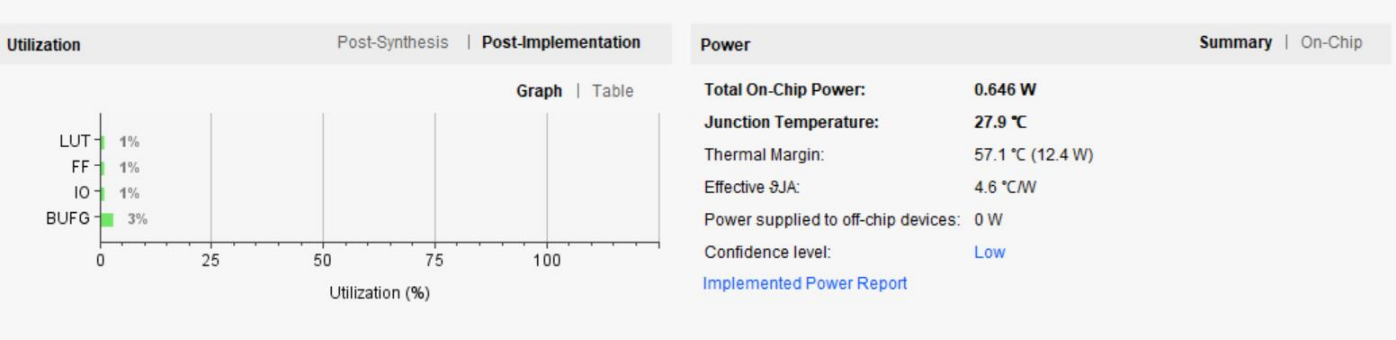
Waveform:



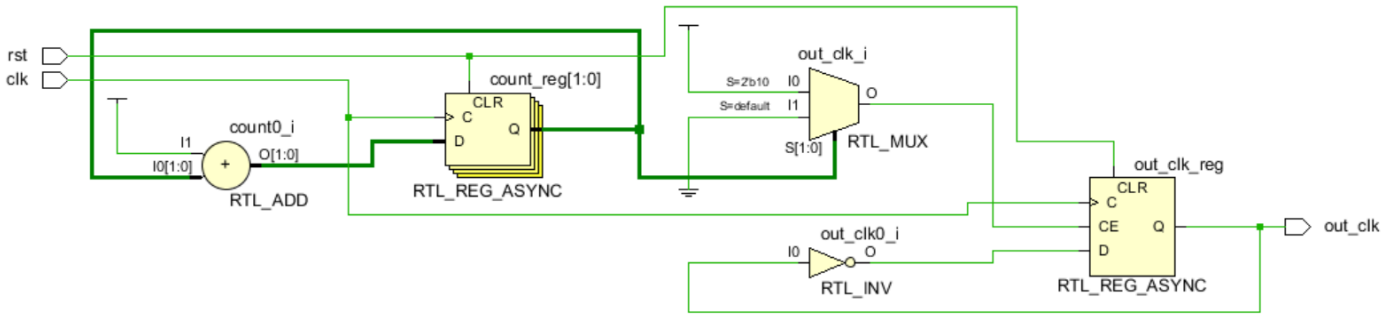
iv. Task 4:

4.1

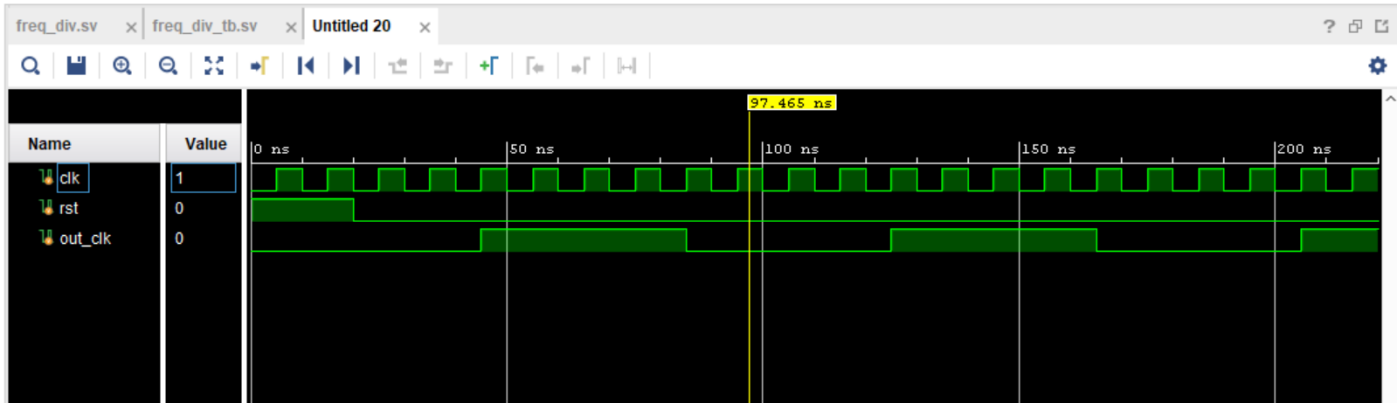
Power Report:



Schematic Diagram:



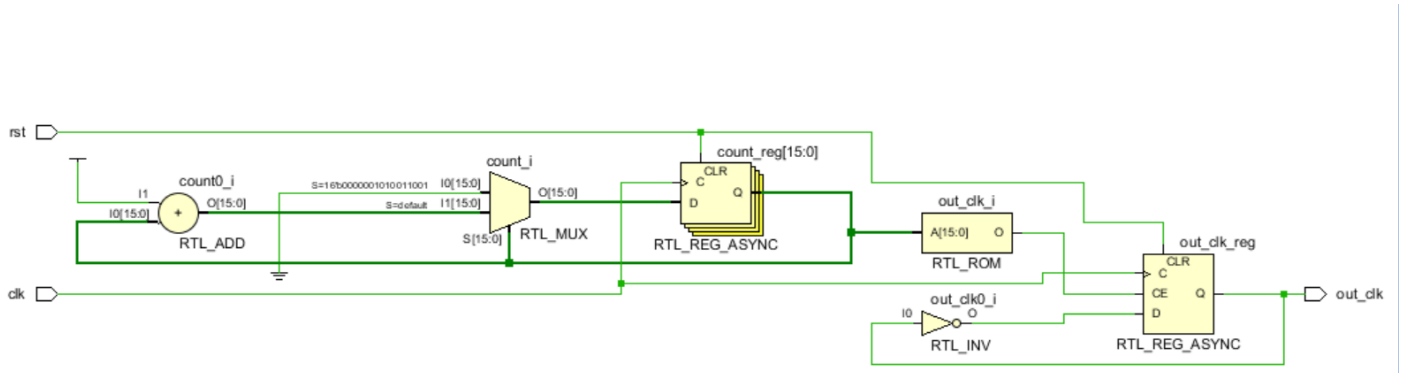
Waveform:



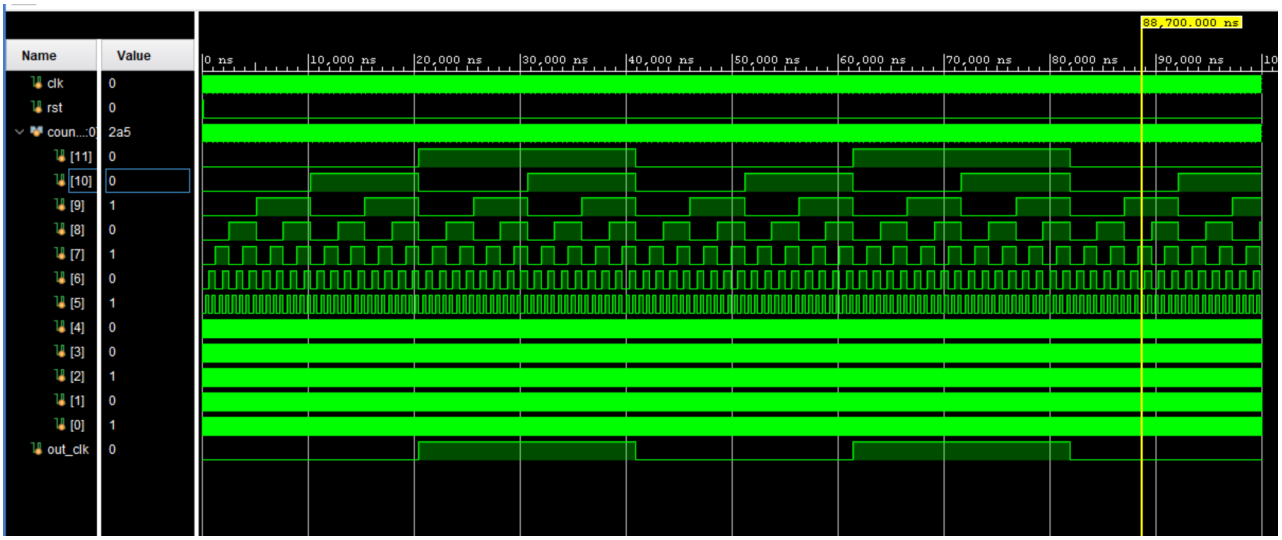
4.2

Power Report:

Schematic Diagram:

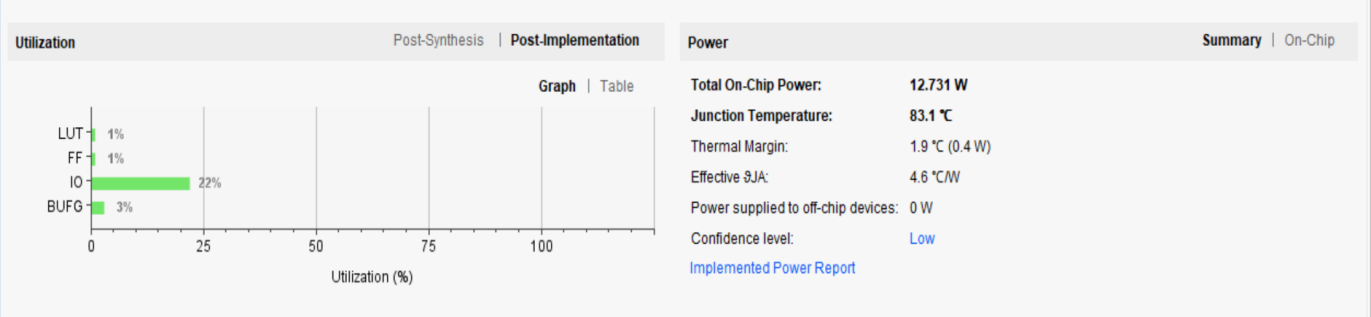


Waveform:

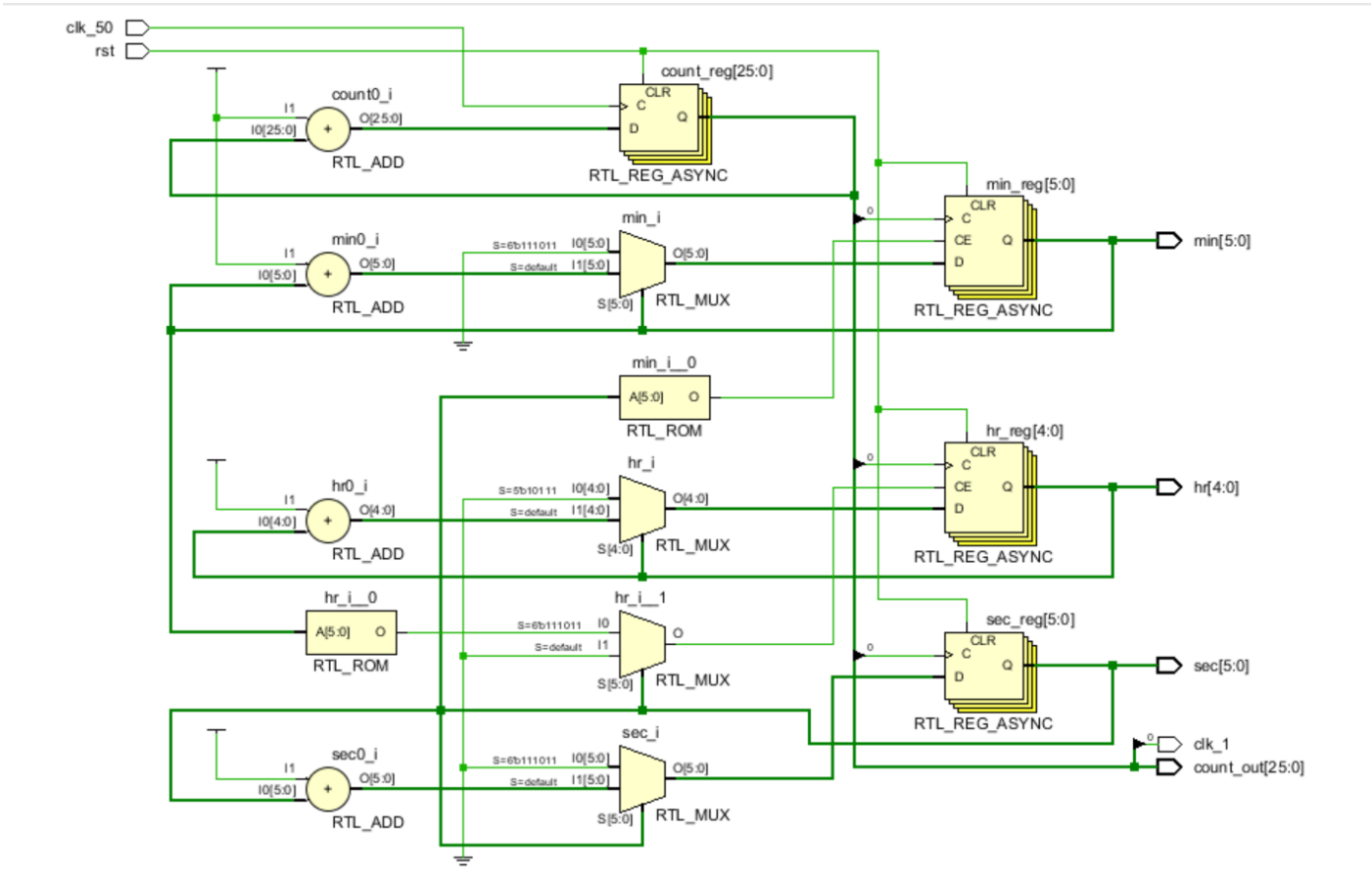


v. Task 5:

Power Report:

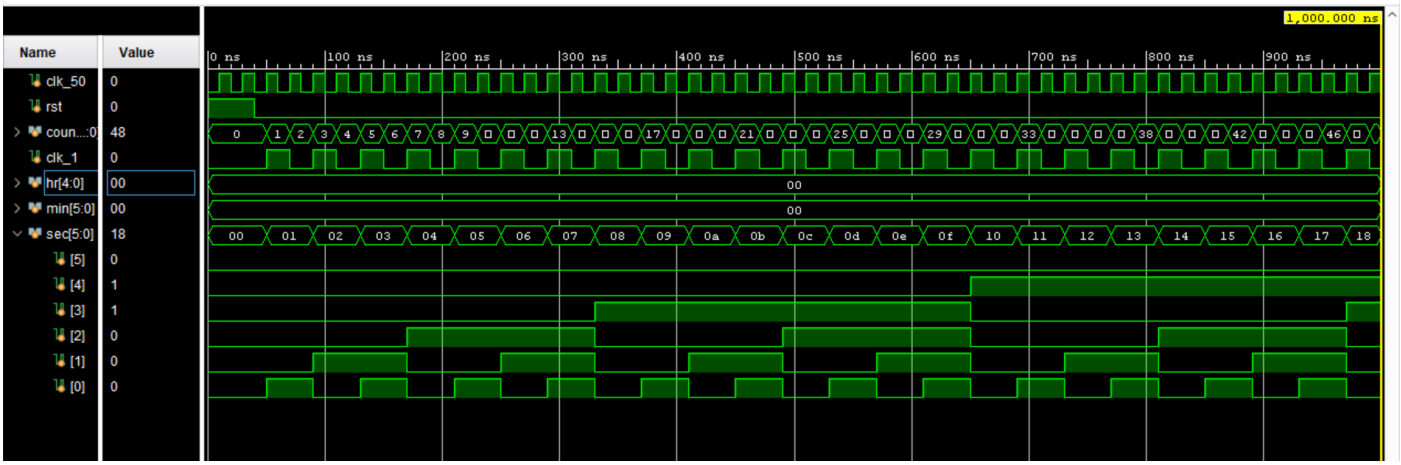


Schematic Diagram

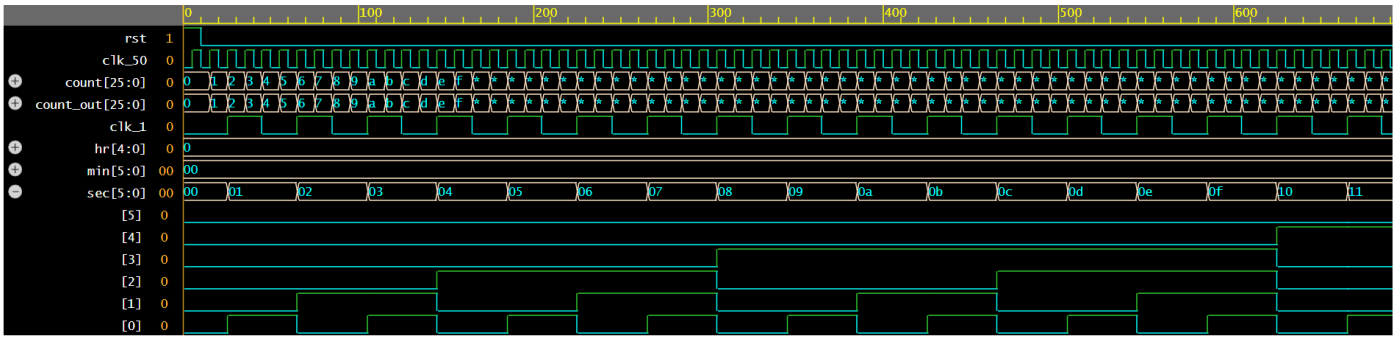


Waveform:

To verify the behavior in simulation, I temporarily used the count[0] bit to generate a faster clock signal (clk_1). This allowed me to observe the output transitions more quickly during simulation. However, for actual FPGA implementation, I will use the count[25] bit to generate a actual 1Hz clock signal from the 50MHz input clock



Using EDA Playground



Source: https://www.edaplayground.com/x/UVX3

Conclusion:

In this lab, I first implemented a Serial-In Serial-Out (SISO) shift register to understand basic data shifting. Then, I extended the concept by designing a Universal Shift Register that supports multiple operations like shift left, shift right, and parallel load. After that, I explored different types of counters to generate sequential patterns. I also designed a frequency divider to scale down a high-frequency clock, which was also used in building a simple digital clock.

According to my understanding, this lab provided strong foundational knowledge in sequential circuits, which will be very helpful in designing more complex modules like UART, as it requires a good understanding of shift registers, counters, and timing control.