Digital Design Verification

DLD – Worksheet 2

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Question 1: Using the method of design and analysis of sequential circuits, design the following SYNCHRONOUS counters

4-bit binary Down counter using D flip-flops

4-bit BCD Up counter using T-flip-flops

Question 2: Implement the counters designed in Question 1, using SystemVerilog HDL.

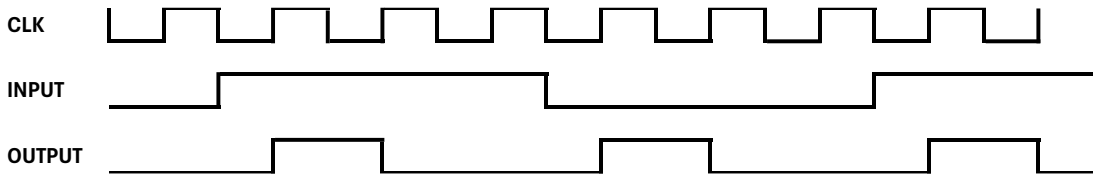
Question 3: Implement the following RIPPLE counters using SystemVerilog HDL.

4-bit binary Ripple Up & Down Counter.

4-bit BCD Ripple Up counter using T-flip-flops

12-bit BCD Ripple Decade counter that counts from 0 to 999

Question 4: Design and implement a circuit to detect level change in the input signal. Specifically, the circuit should generate a pulse for one clock cycle when the input level transitions from low to high (rising edge) and/or from high to low (falling edge). Also write its SystemVerilog code. A sample waveform of such a circuit (positive edge triggered) is given below:



Question 5: Design a serial 2's complement computation circuit with a 1-bit input and 1-bit output. The circuit should compute the 2's complement of the incoming bitstream while a control signal is asserted (set to 1), i.e., when the control signal is high, the circuit generates the 2's complement of the input stream. When the control signal is low (0), the circuit should pass the incoming bitstream directly to the output. Also write its SystemVerilog code.

Submission Instructions:

Please submit your solutions in a single .zip archive. Inside the archive, **create separate subfolders for each question**. Include the following items within each respective subfolder:

Design Documentation: Upload scanned copies (in PDF format) of your design solutions and implementations.

SystemVerilog Code Files: Provide the .sv files containing your SystemVerilog code.