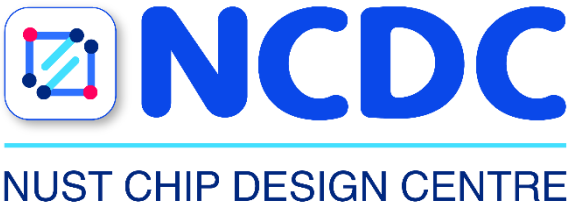

EXERCISE # 01

RISCV Assembly Tasks

Revision History

Revision Number	Revision Date	Revision By	Nature of Revision	Approved By
1.0	01/9/204	Dr. Imran	Document	-

Task 1

Using RISC-V add / addi / sub instructions, implement 1's complement (NOT) of a value in x5 register

i.e., if x5 = 0xFFFFFFFF, after 1's complement x5 = 0x00000000

Task 2

Write a RISC-V assembly code that creates a 32-bit constant value 0x12345678 and places it in x5

Task 3

Write a RISC-V code that tests whether a number in x5 register is even or odd. The result is indicated in x10 such that x10 is 0 if the number is even and 1 if number is odd

Task 4

Write a RISC-V assembly code that toggles a specific bit of x5 with the bit number to be toggled been specified in x10

Task 5

Write a RISC-V assembly code that checks if there are even number of 1's in value specified in register x5 or odd number of 1's. If there are even number of 1's in x5, set x10 to 0 otherwise set x10 to 1.

Task 6

Write a RISC-V assembly code that selects one of the 4 bytes from a register x5 and places the resulting byte (with 0 extension) in x10. The byte number (0,1,2 or 3) is specified in x6.

Task 7

Write a RISC-V assembly code that selects one of the 4 bytes from a register x5 and places the resulting byte (with sign extension) in x10. The byte number (0,1, 2 or 3) is specified in x6.

Task 8

Write a RISC-V assembly code that compares x5 and x6 and sets x10 to 1 if x5 is greater (signed comparison) than x6.

Do this without using slt (set less than) instruction which achieves the same thing!