



NUST CHIP DESIGN CENTRE

Digital Design Verification

EXERCISE # 04 RISCV Assembly Tasks

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1. Tasks:

Task # 1

```
1 .data
2
3 .text
4 .globl main
5
6 main:
7     li a0, -6      # first number
8     li a1, 4       # second number
9     jal ra, multiply
10
11     # Exit properly
12     li a7, 10
13     ecall
14
15 multiply:
16     add t0, a0, x0    # t0 = a
17     add t1, a1, x0    # t1 = b
18     addi a2, x0, 0     # result = 0
19     addi t2, x0, 0     # negative flag = 0
20
21     # Check if a is negative
22     slt t3, t0, x0     # t3 = 1 if t0 < 0
23     beq t3, x0, check_b
24     sub t0, x0, t0     # a = -a
25     xori t2, t2, 1     # toggle negative
26
27 check_b:
28     # Check if b is negative
29     slt t3, t1, x0     # t3 = 1 if t1 < 0
30     beq t3, x0, loop_mul
31     sub t1, x0, t1     # b = -b
32     xori t2, t2, 1     # toggle negative
33
34 loop_mul:
35     beq t1, x0, done_mul # if b == 0, exit loop
36     add a2, a2, t0     # result += a
37     addi t1, t1, -1    # b--
38     j loop_mul
39
40 done_mul:
41     beq t2, x0, end_mul
42     sub a2, x0, a2     # result = -result
43
44 end_mul:
45     jr ra             # return to caller
```

Execution:

-24

a0 (x10)	<input type="text" value="-6"/>	≡
a1 (x11)	<input type="text" value="4"/>	≡
t0 (x5)	<input type="text" value="-6"/>	≡
t1 (x6)	<input type="text" value="4"/>	≡
ra (x1)	<input type="text" value="12"/>	≡
a2 (x12)	<input type="text" value="-24"/>	≡

Task # 2

```
1 .data
2 msg_div: .asciiz "Division result done\n"
3
4 .text
5 .globl main
6
7 main:
8     li a0, -17      # dividend
9     li a1, 5        # divisor
10
11     jal ra, divide  # call divide(a0, a1)
12
13     # a2 = quotient
14     # a3 = remainder
15     li a7, 4        # syscall: print string
16     la a0, msg_div
17     ecall
18
19     # Exit program
20     li a7, 10
21     ecall
22
23 divide:
24     add t0, a0, x0   # dividend
25     add t1, a1, x0   # divisor
26     addi a2, x0, 0    # quotient = 0
27     addi a3, x0, 0    # remainder = 0
28     addi t2, x0, 0    # negative flag = 0
29
30     # if (a0 < 0) → make positive
31     slt t3, t0, x0
32     beq t3, x0, check_div_b
33     sub t0, x0, t0
34     xori t2, t2, 1
35
36 check_div_b:
37     slt t3, t1, x0
38     beq t3, x0, div_loop
39     sub t1, x0, t1
40     xori t2, t2, 1
41
42 div_loop:
43     slt t3, t0, t1    # if (t0 < t1) break
```

RISCV Assembly Task

```
42 div_loop:
43     slt t3, t0, t1      # if (t0 < t1) break
44     bne t3, x0, div_done
45     sub t0, t0, t1      # dividend -= divisor
46     addi a2, a2, 1      # quotient++
47     j div_loop
48
49 div_done:
50     add a3, t0, x0      # remainder = leftover dividend
51     beq t2, x0, div_end
52     sub a2, x0, a2      # apply sign to quotient
53
54 div_end:
55     jr ra
```

Execution:

a0 (x10)	<input type="text" value="-17"/>	≡
a1 (x11)	<input type="text" value="5"/>	≡
a2 (x12)	<input type="text" value="-3"/>	≡
a3 (x13)	<input type="text" value="2"/>	≡