数电实验6

【实验目的】

了解 FPGA 工作原理

了解 Verilog 文件和约束文件在 FPGA 开发中的作用

学会使用 Vivado 进行 FPGA 开发的完整流程

【实验环境】

VLAB 平台： vlab.ustc.edu.cn

FPGAOL 实验平台：fpgaol.ustc.edu.cn

Logisim

Vivado 工具

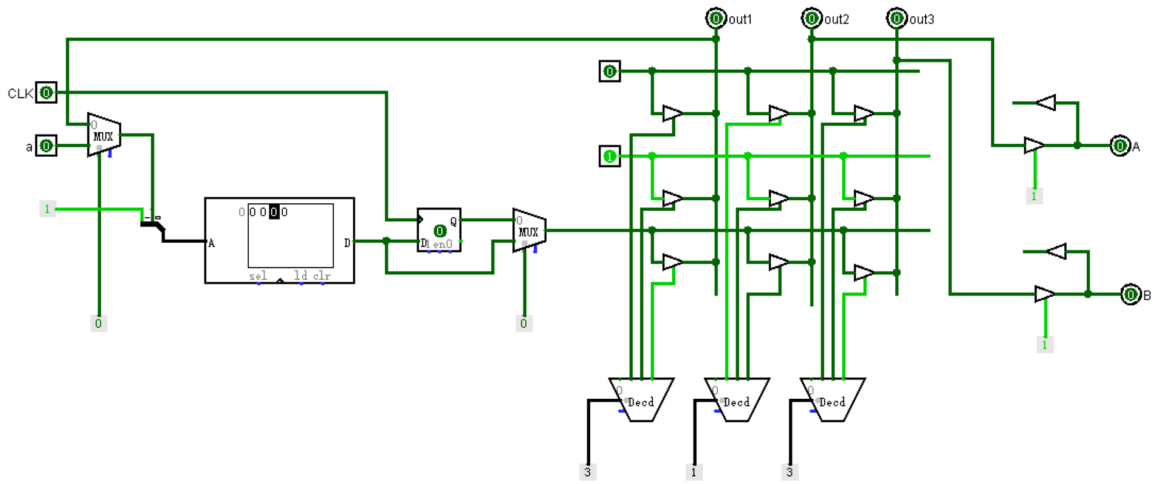
【实验题目】

T1

```
module test(input clk,output reg a);
always@(posedge clk)
a <= a ^ 1'b1;
endmodule
```

配置数据（从左至右）：第一个MUX为0；RAM为0110；第二个MUX为0；为了1与3统一（输出到B引脚），因此将1与3的Decd统一（都令其为3）

此时a,b均为1，拨动CLK，按题目方式变化。



T2

调整一下sw[a]中a的顺序即可

```
set_property -dict { PACKAGE_PIN E3     IOSTANDARD LVCMOS33 } [get_ports { clk }];

set_property -dict { PACKAGE_PIN B18    IOSTANDARD LVCMOS33 } [get_ports { rst }];

set_property -dict { PACKAGE_PIN C17    IOSTANDARD LVCMOS33 } [get_ports { led[0]} ];
set_property -dict { PACKAGE_PIN D18    IOSTANDARD LVCMOS33 } [get_ports { led[1]} ];
set_property -dict { PACKAGE_PIN E18    IOSTANDARD LVCMOS33 } [get_ports { led[2]} ];
set_property -dict { PACKAGE_PIN G17    IOSTANDARD LVCMOS33 } [get_ports { led[3]} ];
set_property -dict { PACKAGE_PIN D17    IOSTANDARD LVCMOS33 } [get_ports { led[4]} ];
set_property -dict { PACKAGE_PIN E17    IOSTANDARD LVCMOS33 } [get_ports { led[5]} ];
set_property -dict { PACKAGE_PIN F18    IOSTANDARD LVCMOS33 } [get_ports { led[6]} ];
set_property -dict { PACKAGE_PIN G18    IOSTANDARD LVCMOS33 } [get_ports { led[7]} ];

set_property -dict { PACKAGE_PIN D14    IOSTANDARD LVCMOS33 } [get_ports { sw[7]} ];
set_property -dict { PACKAGE_PIN F16    IOSTANDARD LVCMOS33 } [get_ports { sw[6]} ];
set_property -dict { PACKAGE_PIN G16    IOSTANDARD LVCMOS33 } [get_ports { sw[5]} ];
set_property -dict { PACKAGE_PIN H14    IOSTANDARD LVCMOS33 } [get_ports { sw[4]} ];
set_property -dict { PACKAGE_PIN E16    IOSTANDARD LVCMOS33 } [get_ports { sw[3]} ];
set_property -dict { PACKAGE_PIN F13    IOSTANDARD LVCMOS33 } [get_ports { sw[2]} ];
set_property -dict { PACKAGE_PIN G13    IOSTANDARD LVCMOS33 } [get_ports { sw[1]} ];
set_property -dict { PACKAGE_PIN H16    IOSTANDARD LVCMOS33 } [get_ports { sw[0]} ];

```

T3

设计文件

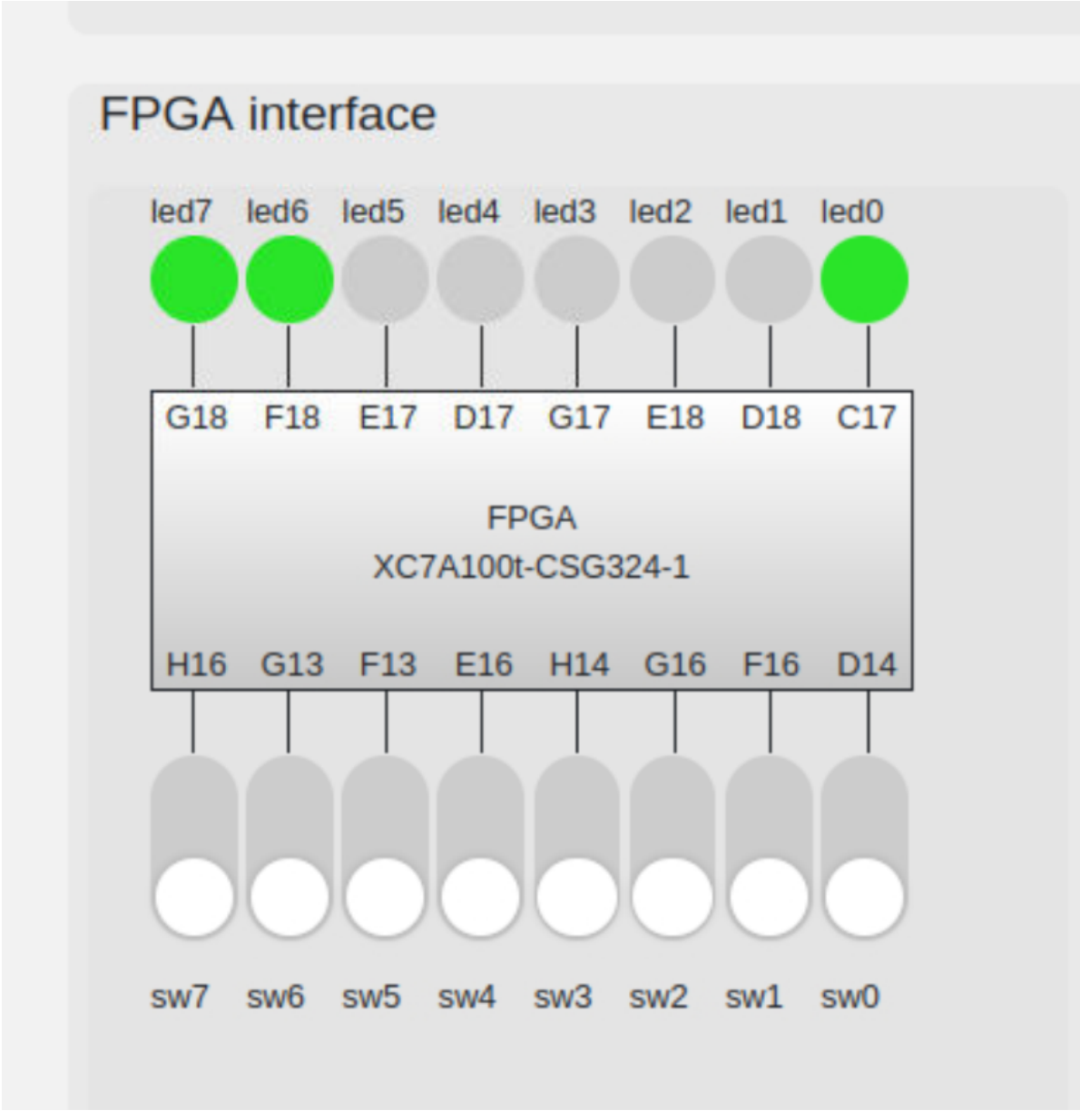
```
module l30(
input clk,rst,
    output reg[7:0] led);//定义输入输出
    reg[29:0] r;
always@(posedge clk)
```

```
begin
    if(rst)
        begin
            r<=30'b0;
            led<=8'haa;
        end
    else
        begin
            r<=r+30'b1;
            led<={r[29],r[28],r[27],r[26],r[25],r[24],r[23],r[22]};//高八位
        end
end
endmodule
```

```
set_property -dict { PACKAGE_PIN E3     IOSTANDARD LVCMOS33 } [get_ports { clk }];

set_property -dict { PACKAGE_PIN B18    IOSTANDARD LVCMOS33 } [get_ports { rst }];

set_property -dict { PACKAGE_PIN G18    IOSTANDARD LVCMOS33 } [get_ports { led[0]} ];
set_property -dict { PACKAGE_PIN F18    IOSTANDARD LVCMOS33 } [get_ports { led[1]} ];
set_property -dict { PACKAGE_PIN E17    IOSTANDARD LVCMOS33 } [get_ports { led[2]} ];
set_property -dict { PACKAGE_PIN D17    IOSTANDARD LVCMOS33 } [get_ports { led[3]} ];
set_property -dict { PACKAGE_PIN G17    IOSTANDARD LVCMOS33 } [get_ports { led[4]} ];
set_property -dict { PACKAGE_PIN E18    IOSTANDARD LVCMOS33 } [get_ports { led[5]} ];
set_property -dict { PACKAGE_PIN D18    IOSTANDARD LVCMOS33 } [get_ports { led[6]} ];
set_property -dict { PACKAGE_PIN C17    IOSTANDARD LVCMOS33 } [get_ports { led[7]} ];

set_property -dict { PACKAGE_PIN D14    IOSTANDARD LVCMOS33 } [get_ports { sw[0]} ];
set_property -dict { PACKAGE_PIN F16    IOSTANDARD LVCMOS33 } [get_ports { sw[1]} ];
set_property -dict { PACKAGE_PIN G16    IOSTANDARD LVCMOS33 } [get_ports { sw[2]} ];
set_property -dict { PACKAGE_PIN H14    IOSTANDARD LVCMOS33 } [get_ports { sw[3]} ];
set_property -dict { PACKAGE_PIN E16    IOSTANDARD LVCMOS33 } [get_ports { sw[4]} ];
set_property -dict { PACKAGE_PIN F13    IOSTANDARD LVCMOS33 } [get_ports { sw[5]} ];
set_property -dict { PACKAGE_PIN G13    IOSTANDARD LVCMOS33 } [get_ports { sw[6]} ];
set_property -dict { PACKAGE_PIN H16    IOSTANDARD LVCMOS33 } [get_ports { sw[7]} ];
```

```
module l32(
input clk,rst,
output reg[7:0] led);
reg[31:0] r;
always@(posedge clk)
begin
    if(rst)
        begin
            r<=32'b0;
            led<=8'h0;
        end
    else
        begin
            r<=r+32'b1;
            led<={r[32],r[31],r[30],r[29],r[28],r[27],r[26],r[25]};
        end
end
endmodule
```

l30



l32

FPGA interface