Computer Architecture

Course Title: Computer Architecture **Full Marks:** 60+ 20+20

Course No: CSC208 **Pass Marks:** 24+8+8

Nature of the Course: Theory + Lab **Credit Hrs:** 3

Course Description: This course includes concepts of instruction set architecture, organization or micro-architecture, and system architecture. The instruction set architecture includes programmer's abstraction of computer. The micro-architecture consist internal representation of computers at register and functional unit level. The system architecture includes organization of computers at the cache and bus level.

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Course Objectives

- Discuss representation of data and algorithms used to perform operations on data
- Demonstrate different operations in terms of Micro-operations
- Explain architecture of basic computer and micro-programmed control unit
- Understand and memory and I/O organization of a typical computer system
- Demonstrate benefits of pipelined systems

Course Contents:

Unit	Teaching Hour
Unit 1: Data Representation (4 Hrs.)	
1.1 Data Representation: Binary Representation, BCD, Alphanumeric Representation, Complements (*(r-1)'s Complement and r's complement)*, Fixed Point representation, Representing Negative Numbers, Floating Point Representation, Arithmetic with Complements (*Subtraction of Unsigned Numbers, Addition and Subtraction of Signed Numbers)* Overflow, Detecting Overflow	**2 Hour**
1.2 Other Binary Codes: Gray Code, self Complementing Code, Weighted Code (*2421 and 8421 codes*), Excess-3 Code, EBCDIC	**1 Hour**
1.3 Error Detection Codes: Parity Bit, Odd Parity, Even parity, Parity Generator & Checker	**1 Hour**

Unit 2: Register Transfer and Microoperations (5)	
2.1 Register Transfer Language: Microoperation, Register Transfer Language, Register Transfer, Control Function	**0.5 Hour**
2.2 Arithmetic Microoperations: *List of Arithmetic Microoperations*, Binary Adder, Binary Adder-subtractor, Binary Incrementer, Arithmetic Circuit	**2 Hour**
2.3 Logic Microoperations: *List of Logic Microoperations*, Hardware Implementation, Applications of Logic Microoperations.	**1.5 Hour**
2.1 Shift Microoperations: Logical Shift, Circular shift, Arithmetic Shift, Hardware Implementation of Shifter.	**1 Hour**
Unit 3: Basic Computer Organization and Design (8)	
3.1 Basic Concepts: Instruction Code, Operation Code, *Concept of Instruction Format*, Stored Program Concept.	**0.5 Hour**
3.2 Basic Computer Registers and Memory: *List of Registers, Memory of Basic Computer*, Common Bus System for Basic Computer.	**1 Hour**
3.3 Basic Computer Instructions: Instruction Format, Instruction Set Completeness, Control Unit of Basic Computer, Control Timing Signals	**1.5 Hour**
3.4 Instruction Cycle of Basic Computer: *Fetch and Decode*, Determining Type of Instruction, Memory Reference Instructions, Input-Output Instructions, *IO Interrupt*, Program Interrupt, Interrupt Cycle.	**4 Hour**
3.5 Description and Flowchart of Basic Computer	**1 Hour**

Unit 4: Microprogrammed Control (4)	
4.1 **Introduction:** *Hardwired and Microprogrammed Control Unit*, Control Word, Microprogram, Control Memory, Control Address Register, Sequencer, 4.2 **Address Sequencing:** Conditional Branch, Mapping of Instructions, Subroutines, Microinstruction Format, Symbolic Microinstructions **4.3 Design of Control Unit:** *Decoding, Microprogram Sequencer.*	**0.5 Hour** **2 Hour** **1.5 Hour**
Unit 5: Central Processing Unit (4)	
5.1 Introduction: Major Components of CPU, CPU Organizations (*Accumulator Based Organization, General Register Organization, Stack Based Organization*) **5.2 CPU Instructions**: Instruction Formats, Addressing Modes, Types of Instructions (*on the basis of numbers of addresses, on the basis of type of operation*: *data transfer instructions, data manipulation instructions, program control instructions)*, Program Control, Subroutine Call and Return, Types of Interrupt **5.3 RISC and CISC:** RISC vs CISC, Pros and Cons of RISC and CISC, Overlapped Register Windows	**0.5 Hour** **2.5 Hour** **1 Hour**
Unit 6: Pipelining (6)	
6.1 Introduction: Parallel Processing, Multiple Functional Units, Flynn's Classification	**0.5 Hour**
6.2 Pipelining: Concept and Demonstration with Example, Speedup Equation, Floating Point addition and Subtraction with Pipelining	**1.5 Hour**

6.3 Instruction Level Pipelining: *Review of* Instruction Cycle, Three & Four-Segment Instruction Pipeline, Pipeline Conflicts and Solutions (*Resource Hazards, Data Hazards, Branch Hazards*)	**3 Hour**
6.4 Vector Processing: *Concept and* Applications, Vector Operations, Matrix Multiplication	**1 Hour**
Unit 7: Computer Arithmetic (6)	
7.1 **Addition and Subtraction:** Addition and Subtraction with Signed Magnitude Data (*Algorithm and Hardware Implementation*), Addition and Subtraction with Signed 2's Complement Data (*Algorithm and Hardware Implementation*) **7.2 Multiplication and Division:** Multiplication of Signed Magnitude Data, Booth Multiplication (*Algorithm and Hardware Implementation),* Restoring and Non-restoring Division Algorithm, Divide Overflow (*Algorithm and Hardware Implementation*).	**2 Hour** **4 Hour**
Unit 8: Input Output Organization (4)	
8.1 Input-Output Interface: *Why IO Interface?*, I/O Bus and Interface Modules, I/O vs Memory Bus, Isolated vs Memory-Mapped I/O **8.2 Asynchronous Data Transfer**: Strobe, Handshaking **8.3 Modes of Transfer**: Programmed I/O, Interrupt-Initiated I/O, Direct memory Access **8.4 Priority Interrupt**: Polling, Daisy-Chaining, Parallel Priority Interrupt **8.5 DMA and IOP**: Direct Memory Access, Input-Output Processor, DMA vs IOP	**1 Hour** **0.5 Hour** **0.5 Hour** **1 Hour** **1 Hour**
Unit 9: Memory Organization (4)	
9.1 Introduction: Memory Hierarchy, Main Memory, RAM and ROM Chips, Memory address Map, Memory Connection to	**1 Hour**

CPU, Auxiliary Memory (*Review of* magnetic Disk, Magnetic Tape) **9.2 Associative Memory**: Hardware Organization, Match Logic, Read Operation, Write Operation **9.3 Cache Memory**: Locality of Reference, Hit & Miss Ratio, Mapping, Write Policies	 **1.5 Hour** **1.5 Hour**

Text Book

- M. Morris Mano, "Computer System Architecture", Prentice-Hall of India, Pvt. Ltd., Third edition, 2007

References

- William Stallings, "Computer Organization and Architecture", Prentice-Hall of India, Pvt. Ltd., Seventh edition, 2005.
- Vincent P. Heuring and Harry F. Jordan, "Computer System Design and Architecture", Prentice-Hall of India, Pvt. Ltd., Second edition, 2003.

Laboratory Work

Student should be able to implement and simulate the algorithms by using high level languages like C/Matlab and/or VHDL/Verilog. Laboratory work must include following exercises:

1 Laboratory work for familiarizing with the syntax, data types, and operators of Verilog/VHDL
2 Design of n-bit 2's complement adder/subtractor
3 Design of Overflow detector in signed number addition
4 Design of parity generator and parity checker
5 Design of encoder and decoders
6 Design of multiplexer
7 Design of registers and memory
8 Memory Mapping
9 Design of control unit
10 Design of ALU

11 Design of CPU

12 Simulation of 5 stage or 4 stage or 3 stage pipelining

13 Simulation of addition and subtraction of signed 2's complement data

14 Simulation of multiplication and division algorithms

Model Questions

Long Answer Questions

1 What is meant by instruction set completeness? Is instruction set of basic computer complete? Discuss instruction cycle of basic computer with suitable flowchart.

2 What is the concept behind pipelining? Discuss different types of pipeline conflicts and their possible solutions briefly

3 Multiply (-13) x (+40) using Booth multiplication algorithm.

Short Answer Questions

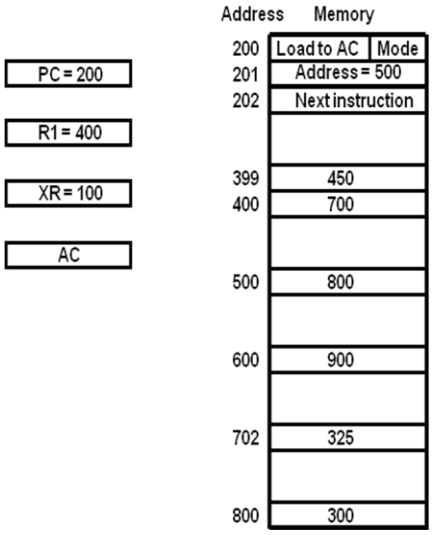
4 What is overflow? Explain overflow detection process with signed and unsigned number addition with suitable example.

5 Write down different arithmetic Microoperations and design a 4-bit binary adder-subtractor.

6 What is the purpose and advantage of common bus system? Explain common bust system of basic computer.

7 What is meant by address sequencing? Draw diagram of address sequencer and Explain in detail about mapping of instruction.

8 Consider that we are provided with following memory content. What will be the value loaded in AC if addressing mode is direct, indirect, immediate, PC-relative and index relative.



9 Define priority interrupt. Explain Daisy-chaining method of handling interrupt priority.

10 What is cache mapping? Explain direct mapping with suitable example.

11 What is space-time diagram? Discuss pipeline speedup equation with suitable example

12 Write short notes on

a) Excess-3 code

b) Input-output processor