Khandaker Shams Arefin

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PROFESSIONAL EXPERIENCE

Engineer, Standard cell & Memory Layout (CSD), Ulkasemi Pvt. Ltd. January '24- Present

- Working on **MRAM** project in **Global Foundries 12LPP.**

Assistant Engineer, Memory Layout, CSD, Ulkasemi Pvt. Ltd. November '22- December '23

- Successfully submitted Standard Cell library development project in **Global Foundries 90sw-soi**
  Major blocks: SDFF, DFF, Full Adder, Half Adder, MUX, etc.

Trainee Engineer, CSD, Ulkasemi Pvt. Ltd. August '22- October '22

- Layout compaction of **MicroLED** project in **Global Foundries 22FDXPLUS**
- Layout compaction of **MicroLED** project in **Global Foundries 28SLPe**
- Layout, LVS and DRC of different blocks of **WSLM** IP, such as **Column MUX, Row Decoder, Column Decoder, Word Line Driver, Bitcell Array**; in **GF's 22FDX**

PROFESSIONAL EXPERTISE

- Layout experience in **Global Foundries 12LP, 12LPP, 22FDX**, **22FDXPLUS, 28FDX, 55BCD, 90SW-SOI**
- Designed layout from standard cell to Hierarchal Blocks
- Chip-top floor planning
- Debugging LVS, DRC, ERC, Antenna, EM, and IR issues.
- Critical net shielding, Device shielding, Device matching
- Providing guidance and training to trainee engineers

RESEARCH INTERESTS

AI Hardware Accelerator, High Performance Computing, Neural Network, Low Power VLSI Circuits

RESEARCH WORKS & PROJECTS

- **Edge AI: ANN Hardware Accelerator for Microcontrollers via SPI Interface** (On-going)
  To enhance security in the current age of AI, neural network computations need to be performed on the edge. However, current microcontrollers lack the computational power required for this task. Therefore, a separate ASIC (Application-Specific Integrated Circuit) is necessary to handle these computations in parallel. This ASIC is designed with parallel multiplication and accumulation units, as well as memory blocks to store the data. It serves as a generalized Artificial Neural Network (ANN) accelerator for microcontrollers, capable of implementing ANNs with any architecture. The circuit have been tested with various datasets, including MNIST, Fashion MNIST, CIFAR-10, and CIFAR-100, across different layers and neuron configurations. The circuit successfully implemented these Artificial Neural Networks.
  Supervisor: Prof. Dr. Satyendra Nath Biswas
  Tools Used: ModelSim, MATLAB, Cadence Virtuoso
  PDK Used: Global Foundries 12nm FinFET and 22nm FDSOI Technology
- **Efficient Floating Point Arithmetic Unit for Neural Network Hardware Acceleration** (On-going)
  Floating point arithmetic is the Achilles' heel for neural network accelerators. Despite advancements, traditional floating point arithmetic units consume substantial cycles, power, and area. To address this, a multiplication unit based on logarithmic multiplication and an addition unit has been designed, which requires considerably less time, power, and area. This multiplication unit has an error rate ranging from +5% to -6%, but when tested with actual neural network datasets such as MNIST, Fashion MNIST, and CIFAR-10, it demonstrated less than 1% error in accuracy compared to MATLAB results, due to the inherent nature of how neural networks operate.
  Tools Used: Cadence Virtuoso, ModelSim, MATLAB

PDK Used: Global Foundries 12nm FinFET and 22nm FDSOI Technology

- **Design and Hardware implementation of human detection robot with voice control & navigation using machine learning.** (Undergrad Thesis)
  This research introduces a personal assistant robot based on AI with Raspberry pi. The robot will communicate with the instructor via a local Wi-Fi network using various means like gesture control, voice control, gyroscope control and direct control. wallets. The possible application of this robot can be home and hospitals.
  Supervisor: Kazi Tauseef Mohammad
  Tool: Tensorflow

- **Motor driver and charger unit for Team Red-X in efficient vehicle challenge technofest 2022.**
  High performance motor driver design for efficient electric vehicle for technofest 2022.
  Supervisor: Kazi Tauseef Mohammad
  Tool: Proteus

- **Avionic system design for AUST Rocketry challenge technofest 2022.**
  Avionic system for model rocket, technofest 2022.
  Supervisor: Prof. Dr. Omar Farrok
  Tool: Proteus, Arduino IDE

PUBLICATIONS

- S.M Kifayat Kabir, Chamak Ganguly, **Khandaker Shams Arefin**, Nawrin Tamim Adity, Satyendra N. Biswas "Analysis of a 10T Full Adder with a new 4T X-NOR using FD-SOI 22nm Mix-VT Technology" 26th International Conference on Computer and Information Technology (ICCIT), 2023.
- Chamak Ganguly; Mazeda Zafor Meem; Mohammed Abdullah Faruque; S. M Kifayat Kabir; Saeed Hossen Rakib; **Khandaker Shams Arefin**; "Comparative Analysis of a Proposed Low-Power Adiabatic NOR Gate," 26th International Conference on Computer and Information Technology (ICCIT), 2023.

ACADEMIC BACKGROUND

November '16- June '22

Ahsanullah University of Science and Technology (AUST)
B.Sc. in Electrical and Electronic Engineering (EEE) CGPA: **2.8**/4.00

TECHNICAL SKILLS

- **Programming Language:** Python, C++, Verilog HDL, MATLAB, System Verilog, HTML5, Skill
- **Layout Design:** Cadence Virtuoso Layout Editor
- **Schematic Design:** Cadence Virtuoso Schematic Editor, Proteus, LTspice, Pspice
- **Simulation:** ModelSim, Quartus II
- **Embedded System:** Arduino,stm32, esp32,pi pico, FPGA

AWARDS & ACHIEVEMENTS

- **2nd position,** Educative Tutorial Competition 2020- BRACU student Branch Chapter
- **Scholarship,** Education Board Scholarship

LEADERSHIP & TEAMWORK

- General Member, IEEE AUST Student Branch (IASB)
- Program Coordinator, IEEE AUST SB
- Vice president of gov. science college science club
- Team leader (Solid Engine and Design) at AUST Rocketry