**Course Code: EE461 Lab**

**Lab -07**

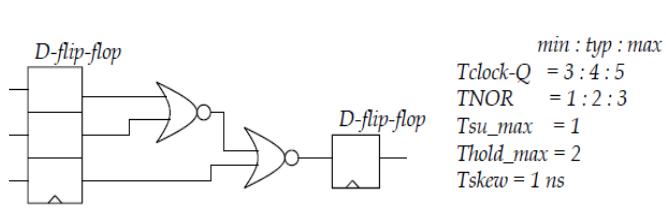
**PREPARED BY**

**Khandoker Samiul Hoque**

**Student Id: 19837**

**Exercises**

What is the fastest clock frequency given the following circuit and delay values? Is there potential for a hold violation?

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**Solution:**

Here,

Propagation delay is 5ns+6ns +1ns = 12ns. Therefore, in that case fastest clock frequency will be

= 76.9 MHz

Propagation delay of the first flip-flop plus propagation delay through one NOR gate is 5ns + 3ns = 8ns from the D input of the second flip-flop to the output of the first NOR gate.

Thold + Tskew <= T cqmin + TNORmin ,Here , Thold <= 3ns +1ns -1ns = 3 ns

So its true, Thold = 2 ns . So there should not be any hold-time valuation.