Lab 1 : Logic Gates

ITI 1100 - Digital Systems
Winter 2018
School of Electrical Engineering and Computer Science
University of Ottawa

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Experiment Date : 22 January 2018
Submission Date : 4 February 2018

Objectives :

- Construct logic circuits
- Determine the function of the circuits
- Determine all the outputs of the circuits with different inputs (truth tables)
- Determine what logic gates are equivalent to the circuits constructed
- Compare theoretical outputs to experimental outputs

Equipment and Components :

- Quartus II 13.0 Service-Pack 1
- Altera DE2-115 card

Circuit Diagrams :

Part 1 - Combinational Logic Circuits Construction

One-Chip Logic Circuit

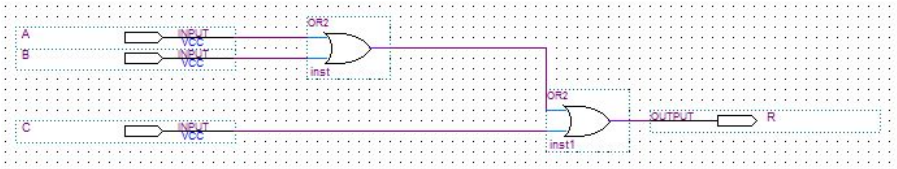

Figure 1: Screenshot of One-chip logic circuit diagram (Figure 5.1.1 of Lab Manual)

Two-Chip Logic Circuit

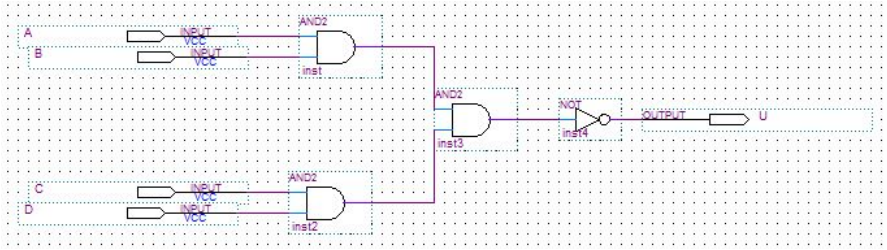

Figure 2: Screenshot of Two-chip logic circuit diagram (Figure 5.1.2 of Lab Manual)

Three-Chip Logic Circuit

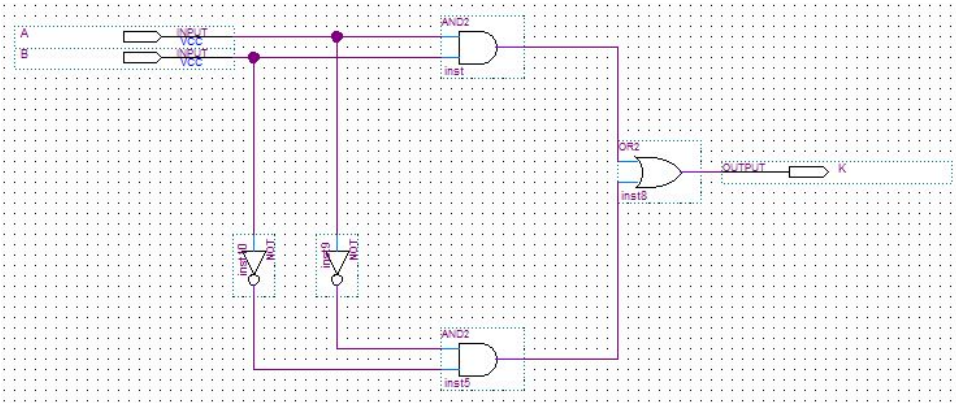

Figure 3: Screenshot of Three-chip logic circuit diagram (Figure 5.1.3 of Lab Manual)

Part II - Combinational Logic Circuits Analysis

Exclusive OR Circuit

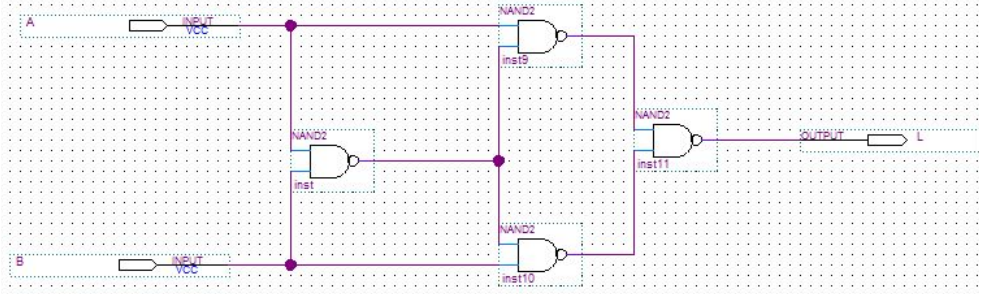

Figure 4: Screenshot of Exclusive OR Circuit diagram (Figure 5.1.5 of Lab Manual)

AND Circuit

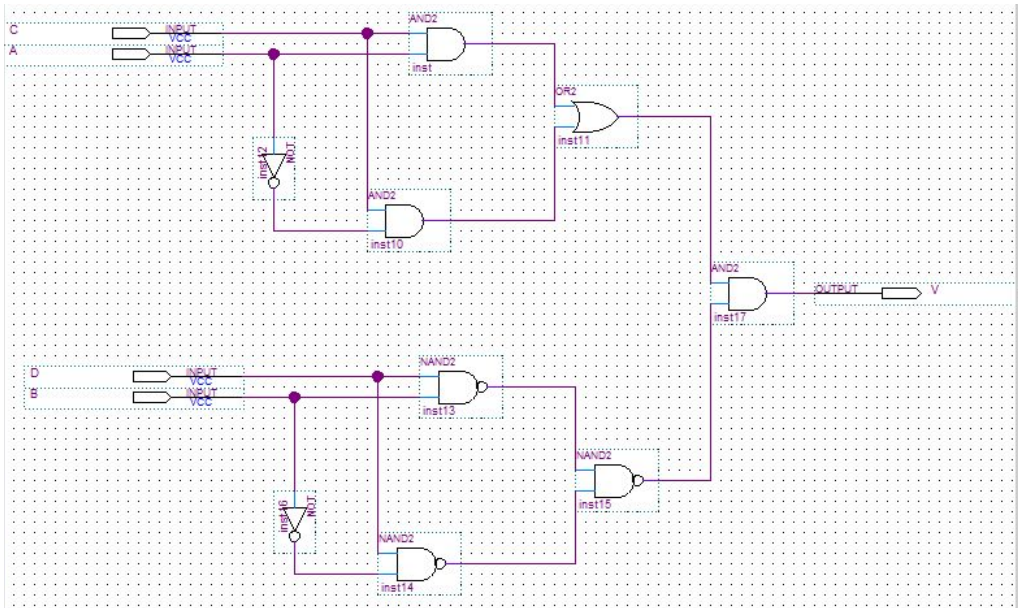

Figure 5: Screenshot of AND Circuit diagram (Figure 5.1.6 of Lab Manual)

Multiple Output Circuit

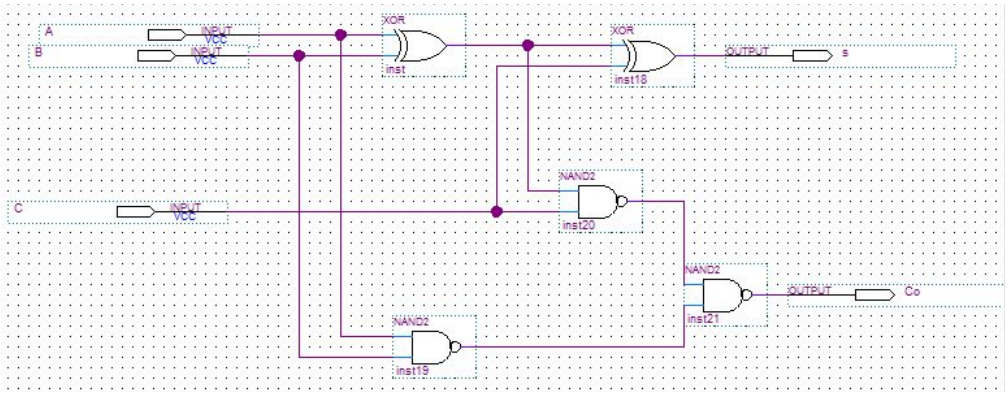

Figure 6: Screenshot of Multiple Output Circuit diagram (Figure 5.1.8 of Lab Manual)

Experimental Data and Data Processing :

Part 1 - Combinational Logic Circuits Construction

One-Chip Logic Circuit

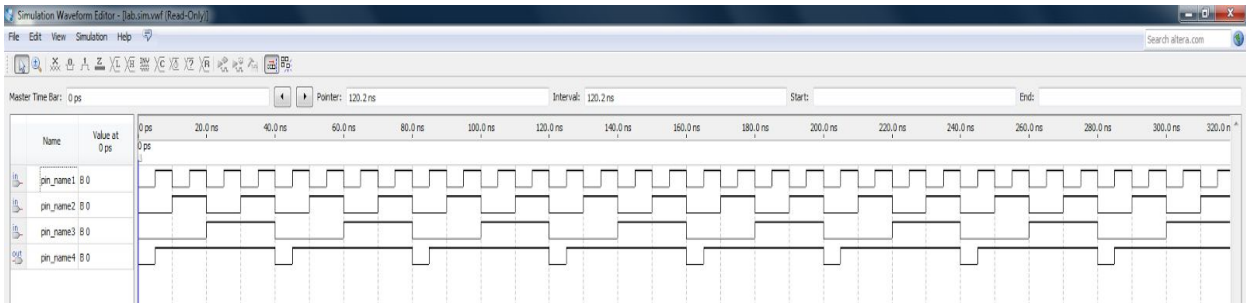

Figure 7 : Simulation Output Waveform of One-Chip Logic Circuit

Inputs			Outputs
A	**B**	**C**	**R**
0	**0**	**0**	**0**
1	**0**	**0**	**1**
0	**1**	**0**	**1**
0	**0**	**1**	**1**
1	**1**	**0**	**1**
1	**0**	**1**	**1**
0	**1**	**1**	**1**
1	**1**	**1**	**1**

Table 1 : Experimental Data Observed From the Altera DE2-115 card

Two-Chip Logic Circuit

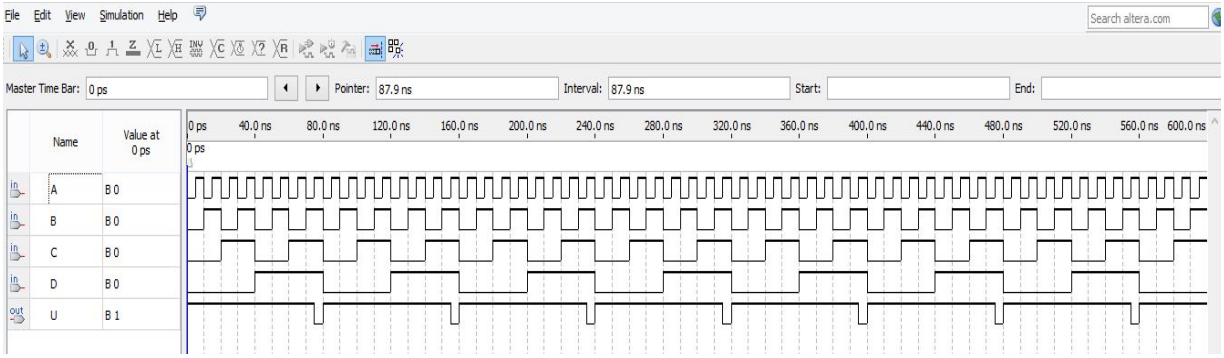

Figure 8 : Simulation Output Waveform of Two-Chip Logic Circuit

Inputs				Outputs
A	**B**	**C**	**D**	**U**
0	**0**	**0**	**0**	**1**
1	**0**	**0**	**0**	**1**
0	**1**	**0**	**0**	**1**
0	**0**	**1**	**0**	**1**
0	**0**	**0**	**1**	**1**
1	**1**	**0**	**0**	**1**
1	**0**	**1**	**0**	**1**
1	**0**	**0**	**1**	**1**
0	**1**	**1**	**0**	**1**
0	**1**	**0**	**1**	**1**
0	**0**	**1**	**1**	**1**
1	**1**	**1**	**0**	**1**
1	**1**	**0**	**1**	**1**
0	**1**	**1**	**1**	**1**
1	**0**	**1**	**1**	**1**
1	**1**	**1**	**1**	**0**

Table 2 : Experimental Data Observed From the Altera DE2-115 card

Three-Chip Logic Circuit

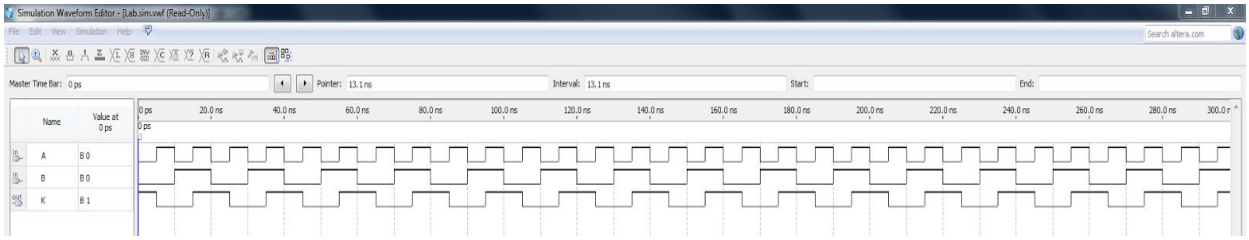

Figure 9 : Simulation Output Waveform of Three-Chip Logic Circuit

Inputs		Outputs
A	B	K
0	0	1
1	0	0
0	1	0
1	1	1

Table 3 : Experimental Data Observed From the Altera DE2-115 card

Part II - Combinational Logic Circuits Analysis

Exclusive OR Circuit

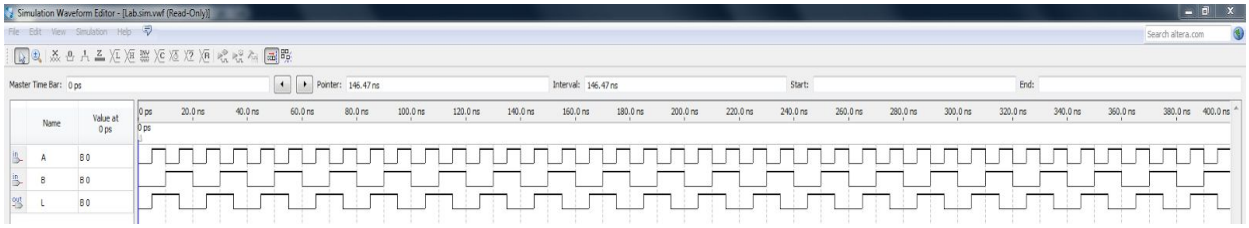

Figure 10 : Simulation Output Waveform of Exclusive OR Circuit

Inputs		Outputs
A	B	L
0	0	0
1	0	1
0	1	1
1	1	0

Table 4 : Experimental Data Observed From the Altera DE2-115 card

AND circuit

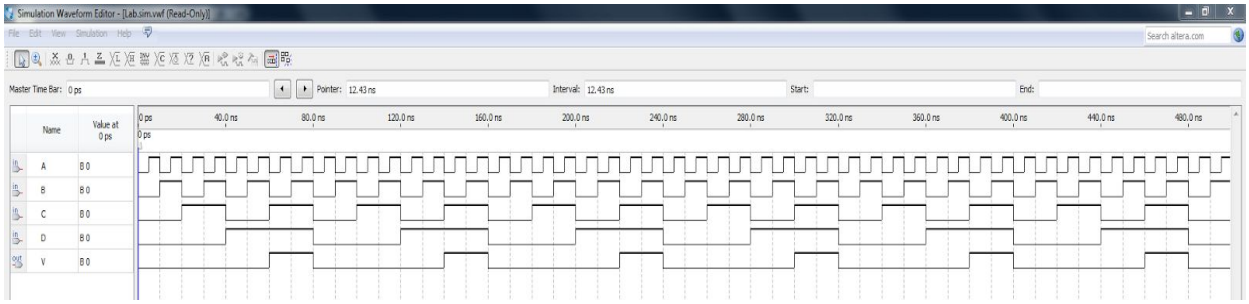

Figure 11 : Simulation Output Waveform of AND Circuit

Inputs				Outputs
A	**B**	**C**	**D**	**V**
0	**0**	**0**	**0**	**0**
1	**0**	**0**	**0**	**0**
0	**1**	**0**	**0**	**0**
0	**0**	**1**	**0**	**0**
0	**0**	**0**	**1**	**0**
1	**1**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**
1	**0**	**0**	**1**	**0**
0	**1**	**1**	**0**	**0**
0	**1**	**0**	**1**	**0**
0	**0**	**1**	**1**	**1**
1	**1**	**1**	**0**	**0**
1	**1**	**0**	**1**	**0**
0	**1**	**1**	**1**	**1**
1	**0**	**1**	**1**	**1**
1	**1**	**1**	**1**	**1**

Table 5 : Experimental Data Observed From the Altera DE2-115 card

Multiple Output Circuit

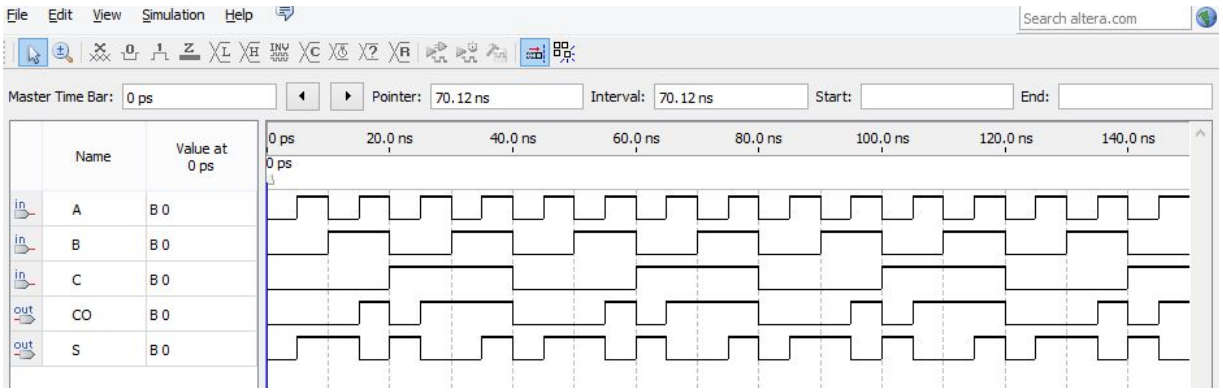

Figure 12 : Simulation Output Waveform of Multiple Output Circuit

Inputs			Outputs	
A	**B**	**C**	**S**	**Co**
0	**0**	**0**	**0**	**0**
1	**0**	**0**	**1**	**0**
0	**1**	**0**	**1**	**0**
0	**0**	**1**	**1**	**0**
1	**1**	**0**	**0**	**1**
1	**0**	**1**	**0**	**1**
0	**1**	**1**	**0**	**1**
1	**1**	**1**	**1**	**1**

Table 6 : Experimental Data Observed From the Altera DE2-115 card

Comparison of Expected Data and Experimental Data :

Part 1 - Combinational Logic Circuits Construction

One-Chip Logic Circuit

Inputs			Expected Outputs	Actual Outputs
A	**B**	**C**	**R**	**R**
0	**0**	**0**	**0**	**0**
1	**0**	**0**	**1**	**1**
0	**1**	**0**	**1**	**1**
0	**0**	**1**	**1**	**1**
1	**1**	**0**	**1**	**1**
1	**0**	**1**	**1**	**1**
0	**1**	**1**	**1**	**1**
1	**1**	**1**	**1**	**1**

Table 7 : Comparison of Expected Data and Experimental Data for One-Chip Logic Circuit

Two-Chip Logic Circuit

Inputs				Expected Outputs	Actual Outputs
A	**B**	**C**	**D**	**U**	**U**
0	**0**	**0**	**0**	**1**	**1**
1	**0**	**0**	**0**	**1**	**1**
0	**1**	**0**	**0**	**1**	**1**
0	**0**	**1**	**0**	**1**	**1**
0	**0**	**0**	**1**	**1**	**1**
1	**1**	**0**	**0**	**1**	**1**
1	**0**	**1**	**0**	**1**	**1**
1	**0**	**0**	**1**	**1**	**1**
0	**1**	**1**	**0**	**1**	**1**
0	**1**	**0**	**1**	**1**	**1**
0	**0**	**1**	**1**	**1**	**1**
1	**1**	**1**	**0**	**1**	**1**
1	**1**	**0**	**1**	**1**	**1**
0	**1**	**1**	**1**	**1**	**1**
1	**0**	**1**	**1**	**1**	**1**
1	**1**	**1**	**1**	**0**	**0**

Table 8 : Comparison of Expected Data and Experimental Data for Two-Chip Logic Circuit

Three-Chip Logic Circuit

Inputs		Expected Outputs	Actual Outputs
A	**B**	**K**	**K**
0	**0**	**1**	**1**
1	**0**	**0**	**0**
0	**1**	**0**	**0**
1	**1**	**1**	**1**

Table 9 : Comparison of Expected Data and Experimental Data for Three-Chip Logic Circuit

Part II - Combinational Logic Circuits Analysis

Exclusive OR Circuit

Inputs		Expected Outputs	Actual Outputs
A	**B**	**L**	**L**
0	**0**	**0**	**0**
1	**0**	**1**	**1**
0	**1**	**1**	**1**
1	**1**	**0**	**0**

Table 10 : Comparison of Expected Data and Experimental Data for Exclusive OR Circuit

AND circuit

Inputs				Expected Outputs	Actual Outputs
A	**B**	**C**	**D**	**V**	**V**
0	**0**	**0**	**0**	**0**	**0**
1	**0**	**0**	**0**	**0**	**0**
0	**1**	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**0**	**0**
0	**0**	**0**	**1**	**0**	**0**
1	**1**	**0**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**	**0**
1	**0**	**0**	**1**	**0**	**0**
0	**1**	**1**	**0**	**0**	**0**
0	**1**	**0**	**1**	**0**	**0**
0	**0**	**1**	**1**	**1**	**1**
1	**1**	**1**	**0**	**0**	**0**
1	**1**	**0**	**1**	**0**	**0**
0	**1**	**1**	**1**	**1**	**1**
1	**0**	**1**	**1**	**1**	**1**
1	**1**	**1**	**1**	**1**	**1**

Table 11 : Comparison of Expected Data and Experimental Data for AND Circuit

Multiple Output Circuit

Inputs			Expected Outputs		Actual Outputs	
A	**B**	**C**	**S**	**Co**	**S**	**Co**
0	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**0**	**1**	**0**	**1**	**0**
0	**1**	**0**	**1**	**0**	**1**	**0**
0	**0**	**1**	**1**	**0**	**1**	**0**
1	**1**	**0**	**0**	**1**	**0**	**1**
1	**0**	**1**	**0**	**1**	**0**	**1**
0	**1**	**1**	**0**	**1**	**0**	**1**
1	**1**	**1**	**1**	**1**	**1**	**1**

Table 12 : Comparison of Expected Data and Experimental Data for Multiple Output Circuit

Discussion & Conclusions :

In this experiment we constructed six circuits and tested them to determine the function of each circuit. With those tests we were able to construct truth tables and compare them to the ones we made in the prelab. According to our comparisons, the outputs we expected were always the same as the ones we obtained experimentally. No matter which circuit we tested, the expected results were the same as the actual ones. For the one-chip logic circuit we determined that the logic gate equivalent to that circuit is the OR gate. For the two-chip logic circuit the equivalent gate is the NAND gate. The three-chip logic circuit appears to be equivalent to an XNOR gate. In part 2, we constructed a circuit that is equivalent to a XOR gate, a circuit that was equivalent to an AND gate for the C and D inputs and finally a circuit with 2 outputs. We were able to accomplish all objectives with no issues whatsoever.

Appendix (Prelab) :

5.1.1 R=A+B+C

A	B	C	A+B	(A+B)+C
0	0	0	0	0
1	0	0	1	1
0	1	0	1	1
0	0	1	0	1
1	1	0	1	1
0	1	1	1	1
1	0	1	1	1
1	1	1	1	1

5.1.2 U=(ABCD)`

A	B	C	D	AB	CD	ABCD	(ABCD)`
0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	1
0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	1
1	1	0	0	1	0	0	1
1	0	1	0	0	0	0	1
1	0	0	1	0	0	0	1
0	1	1	0	0	0	0	1

0	**1**	**0**	**1**	**0**	**0**	**0**	**1**
0	**0**	**1**	**1**	**0**	**1**	**0**	**1**
1	**1**	**1**	**0**	**1**	**0**	**0**	**1**
1	**0**	**1**	**1**	**0**	**1**	**0**	**1**
1	**1**	**0**	**1**	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**0**	**1**	**0**	**1**
1	**1**	**1**	**1**	**1**	**1**	**1**	**0**

5.1.3 K=AB + A`B`

A	B	AB	A`	B`	A`B`	AB + A`B`
0	**0**	**0**	**1**	**1**	**1**	**1**
1	**0**	**0**	**0**	**1**	**0**	**0**
0	**1**	**0**	**1**	**0**	**0**	**0**
1	**1**	**1**	**0**	**0**	**0**	**1**

5.1.5 L= [[A(AB)`]` . [B(AB)`]`]`

A	B	(AB)`	[A(AB)`]`	[B(AB)`]`	[[[A(AB)`]` . [B(AB)`]`]`
0	**0**	**1**	**1**	**1**	**0**
1	**0**	**1**	**0**	**1**	**1**
0	**1**	**1**	**1**	**0**	**1**
1	**1**	**0**	**1**	**1**	**0**

5.1.6 V= (AC+A`C) ((BD)` . (B`D)`)`

A	B	C	D	AC	A`C	AC+A`C	(BD)`	(B`D)`	[(BD)` (B`D)`]`	V
0	0	0	0	0	0	0	1	1	0	0
1	0	0	0	0	0	0	1	1	0	0
0	1	0	0	0	0	0	1	1	0	0
0	0	1	0	0	1	1	1	1	0	0
0	0	0	1	0	0	0	1	0	1	0
1	1	0	0	0	0	0	1	1	0	0
1	0	1	0	1	0	1	1	1	0	0
1	0	0	1	0	0	0	1	0	1	0
0	1	1	0	0	1	1	1	1	0	0
0	1	0	1	0	0	0	0	1	1	0
0	0	1	1	0	1	1	1	0	1	1
1	1	1	0	1	0	1	1	1	0	0
1	0	1	1	1	0	1	1	0	1	1
1	1	0	1	0	0	0	0	1	1	0
0	1	1	1	0	1	1	0	1	1	1
1	1	1	1	1	0	1	0	1	1	1

5.1.7 P= (AB+A`C) + (B`(A+C))

A	B	C	A+C	B`(A+C)	AB	A`C	(AB)+(A`C)	P
0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	1
0	1	0	0	0	0	0	0	0
0	0	1	1	1	0	1	1	1
1	1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	0	1
0	1	1	1	0	0	1	1	1
1	1	1	1	0	1	0	1	1

5.1.8 S = C⊕(A⊕B) **C_0 = [(AB)` . (C(A⊕B))`]`**

A	B	C	A⊕B	C⊕(A⊕B) S	(AB)`	(C(A⊕B))`	[(AB)` . (C(A⊕B))`]` C_0
0	0	0	0	0	1	1	0
1	0	0	1	1	1	1	0
0	1	0	1	1	1	1	0
0	0	1	0	1	1	1	0
1	1	0	0	0	0	1	1
1	0	1	1	0	1	0	1
0	1	1	1	0	1	0	1

1	**1**	**1**	**0**	**1**	**0**	**1**	**1**