CSE2312 Computer Organization & Assembly Language Programming
QUIZ 2 (Chapter 2)

Student Name: _____.

Student ID: _____.

TRUE OR FALSE (2pts per, 20 pts total)

Q:	1	2	3	4	5	6	7	8	9	10
T/F	T	F	F	T	T	T	F	F	T	F

1. The Data Path Cycle defines what the computer can do. The faster the data path cycles is, the faster the computer runs. T

2. Program Counter (PC) is a special register and counts on how many instructions have been executed. F

3. When designing instructions, how long an instruction actually took mattered more than how many could be started per second. F

4. One of benefits of the simple computer with interpreted instructions is the ability to fix incorrectly implemented instructions or make up for design deficiencies in the basic hardware. T

5. Locality Principle is used in cache design. It means that: when a word is referenced, it and some of its neighbors are brought from large slow memory to the cache. T

6. The number of bits in the address determines the maximum number of directly addressable cells in the memory and independent of the number of bits per cell. T

7. Both the magnetic disk and CD has the constant angular velocity. F

8. The Hamming distance between 00001001 and 10011001 is 3. F

9. Both of RAID 0 and RAID 4 work with strips. T

10. The heads of the magnetic disk actually touch the diskettes. F

MULTIPLE CHOICES (4 pts each, 20 pts total)

1. What are the design principles for modern computers? [a, b, c, d]
(a) Instructions directly executed by hardware
(b) Provide plenty of registers
(c) Instructions should be easy to decode
(d) Only loads, stores should reference memory
(e) Minimize rate at which instructions are issued

2. Which of following is true for the Cell? [a, b, d]
(a) Memories consist of a number of cells
(b) A cell with k bits can hold one of 2^k different bit combinations
(c) If an address has m bits, the maximum number of cells addressable is 2m
(d) The number of bits in the address determines the maximum number of directly addressable cells in the memory and independent of the number of bits per cell

3. Which of following is true for the byte? [a, c]
(a) 1 byte is 8-bit
(b) 1 byte is 4-bit
(c) 64-bit Word: 8 bytes per word
(d) 32-bit Word: 8 bytes per word

4. Which of following is true for the CD and magnetic disk? [b, b]
(a) CD has constant angular velocity
(b) CD has constant linear velocity
(c) Magnetic Disk has constant angular velocity
(d) Magnetic Disk has constant linear velocity

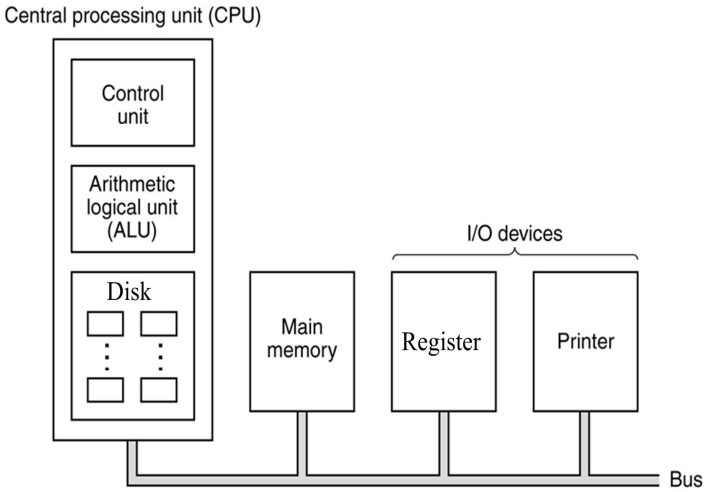
5. Which of following is true for ASDL and Cable? [b, c]
(a) ASDL service is not constant
(b) ASDL service is constant
(c) Cable service is not constant
(d) Cable service is constant

6. Which of following is software task in camera? [a, b, c, d]

(a) Setting the focus
(b) Determine exposure
(c) Performing the white balance
(d) Possibly localizing human faces

Fill in the Blanks and Short Answer (4 pts each, 20 pts total)

1. The following diagram gives the organization of a simple computer with one CPU and two I/O devices. Is it correct? If not, please correct it in the diagram.



Solution:

This is incorrect. In place of Disk, it should be Register. In place of Register, it should be Disk.

2. Three kinds of mice have been produced to operate the computers. What are they?

Solution:

a) Mechanical
b) Optical
c) Optomechanical.

3. The Fetch-decode-execute cycle is central to the operation of all computers. The steps are as follows:

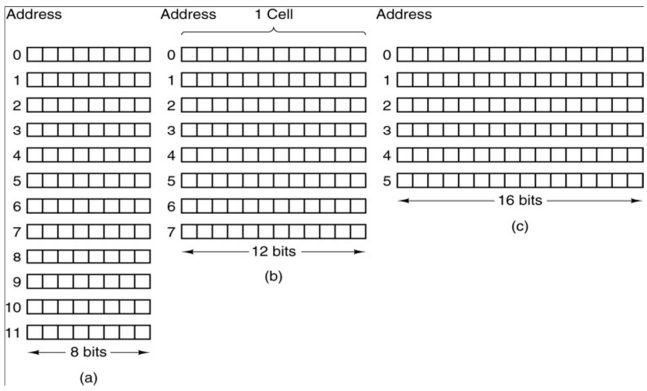
1) Fetch next instruction from memory into instruction register;
2) ?
3) ?
4) If instructions uses a word in memory, determine where it is
5) Fetch the word, if needed, into a CPU register
6) Execute the instruction
7) Go to step 1 to begin executing following instruction

What is the step2 and step 3, respectively ?

Solution:

1) Fetch next instruction from memory into instruction register;
2) Change the program counter to point out the following instruction
3) Determine type of instruction just fetched
4) If instructions uses a word in memory, determine where it is
5) Fetch the word, if needed, into a CPU register
6) Execute the instruction
7) Go to step 1 to begin executing following instruction

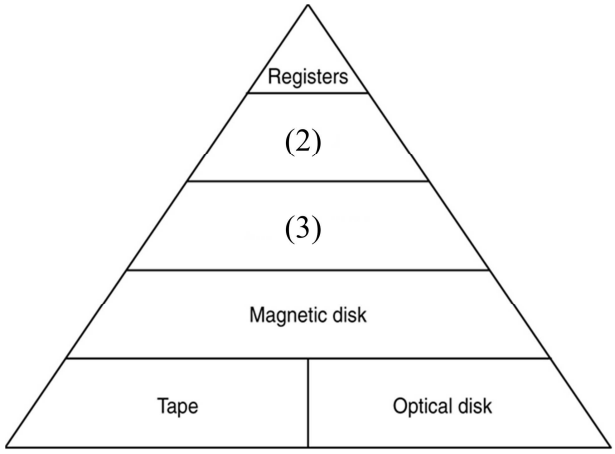
4. How many bits are sufficient for an address to reference the memory of Fig (a), (b), (c) ?



Solution:

4, 3, 3

5. The following diagram gives a 5-level memory hierarchy. What (2) and (3) in the diagram should be? As we move down the hierarchy, three key parameters increase. What are these three key parameters?



Solution:

In (2) → cache. (3) → Main Memory.

a) Access time gets bigger.
b) Storage capacity increases.

Number of bits per dollar increases

Computation and Short Answer (8 pts each, 40 pts total)

1. Consider each instruction has 5 stages in a computer with pipelining techniques. Each stage takes 5 ns.

(1) What is the maximum number of MIPS that this machine is capable of with this 5-stage pipelining techniques?

Solution: 1/5ns = 200MIPS

(2) What is the maximum number of MIPS that this machine is capable of in the absence of pipelining?

Solution: 200/5 = 40MIPS

(3) From the above questions, we can know that the pipelining allows a tradeoff between latency and processor bandwidth. Please explain what is the latency and what is the bandwidth.

Latency: how long it takes to execute an instruction

Processor bandwidth: how many MIPS the CPU has

2. Suppose the memory word is 10010100.

1) To be able to correct single bit error, how many number of check bits we need?

Solution: 4

2) Please give the construction of the even-parity Hamming code for this memory word according to the Hamming algorithm

Solution: 011100110100

3. In a mode-1 CD-ROM, each sector includes a 16 bytes preamble, 2000 bytes data, and 288 bytes error-correcting code.

1) If the CD-ROM has speed 50 sectors/sec, so what is data rate?

50*2000=100,000 bytes/sec

2) If this CD is a 100-minute audio CD, so, what is its data capacity?

100*60*100,000=600,000,000 bytes

4. Suppose we know a video RAM with 1000 x 1000 pixels at 3 bytes per pixel,

1) What is the size for the video RAM at least to store the image?

1000*1000*3= 3,000,000 bytes

2) If display redraw 50 times in a second, how long is the pulse corresponding to one pixel?

1/(1000*1000*50)=20 ns

5. A digital camera has a resolution of 1000*1000 pixels, with 5 bytes/pixel for RGB color.

1) The manufacturer of the camera wants to be able to write a JPEG image at a 10x compression factor to the flash memory in 2 sec. What data rate is required? Assume that 1 MB means 10^6 bytes.

Solution: Each uncompressed image file is 5 million bytes. After 10x compression, it is 1 million bytes. To write this in 2 sec requires a data rate of 0.25 MB/sec.

2) How many pictures can be stored on a 1 GB flash memory card with the compression factor is 10x? Assume that 1 GB means 10^9 bytes.

Solution: The compressed image is 0.5 million bytes. The number of images stored is thus 1000 million / 0.5 million =2000 .