CSE 2312 Computer Organization & Assembly Language Programming Midterm (Spring 2015)

Student Name: _____.

Student ID: _____.

TRUE OR FALSE (1pts per)

Question	1	2	3	4	5	6	7	8	9	10
Answer	F	T	F	F	F	T	F	F	T	T

1. An interpreter converts programs in one language to another, while a translator carries out a program instruction by instruction. F

2. Computer Architecture is to study how to design parts of a computer system that are visible to the programmers. T

3. L1 language is less convenient for people to use than those in built-in machine instructions. F

4. Program Counter (PC) is a special register and counts on how many instructions have been executed. F

5. When designing instructions, how long an instruction actually took mattered more than how many could be started per second. F

6. One of benefits of the simple computer with interpreted instructions is the ability to fix incorrectly implemented instructions or make up for design deficiencies in the basic hardware. T

7. The Hamming distance between 00001001 and 10011001 is 3. F

9. The heads of the magnetic disk actually touch the diskettes. F

8. Both of RAID 0 and RAID 4 work with strips. T

10. The Data Path Cycle defines what the computer can do. The faster the data path cycles is, the faster the computer runs. T

Multiple Choices (2pts each)

(The following questions may have one and more correct answer. Pick all correct answers.)

1. **Which of following is true for Translation and Interpretation?** [a, b, c]

(a) In both of them, the computer carried out instructions in L1 by executing equivalent sequences of instructions in L0

(b) In translation, the entire L1 program is converted to a L0 program.

(c) In interpretation, after each L1 instruction is examined and decoded, it is carried out immediately.

(d) Interpretation is more efficient than Translation

2. **Which of following is true in Multilevel Machines?** [c, d]

(a) Instruction Set Architecture Level lay between Digital Logic Level and Microarchitecture Level.

(b) Assembly Language Level lay between Instruction Set Architecture Level and Operating System Level

(c) Operating System Level lay between Assembly Language Level and Instruction Set Architecture Level

(d) Microarchitecture Level lay between Digital Logic Level and Instruction Set Architecture Level

3. **Which of following is true based on Moore Law:** [b]

(a) 2X processor speed increment every 8 months.

(b) 2X processor speed increment every 18 months.

(c) 4X processor speed increment every 8 months.

(d) 4X processor speed increment every 18 months.

4. **Which of following may affect the execution time?** [a, b, c, d]

(a) Algorithm: determine the number of operations executed

(b) Programming language, compiler, architecture: determine the number of machine instructions executed per operation (IC)

(c) Processor and memory system: determine how fast instructions are executed (CPI) and increase it.

(d) I/O system (including OS): determines how fast I/O operations are executed

5. **What are the design principles for modern computers?** [a, c, d, e]

(a) Instructions directly executed by hardware

(b) Minimize rate at which instructions are issued

(c) Instructions should be easy to decode

(d) Only loads, stores should reference memory

(e) Provide plenty of registers

6. **Which of following is true for the byte?** [b, d]

(a) 1 byte is 4-bit
(b) 1 byte is 8-bit
(c) 32-bit Word: 8 bytes per word
(d) 64-bit Word: 8 bytes per word

7. **Which of following is true for the CD and magnetic disk?** [a, d]

(a) CD has constant linear velocity
(b) CD has constant angular velocity
(c) Magnetic Disk has constant linear velocity
(d) Magnetic Disk has constant angular velocity

8. **Which of following is true for ASDL and Cable?** [a, d]

(a) ASDL service is constant
(b) ASDL service is not constant
(c) Cable service is constant
(d) Cable service is not constant

9. **Which of following is software task in camera?** [a, b, c, d]

(a) Setting the focus
(b) Determine exposure
(c) Performing the white balance
(d) Possibly localizing human faces

10. **Which of following is true for the Cell?** [a, b, d]

(a) Memories consist of a number of cells
(b) A cell with k bits can hold one of 2^k different bit combinations
(c) If an address has m bits, the maximum number of cells addressable is 2m
(d) The number of bits in the address determines the maximum number of directly addressable cells in the memory and independent of the number of bits per cell

11. **Consider a computer with identical interpreters at levels 1, 2, and 3. It takes an interpreter n instructions to fetch, examine and execute one instruction. A level 1 instruction takes k nanoseconds to execute. How long does it take for an instructions at levels 3** [c]

(a) k nanoseconds.
(b) kn nanoseconds.
(c) kn^2 nanoseconds.
(d) kn^3 nanoseconds.

12. What factors could account for the performance discrepancy of computers: [a,b,c,d]

(a) Cycle time.
(b) The number of bytes fetched per cycle.
(c) Memory speed.
(d) I/O architecture.

13. Which of following is not a computer of Von Neumann Architecture: [d]

(a) iPhone.
(b) iPad.
(c) Dell Desktop PC.
(d) Babbage's difference engine.

14. **Which of following is true for the CD and magnetic disk?** [f, g]

(e) CD has constant angular velocity
(f) CD has constant linear velocity
(g) Magnetic Disk has constant angular velocity
(h) Magnetic Disk has constant linear velocity

15. **Which of following is the benefit for RISC compared to CISC?** [a, c]

(a) Instruction can be issued quickly
(b) Provide more powerful instructions for various tasks
(c) More stages of pipeline
(d) Larger number of instructions

Fill in the Blanks and Short Answer (4pts each)

1. **In what sense are hardware and software equivalent? Not Equivalent?**

Solution: Hardware and software are functionally equivalent. Any function done by one can, in principle, be done by the other. They are not equivalent in the sense that to make the machine really run, the bottom level must be hardware, not software. They also differ in performance.

2. **If computer A and Computer B are 10Mhz and 2Ghz respectively, what is their clock times respectively?**

A: 0.1 * 10 ^ (-6) sec.

B: 0.5 * 10 ^ (-9) sec.

3. **The Fetch-decode-execute cycle is central to the operation of all computers. The steps are as follows:**

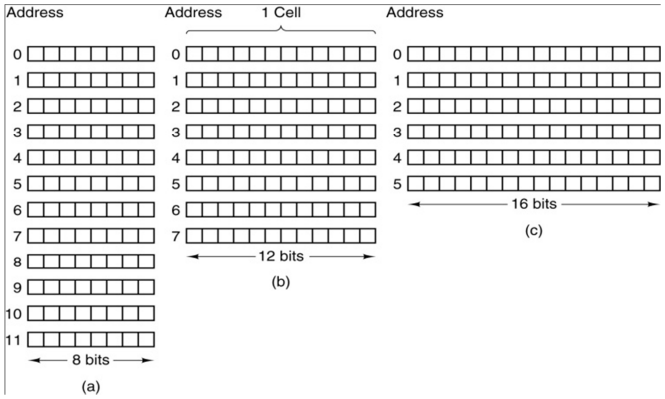
1) Fetch next instruction from memory into instruction register;
2) ?
3) ?
4) If instructions uses a word in memory, determine where it is
5) Fetch the word, if needed, into a CPU register
6) Execute the instruction
7) Go to step 1 to begin executing following instruction

What is the step2 and step 3, respectively ?

Solution:

1) Fetch next instruction from memory into instruction register;
2) Change the program counter to point out the following instruction
3) Determine type of instruction just fetched
4) If instructions uses a word in memory, determine where it is
5) Fetch the word, if needed, into a CPU register
6) Execute the instruction
7) Go to step 1 to begin executing following instruction

4. **How many bits are sufficient for an address to reference the memory of Figure (a), (b), (c) ?**



Solution: 4, 3, 3.

5. What is the key gap in computer design? How to bridge this gap?

Key Gap: Human prefers natural language while it's easy to use machine (binary) language for computers.

Bridging the Gap: Designing a high level language (L1) including a new set of instructions that is more convenient for people to use than those in built-in machine instructions (L0 language).

Computation and Short Answer (8 pts each)

1. **There are two computers: A and B:**

- **Computer A: Cycle Time = 250ps, CPI = 4.0**
- **Computer B: Cycle Time = 600ps, CPI = 10.0**

If they have the same ISA, which computer is faster? How many times it is faster than another?

Solution:

CPU = IC * CPI * Cycle time

So CPU(A) = I*4*250 = 1000I

CPU(B) = I*10*600 = 6000I

So A is (6000/1000) = 6 times faster.

2. **Computer A has 2GHz clock. It takes 10s CPU time to finish one given task. We want to design Computer B to finish the same task within 6s CPU time. The clock cycle number for computer B is 1.5 times as that of Computer A. So, what clock rate should be designed for Computer B?**

Solution:

Clock rate(CR) = Clock Cycle/CPU Time

Clock Cycle(A) = CR(A) * CPU(A) = 2*10^9 * 10=20*10^9

Clock Cycle (B) = 1.5 * Clock Cycle(A) = 30*10^9

CPU(B) = 5s

So Clock Rate(B) = Clock Cycle(B)/CPU(B) = (30/6) * 10^9 = 5 GHz

3. **Consider each instruction has 10 stages in a computer with pipelining techniques. Each stage takes 2 ns.**
   (1) What is the maximum number of MIPS that this machine is capable of with this 10-stage pipelining techniques?
   (2) What is the maximum number of MIPS that this machine is capable of in the absence of pipelining?
   (3) From the above questions, we can know that the pipelining allows a tradeoff between latency and processor bandwidth. Please explain what is the latencyand what is the bandwidth.

Solution:

1) 1/2ns = 500MIPS

2) 500/10 = 50MIPS

3)

Latency: how long it takes to execute an instruction

Processor bandwidth: how many MIPS the CPU has

4. **Devise a 7 bit even parity Hamming code for the digits 0 to 9.**

Solution:

Number	Binary value	Code (1234567)
0	0000	0000000
1	0001	1101001
2	0010	0101010
3	0011	1000011
4	0100	1001100
5	0101	0100101
6	0110	1100110
7	0111	0001111
8	1000	1110000
9	1001	0011001

5. A digital camera has a resolution of 1000*1000 pixels, with 6 bytes/pixel for RGB color.

1) The manufacturer of the camera wants to be able to write a JPEG image at a 6x compression factor to the flash memory in 10 sec. What data rate is required? Assume that 1 MB means 10^6 bytes.

Solution: Each uncompressed image file is 6 million bytes. After 6x compression, it is 1 million bytes. To write this in 10 sec requires a data rate of 0.1 MB/sec.

2) How many pictures can be stored on a 3 GB flash memory card with the compression factor is 2x? Assume that 1 GB means 10^9 bytes.

Solution: The compressed image is 3 million bytes. The number of images stored is thus 3000 million / 3 million =1000 .