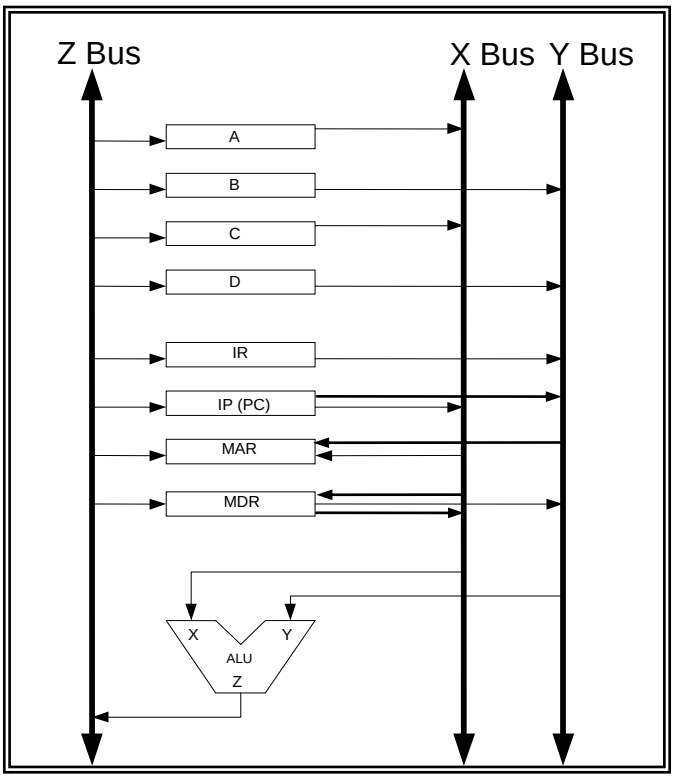
Name:Key ID: Key **Name: Key ID: Key**

Assume that a CPU datapath is connected as shown in the datapath figure. The arithmetic and logic unit (ALU) with inputs X and Y and output Z, can perform any of the operations in the table based on the four selection lines S3,S2,S1, and S0.

Selection lines S3 S2 S1 S0	**ALU Operation**
0000	Z = X
1111	Z = Y
0001	Z = X + 1
0010	Z = X – 1
0011	Z = Y + 2
0100	Z = X + Y
0110	Z = X – Y
0111	Z = Y – X
1000	Z = X **AND** Y
1001	Z = X **OR** Y
1010	Z = X **XOR** Y
1011	Z = SHL X, 1
1100	Z = SHR X, 1

You need to assume the input and output tri-state buffers wherever needed.

Also assume that the instructions for this processor follow the normal 8086 in defining the source and distnation operands.



(i) Suppose the size of each instruction is *two bytes*, write the minimum number of control steps required for fetching an instruction from memory?

T1: IPout-y, MARin-y, Read, WMFC, S3S2S1S0=0011 (ALU: Z=Y+2), IPin
T2: MDRout-x, S3S2S1S0=0000 (ALU: Z=X), IRin

(ii) Write the control steps required for execution of each of the following instructions (don't repet fetching steps):

a) ADD [D], B ; [D]←B+[D] (Add the content of register B to memory location pointed by register D).

T3: Dout-y, MARin-y, Read, WMFC
T4: Bout-y, MDRout-x, S3S2S1S0=0100 (ALU: Z=X+Y), MDRin-z, Write, WMFC
T5: END

b) AND C, A ; C←C AND A (AND the content of register C with content of register A).

T3: Cout-x, MDRin-x
T4: Aout-x, MDRout-y, S3S2S1S0=1000 (ALU: Z=X AND Y), Cin-z, END

c) SHR B, 1 ;B←Shifted B (Shift right register B by 1 bit).

T3: Bout-y, MDRin-z, S3S2S1S0=1111 (ALU: Z=Y)
T4: MDRout-x, S3S2S1S0=1100 (ALU: Z=SHR X,1), Bin-z, END

d) DEC C ;C←C-1 (Decrement register C by one).

T3: Cout-x, S3S2S1S0=0010 (ALU: Z=X-1), Cin-z, END