CSE2312 Computer Organization & Assembly Language Programming
QUIZ 3 (Chapter 5)

Student Name: _____.

Student ID: _____.

TRUE OR FALSE (2pts per)

Question	1	2	3	4	5	6	7	8	9	10
Answer	T	F	F	T	F	F	F	T	T	F

1. The ISA level defines the interface between the compilers and the hardware. T

2. In a multilevel machine, the Instruction Architecture Level should lay between the Assembly Language Level and Operating System Level. F

3. In immediate addressing mode, the operand is not immediately available for use but the address is immediately available for use. F

4. While we design the instructions, if all things being equal, shorter instructions are better. T

5. Interrupts are changes in the flow of control caused by the running program. F

6. DMA always has a lower bus priority than the CPU. F

7. While a priority (n-1) interrupt routine is running, any attempt by a device with a higher priority n to cause an interrupt should be allowed to happen only until the interrupt routine is finished and the CPU goes back to running code. F

8. If the program is rerun a million times with the same input, the traps will reoccur in the same place each time but the interrupts may vary. T

9. Speculative LOADs make it possible to fetch operands in advance, without penalty if it turns out later that they are not needed after all. T

10. IA-64, developed jointly by Intel and Hewlett Packard, is a simple extension of an existing 32-bit machine. F

Multiple Choices (3pts each)

(Some of the following questions may have more than one correct answer. Please give all correct answers.)

1. Given the memory values below and a one address machine with an accumulator,

Word 20 contains 40; Word 30 contains 50;
Word 40 contains 60; Word 50 contains 70

What values do the following instructions load into the accumulator? [c]

LOAD INDIRECT 20

(a) 40
(b) 50
(c) 60
(d) 70

2. **Which of following is true for Loop Control?**[b c]

(a) The loop may not be executed under satisfied conditions in Test-at-the-end looping.
(b) The loop will always be executed at least once in Test-at-the-end looping.
(c) The loop may not be executed under satisfied conditions in Test-at-the-begin looping.
(d) The loop will always be executed at least once in Test-at-the-begin looping.

3. **Which of following can cause the flow of control to be altered** [bcde]

(a) The common "move" instruction
(b) Procedure calls
(c) Coroutines
(d) Traps
(e) interrupts

4. **Which of following is the correct description for Coroutine** [b c]

(a) When a coroutine is resumed, execution begins at its first statement.
(b) When a coroutine is resumed, execution begins at the statement where it left off the previous time
(c) It is useful for testing software that will later actually run on a multiprocessor.
(d) Each coroutinereally runs in parallel with the others since it had its own CPU.

5. **Which of following common conditions can cause traps** [abcd]

(a) floating-point overflow, floating-point underflow, integer overflow
(b) protection violation, undefined opcode, stack overflow
(c) start nonexistent I/O device
(d) division by zero.

6. **Which of the following is the problem of Pentium 4?** [abcd]

(a) Its CISC-ISA with variable-length instructions and different formats.
(b) The IA-32 is a two-address memory-oriented ISA.
(c) The IA-32 has a small and irregular register set.
(d) Deep pipeline is needed for complex tasks

7. **Which of the following is an important feature of the IA-64?**[abcd]

(a) Reducing memory references
(b) Instruction scheduling
(c) Reducing conditional branches
(d) Speculation

8. **Suppose R3 has value 10, R2 has value 5 and R1 has value 0, what is value of R2 after execute the instruction CMOVZ R2, R3, R1** [d]

(a) 0
(b) 1
(c) 5
(d) 10

9. **Which of the following correctly describes the Speculative Loads?** [abd]

(a) It is normally used for the compiler to hoist LOADs to positions before they are needed.
(b) If a LOAD is speculative and it fails, it just stops and a bit associated with the register to be loaded is set marking the register as invalid
(c) If a LOAD is speculative and it fails, it will cause an exception..
(d) By starting early, they may be finished before the results are needed.

10. **A IA-64 machine gets its speed from several sources:**[abcd]

(a) a state-of-the-art pipelined, load/store, three address RISC engine.
(b) explicit parallelism that requires the compiler to figure out which instructions can be executed at the same time without conflicts and group them together in bundles.
(c) predication allows to eliminate the conditional branch and state which way it will go.
(d) speculative LOADs make it possible to fetch operands in advance.

Computation and Short Answer (10pts each)

1. A computer uses DMA to read from its disk. Suppose that the disk has 32 500-byte sectors per track. The disk rotation time is 32 msec. The bus is 32 bits wide, and bus transfers take 500 nsec each. The average CPU instruction requires two bus cycles. How much is the CPU slowed down by DMA? Please give the complete computation process other than only results

Bus width = 32 bits = 4 bytes.

Bus transfer rate = 500 nsec.

The disk rotation time is 32 msec. That means, to transfer entire data of a track, it requires 32 msec.

The amount of data in a track = 32 * 500 byte = 16,000 bytes.

The time spent to transfer 16,000 bytes of data from disk = 32 * 10-3 s.

Transfer 1 byte of data takes 32*10-3s/16000=2000nsec

So, time spent to transfer 4 bytes of data from disk 4*2000=8000 nsec.

Therefore, time spent by the CPU for 4 bytes = (required time – bus transfer time) = (8000-500) = 7500 nsec

So the CPU takes= (7500/8000)*100 = 93.75%

Therefore due to DMA, the CPU is slowed down by (100 –93.75%) = 6.25%

2. Reverse Polish Notation

1) Convert the following reverse Polish notation formulas to infix.

a. A B – C + D *
b. AB / CD / +
c. ABCDE +/**
d. ABCDE * F /+ G – H / *+
Solution:

(A-B+C)*D

A/B + C/D

A/(B*C*(D+E))

A+B*((C+(D*E)/F)-G)/H

2) Convert the following formulas from infix to reverse Polish notation

a. A + B + C + D - E
b. (A - B) * (C + D) + E
c. (A * B) + (C * D) + E
d. (A - B) * (((C – D * E) / F) / G) * H

Solution:

AB+C+D+E-
AB-CD+*E+
AB*CD*+E+
AB-CDE*-F/G/*H*

3.Signed number representations:

1) Suppose one's complement negative number 11111100, what is its value in decimal representation? -3

2) Suppose one's complement negative number 11111010, what is its value in decimal representation? -5

3) What is the negation of a number 00010110 in two's complement? 11101010

4) What is the negation of a number 00011000 in two's complement? 11101000

4. In the following figure, how to transfer all the disks to peg 3, one disk at a time, but at no time may a larger disk rest on a smaller one?

1) Please details the process step by step.

Let us use the following notations:

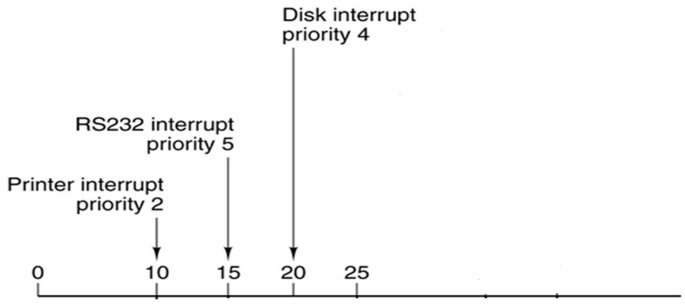
Small Disk = S, Medium Disk = M, Large Disk = L. If we want to represent S is on M we will write MS.

Step	Peg1	Peg 2	Peg 3
0	LMS	-	-
1	LM	-	S
2	L	M	S
3	L	MS	-
4	-	MS	L
5	S	M	L
6	S	-	LM
7	-	-	LMS

2) How many moving-operations are needed in your solution?

Solution: 7

5. The following figure gives a time sequence of a multiple-interrupt example. Suppose user program is running from time 0 until the time 10. Then the printer interrupt with priority 2 is coming. The RS232 interrupt with priority 5 is coming at time 15. The disk interrupt with priority 4 is coming at time 20.



1) Suppose the printer interrupt service routine (ISR) will run with time 10, then, when the printer ISR will finish? Please give the complete computation process other than only results

Solution: Considering both RS232 and Disk ISR takes 10 time unit, and they both have higher priority than Printer ISR, the printer will be finished time at 35+5 = 40.

2) Suppose the RS232 ISR will run with time 10, then, when the RS232 ISR will finish? Please give the computation process other than only results

Solution: RSR232 will be finished at time (15+10) = 25. (Since it has highest priority)

3) Suppose the Disk ISR will run with time 10, then, when the Disk ISR will finish? Please give the computation process other than only results

Solution: RS232 will be finished at time 25. After that Disk ISR will start. So Disk ISR will be finished at time 25+10 = 35.