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High-NA EUV Photoresist Metrology using High-Throughput Scanning Probe Microscopy

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ABSTRACT

High-NA EUV technology enables cost-effective patterning below the 5nm node. The integration is simpler but still requires multiple innovations. Thinner resists are needed for single-patterning enablement. The decrease in thickness poses a challenge for traditional metrology and inspection systems like OCD or CD-SEM, which lose sensitivity due to diminishing interaction volume. The reverse is true for Scanning Probe Microscopy, which excels in the low-height patterning regime. Here we discuss patterning metrology and introduce defect inspection / review applications for High-NA EUV patterning using a high-throughput SPM.

1. INTRODUCTION

High-NA EUV technology enables cost-effective patterning below 5nm node. The integration is simpler but still requires multiple innovations. Thinner resists are needed for single-patterning enablement. The decrease in thickness poses a challenge for traditional metrologies [1]

Scanning Probe Microscopy (SPM) is a technique currently used in process and integration development because it can provide reference-level local imaging and metrology (Figure 1). Two factors are currently limiting deployment of SPM tools for inline process control: 1) ability to fully resolve deep, narrow structures [2] and 2) throughput compatible with other metrologies currently deployed in High Volume Manufacturing (HVM).

High-NA EUV patterning challenges provide the "perfect storm" for SPM adoption for inline process control:

- Existing metrologies are challenged by the thin photoresist pattern (key enabler)
- Thinner resist allows for higher SPM scanning speed (throughput)
- Smaller aspect ratio allows for more robust SPM profile measurement (accuracy)

2. HIGH-THROUGHPUT SPM

Multiple advancements [3] to SPM technology (Figure 1 (a)) were incorporated into a fully automatic platform (Figure 1 (b)) with 4 miniSPM heads measuring in parallel. The (mini)SPM heads are significantly miniaturized, to the approximate size of a large match box, about 2×4×7 cm. This allows placing multiple SPM heads on (under) the wafer and thus allows parallelization (ability to scan multiple areas on the wafer at the same time). Moreover, special design and development features of the miniSPM and the overall system, such as the Z-scanner stage with high frequency first resonance, low-noise optical beam detection system and the z-scanning stage sensor, precise (+/-500nm) navigation to the target of interest on the wafer surface, fast approach, and others, allow for the significant improvement in scanning speed, contributes to the high throughput and enables fast mapping of the whole wafer.

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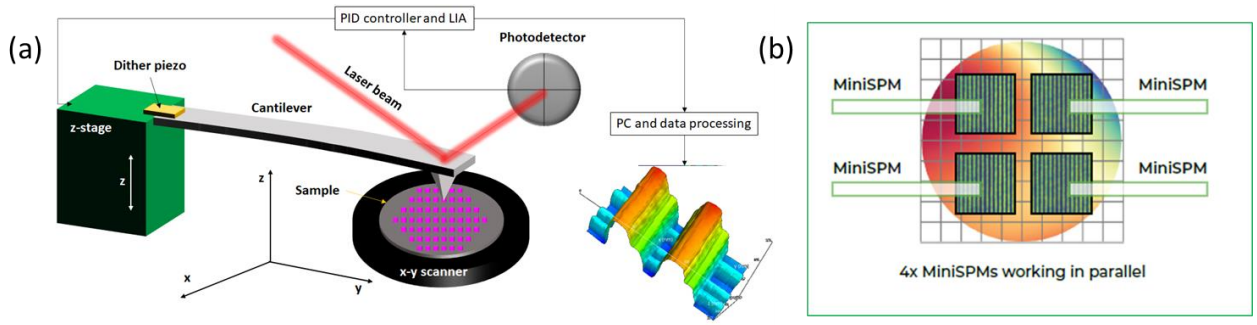

Figure 1 (a) Schematics of SPM. Sample is moving X and Y to enable raster-scanning by the tip. Depending on the scan mode, different outputs can contribute to the reconstruction of the Z-profile of the sample as a function of X and Y. (b) schematics showing 4 mini-scanning probe microscope heads working in parallel.

2.1 Feed Forward Trajectory Planning (FFTP)

Feed Forward Trajectory Planning (FFTP) is a scan mode designed to measure deep trench structures. The FFTP mode avoids resonances of the cantilever, to ensure the tip enters trenches or holes with defined trajectory with disturbance rejection, while minimizing the interactions with sidewalls. The vertical scanning stage has high bandwidth that ensures very small breaking distance, when the trigger signal has been reached. The force-distance curves are measured with real-time signal processing for every interaction to extract topography information. The probe is interacting with the surface based on the defined trajectory, with defined velocities, accelerations and jerks and gets completely retracted from surface for each measurement point.

Z scanner position and tip-wafer force interaction are recorded and processed via optical beam deflection (OBD) to determine the cantilever bending and torsion to extract height of the surface.

3. DEFECTIVITY

Stochastic (random, non-repeating, isolated) defects such as (partial) microbridges, locally thinned or locally-broken lines arise from the fundamental limitation of EUV printing: the shorter wavelength means that the same amount of energy to expose the resist is carried by fewer photons, interacting with thinner resist. Mask technology for EUV is also significantly more complex, mask defects may also influence wafer defectivity.

With the transition from hours-per-wafer (traditional reference metrology) to wafers-per-hour (high throughput Scanning Probe Microscopy), we are also practically entering the defectivity realm. We can now consider exploring and counting defects such as bridging over process-significant areas in reasonable time, helping with stochastic process optimization.

A toolset with multiple scan heads working in parallel opens the possibility of defect inspection metrology and review. Two questions are now relevant:

1. The defect review question: how small a defect can be detected? Do we open up the opportunity of “partial defect” characterization (like local line thickness reduction, or partial bridging at the bottom of trench)?
2. The defect inspection question: what is the area that can be covered per unit time, per probe? Can throughput be increased with resolutions “just-enough” to detect potential presence of defects?

3.1 Programmed defects – review

To address the defect review question, a series of programmed defects of wafers with nominal resist thickness of 15nm and 25nm were investigated. The examined programmed defects include bridges, where 2 lines are merged in a point, and breaks, where there is a discontinuity in a line. Well-defined example of the programmed defects, in a wafer with nominal thickness of 25nm, are displayed in Figure 2. The left image in Figure 2 presents the bridging of two lines in the center of the scanned area. The extracted profile and superposed with the profile of a defect free area, shows the absence of gap between the two consecutive resist lines. Conversely, the right 2D image in Figure 2 shows the disruption a resist line in

the center of the scan. The linear profile, confirm the broken periodicity of the resist lines topography in the center of the scan.

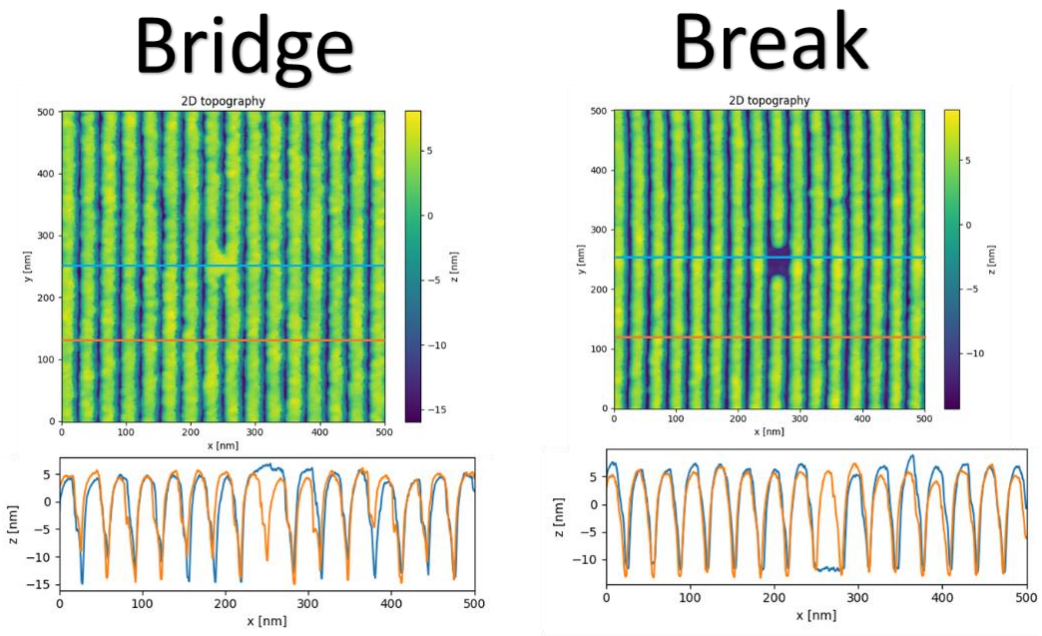

Figure 2 Examples of topography of programed defects with profiles on and out of the defects. Left: bridge defect. Right: break defect.

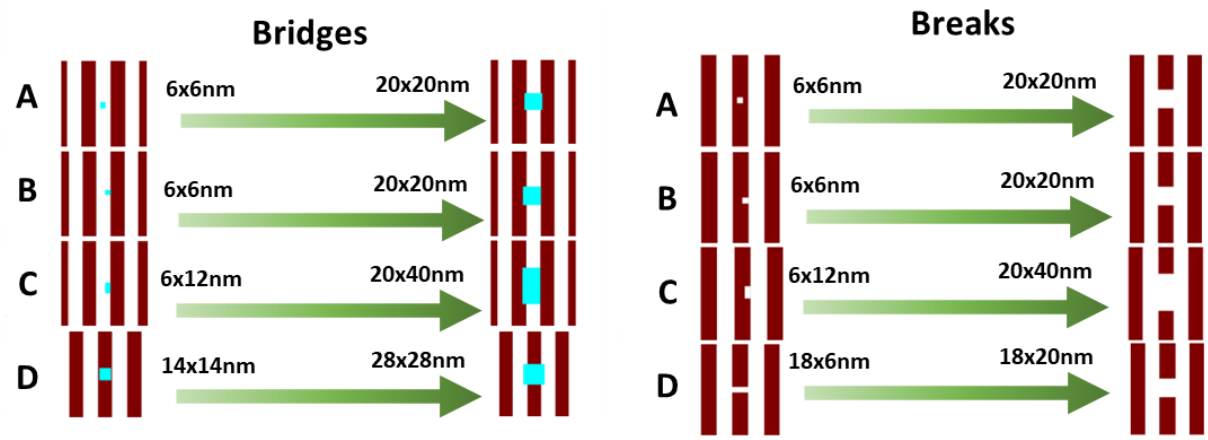

Figure 3 Programmed defects layout.

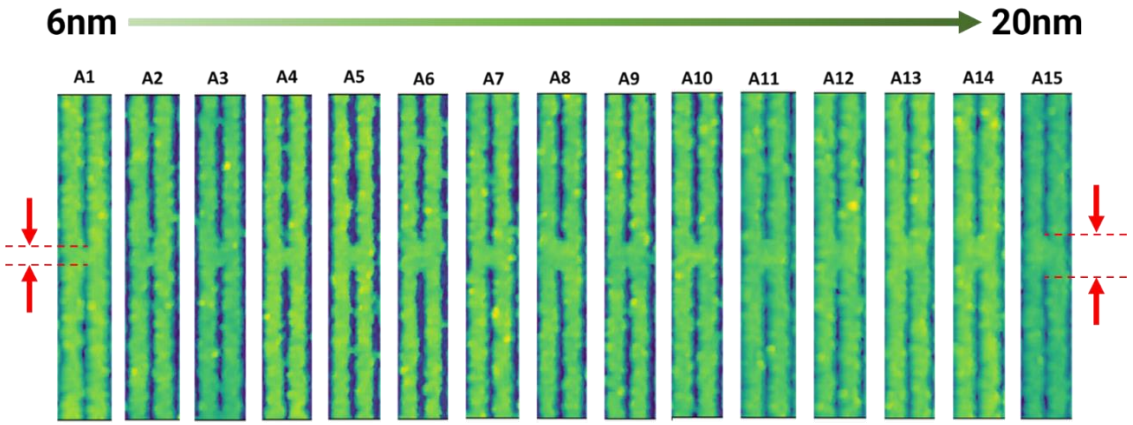

Figure 4 Trimmed images of a series of programmed bridges with increasing nominal size from 6 to 20 nm.

The programmed defects were patterned in an array with two differentiated groups, one for bridges and another for breaks. The programmed defects layout is shown in Figure 3. Each of the groups contains 4 series (A-D) of 15 defects with programmed increasing size. The four series differ in the geometry, location and size of the defects.
In order to prove the capability of the SPM for the defects review, the investigation was focused on the A series, which contains the smallest defects.
Figure 4 presents the cropped region containing the identified defects in the A series of square bridges with increasing nominal size from 6 to 20 nm. It is observed that size of the defects increase from the left to the right of the series, going from nominal 6 to 20 nm. This result shows the successful identification of the full series of defects, including the defects with nominal sizes below to 10 nm.

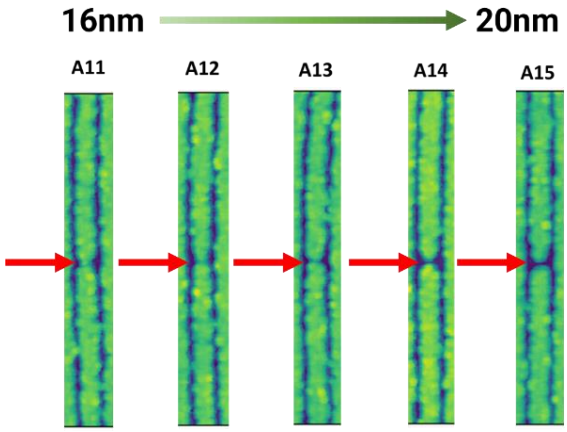

Figure 5 Trimmed images of a series of programmed breaks with increasing nominal size from 16 to 20nm.

Figure 5 presents the analogous investigation of a series of programmed breaks with nominal sizes from 16 to 20nm. The breaks are indicated by a red arrow. It is observable that the cropped region labeled as A11, corresponding with a break of 16 nm nominal size, does not show a clean break. It shows shrinking of the width of the resist line without a its complete disruption. The inability of to identify breaks with nominal sizes below 16 nm can be attributed to the suboptimal parameters during the measurements or difficulties in the patterning of the breaks themselves.

3.2 Programmed defects – inspection

Traditionally, in AFM (see Figure 6) the resist lines are scanned perpendicular to the resist line in order to extract more precise topography of the fins without scan artefacts. Nevertheless, this required of high density of scanned lines in the slow scan axis to obtain enough pixels along the resist lines which allow the defect detection. This way of scanning offers very detailed imaging of the defects with a main drawback, which is the increase of raster-lines is proportional to the increase of scanning time and therefore throughput decrease.

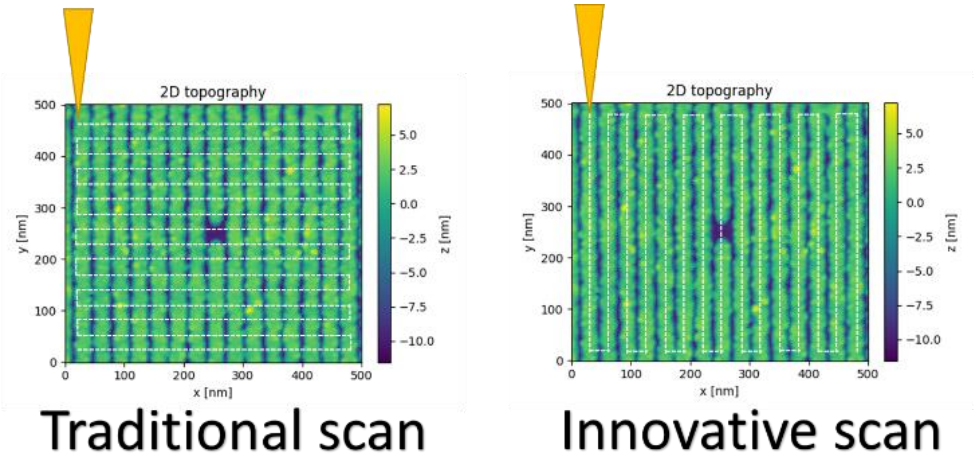

Figure 6 Left: Traditional raster-scan trajectory superposed with white dashed lines on a 2D image with a break defect. Right: analogous image with the innovative trajectory raster-scan superposed.

To address the inspection question for breaks identification, we explored the possibility of scanning parallel to the resist lines. This strategy will reduce the number of lines needed for the defect identification. This methodology allows high density of pixels parallel to the resist lines, with minor increase of the scanning time. To verify the feasibility of this novel scan approach, two break defects from series A and C were implemented during the testing. Figure 7 (a-b) and (f-g) display the orthogonal and parallel scans of defects of 20x20nm and 20x40nm, respectively. The images contain 256 raster-scan lines in both cases. This number of scan lines in a 500x500nm scanned area is equivalent to 1.9nm raster line pitch, which makes negligible the scan orientation for the defect identification. We decreased the number of scan lines to find the limit in which the defects are still identifiable. We observed that scanning with a single scan pitch of the resist line pitch the defects are still observable in the center of the image, see Figure 7 (c-e) and (h-j).

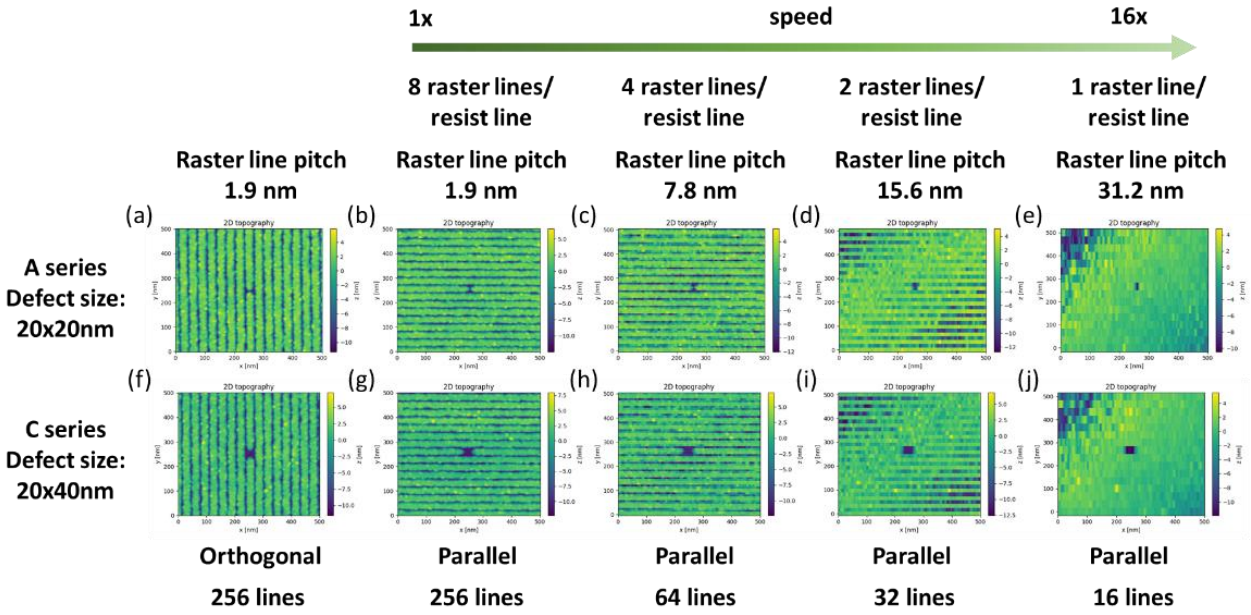

Figure 7 (a) Perpendicular and (b-e) parallel scans to the resist lines of a programmed defect with nominal size of 20x20nm (A series) in the center of the scan. (f) Perpendicular and (g-j) parallel scans to the resist lines of a programmed defect with nominal size of 20x40nm (C series) in the center of the scan.

The reduction of the raster lines proportionally decreases the scan time. Therefore, by the decrease of the number of scan lines to the lower limit (1 raster-line per resist line), scan parameter optimization and parallelization of four AFM heads, the defect inspection in a 50x50μm area can be performed in a minute.

3.3 Naturally occurring defects

In addition to the programmed defects, during the inspection of the wafer with nominal 10nm resist thickness, naturally occurring defects were also found. Left and right panels from Figure 8 show two different locations on the wafer with natural bridges and breaks, respectively. In both panels full and partial examples of each defect can be observed. The full defects are pointed by the black arrow and the partial defects by the purple one.

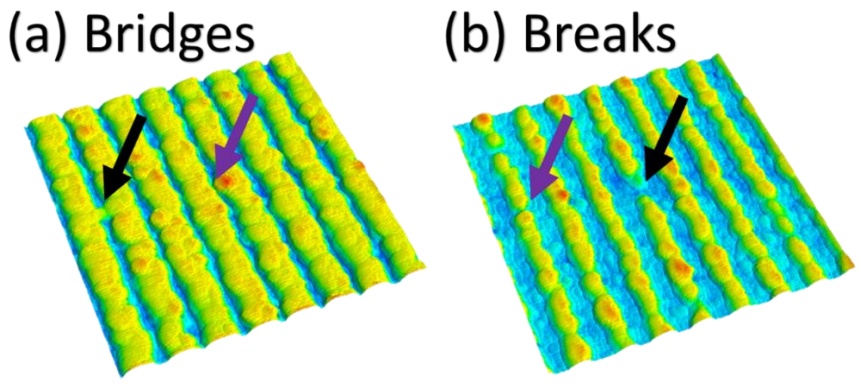

Figure 8 Example of naturally-occurring defects: (a) bridges (black arrow) and partial bridges (purple arrow). (b) gaps (black arrow) and partial gaps (purple arrow).

4. WAFERS and PARAMETERS OF INTEREST

A set of wafers with controlled resist thickness deposition of conventional resist thickness (CRT) and thin resist thickness (TRT), [4] was patterned with controlled dose and focus variation. The pattern pitch is 32nm. The High Throughput SPM (HT-SPM) technique has enough sensitivity to measuring the profile attributes of the thinnest resist (Figure 9).

There are 8 parameters of interest (Figure 10):

1. Blanket Resist Height, measured as difference between no-resist, and un-patterned resist
2. Array Resist Height, measured as difference between top of array and the no-resist area
3. Resist loss, measured as the difference between the blanket and array height
4. Top Line Roughness, measured along the top of resist lines
5. Bottom Trench Roughness, measured along the bottom of the resist trenches
6. Trench Depth, the depth of the patterned trench inside the resist, measured on the array
7. Line CD, the width of the resist line
8. Resist Residue, measured as difference between Array Resist Height and Trench Depth.

(As per AFM best practices: the probe reaching the bottom of the trench is inferred from the bottom profile being imaged with multiple pixels. When the bottom of the trench is imaged as a single pixel strand, then there is implicit uncertainty whether the true bottom of the trench was reached).

Segmentation algorithms were developed to extract all the above parameters from the raw SPM data (line profiles) and generate full wafer maps.

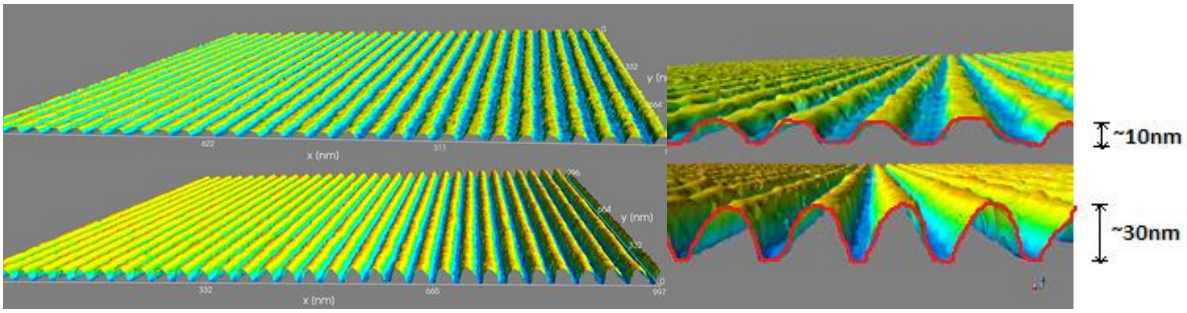

Figure 9 Left: Nominal dose / focus SPM image collected from TRT (top) and CRT (bottom) nominal resist height (measured thickness slightly lower), 32nm pitch high-NA resist pattern – 1×1 micron area; Right: zoom-in to show profile details (note flat bottom indicating enough margin to extract bottom roughness data).

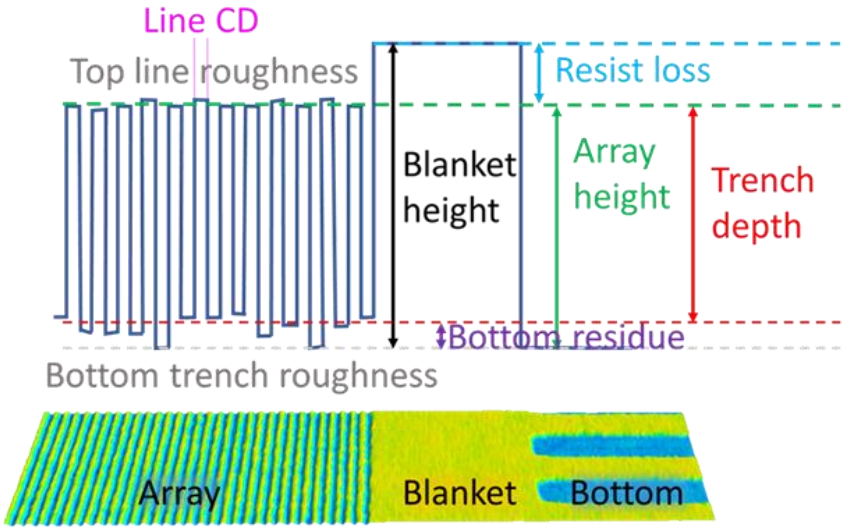

Figure 10 Top: Schematic profile of the resist measured across a dense array, an unpatterned (blanket) area, and an area with fully removed resist. Bottom: 3D render of a mapped area including: array, blanket and bottom regions.

5. FULL WAFER MAPS, THROUGHPUT, PRECISION

Wafer mapping is a powerful tool for yield management. Such a map enables control engineers to visually assess the health of wafers in real time, analyze root causes and correct systematic and operational issues. Recently, there has been an increased interest for statistical and machine learning analysis [5,6] applied to the spatial information in the wafer maps to recognize different spatial patterns, for example, non-uniform distribution of faults throughout the wafer. Additionally, the wafer maps shown in Figure 11 and

Figure 12 can be easily shared with stakeholders upstream and downstream the current process step.

4 of the 8 parameters of interest can be measured using a standard, known resonant scan mode. In this way, the probe might not travel all the way to the bottom of the dense and narrow array. However, blanket and array resist heights, resist loss, and top roughness can be easily extracted. A throughput of 17WPH with 63 dies with a 2×1μm area spanning 3 regions (array, un-patterned, and no-resist), Figure 10) can be reached. Wafer maps of the 4 parameters are in Figure 11.

Three more parameters of interest can be measured using the special FFTP non-resonant scan mode in section 2.1. In this way, the probe penetrates to the bottom of the dense array for all samples. The final 8th parameter is extracted as the difference between data from resonant, and non-resonant mode. This non-resonant mode is slower: it can potentially extract all 8 parameters by itself, but splitting the measurement into a fast, larger area and a slow, smaller area can be more efficient. A throughput of 12WPH with 63 dies with a 0.5×0.5μm area covering the dense array can be reached. Wafer maps of the additional 4 parameters are in Figure 12.

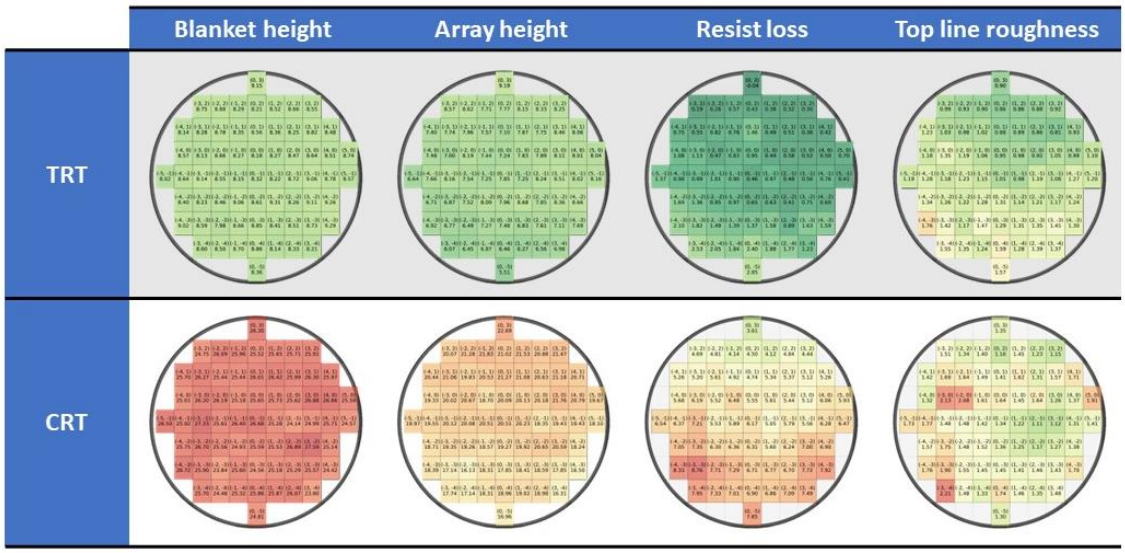

Figure 11 Wafer maps of 2 focus-exposure wafers with different resist height: resonant mode

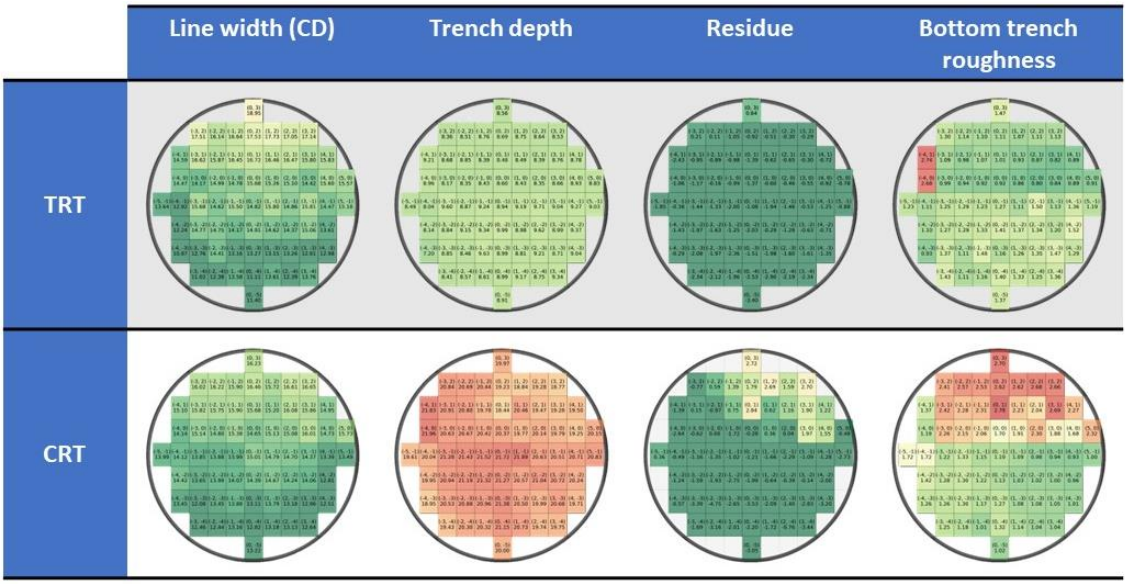

Figure 12 Wafer maps of 2 focus-exposure wafers with different resist height: non-resonant mode and mix

6. SUMMARY and OUTLOOK

High-NA EUV is expected to enter high volume manufacturing by 2025 [7]. Metrology and inspection are critical enablers to the learning cycles needed to bring these plans into fruition.

High-Throughput SPM is key enabler to metrology and defect review and makes significant strides towards defect inspection goals as well. We have demonstrated a high-throughput SPM technique implemented on a fully automated platform and integrated in the semiconductor production process flow. Specifically, we show metrology capabilities: extraction of key parameters with HVM-compatible throughput and performance. For defectivity applications, in 1 minute, our technique maps a 50×50µm area per 4 scanning heads, detailed defect morphology can be extracted.

7. REFERENCES

[1] Severi, J., Lorusso, G. F., Simone, D. de, Moussa, A., Saib, M., Duflou, R. and Gendt, S. de., "Chemically amplified resist CDSEM metrology exploration for high NA EUV lithography," https://doi.org/10.1117/1.JMM.21.2.021207 **21**(2), 021207 (2022).

[2] Bunday, B. D., Orji, N. G. and Allgair, J. A., "High volume manufacturing metrology needs at and beyond the 5 nm node," https://doi.org/10.1117/12.2584555 **11611**, 116110F (2021).

[3] van Reijzen, M., Boerema, M., Kalinin, A., Sadeghian, H. and Bozdog, C., "Recent advancements in atomic force microscopy," https://doi.org/10.1117/12.2595426 **11611**, 595–601 (2021).

[4] Moussa, A., Severi, J., Lorusso, G., de Simone, D. and Charley, A.-L., "High NA EUV: a challenge for metrology, an opportunity for atomic force microscopy," https://doi.org/10.1117/12.2601677 **11854**, 82–87 (2021).

[5] Jin, C. H., Kim, H. J., Piao, Y., Li, M. and Piao, M., "Wafer map defect pattern classification based on convolutional neural network features and error-correcting output codes," Journal of Intelligent Manufacturing **31**(8), 1861–1875 (2020).

[6] Saqlain, M., Jargalsaikhan, B. and Lee, J. Y., "A voting ensemble classifier for wafer map defect patterns identification in semiconductor manufacturing," IEEE Transactions on Semiconductor Manufacturing **32**(2), 171–182 (2019).

[7] "Intel and ASML strengthen their collaboration to drive High-NA into manufacturing in 2025 | ASML.", <https://www.asml.com/en/news/press-releases/2022/intel-and-asml-strengthen-their-collaboration-to-drive-high-na-into-manufacturing-in-2025> (4 May 2022).