

Final Project: LC-3 Simulator

Due Date: Friday 4/28/2017 11:59PM; No late handins

This is the final project for this course. It is a simulator for LC-3, and you will recognize that it is very similar to the SDC virtual machine that you worked on for Labs 5 and 6. What we'll end up with is a line-oriented command-line program that reads in initial memory contents from a file (this time in hexadecimal format) and then lets the user enter commands to execute the program's instructions and inspect registers and memory (much like an interactive debugger such as `gdb`). You'll also be implementing the code that executes instructions on the LC-3. After completing this lab, you'll not only be able to understand how to implement a basic digital computer in software, but also how to implement a read-eval-print-loop (REPL)-based interpreter, like you are probably familiar with if you program with Python or Ruby (or other high-level scripting languages).

Your goal is to fill in all of the missing functionality in `lc3.c` which is indicated by "FILL ME IN" comments. You should add your own code in these locations. You'll want to use your SDC solution(s) as a reference. **Note that you must work alone on this project!**

Simulating the LC-3

- As in the SDC simulator, the LC-3 CPU should be modeled as a value of type `cpu_t`, allocated in the main program. Routines that need the CPU should be passed a pointer to the CPU value.
- A `word_t` is typedef'ed to be a `short int`, 16 bits on fourier. Since `word_ts` are signed, `0x8000-0xffff` represent `-32768` to `-1`.
- An `address_t` is an unsigned `short int` (compare with the unsigned `char` used for the SDC).
- Make sure to read the comments on modeling instruction formats with `structs` in C in `lc3.h`. This is a fairly advanced usage of C `structs` and may take some time to wrap your head around.
- The memory of the machine is represented as an array of `word_t` values indexed by `address_t`. Registers are represented as an array of `word_t` values indexed by integers (0-7 since there are 8 registers). The PC is an `address_t`; the IR is a `word_t`.
- Since unsigned values are never negative, as `address_t` values, `0x8000-0xffff` represent `32768` to `65535`.
- You may need a cast to convert between `word_t`, `address_t`, and integer values. E.g., as a `word_t`, `0xffff` is `-1`, but as an `address_t`, `0xffff` is `65535`. A

base register contains a `word_t`; to use its value as an address, you need to cast it: `(address_t)(word_val + offset)`.

- Loops of the form “for every `address_t`, do ...” are a little tricky. If `i` is an `address_t` variable, then `for (i = 0; i < 65536; i++) { ... }` will cause an infinite loop because an `address_t` is always < 65536 . You can check for `i == 65535` (in which case you’re one iteration short), or you can check for the second time that `i == 0` (which is a little tricky), or you can make `i` not be an `address_t`.

Coding Assignment (*100 points total*)

- As in the SDC simulator, the input file should be a command line parameter. If it’s omitted, your program should produce an error.
- You should be able to process a `.hex` file produced by the LC-3 editor when it assembles a `.asm` file.
 - A `.hex` file is a text file containing a sequence of lines with a four-digit hex number on each line (no leading `x` or `0x`). An `sscanf` format of `%x` will read in an unsigned integer, which you can cast to a `word_t` to store in memory.
 - The first line specifies the `.ORIG` location to start loading values into. The remaining lines contain the values to load.
 - If you read a value into location `xFFFF`, wrap around to `0000` as the next location. No errors are necessary here.
 - If anything appears on a line after the four-digit hex number, ignore it. This will let us add comments to our `.hex` files.
 - **Note:** In general, the LC-3 text editor can translate hex files to executable object code via *Translate* \rightarrow *Convert Base 16*, but it won’t handle a hex file with comments added to it.
- All other memory locations should be set to zero. In particular, don’t simulate the TRAP table in low memory (`00 - FF`) or the trap-handling code in upper memory.
- Once the program is read into memory, initialize the `PC` to the `.ORIG` value, the `IR` to zero, the condition code to `Z`, and the running flag to `1`, then dump the CPU and memory.
- Once the `.hex` file is loaded into memory, a prompt will be displayed to start the command loop. The user should enter a carriage return after each command (`h\n`, for example).
- The possible commands are the same as in SDC (`?`, `h`, `d`, `q`, `N`, and an empty line, where `N` is some integer).
- Just like in the SDC project, you must be careful with whitespace. You can redirect your program’s output to a file, do the same with the solution, and use the `diff` command to spot differences that aren’t obvious to the eye.

Differences from the Patt & Patel Simulator

Your simulator should produce the same results as the Patt & Patel simulator with some slight differences.

- If you execute an instruction at `xFFF` then incrementing the PC should wrap it around to `x0000`. (Patt & Patel's simulator causes an error if you execute the instruction at that location.) By default, for us, `M[xFFFF] = 0` is a NOP.
- Executing the `RTI` instruction (Return from Interrupt, opcode 8) or the unused opcode 13 will print an error message but continue execution. (Patt & Patel's LC-3 simulator behaves differently.)
- Only traps `x20`, `x21`, `x22`, `x23`, and `x25` need to be implemented. For any other trap vector (including `x24`, `PUTSP`), an error message will be printed and execution will halt.
- A `TRAP` command will be executed in one instruction cycle. Their simulator actually simulates I/O register interactions. Because of this, we say that we are *emulating* I/O, rather than *simulating*.
- For the `IN` and `GETC` traps, the user should enter a `\n` after the character to be read in. If the user just enters `\n` without a preceding character, then use `\n` as the character read in.
- Because the simulator prints out a trace of execution, printing a prompt and doing a read (using `PUTS` and `GETC`) doesn't behave exactly like it does with Patt & Patel's simulator: You have to wait until the `GETC` executes and asks for your input before actually typing in the character.

Code Framework

- You should be able to adapt your SDC smulator to do this project.
- Feel free to use the standard library functions like `strcmp`. (Don't forget to `#include <string.h>`.)
- Remember, your program gets tested on `fourier`, so don't use libraries like `conio` that aren't available there.

Getting the Code Get the `lc3` project code by logging into `fourier` and running the following:

```
$> cp /home/khale/HANDOUT/final.tgz .
$> tar xvzf final.tgz
final/
final/tests/
final/tests/t1.exp
final/tests/t3.exp
final/tests/t8.hex
final/tests/t6.exp
final/tests/t5.exp
```

```
final/tests/t1.hex
final/tests/t7.hex
final/tests/t2.exp
final/tests/t8.exp
final/tests/t3.hex
final/tests/t2.hex
final/tests/t0.exp
final/tests/t4.hex
final/tests/t4.exp
final/tests/t10.exp
final/tests/t7.exp
final/tests/t9.exp
final/tests/t5.hex
final/tests/t6.hex
final/test_harness
final/Makefile
final/lc3.h
final/lc3.c
final/lc3-soln
$> cd final
$> ls
lc3.c  lc3.h  lc3-soln  Makefile  test_harness  tests
$> make
gcc -Wall -Wno-unused-function -Wno-unused-variable -Wno-unused-but-set-variable -Wno-packed-bitfield-compat -lm -o lc3 lc3.c
```

If you run the skeleton code you'll see the following (just like in Lab 5 and 6):

```
$> ./lc3
CS 350 Final Project: LC-3 Simulator Usage: ./lc3 <.hex file>
```

Your job here is to fill in the functions in `lc3.c` which have `FILL ME IN` comments written in them. Many of these you can take directly from your Lab 5 and 6 solutions (this in most cases is noted in the comments). See the comments in the code for further instructions. I've also included a test harness for you to test your code. You can run it like so:

```
$> make test
# Testing lc3...
Test 0 - [FAIL]
Test 1 - [FAIL]
Test 2 - [FAIL]
Test 3 - [FAIL]
Test 4 - [FAIL]
Test 5 - [FAIL]
Test 6 - [FAIL]
Test 7 - [FAIL]
Test 8 - [FAIL]
Test 9 - [FAIL]
```

```
Test 10 - [FAIL]
0 out of 11 test cases passed
```

Notice that the code will initially fail all the test cases or hang. Your job is to make it pass them all. These are example `.hex` files, and I've included them in a separate directory named `tests`. Notice that if you add more `.hex` files in the `tests` directory this time, you will break the test harness. This is because there is something special going on in order to test your program interactively. For grading, we will be using other tests in addition to the ones in this directory, so make sure you pass all the tests we provide.

A good strategy here to get started is to start with the `main()` function and work your way down based on the functions that are called from there.

Extra Credit Opportunities

There are several possibilities for extra credit. They will involve some ambitious extension to the project or something related to it. The credit earned for such projects will vary, but can be significant for the more ambitious ones. It's really more for the fun of it. Come see me if any of these sound exciting to you.

- Extend your simulator to actually simulate I/O interactions at the register level (like the Patt & Patel simulator does.)
- Design the hardware for a floating point unit for LC-3 and add appropriate ISA extensions for it.
- Design the hardware to make the LC-3 virtualizable.
- Pick a one-instruction-set (OISC) computer of your choice and write an assembler that translates from LC-3 assembly to that OISC assembly. Some people would call such a tool a *trans-piler*.
- Write an x86 \rightarrow LC-3 assembler.
- Implement LC-3 as a breadboard-based computer.
- Write a custom operating system for the LC-3.
- Add virtual memory support to the LC-3. This would, in theory, allow you to port a real-life OS like Linux to LC-3.
- Learn a hardware description language such as Verilog or VHDL and write an implementation of the LC-3. If you are *really* ambitious, and would like to synthesize your design (going from an HDL to a transistor based design using automated tools), I might even pay for you to have your chip design "taped out" (fabricated). It must, of course, work!
- Make a web-based LC-3 simulator, e.g. using Javascript, HTML5 canvases, or whatever hot web language the kids are using these days. This is something that could be used in later instantiations of this course!

Hand-in Instructions

Make sure to put your name on your submission. Submissions without names will be given zero points! For code, this means put a comment at the top of your C file with your name on it.

For the code, you must hand it in digitally. Once you're happy with your code, in the directory where your code is (`final`), run the following **on fourier**:

```
$> make handin
```

Late handins

NO LATE HANDINS FOR THIS ASSIGNMENT!

Programming Notes

- `lc3.c` contains the skeleton code for this lab. Note that there are some places where you can reuse your code from labs 5 and 6.
- Remember, `sscanf` returns the number of items it was able to read. E.g.,
`x=sscanf(s, "%d", &y);` tries to read an integer from a string `s` into a variable `y`. If it succeeds, `x` is set to 1, else `x` is set to EOF (which you should **not** assume will be zero).
- Note that this time your program is an interactive program. We are testing your program by recording interactions with the instructor solution, and making sure that your program behaves the same way. If you're curious how we do this, lookup the `expect` program. Pretty nifty.
- If, when you run `make test`, your program hangs, it is because `expect` does not understand your program's output and is waiting for the correct output. If this happens, invoke `expect` manually with `expect -f tests/tN.exp ./lc3` where `N` is the test number. Spot where the output stops with `expect` and look back to the previous input that `expect` typed at your prompt. The difference between the solution and your program will lie somewhere between those two points.

LC-3 ISA Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD ⁺	0	0	0	1	DR			SR1			0	00		SR2		
ADD ⁺	0	0	0	1	DR			SR1			1	imm5				
AND ⁺	0	1	0	1	DR			SR1			0	00		SR2		
AND ⁺	0	1	0	1	DR			SR1			1	imm5				
BR	0	0	0	0	n	z	p	PCoffset9								
JMP	1	1	0	0	000			BaseR			000000					
JSR	0	1	0	0	1	PCoffset11										
JSRR	0	1	0	0	0	00	BaseR			000000						
LD ⁺	0	0	1	0	DR			PCoffset9								
LDI ⁺	1	0	1	0	DR			PCoffset9								
LDR ⁺	0	1	1	0	DR			BaseR			offset6					
LEA ⁺	1	1	1	0	DR			PCoffset9								
NOT ⁺	1	0	0	1	DR			SR			111111					
RET	1	1	0	0	000			111			000000					
RTI	1	0	0	0	000000000000											
ST	0	0	1	1	SR			PCoffset9								
STI	1	0	1	1	SR			PCoffset9								
STR	0	1	1	1	SR			BaseR			offset6					
TRAP	1	1	1	1	0000			trapvect8								
reserved	1	1	0	1												

Note here that we will be ignoring the `RTI` instruction.