DEFAULT CONFIGURATION				
	BASIC MATH	**BIT COUNT**	**QUICK SORT**	**SUSAN**
# of instructions simulated	208485148	4657434	34080624	22573809
# of instructions committed	213077480	4689040	38634686	22937598
# of CPU Clock Cycles	426620025	5370557	78733686	31535883
CPI	2,0462850	1,1531150	2,3102180	1,3970120

Default Configuration:

CONFIG #1				
	BASIC MATH	**BIT COUNT**	**QUICK SORT**	**SUSAN**
# of instructions simulated	208485148	4657434	34080624	22573809
# of instructions committed	213077480	4689040	38634686	22937598
# of CPU Clock Cycles	426619935	5369839	78547596	31533199
CPI	2,0462850	1,1529610	2,3047580	1,396893

CONFIG #1:
Set LQ and SQ entries to 32

CONFIG #2				
	BASIC MATH	**BIT COUNT**	**QUICK SORT**	**SUSAN**
# of instructions simulated	208485148	4657434	34080624	22573809
# of instructions committed	213077480	4689040	38634686	22937598
# of CPU Clock Cycles	419340228	5098108	78362721	32169402
CPI	2,011367	1,094617	2,299334	1,425076

CONFIG #2:
2 IntegerALU instead of one

CONFIG #3				
	BASIC MATH	**BIT COUNT**	**QUICK SORT**	**SUSAN**
# of instructions simulated	208485148	4657434	34080624	22573809

CONFIG #3:
FloatAdd -> 8
FloatCmp -> 8

# of instructions committed	213077480	4689040	38634686	22937598	FloatCvt -> 16
# of CPU Clock Cycles	431073476	5371302	78733686	32169402	
CPI	2,0676460	1,1532750	2,3102184	1,4250764	

CONFIG #4					
	BASIC MATH	**BIT COUNT**	**QUICK SORT**	**SUSAN**	**CONFIG #4:**
# of instructions simulated	208485148	4657434	34080624	22573809	localPredictorSize = 128
# of instructions committed	213077480	4689040	38634686	22937598	
# of CPU Clock Cycles	423520227	5370621	78305069	31531232	
CPI	2,031417	1,153129	2,297642	1,396806	

CONFIG #5					
	BASIC MATH	**BIT COUNT**	**QUICK SORT**	**SUSAN**	**CONFIG #5:**
# of instructions simulated	208485148	4657434	34080624	22573809	fetchWidth -> 8
# of instructions committed	213077480	4689040	38634686	22937598	issueWidth -> 8
# of CPU Clock Cycles	419266512	5098056	78327223	32169341	INT_ALU# -> 8
CPI	2,011014	1,094606	2,298292	1,425074	

CONFIG #6					**CONFIG #6:**
	BASIC MATH	**BIT COUNT**	**QUICK SORT**	**SUSAN**	fetchWidth -> 8
# of instructions simulated	208485148	4657434	34080624	22573809	issueWidth -> 8
# of instructions committed	213077480	4689040	38634686	22937598	INT_ALU# -> 4
# of CPU Clock Cycles	419279314	5098058	78327223	32168011	FP_ALU -> 4
CPI	2,11075	1,094607	2,298292	1,425015	FP_MULTDIV -> 4