

# Introduction

Logic Circuit Laboratory

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## Outline

1. Lecturer
2. Course Introduction
3. Assessment
4. Motivation
5. Introduction to Logic circuit Laboratory
6. Rules / Safety for Laboratory
7. Devices

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# Logic Circuit Laboratory

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## Analog device



source: <http://www.onlyinyourstate.com>

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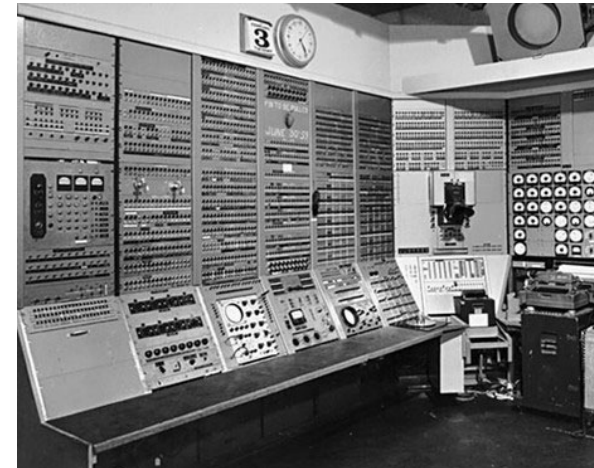
## Digital Device



source: <http://www.dmnnews.com/>

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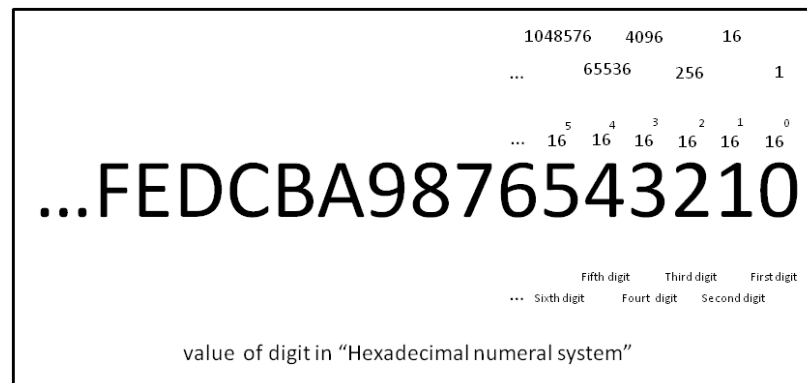
Computer -> Analog/ Digital



source: <https://www.computerhope.com>

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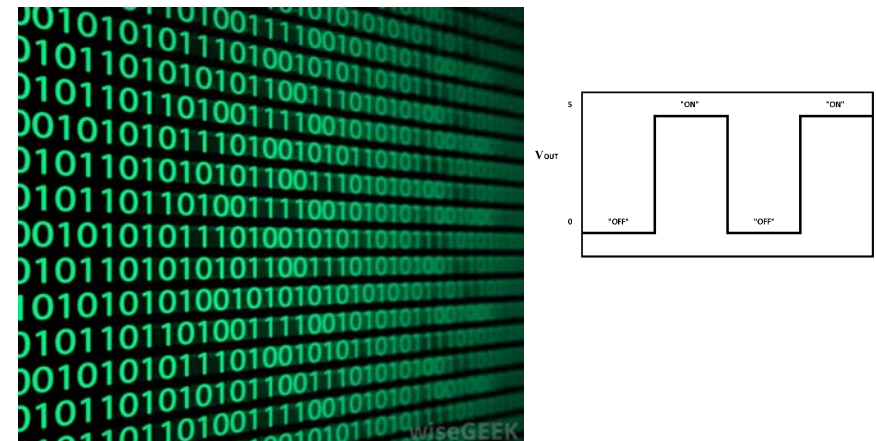
## Base number



source: [https://en.wikiversity.org/wiki/Numeral\\_systems](https://en.wikiversity.org/wiki/Numeral_systems)

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Logic computer status



source: <https://www.computerhope.com>

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## กำเนิด Logic

1. Intro to circuit analysis for CPE
2. Electronic for CPE
3. Digital circuit design

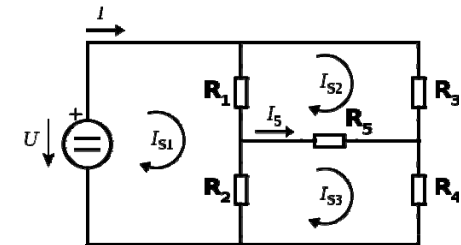
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## 1. Intro to circuit analysis for CPE

R – Resistor

L – Inductor

C - Capacitor



Analog circuit

CPE -> Direct current circuit design

RLC = Passive component

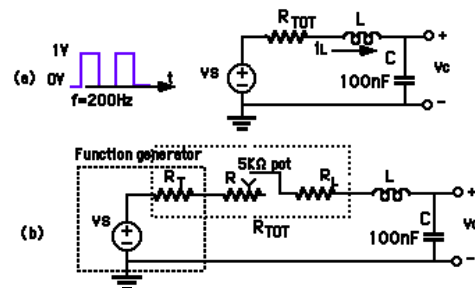
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## 1. Intro to circuit analysis for CPE

R – Resistor

L – Inductor

C - Capacitor



Analog circuit

CPE -> Alternating current circuit design

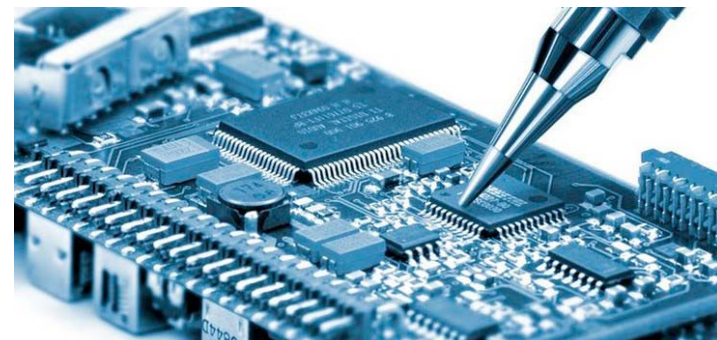
Frequency response + Filter circuit

Digital?

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## 2. Electronic for CPE

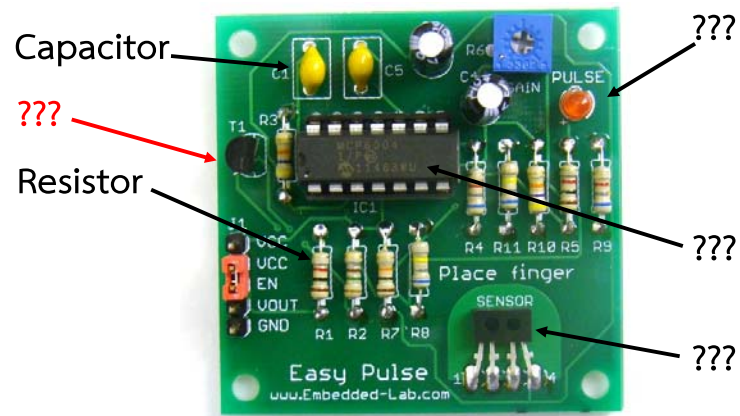
Electronic ?



Electronic = Semiconductor + Passive component

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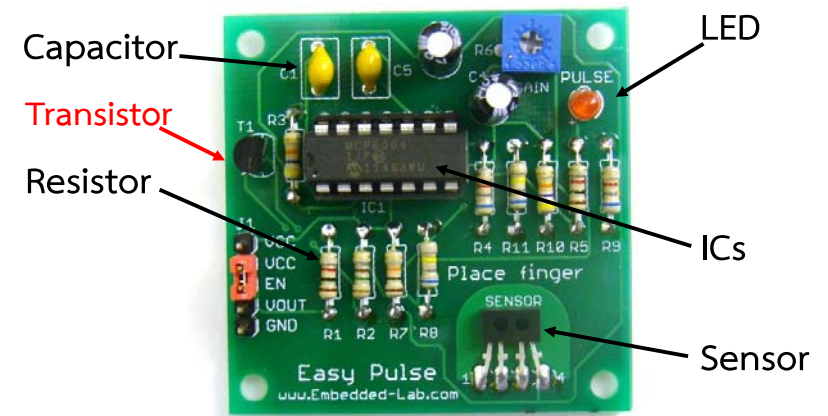
## 2. Electronic for CPE



Electronic = Semiconductor + Passive component

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## 2. Electronic for CPE

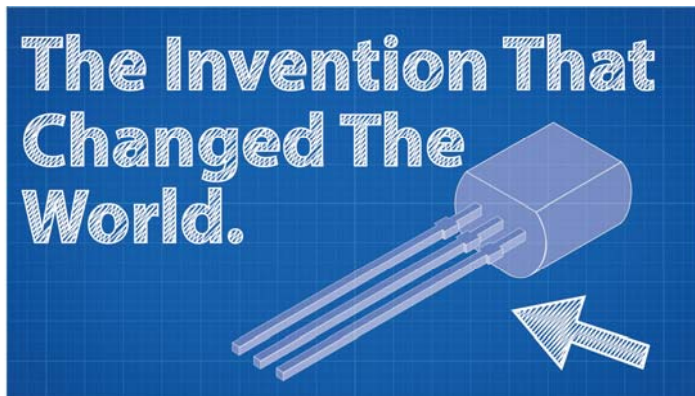


Electronic = Semiconductor + Passive component

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## 2. Electronic for CPE

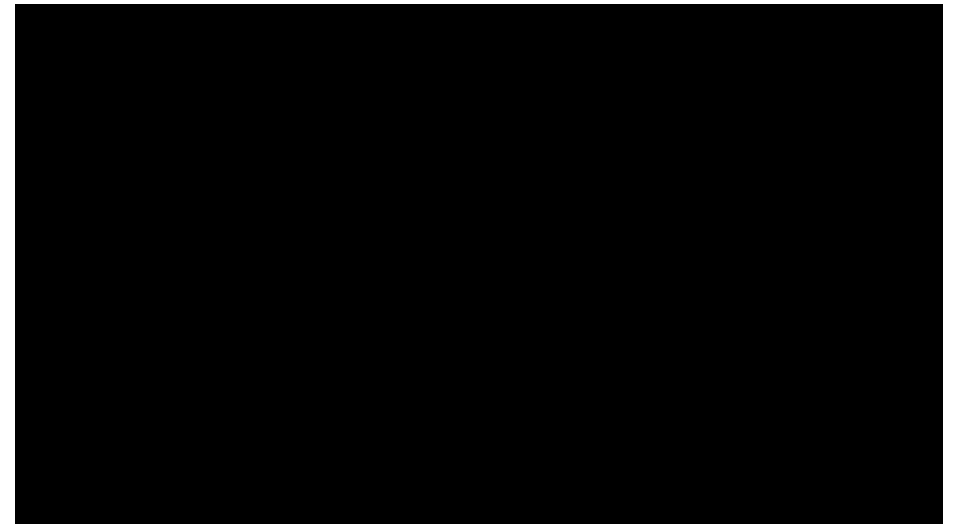
Transistor change the world



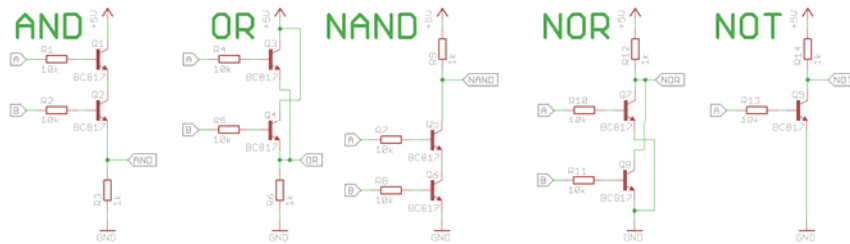
Electronic = Semiconductor + Passive component

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Transistor change the world



## 2. Electronic for CPE



Digital?

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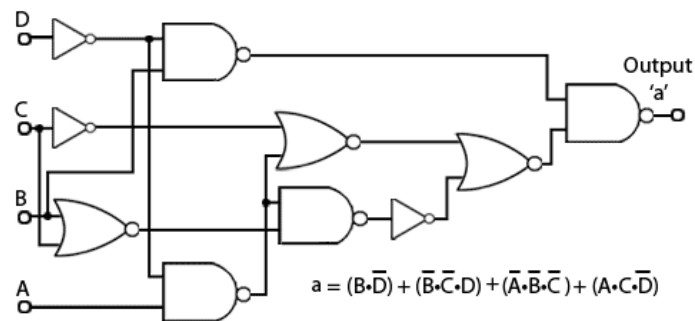
## 3. Digital circuit design

| INPUT |    |    | OUTPUT |
|-------|----|----|--------|
| x1    | x2 | x3 | S      |
| 1     | 1  | 1  | 1      |
| 1     | 1  | 0  | 1      |
| 1     | 0  | 1  | 1      |
| 1     | 0  | 0  | 0      |
| 0     | 1  | 1  | 0      |
| 0     | 1  | 0  | 0      |
| 0     | 0  | 1  | 0      |
| 0     | 0  | 0  | 1      |

BOOLEAN ALGEBRA

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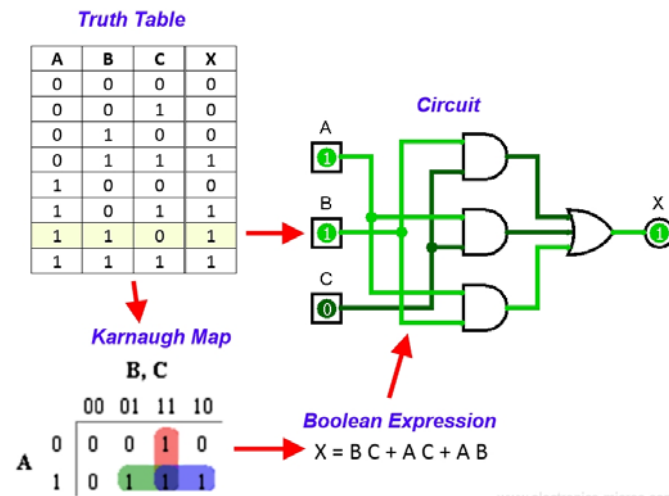
## 3. Digital circuit design



EQUIVALENT CIRCUITS

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## 3. Digital circuit design

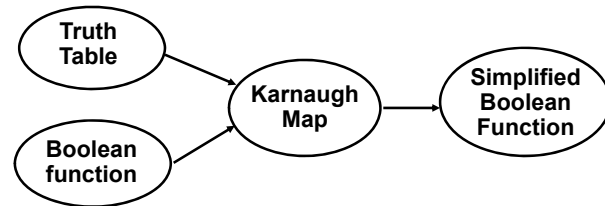


KARNAUGH MAP

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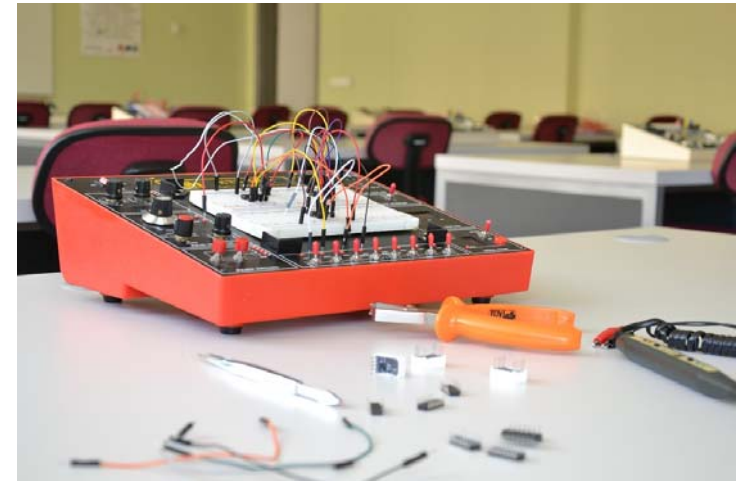


### 3. Digital circuit design



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### Logic Circuit Laboratory



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### Course Outline

- |                                 |                              |
|---------------------------------|------------------------------|
| 1. Introduction                 | 8. Sequential Circuit III    |
| 2. Logic Gats & Related Devices | 9. Sequential Circuit IV     |
| 3. Combination Circuits I       | 10. FPGA I                   |
| 4. Combination Circuits II      | 11. FPGA II                  |
| 5. Combination Circuits III     | 12. Logic circuit project I  |
| 6. Sequential Circuit I         | 13. Logic circuit project II |
| 7. Sequential Circuit II        | 14. Lab Exam                 |

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### Digital + Lab logic Motivation

Combination Circuits I - III

Adder circuit

Subtractor circuit

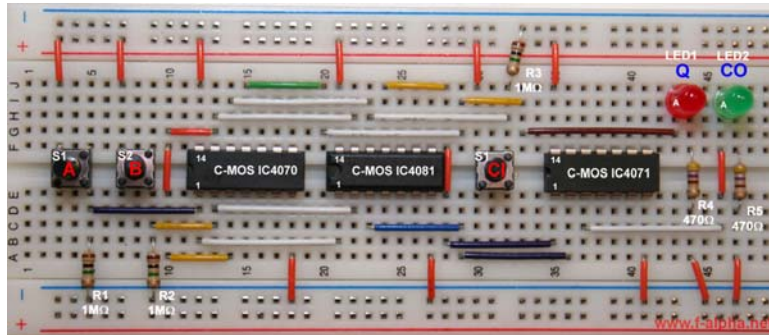
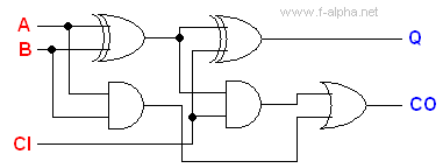
Multiplier circuit

Divider circuit

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## Digital + Lab logic Motivation

The Full Adder Circuit



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## Digital + Lab logic Motivation

Sequential Circuit I - IV

Clock / Timer

Storage elements (Latches, Flip-Flops, Register)

Shift registers

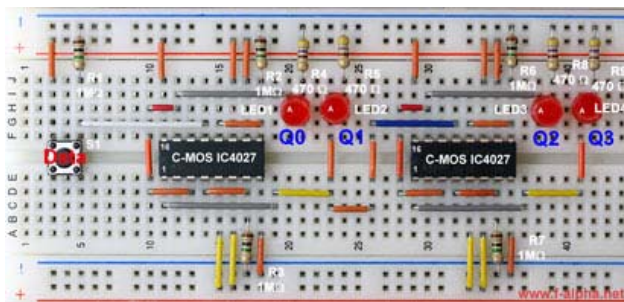
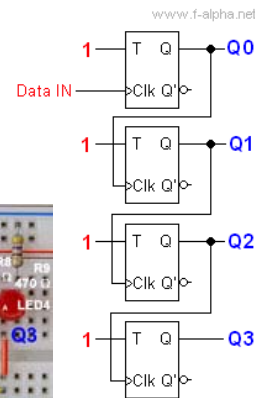
Counters

RAM/ROM

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## Digital + Lab logic Motivation

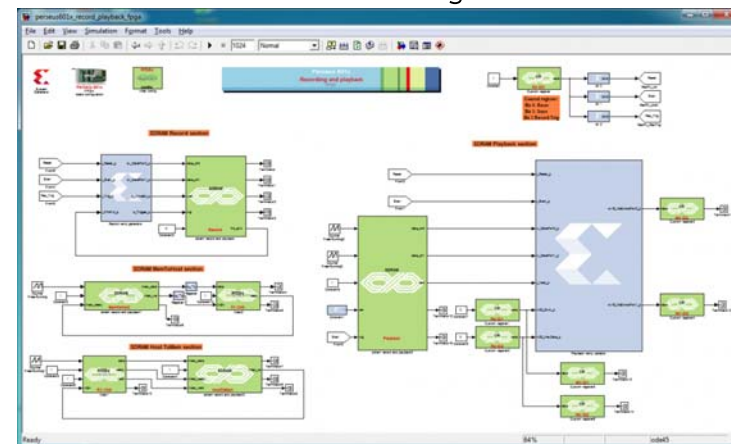
4-bit Down Counter



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## Digital + Lab logic Motivation

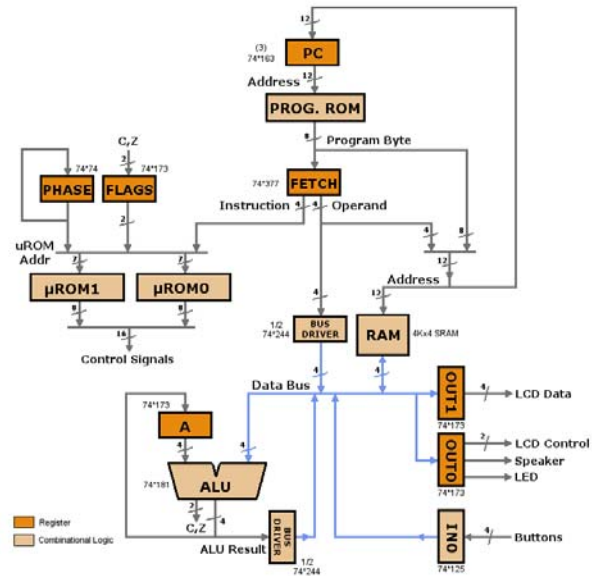
FPGA - Model Base design



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## Digital + Lab logic Motivation

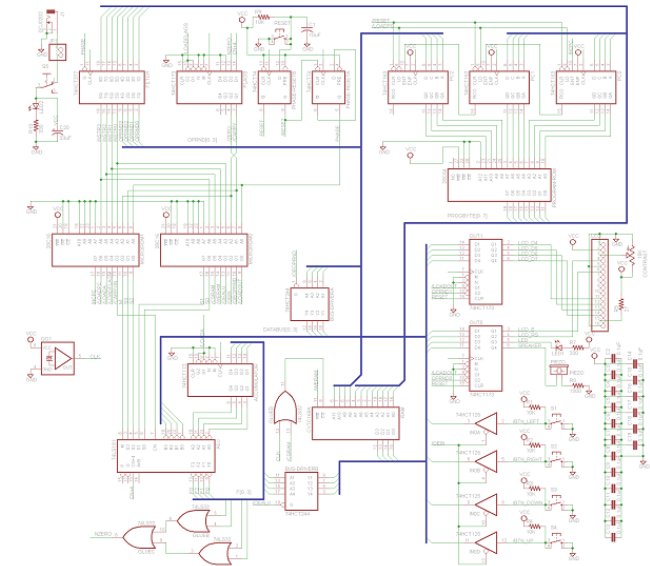
### Basic CPU



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## Digital + Lab logic Motivation

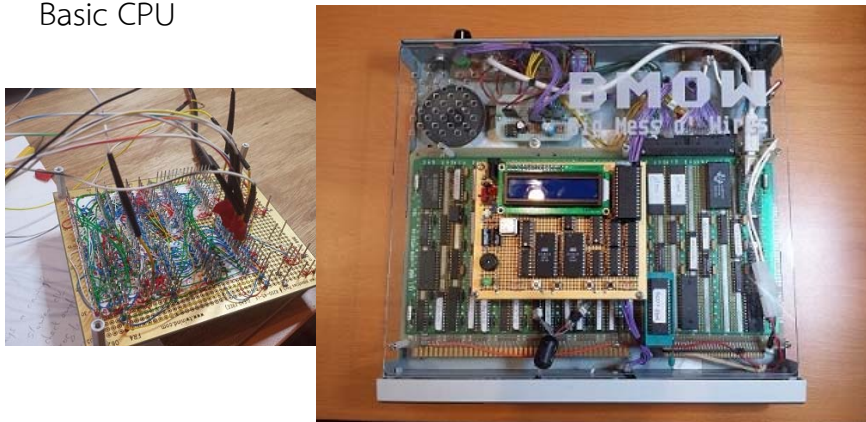
### Basic CPU



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## Digital + Lab logic Motivation

### Basic CPU



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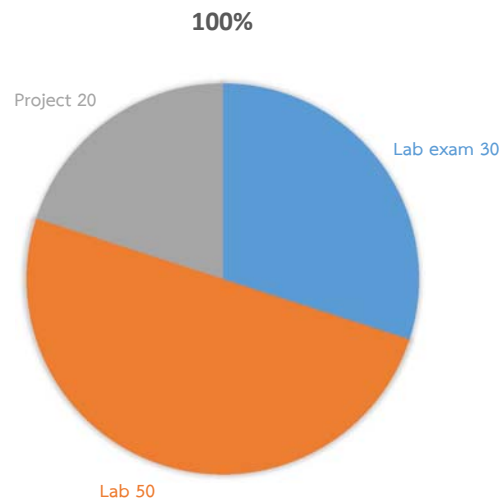
## Course Outline

1. Introduction
2. Logic Gates & Related Devices
3. Combination Circuits I
4. Combination Circuits II
5. Combination Circuits III
6. Sequential Circuit I
7. Sequential Circuit II
8. Sequential Circuit III
9. Sequential Circuit IV
10. FPGA I
11. FPGA II
12. Logic circuit project I
13. Logic circuit project II
14. Lab Exam

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## Assessment



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## Assessment

- Project Lab logic ทำกลุ่ม จะแจ้งขั้นตอนอีกครั้งหนึ่ง
- Lab exam ทำการสอบครั้งเดียว
- การเข้าแลป  $\leq 80\%$ , หมดสีทธีสอบ
- คะแนน lab 50% จะแบ่งอัตราส่วนคะแนนจาก
  - ความสนใจเรียน
  - ใบงานในการเรียนแลป
  - การส่งงานภายในเวลาที่กำหนด

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## Group FB

- ไว้ติดต่อสื่อสาร
- Download Sheet Lab
- ประกาศคะแนน



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