

Logic Gates

Related Devices

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Outline

1. Logic level and Status
2. Logic gates
3. Truth table
4. Logic gates series
5. ICs Package
6. Datasheet

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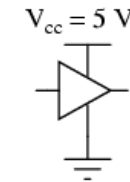
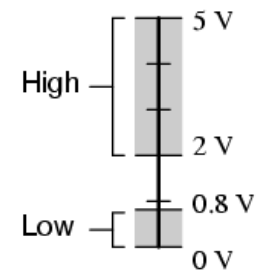
Logic Circuit

Laboratory

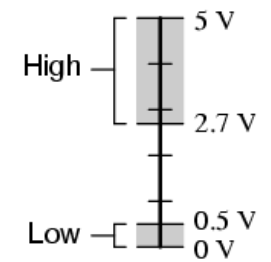
3

Logic level

*Acceptable TTL gate
input signal levels*










*Acceptable TTL gate
output signal levels*



TTL : Transistor-Transistor Logic

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Logic gates

Name	NOT	AND	NAND	OR	NOR	XOR	XNOR																																																																																																
Alg. Expr.	\overline{A}	AB	\overline{AB}	$A + B$	$\overline{A + B}$	$A \oplus B$	$\overline{A \oplus B}$																																																																																																
Symbol																																																																																																							
Truth Table	<table><tr><th>A</th><th>X</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	A	X	0	1	1	0	<table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	B	A	X	0	0	0	0	1	0	1	0	0	1	1	1	<table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	B	A	X	0	0	1	0	1	1	1	0	1	1	1	0	<table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	B	A	X	0	0	0	0	1	1	1	0	1	1	1	1	<table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	B	A	X	0	0	1	0	1	0	1	0	0	1	1	0	<table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>	B	A	X	0	0	0	0	1	1	1	0	1	1	1	0	<table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	B	A	X	0	0	1	0	1	0	1	0	0	1	1	1
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ANSI, IEEE, IEC Standard Symbol

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Truth table

$$\text{AND } Y = AB$$

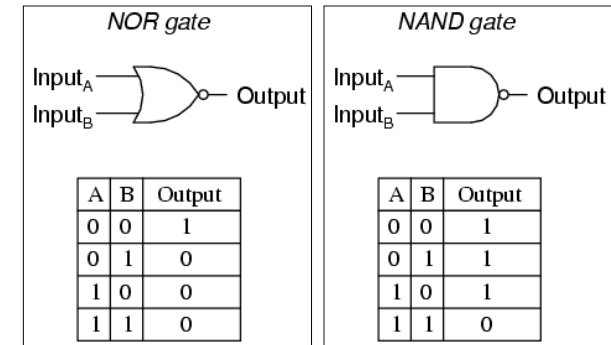
$$\text{OR } Y = A + B$$

$$\text{NOT } Y = \bar{A}$$

$$\text{NOR } Y = \overline{A + B}$$

$$\text{NAND } Y = \overline{AB}$$

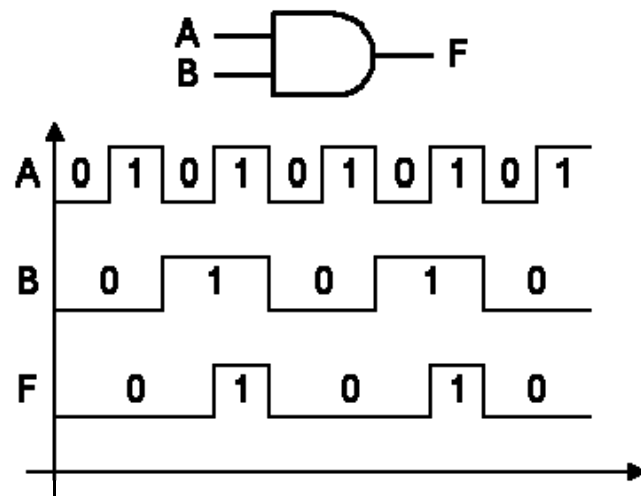
$$\text{XOR } Y = A \oplus B$$



ANSI, IEEE, IEC Standard Symbol

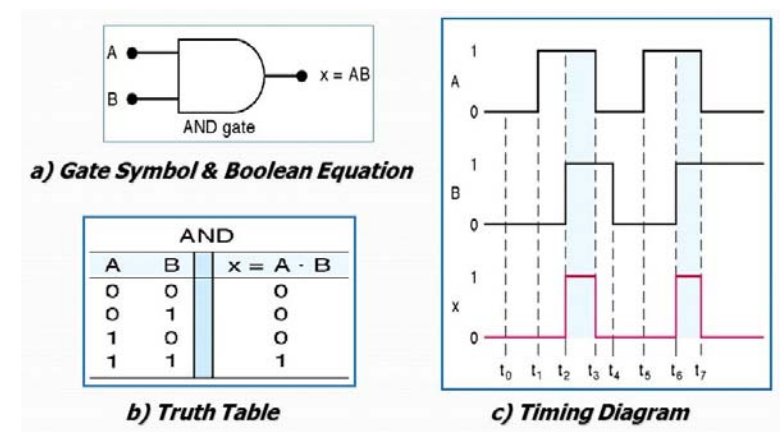
6

Time diagram



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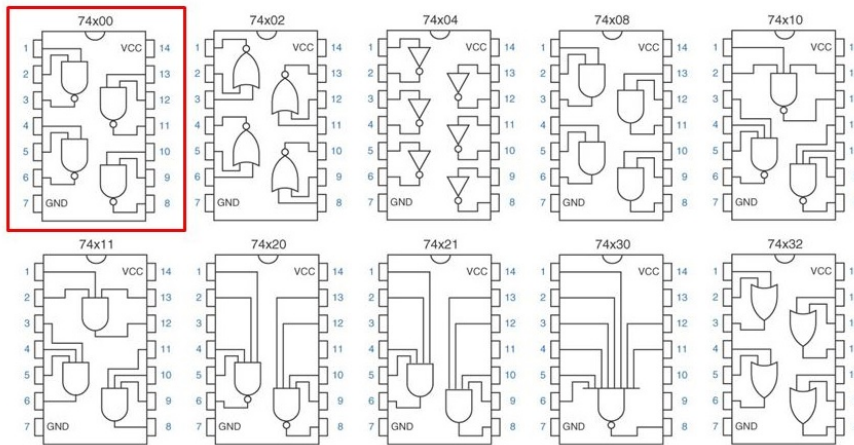
Logic gate



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Logic gates series

7400-series Pin Diagrams



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Logic gates series

ไอซีลอจิก	ชนิดของลอจิกเกต
7400	Quad 2-input NAND gate
7402	Quad 2-input NOR gate
7404	Hex (Inverter) NOT gate
7408	Quad 2-input AND gate
7432	Quad 2-input OR gate

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Logic gates series

ตระกูลลอจิกเกต	ความหมาย
74-	Standard TTL
74L-	Low-Power TTL
74S-	Schottky TTL
74LS-	Low-power Schottky TTL
74AS-	Advanced Schottky TTL
74ALS-	Advanced Low-Power Schottky TTL
74F-	Fast Advanced Schottky TTL

TTL : Transistor-Transistor Logic

TTL จะใช้ BJT (Bi-Junction Transistor) ขั้วเกต เป็นเทคโนโลยีเก่า ปัจจุบันส่วนมากจะใช้ Transistor ชนิด MOSFET ในการขั้วเกตแทน

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Logic gates series

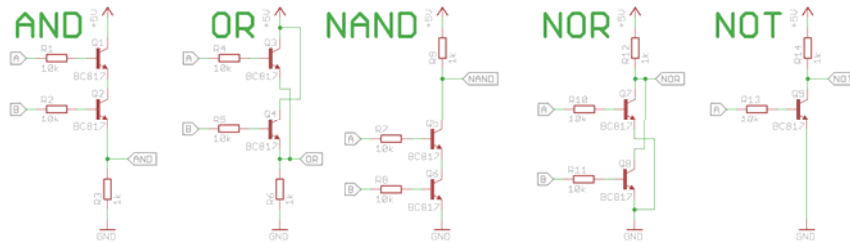
ตระกูลลอจิกเกต	ความหมาย
74HC-	High-Speed CMOS
7HCT-	High-Speed CMOS (TTL-compatible input)
74AC-	Advanced CMOS
74AHC-	Advanced High-Speed CMOS
74LVC-	Low-Voltage CMOS
74VHC-	Very High-Speed CMOS

TTL : Transistor-Transistor Logic

CMOS ข้อดีจะเด่นด้านกำลังขับและการใช้พลังงาน แต่จะออกแบบภายในค่อนข้างซับซ้อน ดังนั้นถ้าจะทำ Logic gates จาก Transistor แนะนำให้การต่อแบบ TTL จะดีกว่า

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Logic gates series



TTL : Transistor-Transistor Logic

CMOS ข้อดีจะเด่นด้านกำลังขับและการใช้พลังงาน แต่จะออกแบบภายในค่อนข้างซับซ้อน ดังนั้นถ้าจะทำ Logic gates จาก Transistor แนะนำให้การทำแบบ TTL จะดีกว่า

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Recommend Electronic Parts



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Recommend Electronic Parts

ถ้าไม่มีใน www.es.co.th ส่วนมากต้องสั่งจาก ตปท



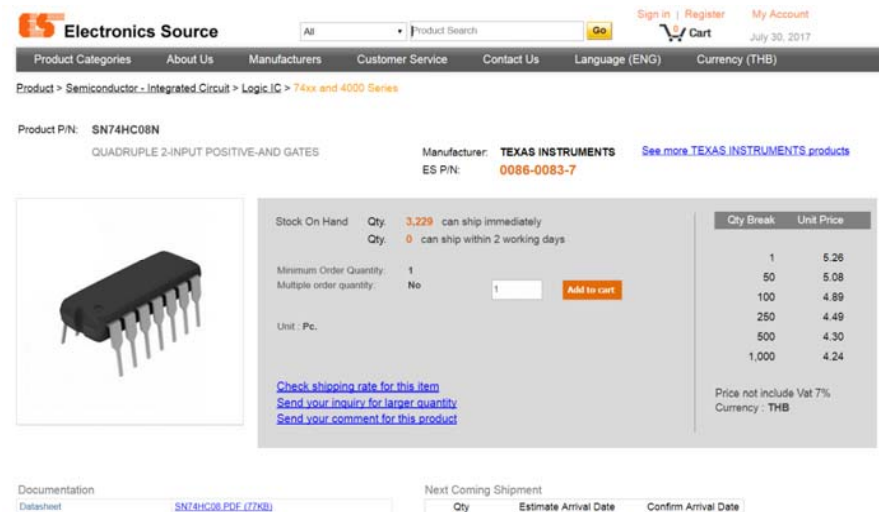
<http://th.element14.com>



www.digikey.com

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Search Ex. Logic gates -> 74HC08 AND Gate



www.es.co.th

download Datasheet

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Search Ex. Logic gates -> 74HC08 AND Gate

SN54HC08, SN74HC08
QUADRUPL 2-INPUT POSITIVE-AND GATES

SCL5081B - DECEMBER 1982 - REVISED MAY 1997

SN54HC08... J OR W PACKAGE
SN74HC08... D, N, OR PW PACKAGE
(TOP VIEW)

description

These devices contain four independent 2-input AND gates. They perform the Boolean function $Y = A \cdot B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

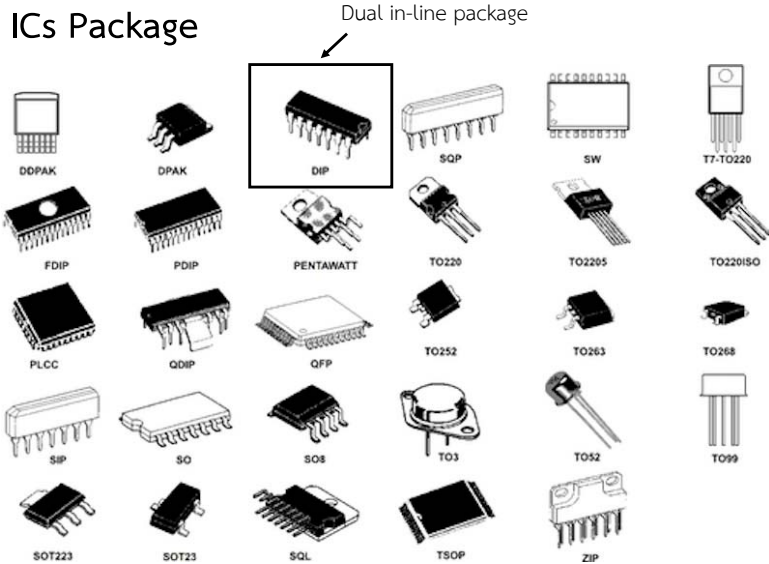
The SN54HC08 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC08 is characterized for operation from -40°C to 85°C .

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†

PIN

ICs Package



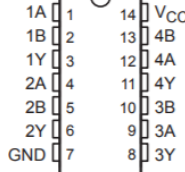
source: SparkFun Electronics

ICs Package

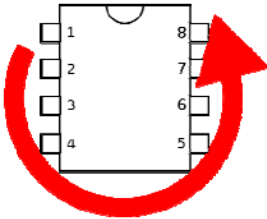
SN54HC08, SN74HC08
QUADRUPL 2-INPUT POSITIVE-AND GATES

SCL5081B - DECEMBER 1982 - REVISED MAY 1997

SN54HC08... J OR W PACKAGE
SN74HC08... D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC08... FK PACKAGE
(TOP VIEW)



Search Ex. Logic gates -> 74HC08 AND Gate

SN54HC08, SN74HC08
QUADRUPL 2-INPUT POSITIVE-AND GATES

SCL5081B - DECEMBER 1982 - REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	$-0.5\text{ V to }7\text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	$\pm 20\text{ mA}$
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	$\pm 20\text{ mA}$
Continuous output current, I_O ($V_O = 0$ to V_{CC})	$\pm 25\text{ mA}$
Continuous current through V_{CC} or GND	$\pm 50\text{ mA}$
Package thermal impedance, θ_{JA} (see Note 2): D package	127°C/W
N package	78°C/W
PW package	170°C/W
Storage temperature range, T_{Stg}	$-65^{\circ}\text{C to }150^{\circ}\text{C}$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

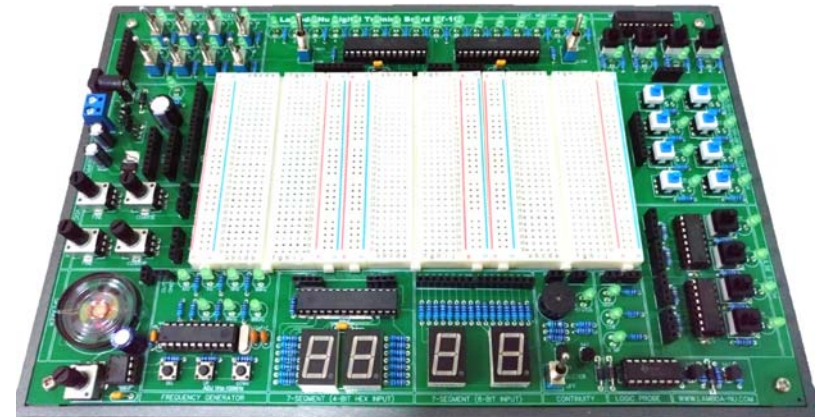
		SN54HC08			SN74HC08			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$		1.5	$V_{CC} = 2\text{ V}$		1.5	V
		$V_{CC} = 4.5\text{ V}$		3.15	$V_{CC} = 4.5\text{ V}$		3.15	
		$V_{CC} = 6\text{ V}$		4.2	$V_{CC} = 6\text{ V}$		4.2	
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0	$V_{CC} = 2\text{ V}$		0	V
		$V_{CC} = 4.5\text{ V}$		0	$V_{CC} = 4.5\text{ V}$		0	
		$V_{CC} = 6\text{ V}$		0	$V_{CC} = 6\text{ V}$		0	
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
t_t	Input transition (rise and fall) time	$V_{CC} = 2\text{ V}$		0	$V_{CC} = 2\text{ V}$		1000	ns
		$V_{CC} = 4.5\text{ V}$		0	$V_{CC} = 4.5\text{ V}$		500	
		$V_{CC} = 6\text{ V}$		0	$V_{CC} = 6\text{ V}$		400	
T_A	Operating free-air temperature	-55	125	-40	85			$^{\circ}\text{C}$

LAB1 START

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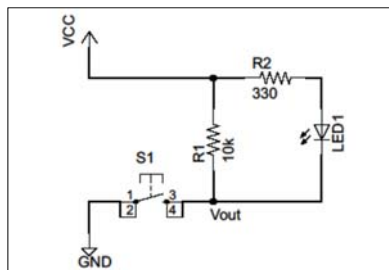
LAB1.1 เรียนรู้การใช้งานบอร์ด Logic circuit lab

บอร์ดทดลอง Logic circuit

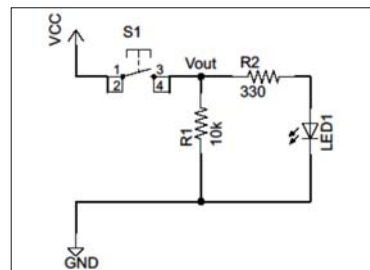


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LAB1.2 ทดลองการใช้งานเบื้องต้น ผ่านการต่อ Switch



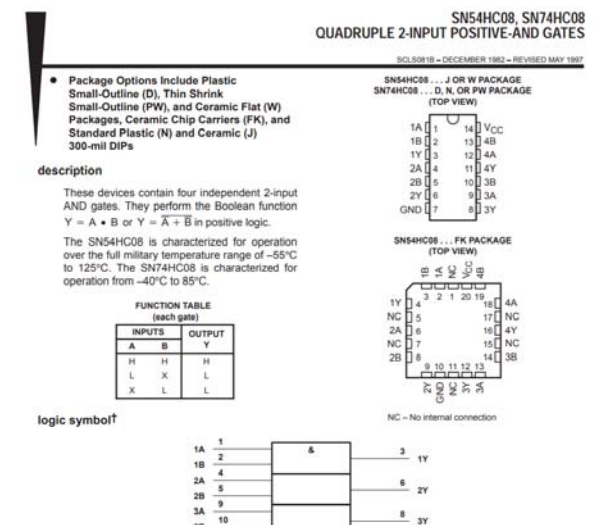
Pull up



Pull down

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LAB1.3 หาข้อมูล ICs



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LAB1.2 ทดลอง Logic gates แบบง่าย

