Micro Processor: is a central processing unit (cpu) that serves as the Primary component of a Computer responsible for executing instructions and performing arithmetic and logic operations in electronic devices it contain: Alu > (arithmetic logic unit) using in perform some basic calculation for example: addition, divison, etc. Cu_s(controlunit) used in decode and exacute instraction Registers _ to store data In ALU out Micko phocesson Cu Registers Memory unit

Micro Controller: It is a Ic contain processor Ray, Roy and Input foutput ports sate of different peripherals designed for embedded Systems to perform a spacific bask Send TiMers 1/20010 NOM Mich Controller Liagram

| 1111 |
|---|
| embedded systeam: it is alimited legatice computing control system with |
| |
| a specific functions |
| Micatronic system: the integration of Mechanical |
| Systems with electronics and software to deate |
| More functional and efficient products and |
| Processes |
| N-bit Processor: |
| 1 - processor works only on n-bit of data at a time |
| 2. Data larger than n-bit has to be broken into n-bi |
| Pieres to be processed |

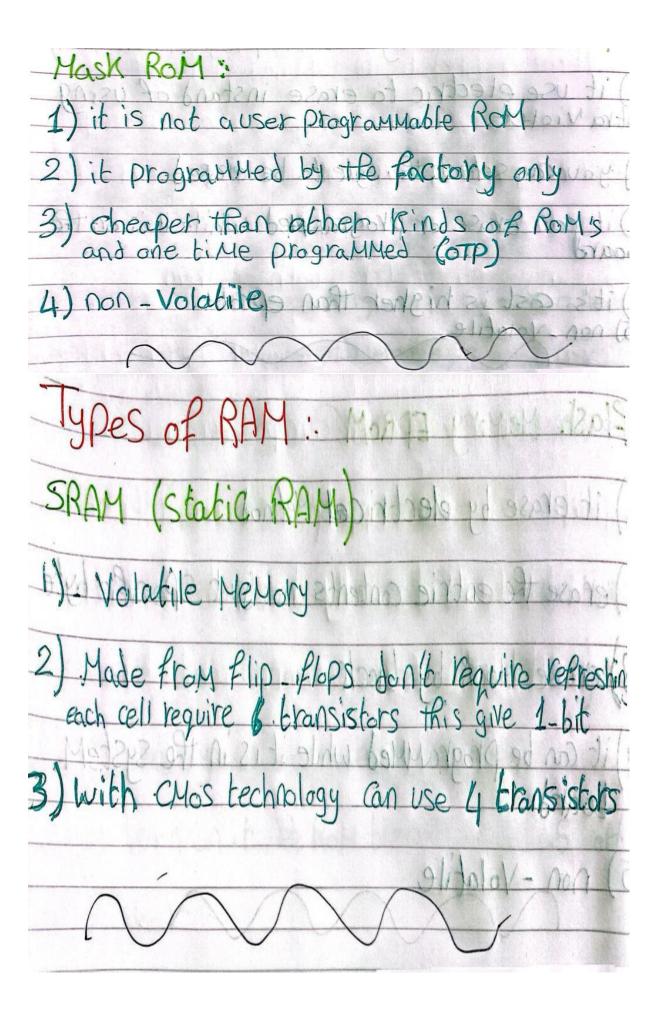
| realistic said 1: The interpretage of technical | | | | | |
|--|--|--|--|--|--|
| Micro Processor | Microcontroller | | | | |
| used in personal computer | A CONTRACTOR OF THE CONTRACTOR | | | | |
| Costishigh | Cost is lowe 922 900 19 | | | | |
| high power usage | low power usage id | | | | |
| Based on von NeuMann | Based on harvard | | | | |
| Ram, RoM, I/o units and other peripherals are not embedded on asingle chip | periperals are embedded | | | | |
| since MeMory and I/o are connected externally the circuit become large in size | Since Meuory and IB are present together the internot circuit is small in Size | | | | |

Von Neumann Architecture: is adigital Computer earchitecture whose design is based on the concept of stored program computers where program data and instruction data are stored in the same Memory also single bus fetches both of them

Harvard Architecture: is a digital computer architecture whose design is based on the concept where there are separate storage and separate buses for instruction and data it was basically developed to overcome the battlemeck of von Neumann architecture

| Types of Rom: |
|--|
| DR-11 (Dravallable ROU) |
| 1) User an burn information into it |
| 2) For every bit there is a fuse |
| 3) programmed by blowing the fuses |
| 4) PROM programmed only once so it is called |
| otp (one The programmable) 5) non-volatile |
| - EPROM (Erosable programable ROM) so |
| 1) can be programed and erased thousands live |
| 2) widely used (eprom) called (uvertoM) |
| 3) erased by ultra violet radiation |
| 4) to burn on it - the ROM burner uses 12.5 volt |
| or higher |
| 5) one of its disadvantage that it cannot be erased while it is in the system board 6) non-volatile |
| |

EEProm (electrically erosable Programmable Rom) 1) it use electric to erase instand of using vitra Violety oldining org 15 2012 don Ri 2) you can select the byte to be erosed 3) it can exase or programped while it is on the 4) it's cost is higher than eproved of 5) non-volatile Flash Memory EPROM 1) it erase by electrical Method 2) erase the entrie contents not just specific byte 3) erase block by block 4) it can be programmed while it is in the system board 5) non-Volatile



NVROM (non volatile RAM 1) it allow cpu to write and read on-it and when the power is off the contents are not lost 2) it can store contents up to lo years after power is off 3) use lithium battery as a backup energy source 4) it use show cells built out of Mos DRAM (Dynamic RAM) 1) Volatile Memory 2) cheaper than SRAM 3) Use copacitors as storage cells and it require constant refreshing due to charge leakage 4) While it is in refreshing data Cannot access

Mornal aperations the cpu does not have the Capability to write to it

It May be written to by an external device or there May be a special configuration within the system wherein the cpu is granted access to write to it

| Type | volatile | writeable | Erase Size | Max erase Cycle | Cost for bute | speed |
|---------------|----------|-----------|----------------|--------------------|-------------------------------|-------------------------------|
| SRAM | yes | yes | Byte | unlimited | expensive | Fast |
| DRAM | yes | yes | Byte | unlimited | Moderate | Moderate |
| Masked RoM | No | No | NA | NIA | Inexpensive | Fast |
| PROM | No | once | NIA | NIA | Moderate | fast |
| EPROM | No | yes | entrie Chip | limited | Moderate | fast. |
| EEPROM | No | yes | Byte | limited | expensive. | Fast to read slow to write |
| <i>Plash</i> | Νο | yes | Sector | Limited | Moderate | Rast to read slow to writ |
| LVRAM | No | yes | Byte | unlimited | expensive SAAM+ battery | Fast |