

Creating a schematic diagram using Quartus 17.0

This tutorial creates a schematic diagram for a full adder on Quartus and simulate its behavior with timing diagrams. There are two video tutorials to follow, both were created using an older version of Quartus (version 15.0). This document highlights the differences between version 15.0 and 17.0 so please refer to this document while watching the videos to adjust the steps to match version 17.0

I. Creating a Schematic diagram for a full adder

Please follow the steps in the following video tutorial while making the necessary adjustments highlighted in this document for version 17.0

<https://www.youtube.com/watch?v=qn6ggwxdjQ&t=109s>

The steps are all the same. However, here is a clearer picture of the **Family, Device & Board Settings**, in case they were not clearly visible in the video from **0:48-1:15**

Family, Device & Board Settings

Device

Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Device: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: FBGA

Pin count: 896

Core speed grade: 6

Name filter:

☒ Show advanced devices

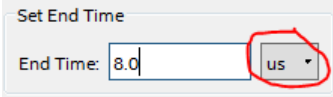
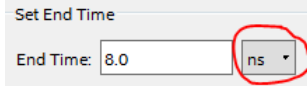
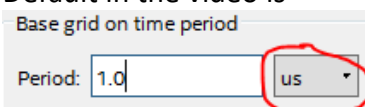
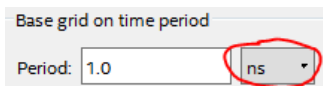
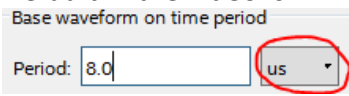
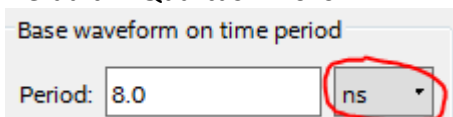
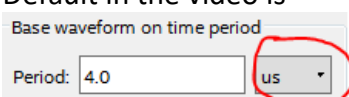
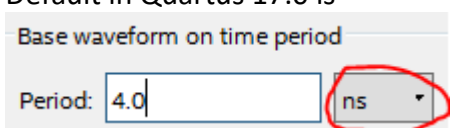
Available devices:

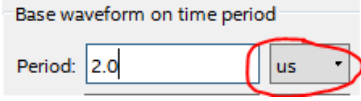
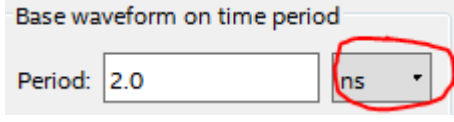
| Name | Core Voltage | ALMs | Total I/Os | GPIOs | GXB Channel PMA | GXB Channel PCS |
|--------------|--------------|-------|------------|-------|-----------------|-----------------|
| 5CSEMA5F31C6 | 1.1V | 32070 | 457 | 457 | 0 | 0 |

II. Simulating the full adder with Waveforms

After creating the schematic diagram please follow the steps in the following video to simulate the full adder circuit. Note the differences listed in the table to adjust to version 17.0

https://www.youtube.com/watch?v=e_ksjHd6sY0&t=6s

| Timestamp | Function | Old Instructions in Video | Updated instructions |
|-----------|-------------------------------|---|--|
| 1:28 | Set end time | Default in the video is  | Default in Quartus 17.0 is  Note: Please ensure that you change this default nanoseconds to microseconds as mentioned in the video |
| 1:42 | Set grid size | Default in the video is  | Default in Quartus 17.0 is  Note: Please ensure that you change this default nanoseconds to microseconds as mentioned in the video |
| 2:09 | Input A value-Overwrite Clock | Default in the video is  | Default in Quartus 17.0 is  Note: Please ensure that you change this default nanoseconds to microseconds as mentioned in the video |
| 2:24 | Input B value-Overwrite clock | Default in the video is  | Default in Quartus 17.0 is  Note: Please ensure that you change this default nanoseconds |

| | | | |
|------|-----------------------------------|---|--|
| | | | to microseconds as mentioned in the video |
| 2:43 | Input C value- Overwrite clock | Default in the video is  | Default in Quartus 17.0 is  <p>Note: Please ensure that you change this default nanoseconds to microseconds as mentioned in the video</p> |

II.a. Additional instructions for running waveform

Follow the instructions on the video until **3:30**. Then follow the given steps after saving the “fulladder.vwf” in the project directory.

1. Go to Simulation -> Simulation Settings

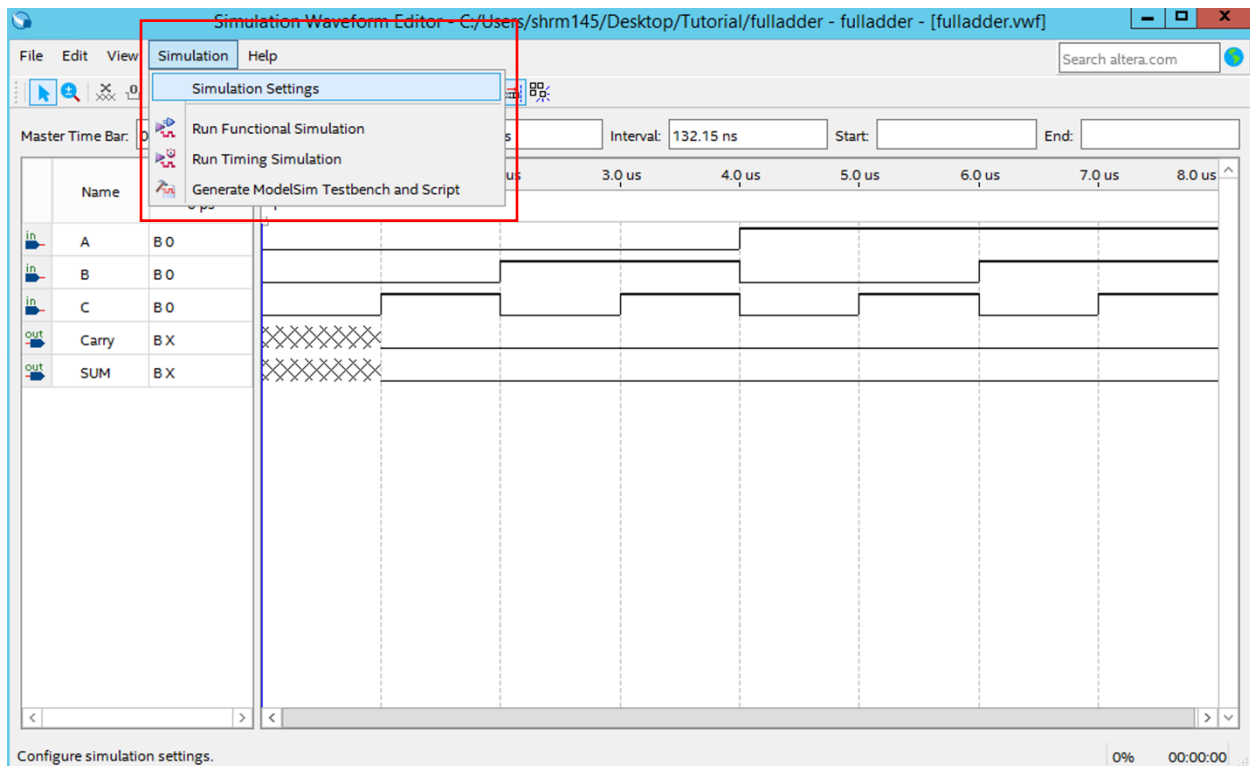


Fig 1.

2. Under the “**Functional Simulation Settings**” tab, make the following changes:
 - a. Change the highlighted **Waveform.vwf.vt** in the above image to **fulladder.vwf.vt** (See Fig 2a.)

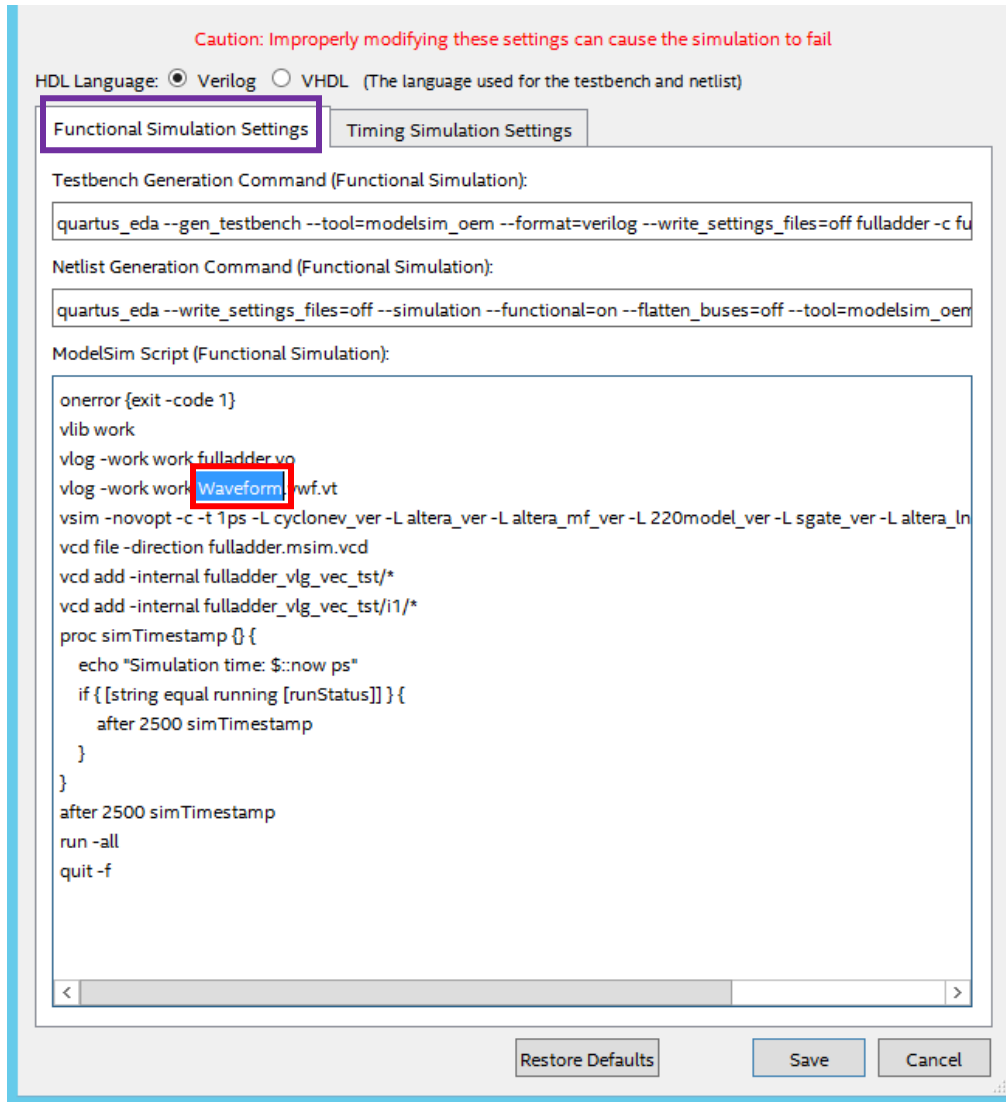


Fig 2a.

- b. In the **Testbench Generation Command (Functional Simulation)**, keep scrolling right until you reach the blue highlighted text, which dictates the file for the “vector-source”. Again, change this from **Waveform.vwf** to **fulladder.vwf** (See Fig 2b.)

Note the green box that depicts the change made in step 2a

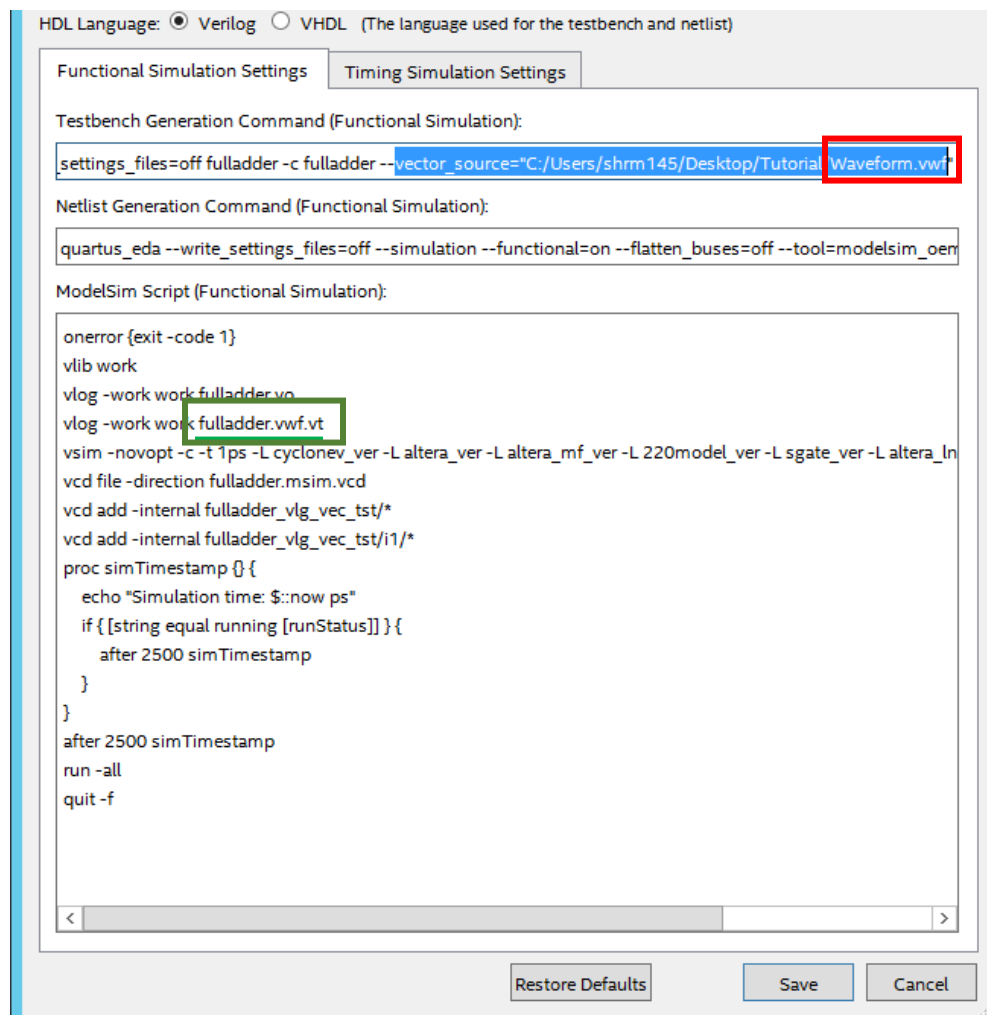


Fig 2b.

- c. In the **Testbench Generation Command (Functional Simulation)**, continue scrolling right until you reach the blue highlighted text, which dictates the file for the “testbench-file”. Again, change this from **Waveform.vwf** to **fulladder.vwf** (See Fig 2c.)

Note the green boxes that depicts the change made in step 2a and 2b.

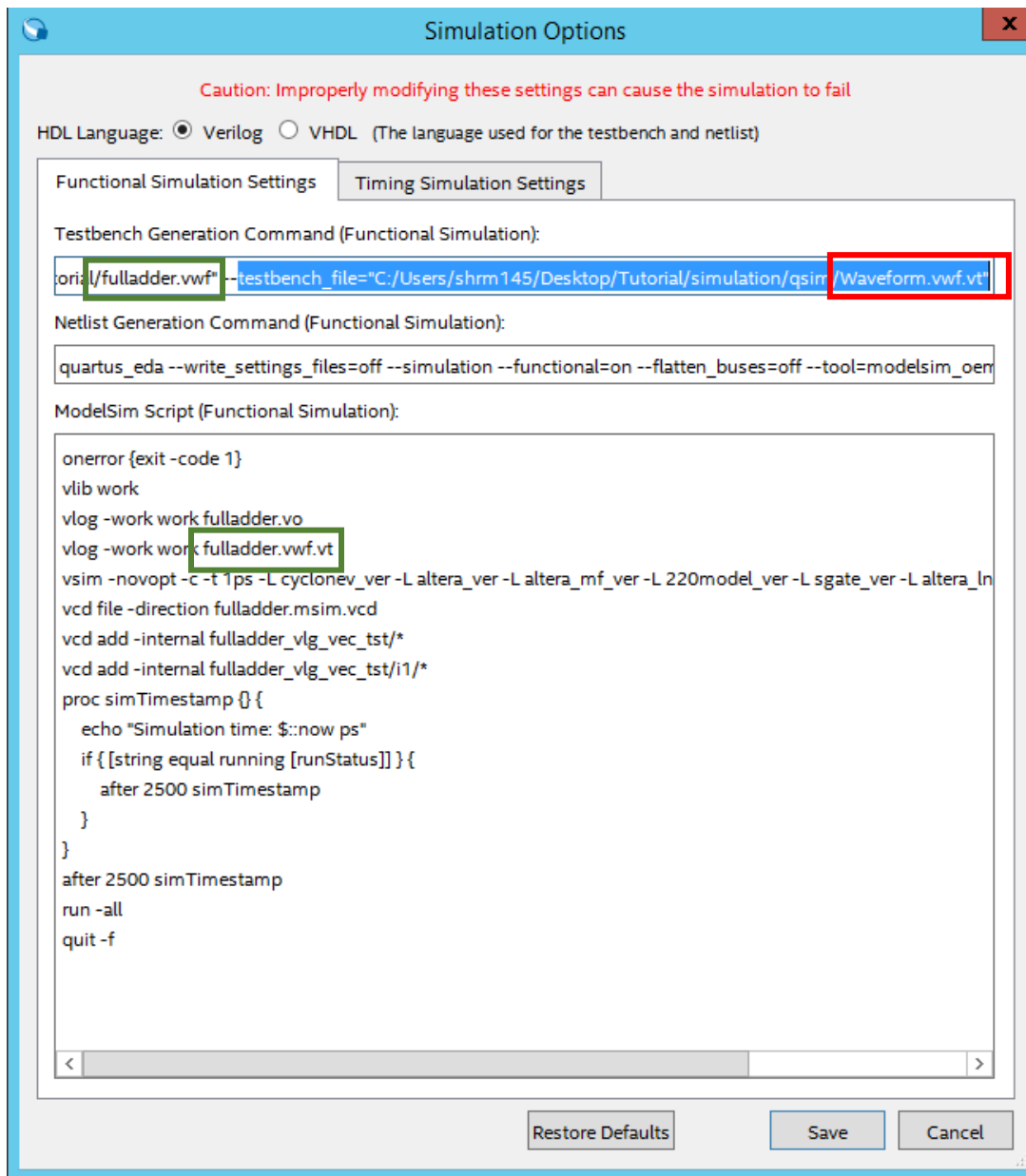


Fig 2c.

3. Next, go to the **Timing Simulation Settings** and repeat steps 2b. and 2c. and then **SAVE** your changes (See Fig 3).

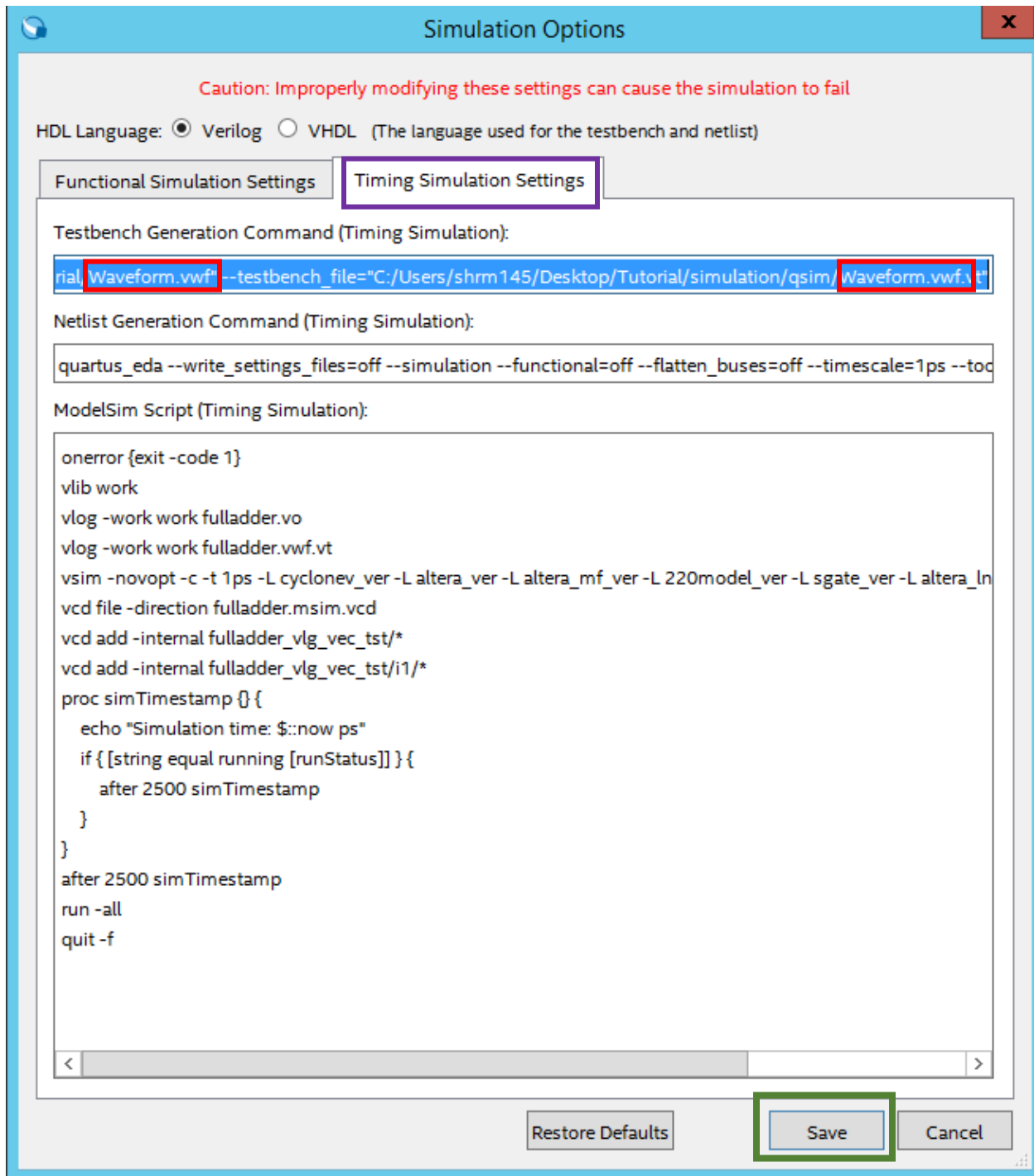


Fig 3: Change the “Waveform.vwf” in the red boxes to “fulladder.vwf”. **DO NOT FORGET** to save your settings by clicking on the “Save” button in the green box

4. Now you are all set! You can go ahead and run the simulation by clicking on **Run Function Simulation** (See Fig 4.)

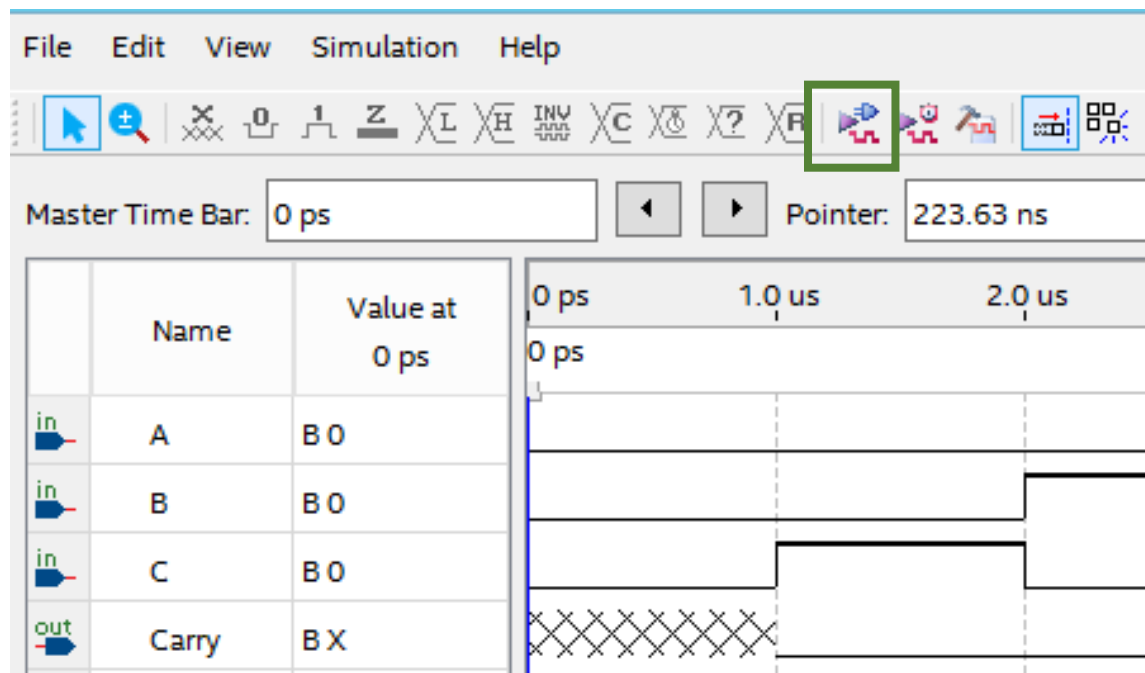


Fig 4: Click on the symbol in the green box to “Run functional simulation”