

EE/CSE 371:
Design of Digital Circuits and Systems

DE1 SoC & LabsLand Breadboard GPIO guide

GPIO on the DE1-SoC board:

The DE1-SoC board has two General Purpose I/O ports (GPIO_0 and GPIO_1) with 40-pin (2x20) expansion headers that are used to connect peripherals to the board. The GPIO pin assignments for the two 2x20 pin expansion headers are already defined in a .qsf file (generated by Quartus), so you can add them to your top-level SystemVerilog module in the same way as the switches and LEDs.

The objective of this document is to interface a circuit built on a breadboard with the DE1-SoC through GPIO. We will use a virtual breadboard on LabsLand.

Steps of interfacing a virtual breadboard with a remote FPGA on LabsLand:

1. Log into your LabLands account (please refer to Lab 0 on setting up a LabsLand Account).
2. Navigate to the SystemVerilog IDE.
3. Locate the “User interface” heading above the Documentation box and click “Edit” next to it. The resulting pop-up window can be seen in Figure 1. In the pop-up window, select the “Breadboard” option and click the “Configure” button under the “Breadboard” tile.

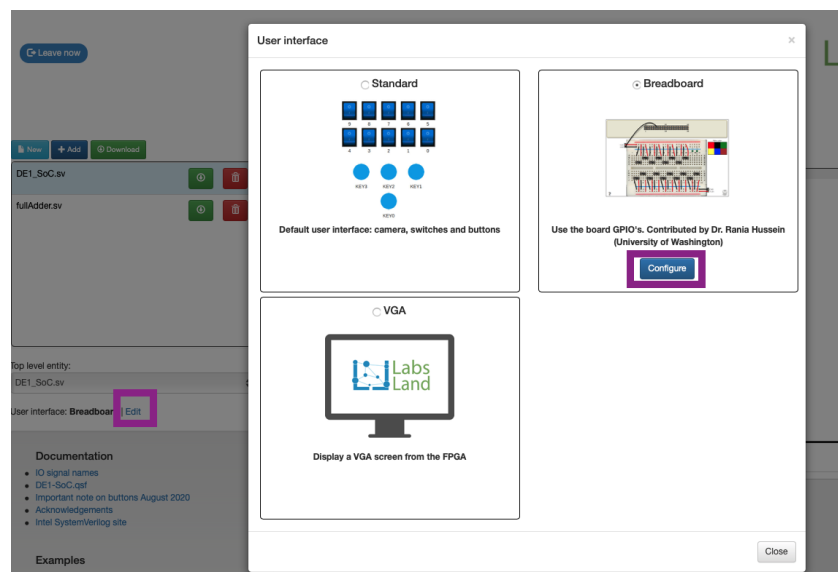


Figure 1. LabsLand Select Interface

- You will be directed to the setup window that can be seen in Figure 2. In this window, you can connect circuit components that are available on the breadboard (switches and LEDs) to the GPIOs. The left side shows the relationship between GPIO_0 and JP1. The right side is the actual configurator you will use to connect wires between the GPIO_0 and the circuit components. First, click on a wire color on the right to select a wire. With the wire selected, your mouse now acts as a pen for drawing wires, and thus you need to click and hold your mouse to draw a cable connecting the GPIO header and the breadboard. Repeat the process to create all the wires for your design. All the connections on the breadboard will be automatically saved at this point.

Note: You can only use GPIO0_0[5] - GPIO0_0[22] as inputs, and GPIO0_0[26] / GPIO0_0[27] as outputs. Please make sure you wire your components accordingly on the configurator.

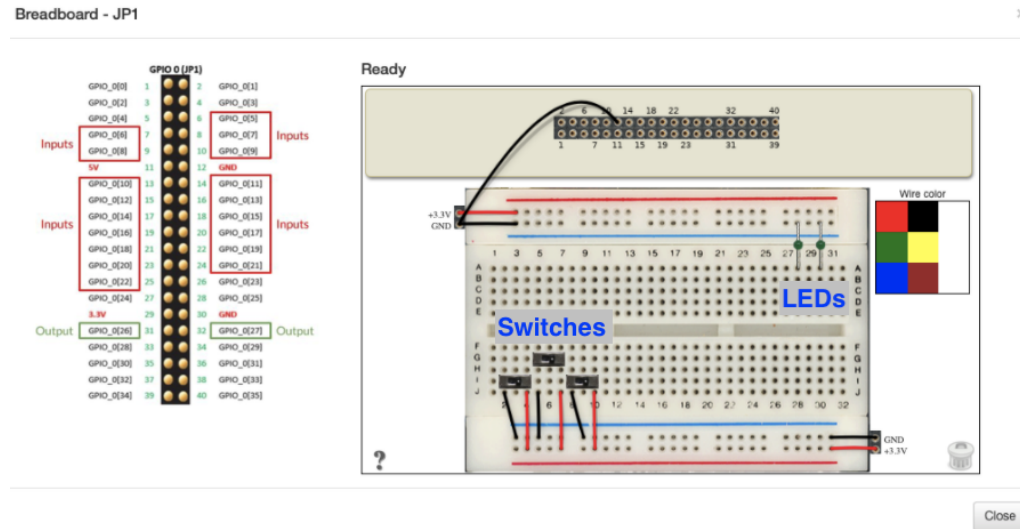


Figure 2. The breadboard configurator on LabsLand

- Once you send the code to the FPGA, you will see the breadboard exactly as you left it in the breadboard configurator shown in Figure 2. Please see Figure 3 as a reference.

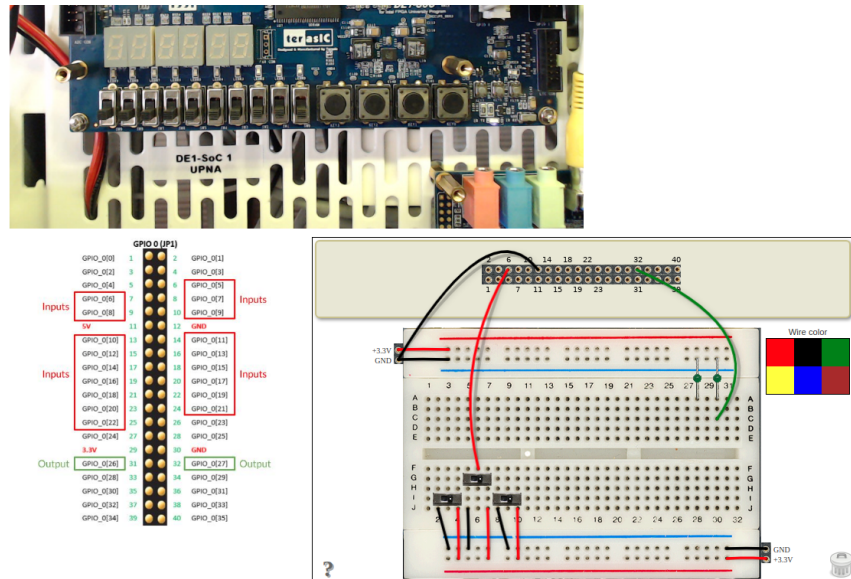


Figure 3: LabsLand load onto FPGA

Sample Code

```
// DE1_SoC.sv
// This example shows how to control a LED on the breadboard using a
// switch on the breadboard. The components on the breadboard are
// wired according to Figure 3. Specifically, one switch is connected
// to GPIO_0[5] (pin #6 of JP1), and one LED is connected
// to GPIO_0[27] (pin #32 of JP1).
```

```
module DE1_SoC (GPIO_0);
    // SW and KEY cannot be declared if GPIO_0 is declared on LabsLand
    inout logic [33:0] GPIO_0;
    // Assign GPIO_0[27] (LED) to GPIO_0[5] (switch)
    assign GPIO_0[27] = GPIO_0[5];
endmodule
```

```
module DE1_SoC_testbench();
    wire [33:0] GPIO_0;
    logic sw;
    DE1_SoC dut (.GPIO_0);
    // Use logic to drive GPIO_0[5] (switch) in the testbench
    assign GPIO_0[5] = sw;
    initial begin
        sw=1; #50;
        sw=0; #50;
    end
endmodule
```