EE/CSE 371:
Design of Digital Circuits and Systems

Lab6: Design Project

System Requirements

- At least one input device
  - N8 Controller[1]
  - Keyboard
  - Joystick
- At least one output device
  - VGA
  - Audio

A collection of drivers are available to you, to use as you see fit. You can find these drivers on Canvas.

Your project is entirely your own. Come up with the idea that fits the above requirements and appeals to you.

Our Project Ideas

The following are some ideas to consider:

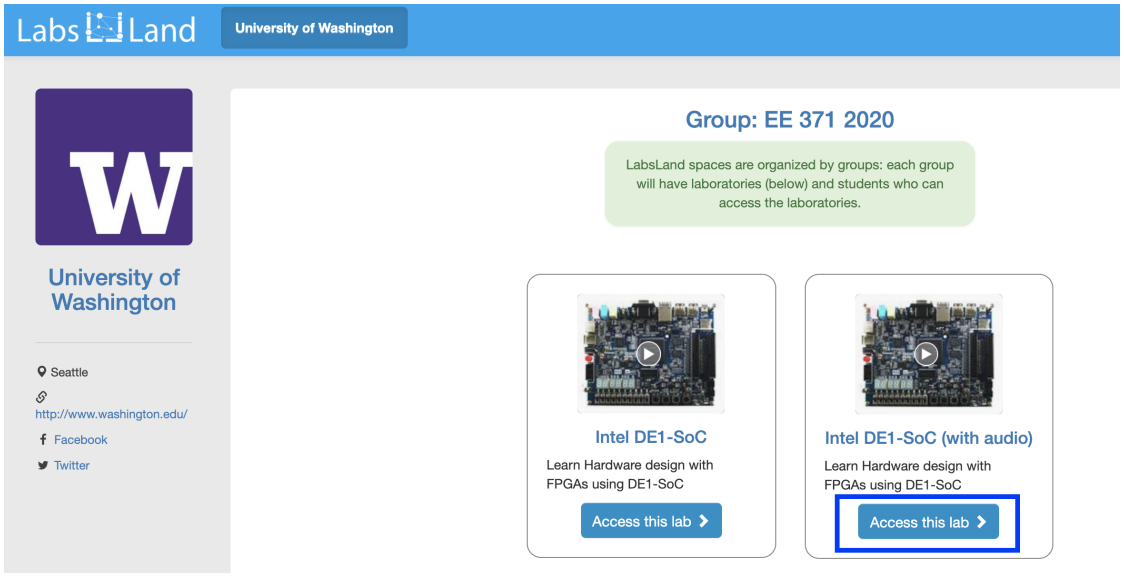
- Games:
  - Sidescrollers: The player moves through a level, avoiding or destroying some kind of obstacles or enemies.
  - Combat: Two or more players compete to collect points, maybe with projectiles or by growing their own body as an obstacle.
    - These projects could potentially be implemented with very basic low-resolution squares that move around a screen. You need to come up with innovations (extra animation, features, etc.) that make the project stand out, and distinguish it from a 271 project in terms of complexity and creativity.
  - Puzzle Games: Tetris, or something of similar complexity.
- Video-centric:
  - Audio spectrum visualizer: create an audio spectrum visualizer using the VGA output of the DE1 board and the Audio CODEC

[1]The N8 Controller cannot be used with the keyboard and the Joystick at the same time

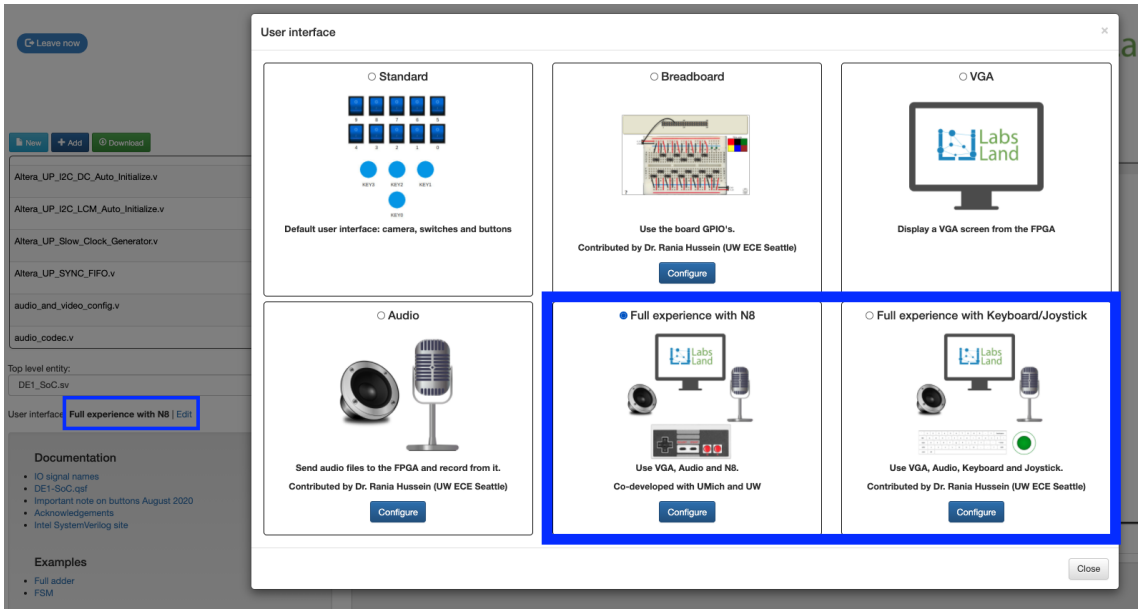
Using the “Full Experience” Interface on LabsLand

You will need to use the “Full Experience” interface in the LabsLand IDE to implement your project. Please follow these steps:

1. Log in to your LabsLand account. Enter the EE371 group and locate the “Intel DE1-SoC (with audio)” lab. Click on the “Access this lab” button.



2. Enter the “DE1 IDE SystemVerilog” IDE and click on the “Edit” next to the user interface switch. Then, in the pop-up window, select “Full experience with N8” or “Full experience with Keyboard/Joystick”, depending on your preferences.



Lab Demonstration and Submission Requirements

- While working on the lab, on Padlet, write about a problem you had in the lab and the fix to it, and share a tip or trick you learned. You can also share an aha moment that you discovered while working on the lab. Avoid duplicating comments made by your classmates. NO videos for this Padlet task, please use textual comments. The link to the Padlet can be found in the corresponding Canvas assignment. Please note that the grace period does **not** apply to this portion of the lab.
- Record a demo video for your project. The length of the video is expected to be 2-3 minutes. You will need to demonstrate the soundness of your design by executing the design on the FPGA. You do not need to include Modelsim simulations in your demo for this lab. You only need to demonstrate the functionality of your system. Your demo video must be a screen recording created from software like ActivePresenter or Zoom. Please refer to the grading rubric on Canvas. Please note that the grace period does **not** apply to this portion of the lab.
- Write a Lab Report, as framed by the Lab Report Outline document on Canvas. Comment your code. Follow commenting guidelines as discussed in the Commenting Code document on Canvas. Please be sure to include required diagrams in your Lab Report. Please include the simulation results in your lab report. Please include waveforms for all modules you used unless it is explicitly stated otherwise. Submit your lab report as a pdf file and all of your Verilog, SystemVerilog, and other relevant files on Canvas. Please refer to the grading rubric on Canvas. As the grace period applies to the lab report and code assignment, you may submit it up to 2-days late without receiving a late penalty.