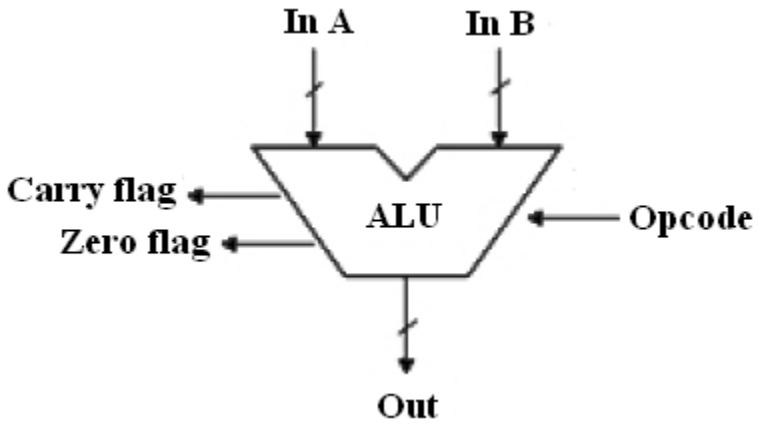
Verilog training – second session

Covered modules: 3, 4, 5, 7, 11

Assignment:

- Create 8-bit full-adder/subtractor using your own 1-bit full-adder. Note, while testing this module use only positive numbers, which means most significant bit must be 0. Do you why?
- Use your 8-bit full-adder/subtractor to create the described 8-bit ALU in the figure below.



  - Inputs:
    - A, B : 8-bits
    - Opcode : 3-bits
    - Carry_in : 1-bit
  - Outputs:
    - Out : 8-bits
    - Carry_out : 1-bit
    - C_flag : 1-bit (c_flag=1 only if A > B, and 0 otherwise)
  - Operations:

000	A + B
001	A - B
010	A & B
011	A | B
100	A ^ B
101	A > B
110	A << 1
111	B << 1

P.S. create your own test fixture to test your design, generate all possible input patterns and check correctness of output automatically.