Simple Arithmetic and Logic Unit Spec

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- Given a simple ALU design.
- Write a UVM based testbench to verify the design.

1. Design is clocked.
2. Reset type is Active High. (Reset when value=1).
3. Send input on current cycle, DUT gives output on next cycle.
4. Does not support back-to-back transactions.
5. Only four operations supported (ADD, SUB, MULT, DIV).
6. Input A should always be greater or equal to Input B.

Port Name	Type	Property	Size "bits"
Clock	Input	Wire	1
Reset	Input	Wire	1
In_1	Input	Wire	8
In_2	Input	Wire	8
Alu_Sel	Input	Wire	4
Alu_Out	Output	Reg	8
Carry_Out	Output	Bit	1

Alu_Sel	Operation
0	Add
1	Sub
2	Mul
3	Div
4	And_bw
5	Or_bw
6	Xor_bw
7:15	Reserved

bw means bitwise.