Chipions 24

UART-TX

Universal Asynchronous Receiver/Transmitter

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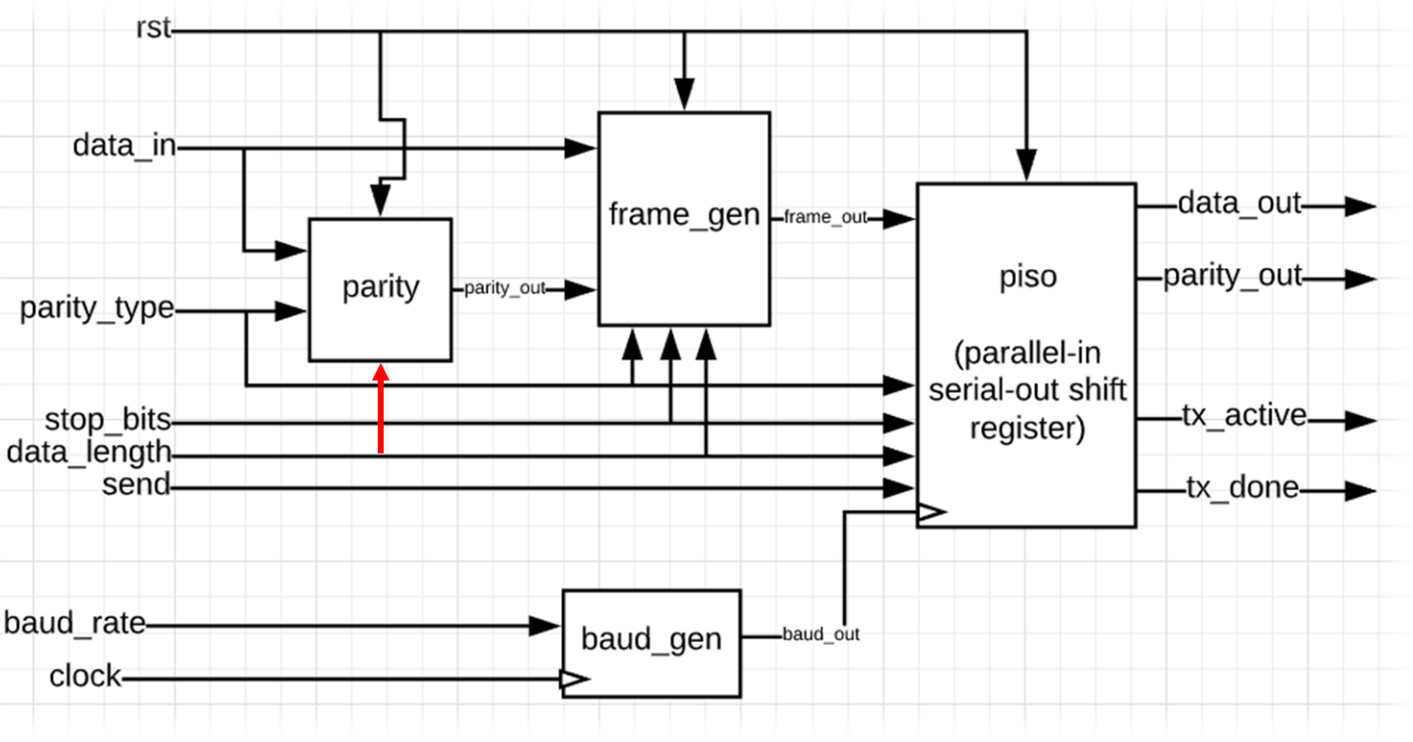
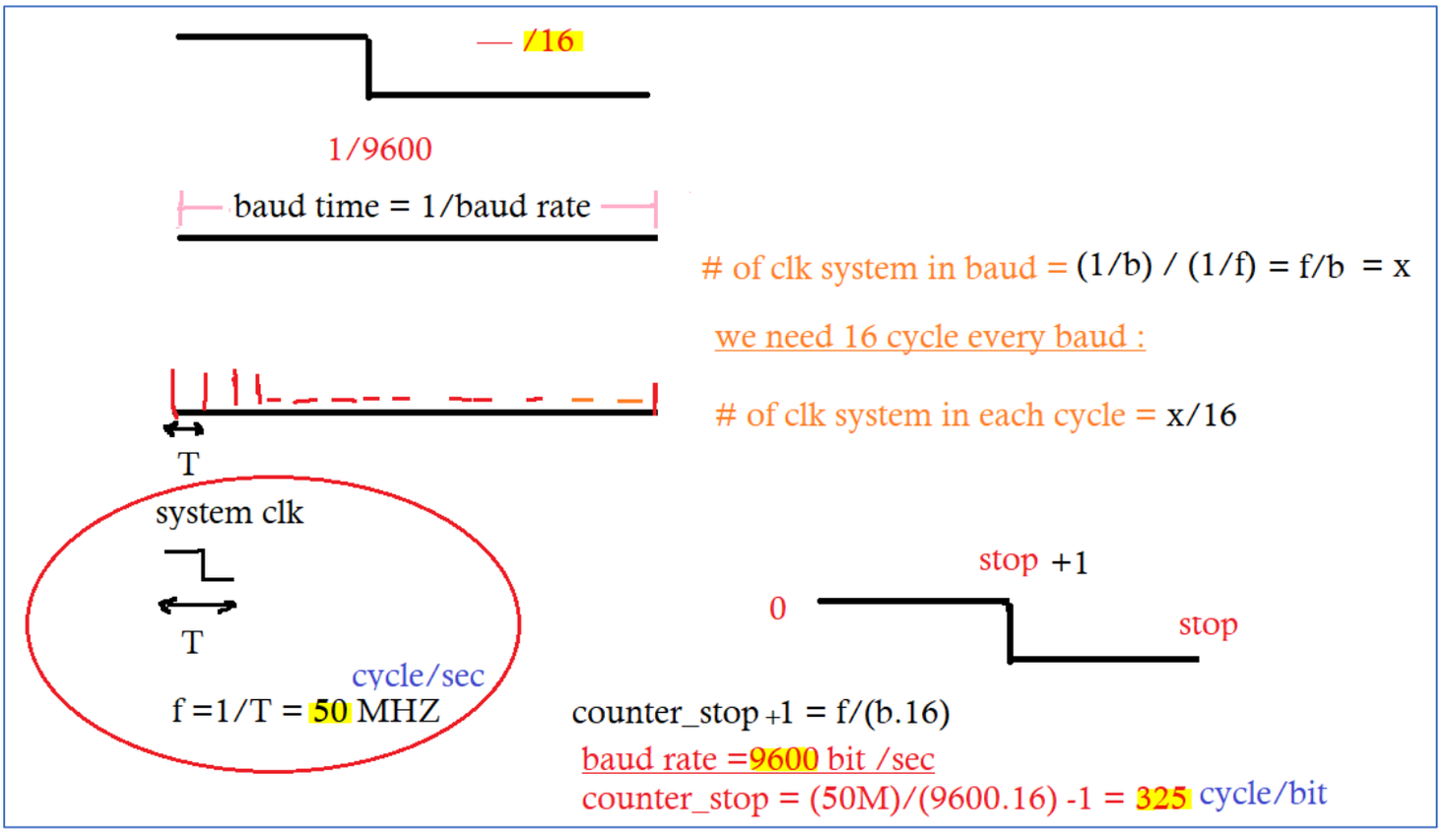
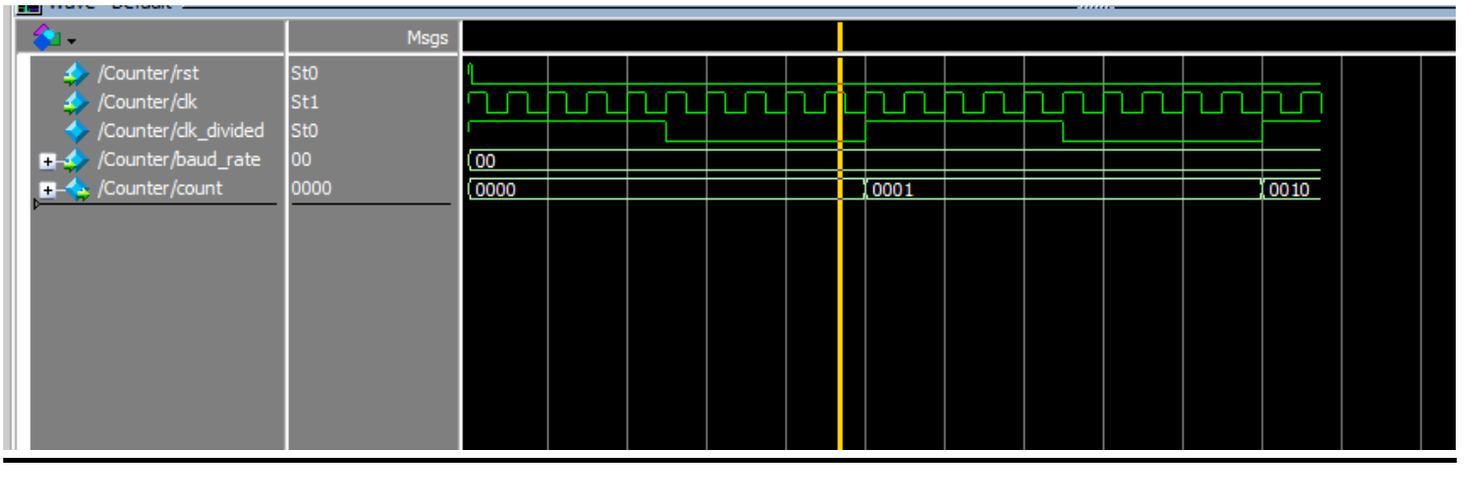
- We have 4 modules:
  1. Baud Genterator.
  2. Parity.
  3. Frame Generator.
  4. PISO [Parallel in Serial out].
- In this file we will show only how we generate the baud rate, RTL of each module, all cases of the inputs and the inputs that we used in Test-Bench.



- how we generate the baud rate:



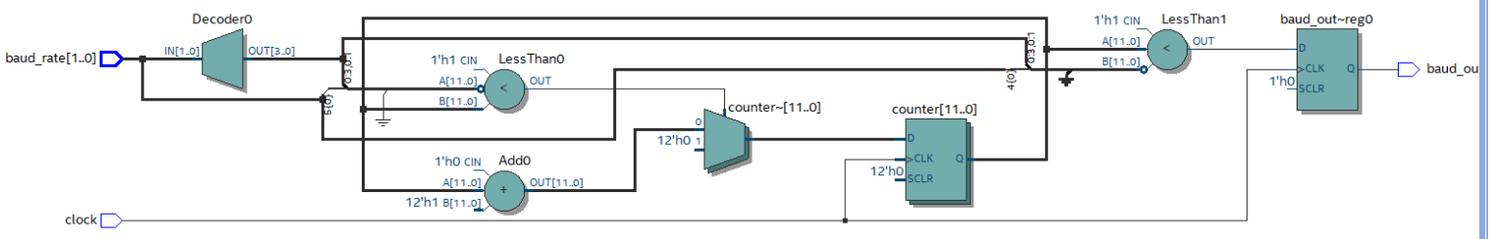
- Check baud generator for a small rate:



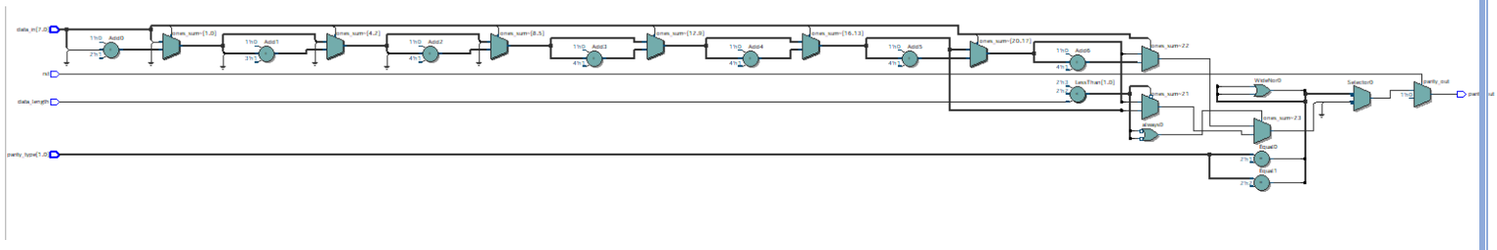
We haven't any latches in the whole modules

- The RTL of each module:

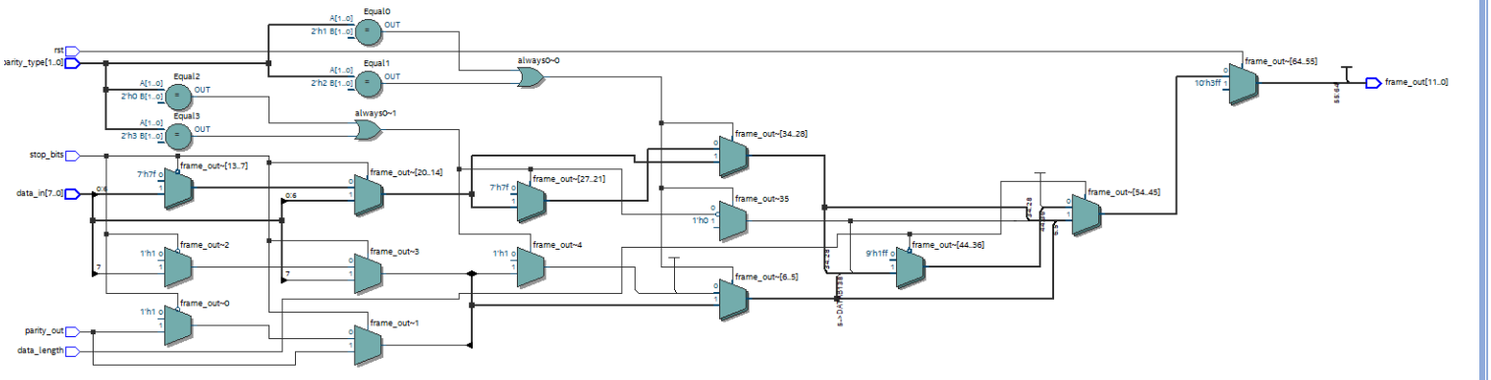
1. Baud Genterator:



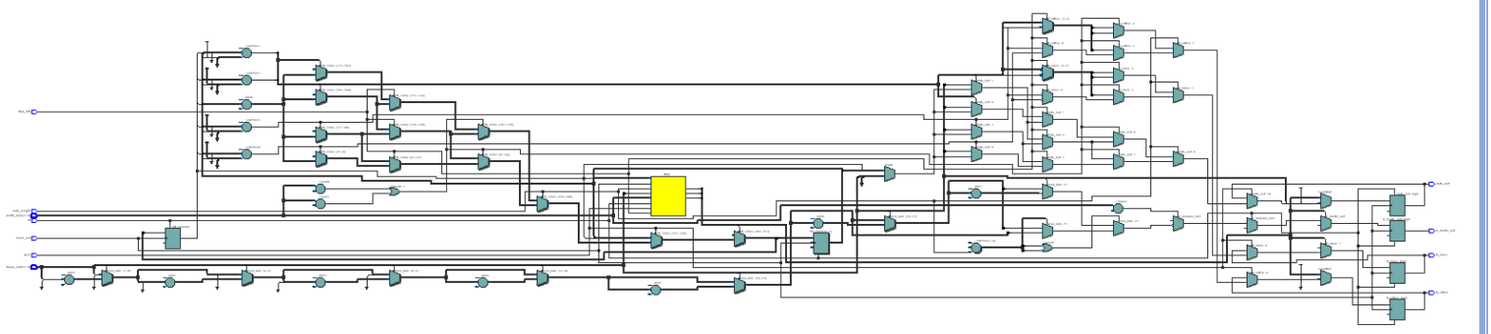
2. Parity:



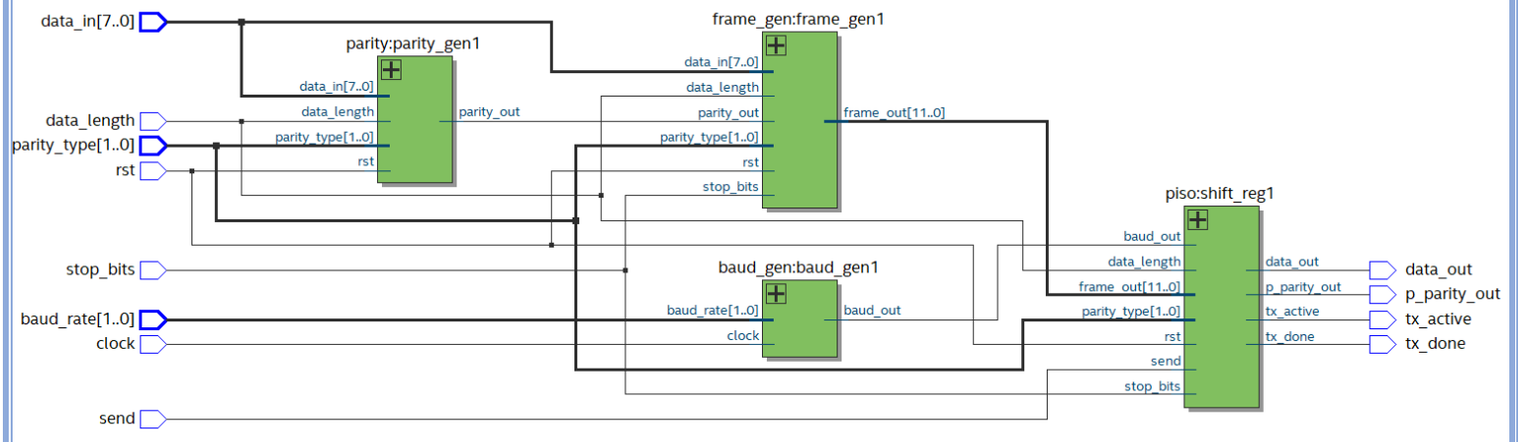
3. Frame Generator:



4. PISO [Parallel in Serial out]:



- The top module [uart_tx]:



- All cases of the inputs:

send	send	no send
	1	0

baud_rate	2400	4800	9600	19.2K
	00	01	10	11

data_length	8 bit	7 bit
	1	0

parity_type	no parity	odd parity	even parity	odd parallel
	00	01	10	11

stop_bits	2 stop bits	1 stop bit
	1	0

send	baud_rate	data_length	parity_type	stop_bits
0				
1	00	1	00	1
				0
			01	1
				0
			10	1
				0
			11	1
				0
		0	00	1
				0
			01	1
				0
			10	1
				0
			11	1
				0

send	baud_rate	data_length	parity_type	stop_bits
0				
1	01	1	00	1
				0
			01	1
				0
			10	1
				0
			11	1
				0
		0	00	1
				0
			01	1
				0
			10	1
				0
			11	1
				0

send	baud_rate	data_length	parity_type	stop_bits
0				
1	10	1	00	1
				0
			01	1
				0
			10	1
				0
			11	1
				0
		0	00	1
				0
			01	1
				0
			10	1
				0
			11	1
				0

send	baud_rate	data_length	parity_type	stop_bits
0				
1	11	1	00	1
				0
			01	1
				0
			10	1
				0
			11	1
				0
		0	00	1
				0
			01	1
				0
			10	1
				0
			11	1
				0

The cases that we will test is the marked with black only, but all cases will be covered.

- The cases that we used in Test-Bench:

	send	baud_rate	data_length	parity_type	stop_bits
1	0				
2	1	00	1	01	0
3	1	00	1	11	1
4	1	00	0	01	1
5	1	00	0	11	1
6	1	01	1	00	1
7	1	01	1	10	1
8	1	01	0	00	1
9	1	01	0	10	1
10	1	01	0	11	0
11	1	10	1	00	0
12	1	10	1	10	0
13	1	10	0	00	0
14	1	10	0	10	0
15	1	11	1	01	1
16	1	11	1	11	1
17	1	11	0	01	1
18	1	11	0	11	1

Check the Test Bench