De multiplexer

It is a combinational circuit, that performs the reverse operation of Multiplexer. It has single input, 'n' selection lines and maximum of 2^n outputs. The input will connected to one of these outputs based on the values of selection lines.

A De-mux has: (i) N control inputs
(ii) 1 data input
(iii) 2^n output

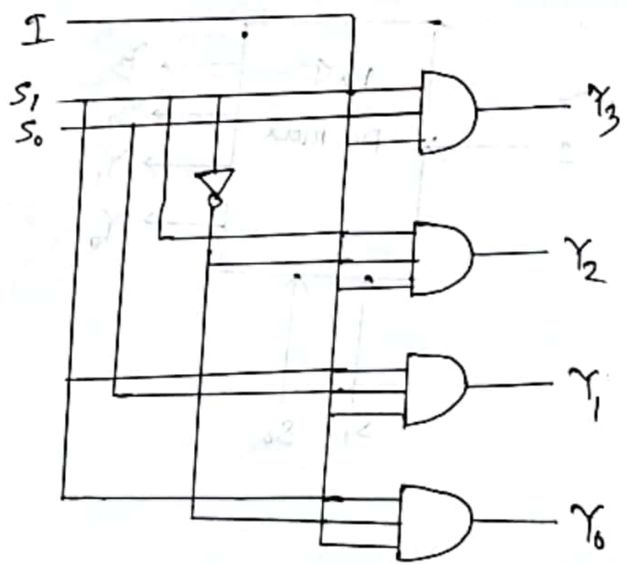
H.W

Truth table: 1x4 De-mux:

selection inputs		outputs			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

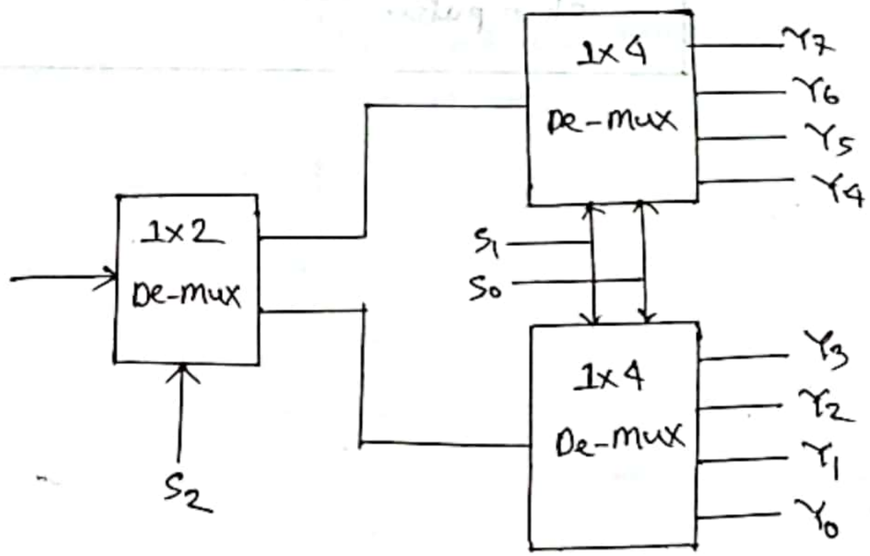
$Y_3 = S_1 S_0 I$, $Y_2 = S_1 S_0' I$

$Y_1 = S_1' S_0 I$, $Y_0 = S_1' S_0' I$



Implement 1x8 De-mux:

Input			Output							
S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0



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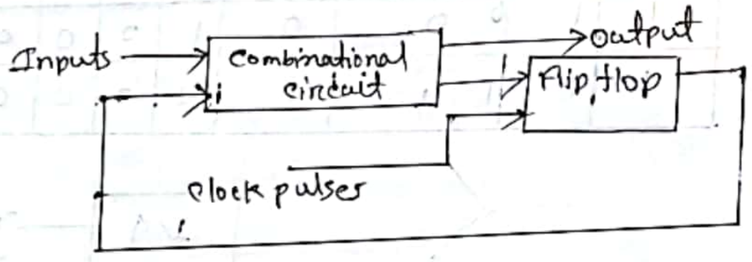
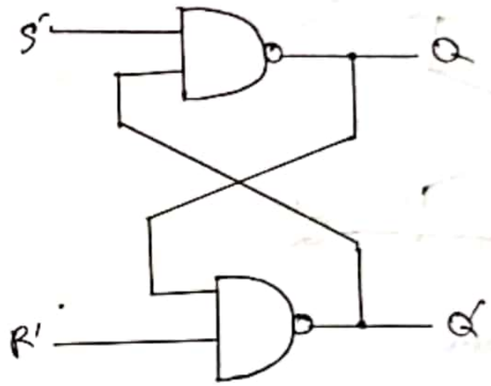
Sequential Logic

Sequential circuit



Laches

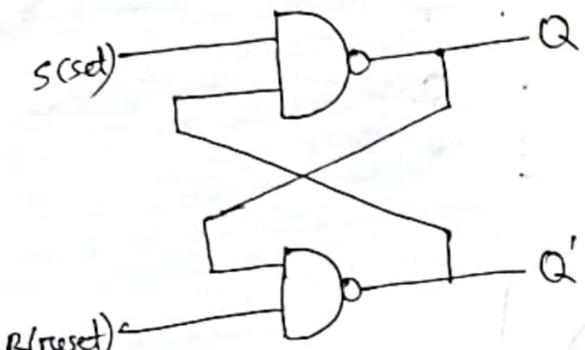


Latch using NAND Gate

There are two type of Latches

① S-R Latches
② D-Latches

S-R Latches using NAND-Gate



Logic diagram

S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

after S=1, R=0

after S=0, R=1

S-R flip-flop

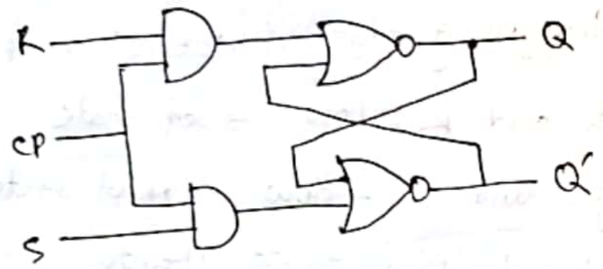
- on the triggering edge of the clock-pulse
  - S = High and R = Low → set state
  - R = High and S = slow → Reset state
  - both inputs Low → no change
  - both inputs High → Invaid

S	R	CLK	Q(t+1)	comments
0	0	x	Q(t)	No change
0	1	↑	0	Reset
1	0	↑	1	Set
1	1	↑	?	Invalid

x = Irrelevant ("don't care")

↑ = clock transition Low to High

Clocked S-R flip flop



Truth table:

clk	S	R	Qn+1
0	x	x	Qn → P.S
1	0	0	Qn → (memory)
1	0	1	0
1	1	0	1
1	1	1	Invalid

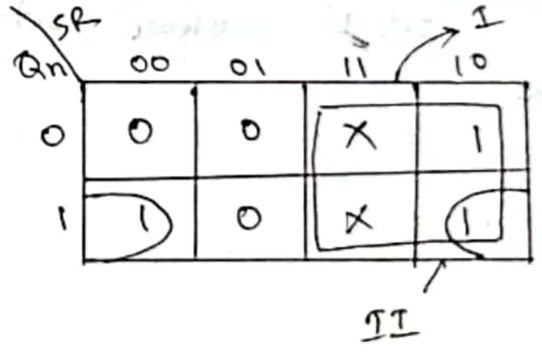
Characteristic Table

clk = 1

Qn	S	R	Qn+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	x
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	x

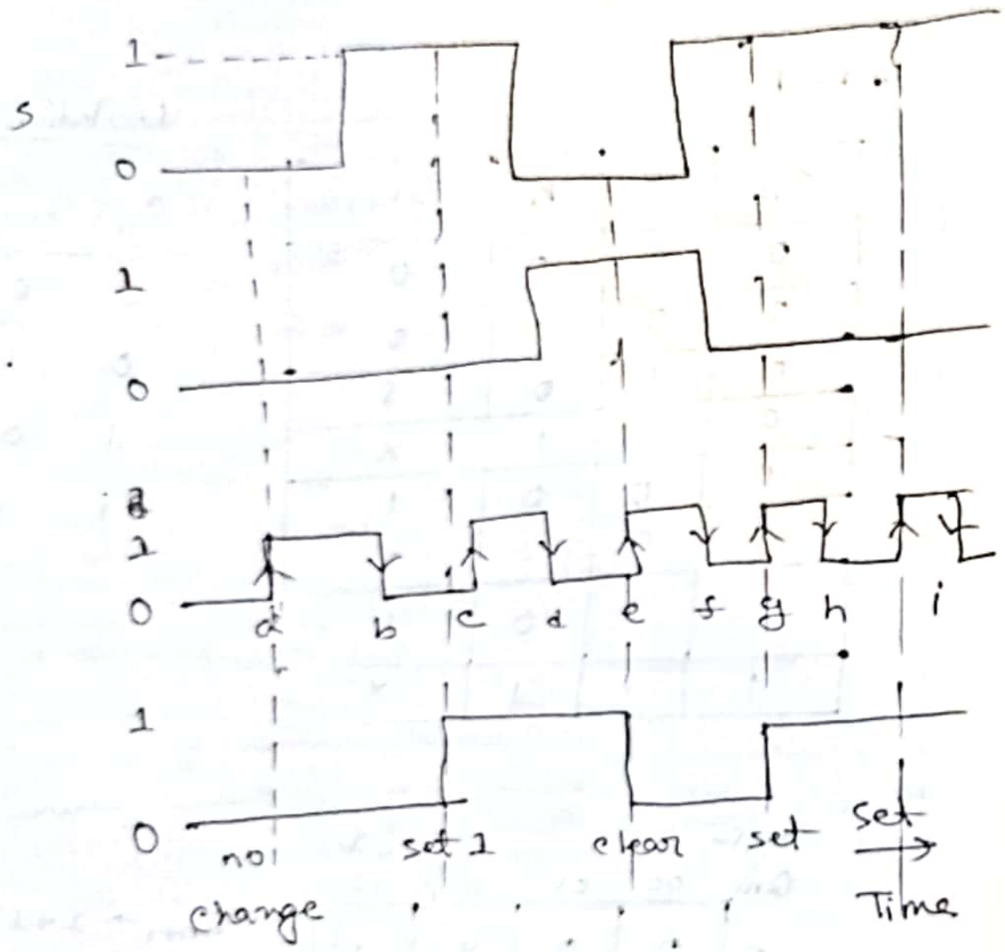
Excitation table

Qn	Qn+1	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

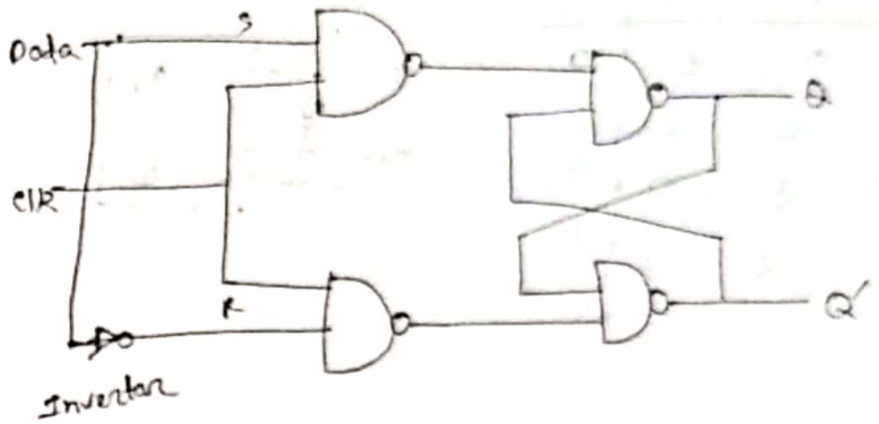


$Q_{n+1} = I + II$

$Q_n = S + Q_n\bar{R}$



D-flip-flop



Truth table

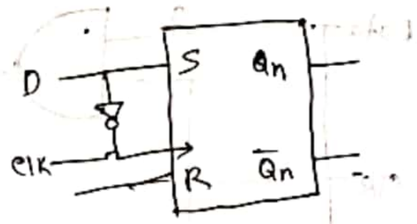
Clk	D	Qn+1
0	x	Qn
1	0	0
1	1	1

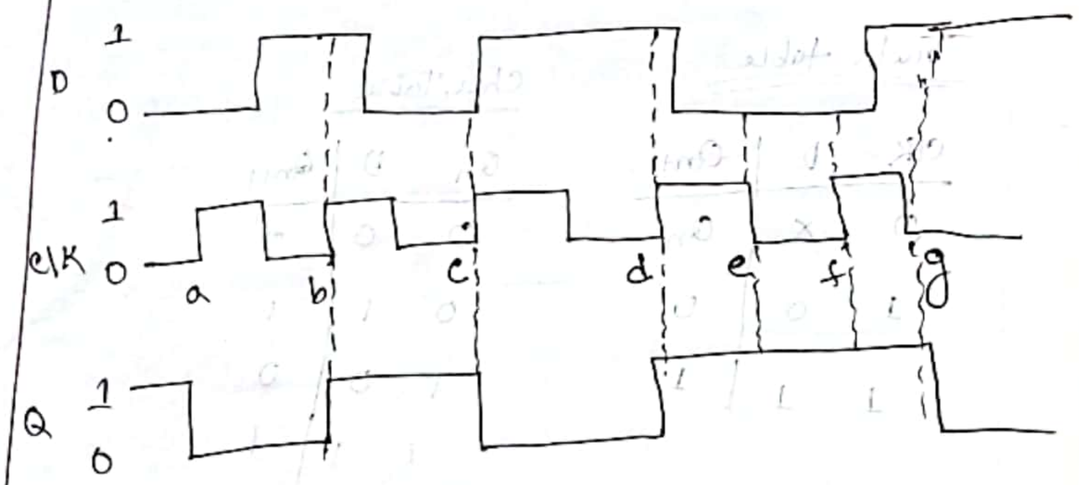
Char. Table

Qn	D	Qn+1
0	0	0
0	1	1
1	0	0
1	1	1

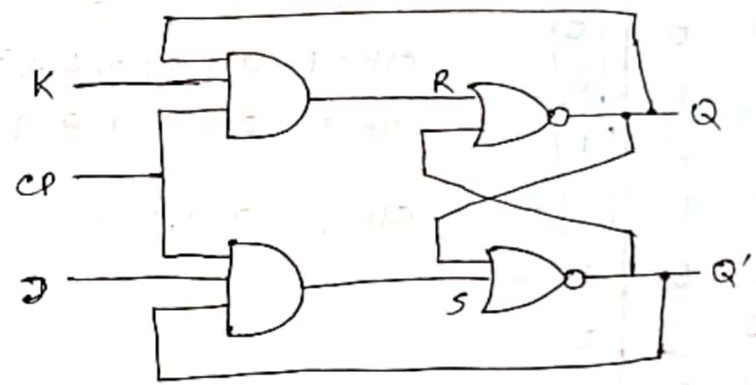
Excitation table

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1





JK flip flop



Truth table:

clk	J	K	Qn+1
0	X	X	Qn (memory)
1	0	0	Qn (memory)
1	0	1	0
1	1	0	1
1	1	1	Qn → toggle

Excitation table

Qn	Qnm	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

characteristic table

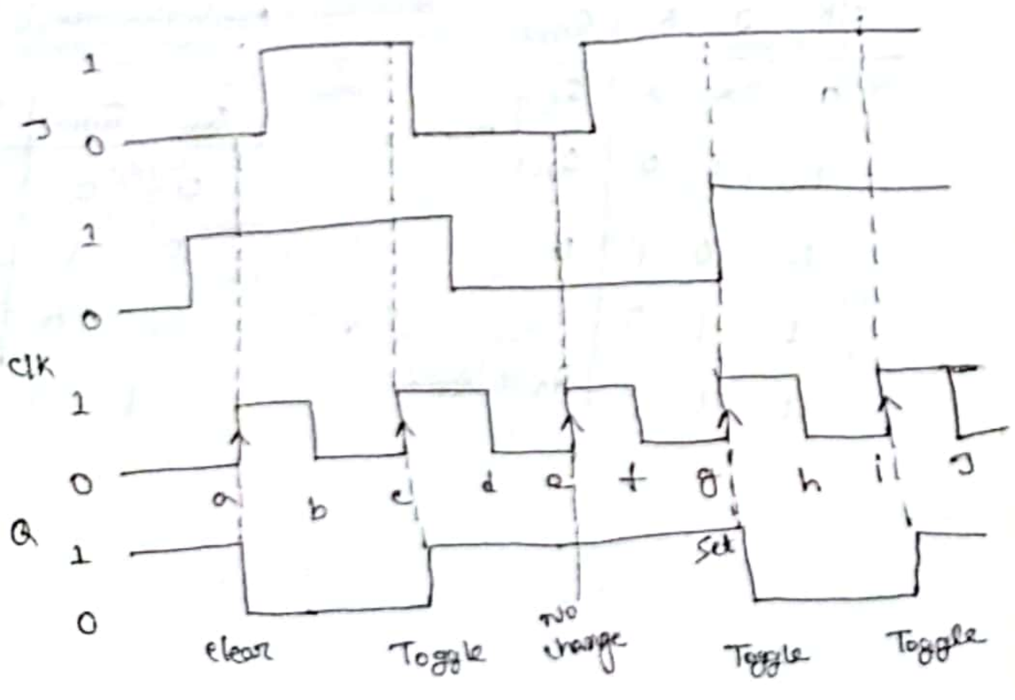
Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

* CLK = 0 memory

CLK = 1 J=1, K=0, Q=1, $\bar{Q}$=0

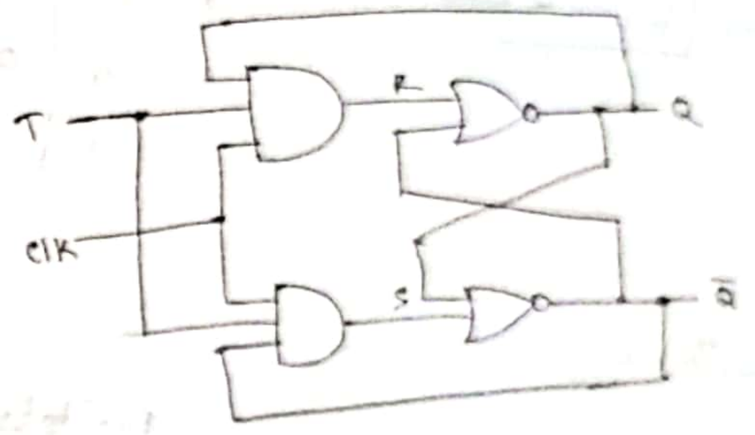
CLK = 1 J=0, K=1, Q=0, $\bar{Q}$=1

CLK = 1 J=1, K=1



T-flip flop

In T flip flop "T" defines the term "toggle"

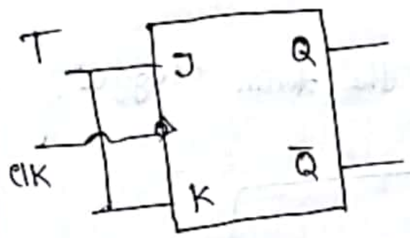


Truth table

	previous		Next	
T	Q	Q'	Q	Q'
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

toggle

T.T for T. FF



CIK	T	Qn+1	
0	X	Qn	memory
		Qn	
↑	0	Qn	
↑	1	$\bar{Q}_n$	toggle

cha. Table

Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

odd 1's detector
X-OR

Excitation table

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

Diagram: (rising edge)