Date : 02-05-23

Encoder :

A circuit that perform the inverse operation of a decoder.

It have 2^n input line and n out put lines.

if

$n = 1$

input	output
$2^n = 2^1 = 2$	1
$2^2 = 4$	2
$2^4 = 8$	4

example of 8X3 encoder :

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$$Z = D_1 + D_3 + D_5 + D_7$$

$$Y = D_2 + D_3 + D_6 + D_7$$

$$x = D_4 + D_5 + D_6 + D_7$$

Decoder:

A circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.

** The output may have fewer than 2^n.

input (n)	output (max 2^n)
2	max 4
4	max 16

example 3×8 line decoder:

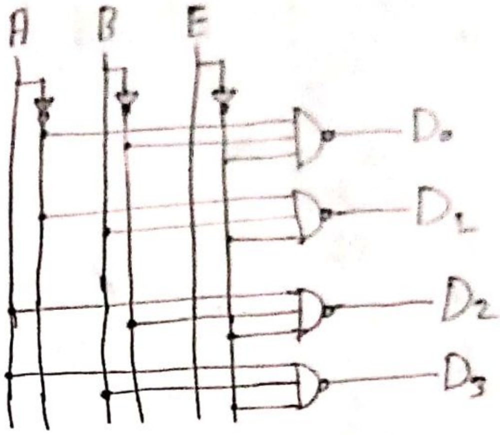
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0		1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

2×4 Line Decoder with enable:

Here E = 1 : disabled

Input			Output			
E	A	B	D_0	D_1	D_2	D_3
1	x	x	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Circuit Diagram:



Priority Encoder:

Priority encoder is a circuit, if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

$$D_3 > D_2 > D_1 > D_0$$

truth table:

Input				Output		
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1
D_0	D_1	D_2	D_3	X	Y	V

→ 0 = no valid input

$D_0D_1 \backslash D_2D_3$	00	01	11	10
00	x	1	1	1
01	0	1	1	1
11	0	1	1	1
10	0	1	1	1

$$x = D_3 + D_2$$

$D_0D_1 \backslash D_2D_3$	00	01	11	10
00	x	1	1	0
01	1	1	1	0
11	1	1	1	0
10	0	1	1	0

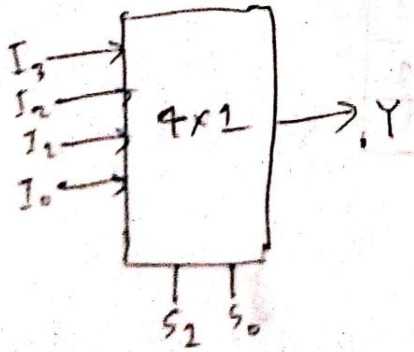
$$Y = D_3 + D_1 \cdot \overline{D_2}$$

$D_0D_1 \backslash D_2D_3$	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$$V = D_1 + D_0 + D_2 + D_3$$

Multiplexer :

* multiplexer is a combinational circuit that has maximum 2^n data inputs, 'n' selection line.
* One of these data input will connect to the output based on the value of selection line.



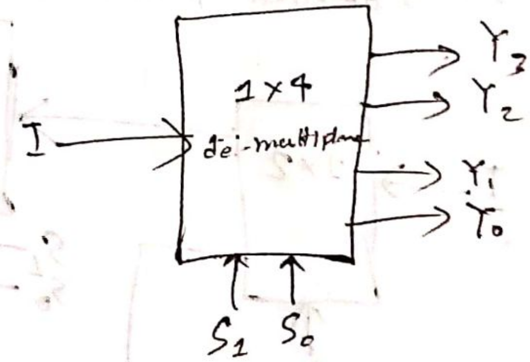
Selection lines		output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

De-Multiplexer:

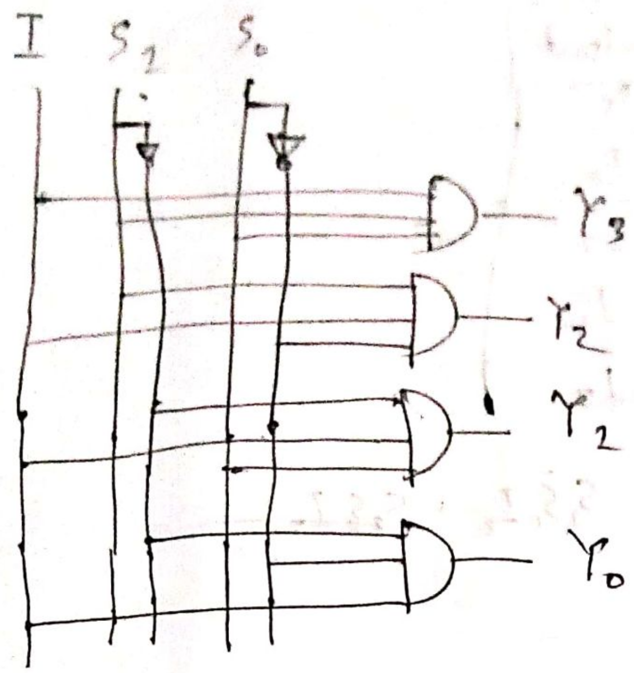
De multiplexer has

* n control inputs
* 1 data input
* 2^n Output.

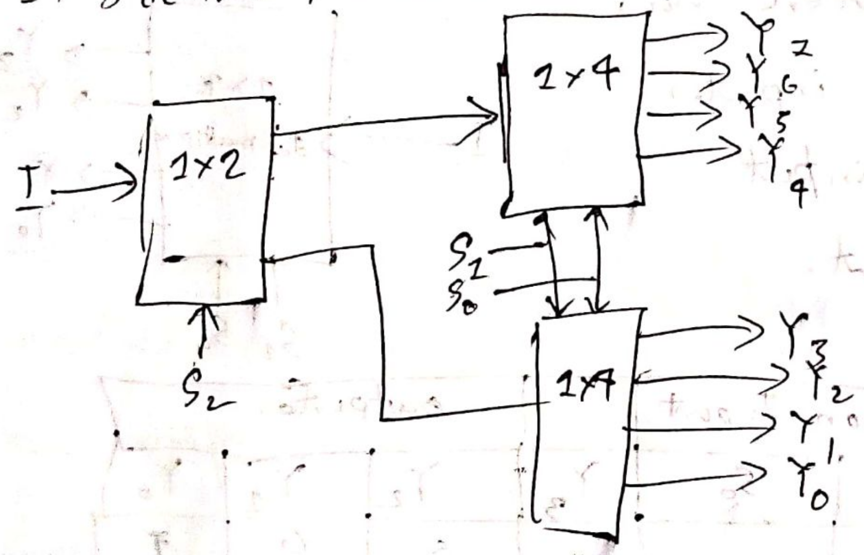


Data input	Selection Input		outputs			
I	S_1	S_0	Y_3	Y_2	Y_1	Y_0
I	0	0	0	0	0	I
I	0	1	0	0	I	0
I	1	0	0	I	0	0
I	1	1	I	0	0	0

$Y_0 = \bar{S}_1 \bar{S}_0 I$ $\quad Y_1 = \bar{S}_1 S_0 I$ $\quad Y_2 = S_1 \bar{S}_0 I$ $\quad Y_3 = S_1 S_0 I$

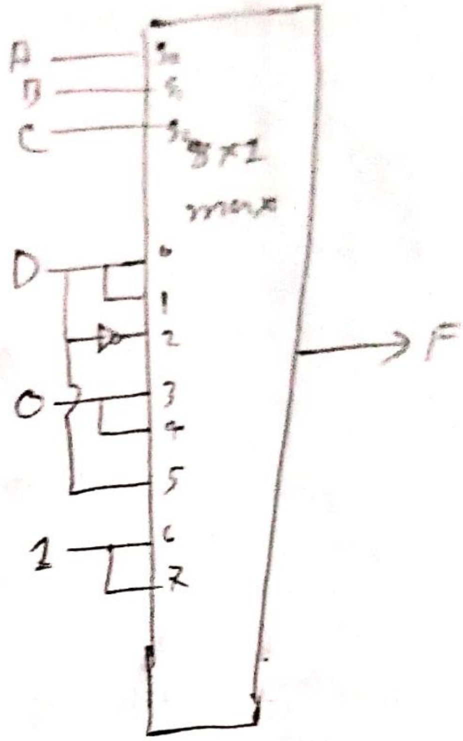


1×8 demultiplexer using 1×4 multiplexer



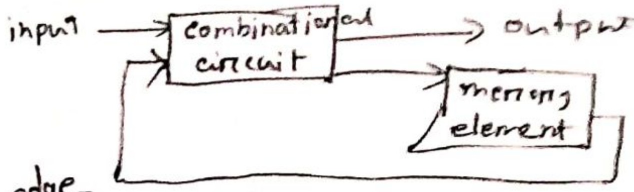
$F(A,B,C,D) = \Sigma\ 1, 3, 4, 11, 12, 13, 14, 15)$

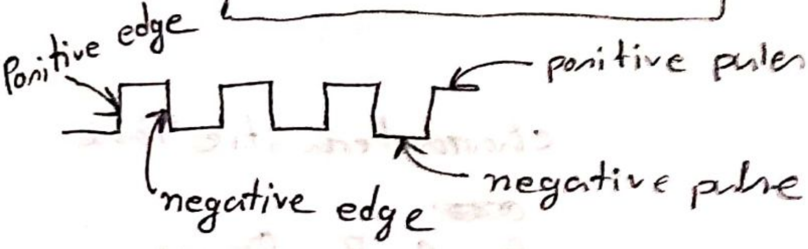
A	B	C	D	F	
0	0	0	0	0	F = D
0	0	0	1	1	
0	0	1	0	0	F = D
0	0	1	1	1	
0	1	0	0	1	F = D'
0	1	0	1	0	
0	1	1	0	0	F = 0
0	1	1	1	0	
1	0	0	0	0	F = 0
1	0	0	1	0	
1	0	1	0	0	F = D
1	0	1	1	1	
1	1	0	0	1	F = 1
1	1	0	1	1	
1	1	1	0	1	F = 1
1	1	1	1	1	



11-05-23

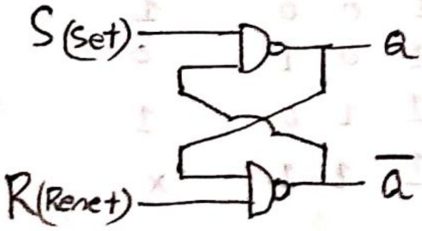
* Combinational circuit does not contain memory element.
* Sequential circuit contain memory element.





Latch:

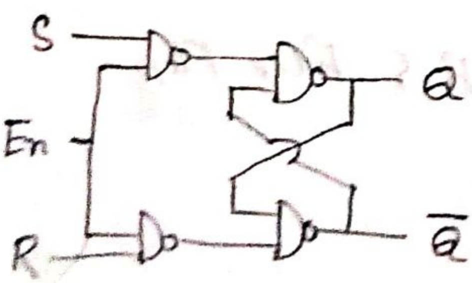
SR Latch:



Characteristic table.

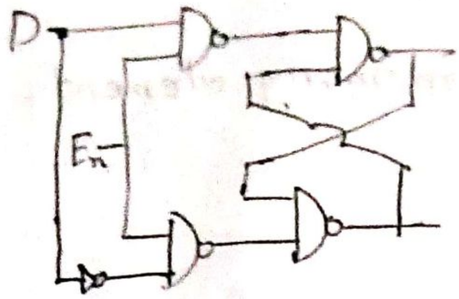
S	R	Q	$\overline{Q}$
0	0	memory	memory
1	0	1	0
0	1	0	1
1	1	Invalid	

S-R Latch with enable:



En	S	S	Q
0	x	x	no change
1	0	0	no change
1	0	1	0
1	1	0	1
1	1	1	invalid

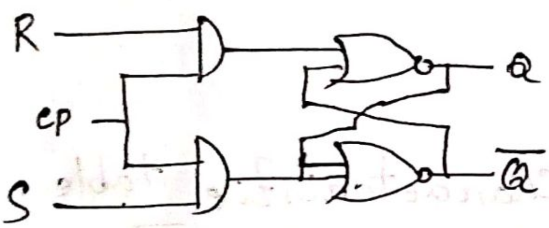
D-Latch:



En	D	Q
0	x	No change
1	0	0
1	1	1

Flip-Flop :

S-R Flip Flop



S=0 হলে output 0
S=1 " " 1

characteristic Table

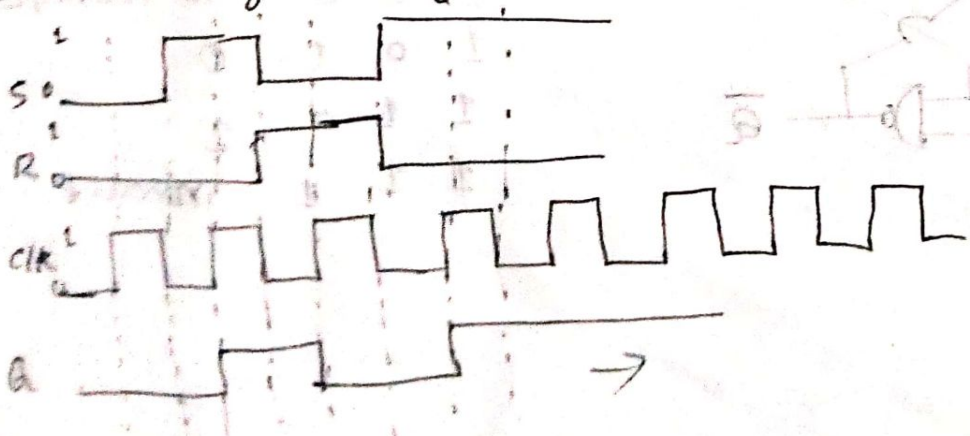
Qn	S	R	Q(n+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	x

exytation table

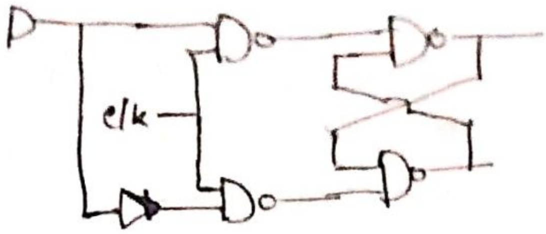
Qn	Q(n+1)	S R
0	0	0 X
0	1	1 0
1	0	0 1
1	1	X 0

16-05-23

Timing diagram of R-S Flip Flop..



D Flip Flop:



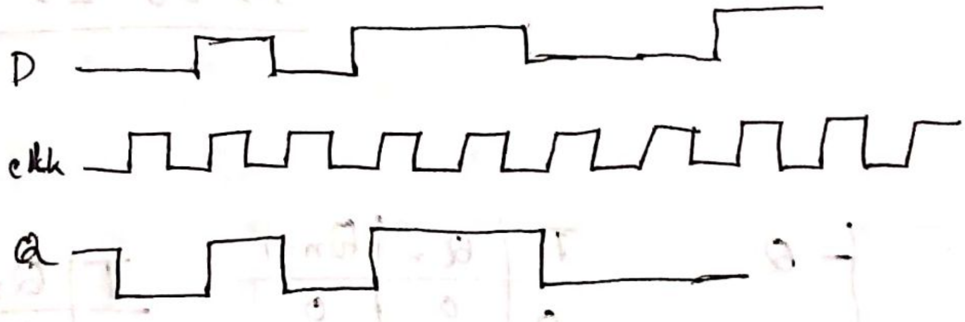
characteristic table

Q	D	$Q_{(n+1)}$
0	0	0
0	1	1
1	0	0
1	1	1

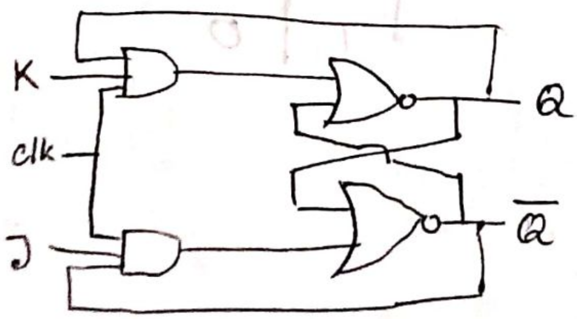
exitation table:

Q_n	$Q_{(n+1)}$	D
0	0	0
0	1	1
1	0	0
1	1	1

Timing diagram:



JK Flip Flop:



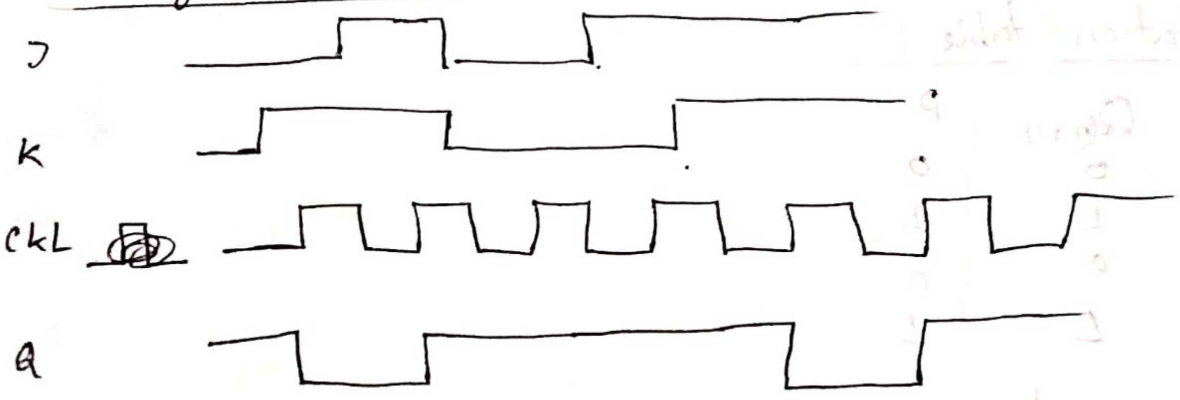
characteristic table

Q	J	K	$Q_{(n+1)}$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation table

Q	Q(n+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Timing diagram :



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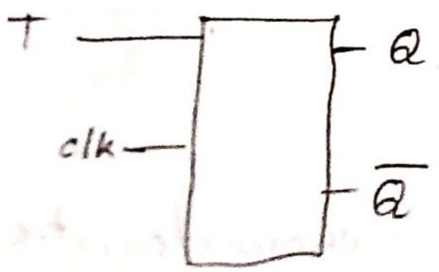
T-flip flop



T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

T	Q_{n+1}
0	Hold
1	Toggle

excitation table

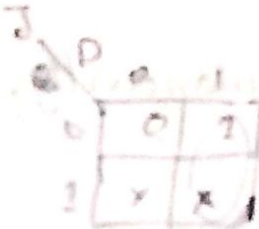
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

JK flip flop using D

Q_n	D	Q_{n+1}	J	K
0	0	0	0	x
0	1	1	1	x
1	0	0	x	1
1	1	1	x	0

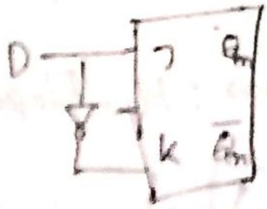
exitation table of JK

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0



$J = D$

$K = \overline{D}$

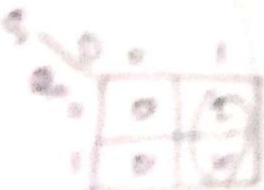


SR flip flop using D

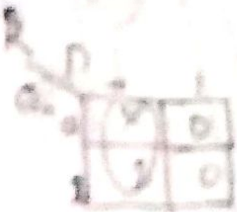
Q_n	D	Q_{n+1}	S	R
0	0	0	0	x
0	1	1	1	0
1	0	0	0	1
1	1	1	x	0

SR- exitation table

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0



$S = D$



$R = \overline{D}$

20-05-23

Counter

Counter is a sequential circuit.

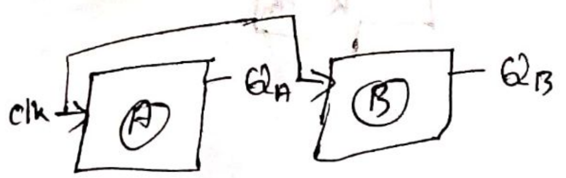
There are two types of counters

01. ASynchronous counter.

02. Synchronous counter.

ASynchronous : Flip Flops are not clocked simultaneously.

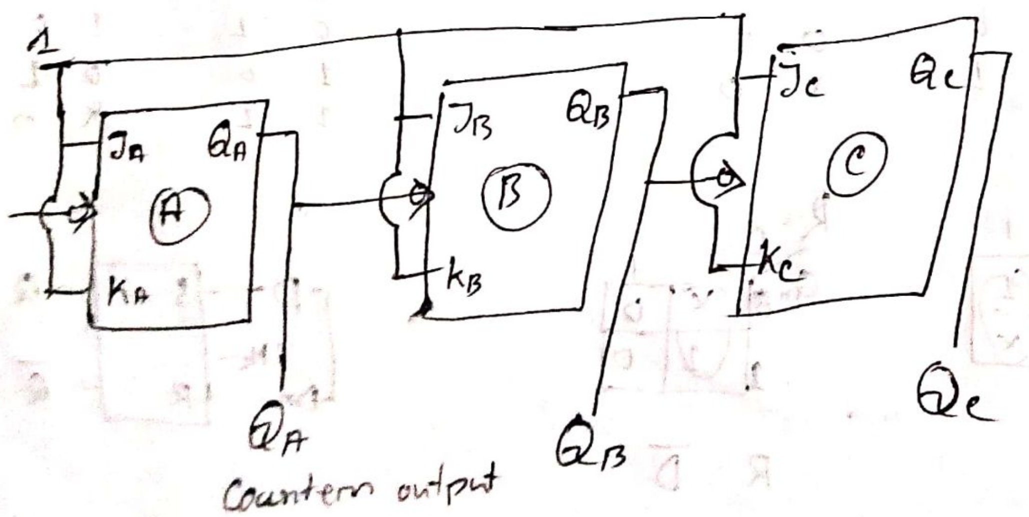
Synchronous : Flip Flops are clocked simutanously.

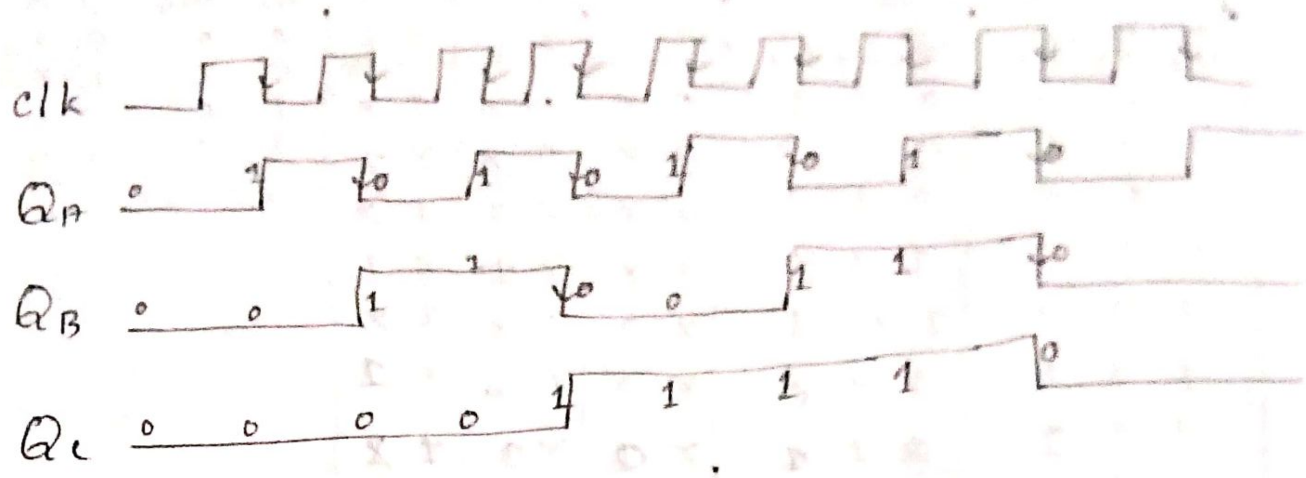


up counter : 0 → 1, → 2 → 3 ....

Down counter : 7, 6, 5, 3, ... 0

3 bit Asynchronous Up counter :





Q_C	Q_B	Q_A	Decimal value
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	0

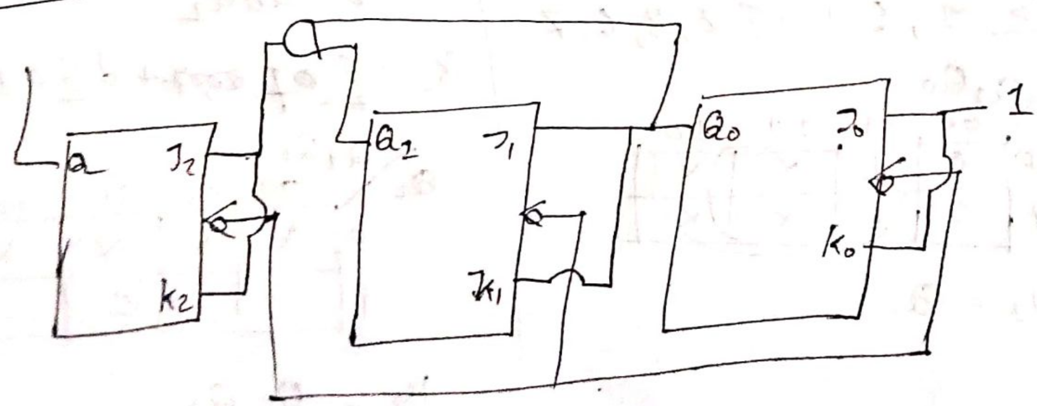
8 state

$2^n = 2^3 = 8$

$\boxed{n = \text{no of flip flop}}$

max count $= 2^n - 1 = 8 - 1$
$= 7$

3 bit Synchronous counter:



Present			next State								
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	0	0	0	x	1	x	1	x	1

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

$J_0 = \sum 0, 2, 4, 6 + d\sum 1, 3, 5, 7$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	1	x	x	1
1	1	x	x	1

$J_0 = 1$

$K_0 = \sum 1, 3, 5, 7 + d\sum 0, 2, 4, 6$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	x	1	1	x
1	x	1	1	x

$K_0 = 1$

$J_1 = \sum 1, 5 + d\sum 2, 3, 6, 7$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	1	x	x
1	0	1	x	x

$J_1 = Q_0$

$K_1 = \sum 3, 7 + d\sum 0, 1, 4, 5$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	x	x	1	
1	x	x	1	

$K_1 = Q_0$

$J_2 = \sum 3 + d\sum 4, 5, 6, 7$

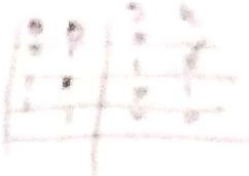
$Q_2 \backslash Q_1Q_0$	00	01	11	10
0			1	
1	x	x	x	x

$J_2 = Q_0Q_1$

$K_2 = \sum \cancel{0} 7 + d\sum 0, 1, 2, 3$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	x	x	x	x
1			1	

$K_2 = Q_0 Q_1$



HW

0, 1, 4, 5, 6, 7

Q_2	Q_1	Q_0				J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	1	0	0	1	x	0	x	x	1
0	1	0	x	x	x	x	x	x	x	x	x
0	1	1	x	x	x	x	x	x	x	x	x
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	0	0	0	x	1	x	1	x	1

H.W 01-06-23

(7) Difference between Synchronous counter & Asynchronous counter

Synchronous counter :

1. There is no connection between output of first flipflop and clock of next flip flop.
2. Flip Flops are clocked simultaneously.
3. Circuit becomes complicated as number of state increases.
4. Speed is high as clock is given at a same time.

Asynchronous counter:

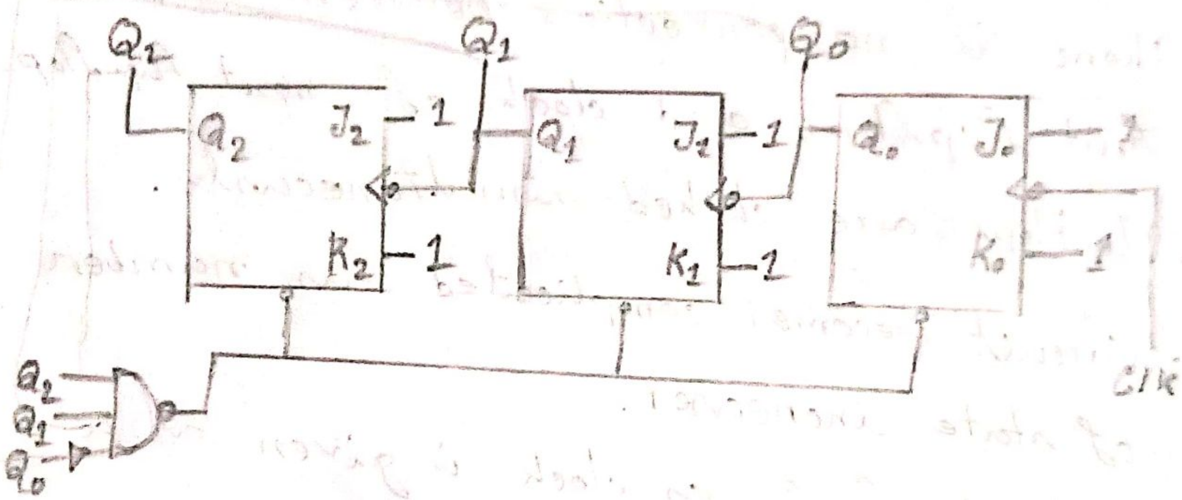
1. Flip Flop are connected in such a way that output first flip flop drives the clock of next flip flop.
2. Flip Flops are not clocked simultanously.
3. Circuit is simple for more number of states.
4. Speed is slow as the clock is propagated through number of stages.

Determine MOD 6 Asynchronous down counter.

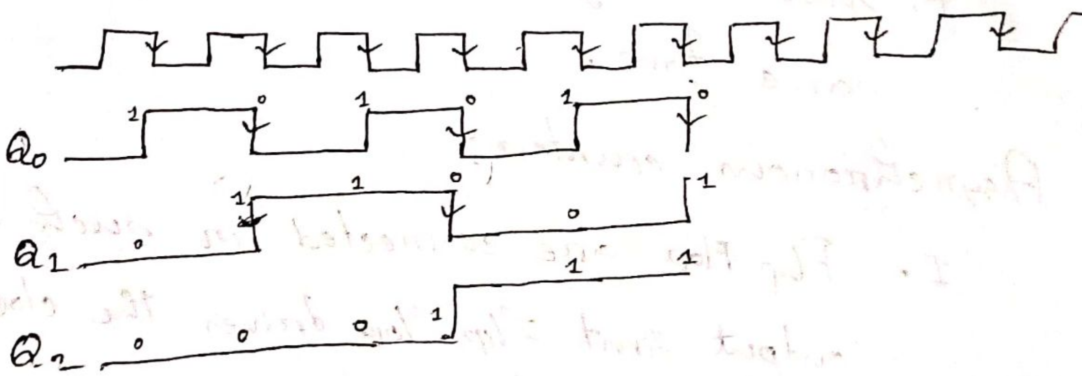
$2^n = m$

$\Rightarrow 2^2 = 4 \quad \Rightarrow 2^3 = 8$

we will need 3 Flip Flop



Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
~~0~~	~~1~~	~~0~~
1	1	0
0	0	0

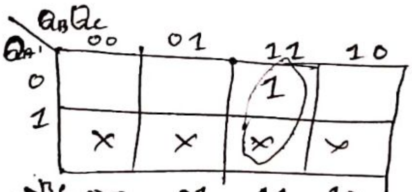


Determine MOD 6 Counter Synchronous.

Present State			Next state								
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

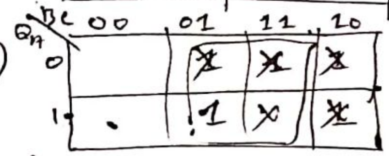
$J_A = \sum m(3) + d(4,5,6,7)$

$J_A = Q_B Q_C$



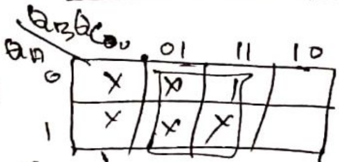
$K_A = \sum m(5) + d(1,2,3,\cancel{6},7)$

$K_A = Q_C$



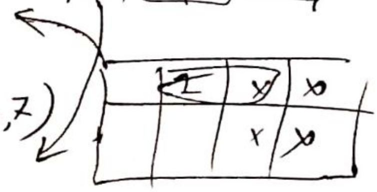
$J_B = \sum m(1) + d(2,3,6,7)$

$J_B = \overline{Q_A}\, Q_C$



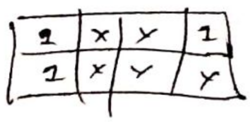
$K_B = \sum m(3) + d(0,1,4,5,6,7)$

$K_B = Q_C$



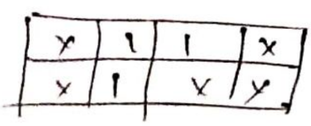
$J_C = \sum m(0,2,4) + d(1,3,5,6,7)$

$J_C = 1$



$K_C = \sum m(1,3,5) + d(0,2,4,6$

$K_C = 1$



characteristic table
JK·FF

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

06-06-23

ROM

Rom size $2^n \times m$

n = input

m = output

$1K = 2^{10}$ bytes

$1M = 2^{20}$

$1G = 2^{30}$

$1T = 2^{40}$

2 M word

= ~~[illegible]~~

$= 2 \times 2^{20}$

= 21

PROM / PAL / PLA

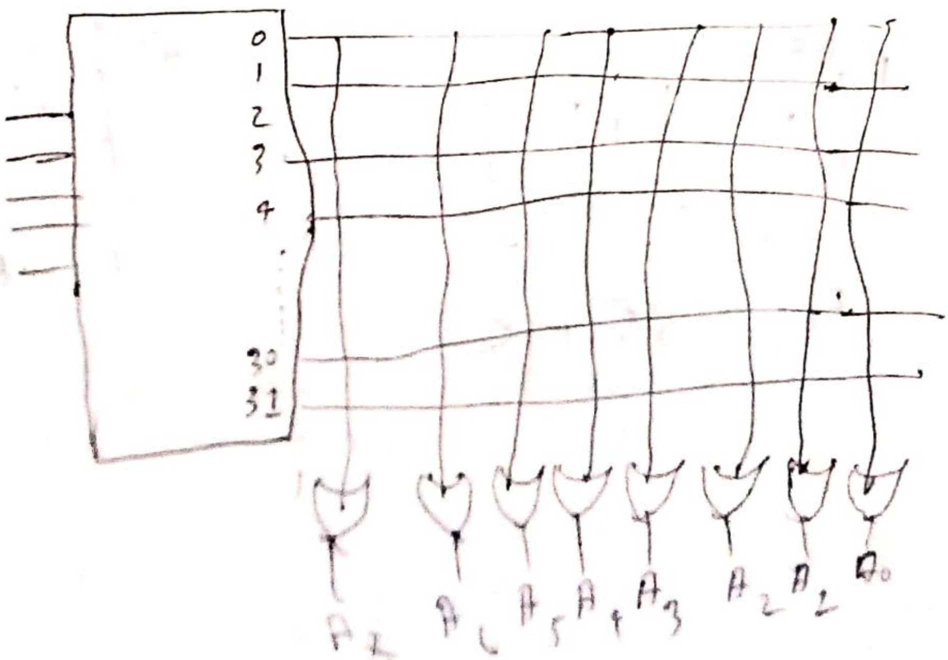
32 × 8 ROM

32 × 8

$= 2^5 \times 8$

5 input

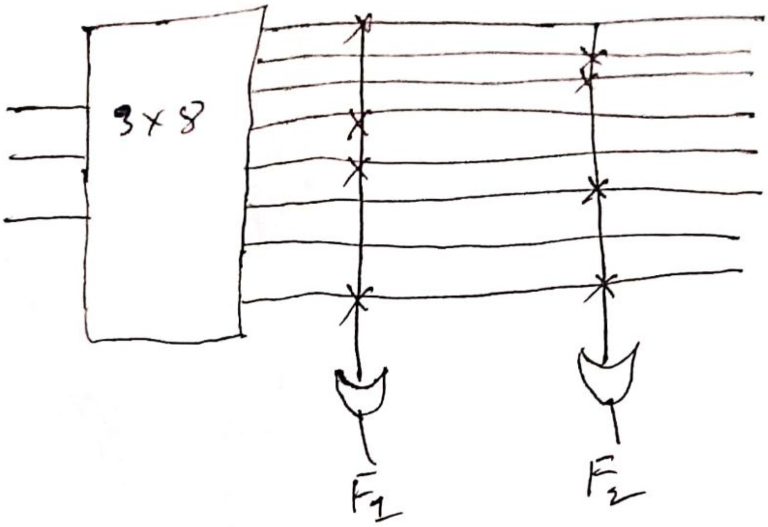
8 output



$F_1 = \sum(0, 3, 4, 7)$

$F_2 = \sum m(1, 2, 5, 7)$

ROM



PLA

$F_1 = \sum m(0, 3, 4, 7)$

A\BC

1	0	1	0
1	0	1	0

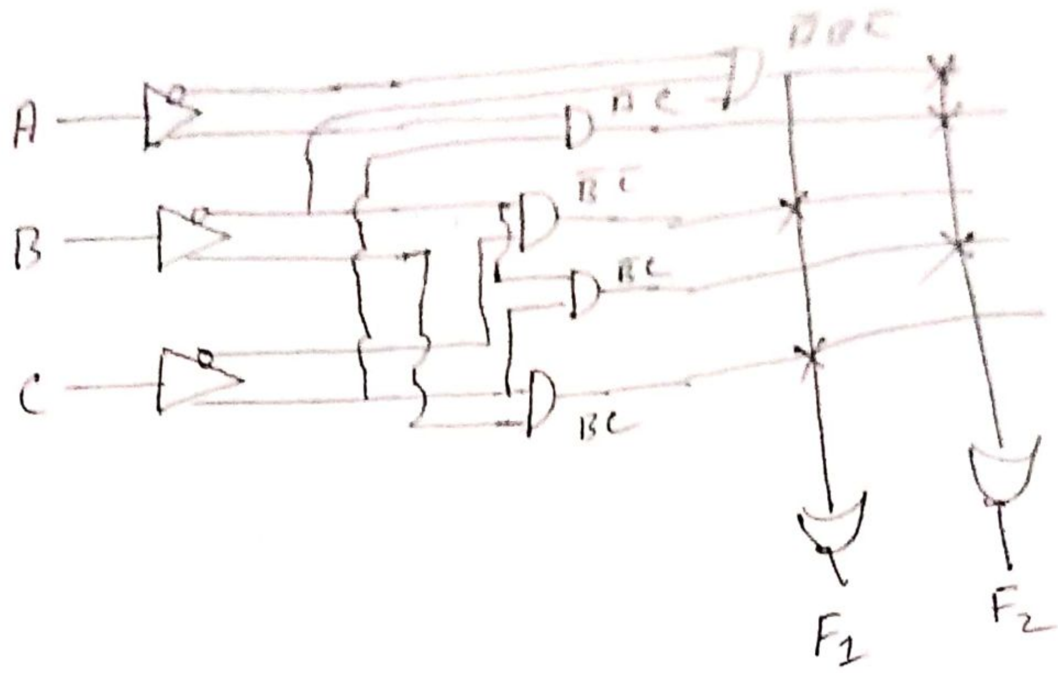
$F_1 = \bar{B}\bar{C} + BC$

$F_2 = \sum m(1, 2, 5, 7)$

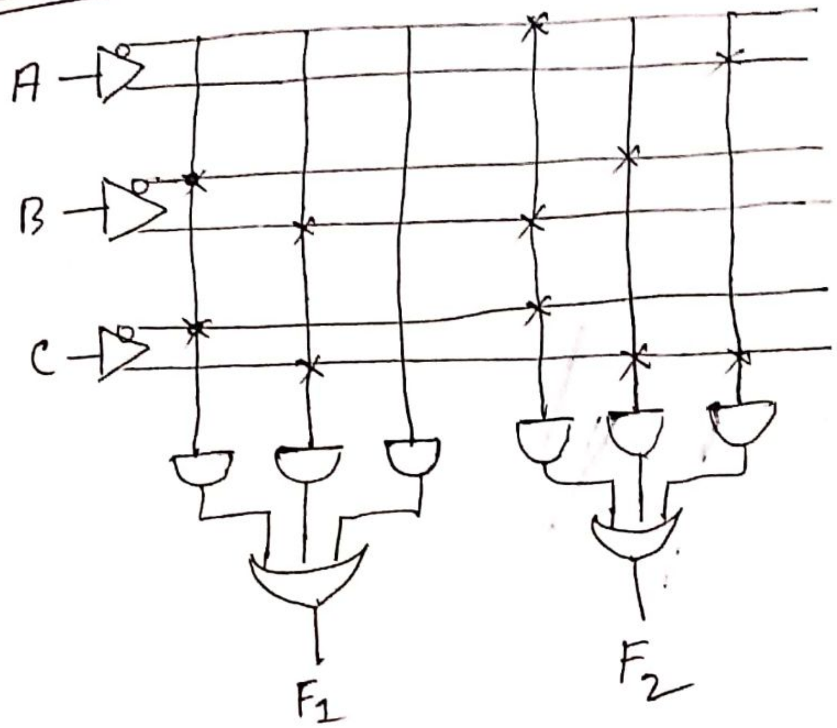
A\BC

0	1	0	1
0	1	1	0

$F_2 = \bar{A}\bar{B}C + AC + \bar{A}B\bar{C}$



PAL



A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

$A > B = A\overline{B}$

$A < B = B\overline{A}$

$A = B = \overline{A}\,\overline{B} + AB$