RISC-V Processor

Milestone 02: Single Cycle Implementation

Computer Architecture

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* **Project Description**
* **Supported Instructions**

Developed and Tested Instructions:

R-Type: ADD, SUB, SLL, SLT, SLTU, XOR, SRL, SRA, OR, AND

I-Type: LW, ADDI, SLTI, SLTIU, XORI, ORI, SLLI, SRLI, SRAI

U-Type: LUI, AUIPC

J-Type: JAL

B-Type: BEQ

S-Type: SW

Developed But yet to Be Tested:

B-Type: BNE, BLT, BGE, BLTU, BGEU

Yet to Be Developed:

I-Type: LB, LH, LBU,LHU

S-Type: SB, SH

ECALL, EBREAK

* **Implemented Datapath** A diagram of a machine

  Description automatically generated
* **Simulations**

A screenshot of a computer screen

Description automatically generated

A screenshot of a computer

Description automatically generated