

A Millimeter-Wave Concurrent LNA in 22-nm CMOS FDSOI for 5G Applications

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Abstract—This article presents a concurrent dual-band low-noise amplifier (LNA) in a 22-nm fully-depleted silicon-on-insulator (FDSOI) CMOS process. This three-stage cascode LNA is designed to operate concurrently between 23.3 and 30.3 GHz and 38 and 44.7 GHz (K -/ Ka -band) for 5G mm-wave bands. To achieve a high rejection in the stopband between the two passbands, a notch circuit is designed using a cross-coupled pair (XCP) to mitigate the limited inductor/capacitor quality factors, thus enhancing notch depth in the second stage. The gain of the LNA can be digitally controlled in the third stage by over eight steps of 1 dB. The input matching network also acts like a high-pass filter to generate a sufficient rejection for frequencies below 13 GHz. The measured gain is 22 dB at 24 GHz and 16 dB at 40.5 GHz, with a 3-dB bandwidth of 23.3–30.3 GHz for low passband and 38–44.7 GHz for high passband. The LNA achieves a noise figure (NF) of 2.55/4.75 dB at 28/40 GHz, a rejection of 19.2 dB at 34.1 GHz, and a power consumption of 18 mW with supply voltages of 0.8 V for the first stage, and 1.0 V for the rest. The chip has a length of 1035 μm , a width of 885 μm , and an area of 0.916 mm^2 including all pads and decoupling capacitors.

Index Terms—5G, concurrent dual-band, fully-depleted silicon-on-insulator (FDSOI) CMOS, low-noise amplifier (LNA), mm-wave, notch, wideband.

I. INTRODUCTION

5G WIRELESS communications have been a popular area of research in recent years both in industry and academia. FCC allocates frequency bands from 24.25 to 28.35 and 37.6 to 42.5 GHz for mm-wave mobile communications covering a wide frequency range [1]. For traditional communication systems, multiple independent modules are needed to achieve concurrent functionality. This would significantly increase system area, power consumption, and cost, especially for mass-produced mobile units. For mm-wave applications, phase arrays are often necessary. This further increases the number of independent modules needed.

To cover both 5G mm-wave bands, there are three different possible low-noise amplifier (LNA) topologies: wideband, switching, and concurrent LNAs. Numerous wideband LNAs

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have been published recently to address this issue at mm-wave frequencies [2], [3], [4], [5], [6], [7]. Some of them cover bands even wider than the 5G mm-wave range. This makes utilizing a single LNA for the whole band possible. However, between the aforementioned 5G bands, and below 20 GHz as well, there are bands allocated for other applications such as satellite communication, radio location, and so on [8], which can degrade the sensitivity and linearity of the desired 5G bands. Thus, the stopband performance also needs to be addressed properly. Some switching-type LNAs with some rejections were presented in [9], [10], and [11]. The switching LNA can achieve sufficient rejections, but its main drawback is that it cannot work concurrently. Carrier aggregation techniques have been commercially implemented in sub-6-GHz 5G system [12] and are potentially going to be implemented in mm-wave 5G systems to improve download and upload speed in the future. For the interband carrier aggregation, wideband/concurrent functionalities are needed. Thus, the concurrent LNA has the advantage over both switching and wideband LNAs.

Several published concurrent LNAs targeted the mm-wave frequency range. A synthetic quasi-TEM transmission line based on-chip solution was introduced in [14]. It provided a large rejection of 44 dB with a narrowband response at lower frequencies and a wider passband separation between lower and upper passbands. A triple-band feedback notch-based BJT-type LNA was presented in the SiGe BiCMOS process with a power supply of 1.8 V [15]. It utilized a feedback notch in resonator load to enhance the stopband rejection to 30/41 dB, while the bandwidth of each passband was not very wide, especially a 3.4-GHz 3-dB bandwidth for the central passband. A revised dual-band version was introduced with a 37-dB rejection by an increased power supply of 2.5 V [16]. However, its input matching was not enough. A dual-band concurrent LNA was presented in a beamforming receiver directly targeting 5G bands [17], while each covered passband was not wide enough with a bandwidth of 2.75 and 3.75 GHz, respectively.

In this article, a concurrent mm-wave LNA is presented based on a cross-coupled-pair (XCP) for Q-enhancement of a passive LC notch at mm-wave frequencies with power supplies of 0.8 and 1.0 V in 22-nm fully-depleted silicon on insulator (FDSOI) CMOS process. This XCP Q-enhancement solution overcomes the issue of limited quality factors of passive inductors and capacitors to achieve sufficient stopband rejection at mm-wave frequency. This three-stage cascode

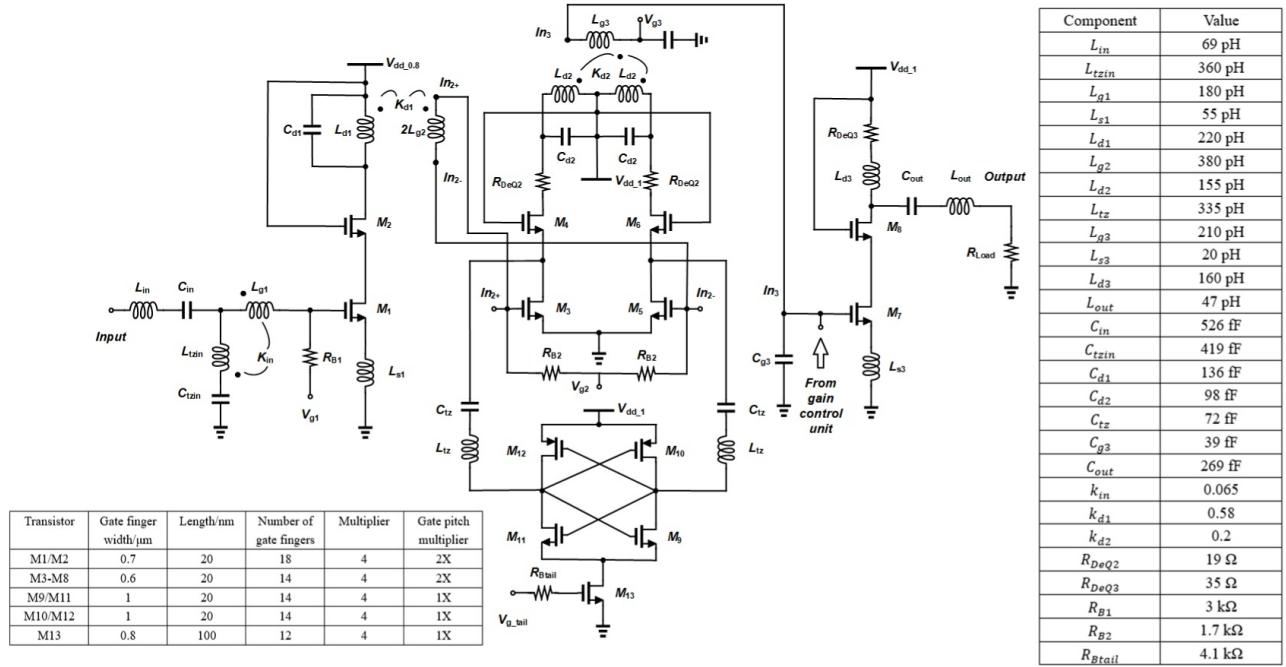


Fig. 1. Schematic of the concurrent LNA.

LNA operates as a wideband LNA between 23.3 and 30.3 GHz and 38 and 44.7 GHz (K -/ Ka -band) simultaneously for 5G mm-wave bands, while achieving a stopband rejection of 19.2 dB at 34.1 GHz.

II. LNA DESIGN

Fig. 1 shows the schematic of the proposed concurrent LNA. It is based on a three-stage cascode design for better gain and reverse isolation. The first stage is a single-ended (SE) cascode structure including M1 and M2 designed to minimize the noise figure (NF). The input matching network utilizes inductive source degeneration and coupled inductors for wideband matching. The interstage matching between the first and second stages includes baluns for SE to differential conversion. The second gain stage is differential to allow for XCP realization of M9–M12 and boosts the quality factor of the in-band series notch generated by L_{tz} and C_{tz} . The XCP is placed between the input and the cascode transistor. Tradeoffs have been made to place the notch in the second stage instead of in the first stage. This implementation allows reducing its effect on deteriorating the overall NF, and the wideband input matching which is already very challenging to achieve. The interstage matching between the second and third stages also acts as a balun since the third stage is also designed to be SE. The SE input/output design is for convenience of measurement. The gain of the third stage is varied in a digital fashion with a 3-bit DAC to achieve eight different gain steps and a 7-dB gain difference. De-Q resistors are implemented in second- and third-stage loads (R_{DeQ2} , R_{DeQ3}) for achieving a wideband frequency response, output matching, and help with the stability. The supply voltages are 0.8, 1.0, and 1.0 V, respectively, for each stage. The supply voltage of the second and third stages is slightly increased to improve linearity.

V_{g1} , V_{g2} , V_{g3} , and V_{gtail} are externally applied with a value of 0.4, 0.27, 0.35, and 0.2 V, respectively. The dc biasing current of the first, second, and third stages are 9, 2.5, and 5 mA, and all the gain stages are biased in class-A.

A. Signal Analysis

The simplified small-signal ac equivalent circuit is shown in Fig. 2. Some simplifications and approximations have been made to make the analysis more straightforward, ignoring the body effect of the cascode transistor, C_{gd} , and r_0 . The detailed performance of the notch will be analyzed in Section II-C.

The gain of the first-stage A_{v1} can be written as

$$A_{v1} = \frac{V_{gs1}}{V_{in}} \frac{V_{g2}}{V_{gs1}} \approx \frac{1}{2} \frac{G_{m1} Z_{d21}}{sL_{tzin} + \frac{1}{sC_{tzin}} + R_{ptzin}} \quad (1)$$

where $V_{g2} = 2V_{gs3}$ or $2V_{gs5}$. Z_{d21} is the transimpedance between the first-stage transformer-coupled resonator passive load and the second-stage input and can be calculated by (1)–(5) in [18]. In the bands of interests, assuming the input of the LNA is matched to $R_s = 50 \Omega$ and Z_{in} is approximately 50Ω . So, V_{in} is equally divided between R_s and Z_{in} . G_{m1} is the equivalent transconductance of the first stage. At the input matching network, the inductance L_{tzin} and capacitance C_{tzin} forms a series LC network resonance to generate a transmission zero at $f_{tzin} = (1/(2\pi(L_{tzin}C_{tzin})^{1/2}))$, which was chosen around 12 GHz. The poles of the first stage load Z_{d21} are located at $f_{p1} = 24$ GHz and $f_{p2} = 63$ GHz, respectively. The coupling factor k_{d1} is chosen as 0.58. The location of the second pole is due to limitations and tradeoffs, such as the self-resonant frequency of the inductor, the quality factor of the inductor, and especially the allowed maximum inductance value for an acceptable quality factor in this process.

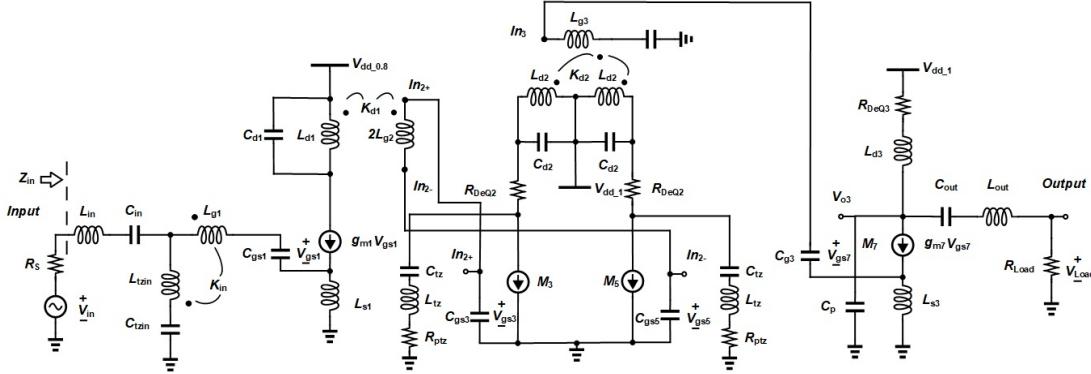


Fig. 2. Simplified small-signal ac equivalent circuit.

The gain of the second stage, A_{v2} , is calculated as follows:

$$A_{v2} = \frac{V_{gs7}}{V_{g2nd}} = \frac{g_{m3} Z_{d43}}{sL_{tz} + \frac{1}{sC_{tz}} + R_{ptz}} \quad (2)$$

where Z_{d43} is the transimpedance between the second-stage transformer-coupled resonator passive load and the third-stage input, which can be calculated by (1)–(5) in [18]. At the second stage between input (M3, M5) and cascode (M4, M6) transistors, the inductance L_{tz} and capacitance C_{tz} form a series LC network resonance to generate a transmission zero at $f_{tz} = (1/(2\pi(L_{tz}C_{tz})^{1/2}))$ which was chosen around 33 GHz. The effect of XCP is considered in this simplified analysis with the inclusion of R_{ptz} . For L_{d2} , the effect of De-Q resistor R_{DeQ2} is included in the quality factor. The location of the poles of Z_{d43} are at $f_{p3} = 30$ GHz and $f_{p4} = 39$ GHz, respectively.

The gain of the third stage, A_{v3} , is calculated as follows:

$$A_{v3} = \frac{V_{o3}}{V_{gs7}} \frac{V_{Load}}{V_{o3}} = G_{m7} Z_{d3} A_{vout} \quad (3)$$

where Z_{d3} is the impedance of the third-stage passive load and A_{vout} defines the ratio between the voltage of the third-stage output node and voltage delivered to $R_L = 50 \Omega$. G_{m7} is the equivalent transconductance of the third-stage input transistor M7. C_p is the parasitic capacitance of output node of M8.

Then the total voltage gain of the LNA $A_{v,LNA}$ can be found using (4). The gain of each stage and the total system gain are shown in Fig. 3. They are based on the previously mentioned equations in this section. The result matches the trend in the simulation and the measurement as will be shown later

$$A_{v,LNA} = \frac{V_o}{V_{in}} = A_{v1} A_{v2} A_{v3}. \quad (4)$$

B. Input Matching Circuit

The equivalent circuit of the input matching network is shown in Fig. 4(b). The input matching network consists of the pad capacitance C_{pad} , inductors L_{in} , L_{g1} , and L_{tzin} , capacitors C_{tzin} , C_{in} , and C_{gs1} , and $R_{eq} = ((g_{m1}L_{s1})/C_{gs1})$. L_{g1} and L_{tzin} are coupled with a coupling factor of $k_{in} = 0.15$, or the mutual inductance is $M_{in} = k_{in}(L_{g1}L_{tzin})^{1/2}$. As mentioned before, L_{tzin} and C_{tzin} form a transmission zero around 12 GHz in S_{21} .

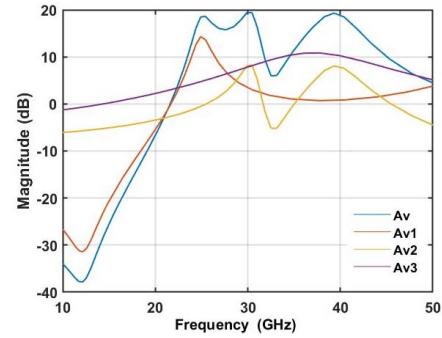


Fig. 3. Total system gain, the gain of each stage.

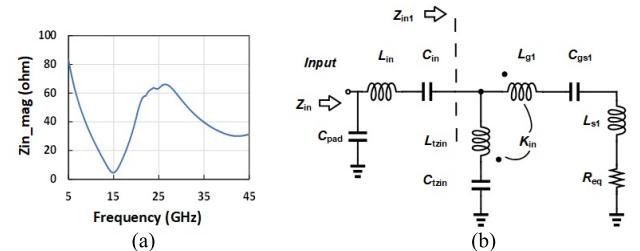


Fig. 4. (a) Input impedance Z_{in} . (b) Equivalent circuit of input matching network.

This transmission zero helps to reduce the low-frequency out-of-band unwanted interference. The dominant poles in the input matching network impedance frequency response are located at 24 and 28 GHz, respectively. The position of these two poles is controlled by k_{in} . A relatively smaller $k_{in} = 0.15$ is chosen to keep the poles closer to each other. Otherwise, excessive separation of those two poles will create a hump in the middle which degrades the wideband matching. The calculated input impedance of the concurrent LNA, Z_{in} , is plotted in Fig. 4(a), and it is close to Z_{in} from Cadence simulations.

C. Active Notch Circuit

A conventional passive notch is usually implemented by a series LC to form a transmission zero as shown in Fig. 5(a). The frequency of the notch/stopband is located at

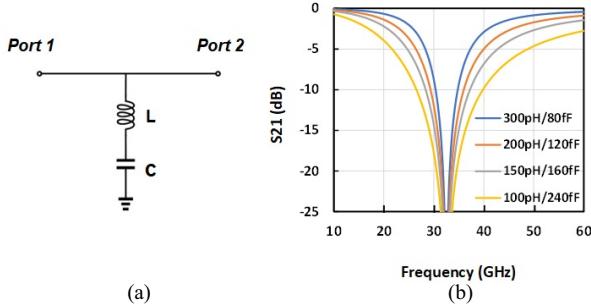


Fig. 5. (a) Conventional transmission zero notch. (b) Insertion loss S_{21} for the conventional transmission zero notches with ideal components.

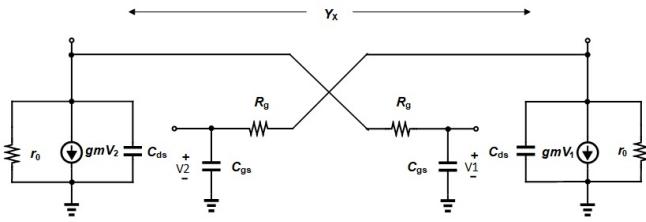


Fig. 6. Equivalent circuit of nMOS XCP.

$\omega = (1/\sqrt{LC})$, and the impedance of the series LC approaches zero creating a shorting path to ground. Different L and C combinations can achieve the same stopband frequency for a constant LC value. For the demonstration, the stopband chosen at 32.5 GHz is shown in Fig. 5(b) for five different L and C combinations with a constant LC value. Assuming k is the ratio of L over C , when the value of k is increasing, the transition between the passband and stopband becomes sharper. Hence, a larger value of L and a smaller value of C must be chosen to achieve a flatter passband and a steeper roll-off. In this project, $L = 335$ pH and $C = 72$ fF were chosen. However, due to the limited quality factor (for this inductance value, a typical value of a quality factor is 10–12 at 33 GHz) of the on-chip inductors, the practical depth of the notch is dramatically reduced to just several dBs at mm-wave frequencies [15]. To overcome this issue, an active XCP is implemented to enhance the quality factor of the transmission zero notches. The XCP is implemented to create a negative resistance and reduce the total series resistance of the notch inductor as analyzed thoroughly in [20], [21], [22], and [24].

The equivalent circuit of an nMOS XCP considering g_m , r_0 , R_g , C_{gs} , and C_{ds} of each pair is shown in Fig. 6. It includes a negative resistance of $R_{nn} = (2/g_m)$, a positive resistance of r_0 , a positive resistance of $R_{pn} = (2/(R_g C_{gs}^2 \omega^2))$, and a capacitance of $C_{xcpn} = (((1+g_m R_g)C_{gs} + C_{ds})/2)$ all in parallel representing Y_X [25]. If $R_g^2(C_{gs} + C_{gd})\omega^2 \ll 1$, then

$$\text{Re}(Y_X) \approx \frac{-g_m}{2} + \frac{1}{r_0} + \frac{R_g C_{gs}^2 \omega^2}{2} \quad (5)$$

$$\text{Im}(Y_X) \approx \frac{(1+g_m R_g)C_{gs} + C_{ds}}{2}\omega. \quad (6)$$

The CMOS version of XCP is realized in the schematic (M9–M12 in Fig. 1), and the equivalent circuit of XCP

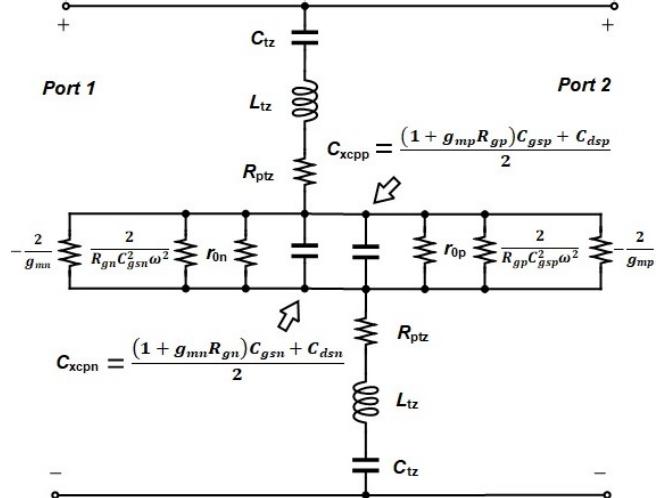


Fig. 7. Equivalent circuit of XCP with series LC s.

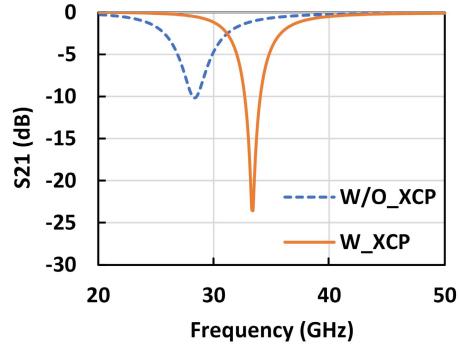


Fig. 8. Comparison of simulated notch depth with and without XCP.

including series LC s is shown in Fig. 7. The length of the nMOS tail current source of XCP is increased to five times of minimal length to help with the stability. For the same biasing current, the CMOS pairs have better noise performance than nMOS only pair, which means more energy is concentrated on the notch frequency. This is because the CMOS structure has better transconductance for the same biasing current [26]. Based on transistor characterization of notch nMOS and pMOS, the real part of the impedance of the CMOS XCP has one small negative resistance which is the result of all resistances in parallel, $R_{xcp} = R_{nn}/(R_{pn}/(r_{on}/(R_{np}/(R_{pp}/r_{op}))$. It partly compensates the series parasitic resistance of the inductor R_{ptz} . The imaginary part of the impedance has a capacitance, the result of two small capacitors in parallel, $C_{xcp} = C_{xcpn} + C_{xcp}$. This capacitance reduces the effect inductance of L_{tz} resulting in a slightly higher-shifted resonance frequency (transmission zero) when compared to the case without XCP, as shown in Fig. 8. Thus, the crucial effect of enhanced notch depth is from the negative resistance. The simulated S_{21} of notches are shown in Fig. 8 using a differential setup with EM-simulated inductors. The notch with the XCP case has a deeper notch depth with the same passives compared to the notch without XCP. The active XCP does not degrade the LNA linearity according to additional

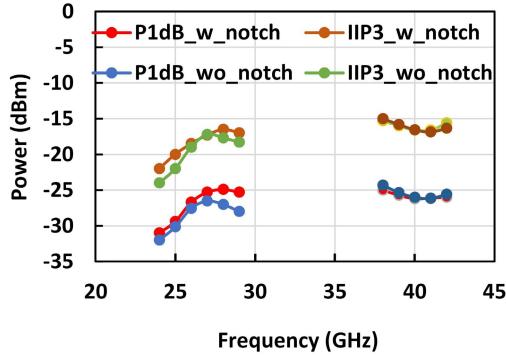


Fig. 9. Simulated input 1-dB compression point, input third order intercept point (IIP3) of LNA with and without the XCP.

simulations of LNA without the active notch, as shown in Fig. 9.

ADS system-level simulation has been studied to investigate the effectiveness of the notch on the cross-modulation phenomenon. An LNA model with a similar notch, comparable input-output matching, linearity, and gain to the LNA in this manuscript was built in ADS. A wideband LNA model (3-dB gain BW 20–40 GHz, without a notch) with similar specs was also built in ADS as a comparison. An amplitude-modulated blocker is applied at the input of both LNAs models with a frequency of 33 GHz (notch frequency) and a single-tone signal is applied at 25 GHz. The system works effectively to suppress the cross-modulation at the output of LNA with notch until $P_{\text{input-signal}} = -50$ dBm and $P_{\text{input-blocker}} = -30$ dBm, as shown in Fig. 10(a). At this input power level, the cross-modulation starts to appear at the output, and the cross-modulation is not observed for input power below this level in the LNA with the notch. When the power of the blocker and desired signal keep increasing, the 25-GHz signal shows more spectrum leakage due to the cross-modulation, but still has lower and narrower spectrum leakage than the wideband LNA case, thanks to the notch. This is shown in Fig. 10(b) when $P_{\text{input-signal}} = -40$ dBm and $P_{\text{input-blocker}} = -20$ dBm.

A new SE three-stage LNA with a passive LC notch located at its second stage has been designed and simulated in Cadence schematic level for comparison, as shown in Fig. 11. The newly designed SE LNA adopts a similar biasing point but with different interstage matching/load. Despite the fact that the peak gain and minimal NF are similar, as shown in Fig. 12, the low-quality factor of the notch inductor and capacitor not only decreases the notch depth, but also degrades the passband gain response, especially for 3-dB gain bandwidth of the lower passband. The reduced notch does affect the blocker resilience of the SE LNA. The power consumption is less as expected decreased from 18 to 13 mW, and the maximum blocker power is reduced from -30 dBm in the proposed LNA to -41 dBm in the SE version ($P_{\text{input-signal}} = -61$ dBm and $P_{\text{input-blocker}} = -41$ dBm) due to the reduced notch depth of passive LC , as shown in Fig. 10(c). The linearity has a similar trend compared to the original LNA, as shown in Fig. 13. The linearity is getting worse at the lower band due to the

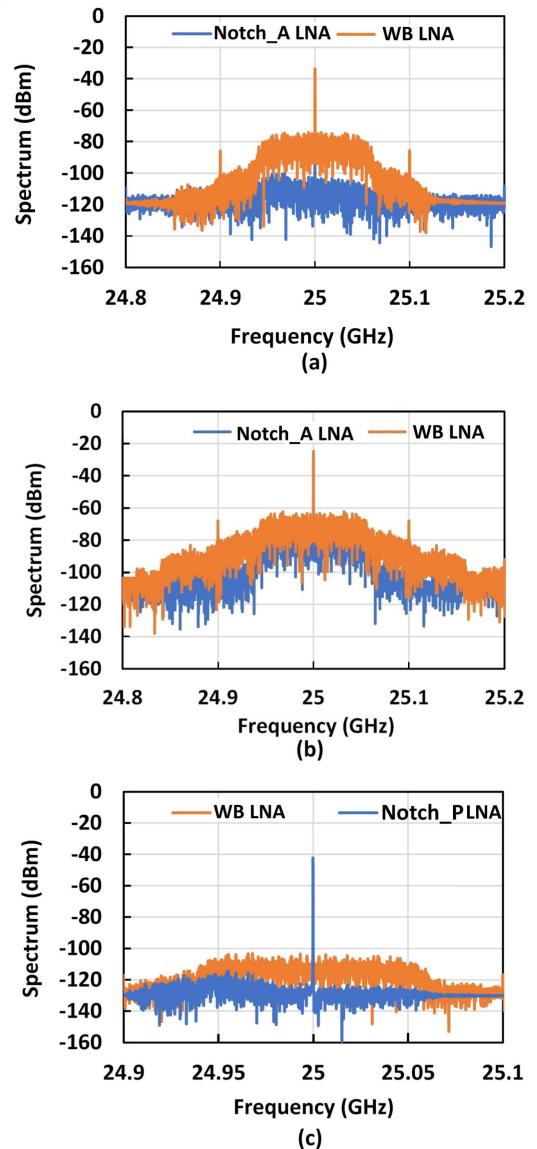


Fig. 10. Output power spectrum of wideband LNA and LNA with a notch in system analysis. (a) Active notch with input power: $P_{\text{signal}} = -50$ dBm and $P_{\text{blocker}} = -30$ dBm. (b) Active notch with input power: $P_{\text{signal}} = -40$ dBm and $P_{\text{blocker}} = -20$ dBm. (c) Passive notch with input power: $P_{\text{signal}} = -61$ dBm and $P_{\text{blocker}} = -41$ dBm.

SE design. The original LNA has a differential second stage which helps the linearity. The SE LNA has slightly better linearity at the upper band due to the reduced gain.

Desired variations were enabled for both process and mismatch, with the target yielding 3-sigma. The second-stage transistors M_3 – M_6 , XCP pair transistors M_9 – M_{13} , and notch capacitor C_{tz} are selected to run this 100-point Monte-Carlo simulation. However, notch inductor L_{tz} and interstage matching baluns L_{d1g2} and L_{d2g3} are customized designs, and this simulator/process design kit (PDK) cannot take them into consideration in Monte-Carlo simulations. This schematic-level simulation shows the variation of gain and notch in Fig. 14. The notch frequency varies from 31.5 to 34.9 GHz, the notch depth varies from 20 to 41 dB, and the peak gain of the lower/upper passband varies 7/6 dB.

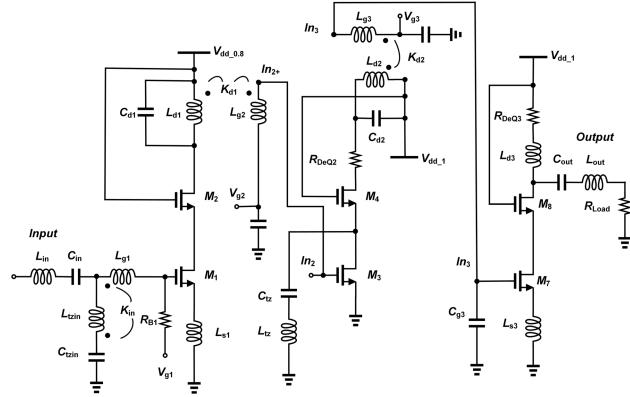


Fig. 11. Schematic of SE LNA with a passive notch.

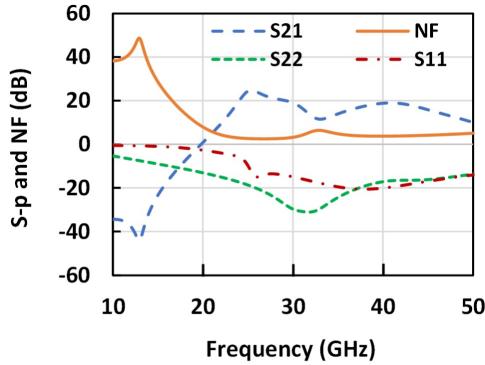


Fig. 12. Simulated S-parameter and NF of SE LNA with a passive notch.

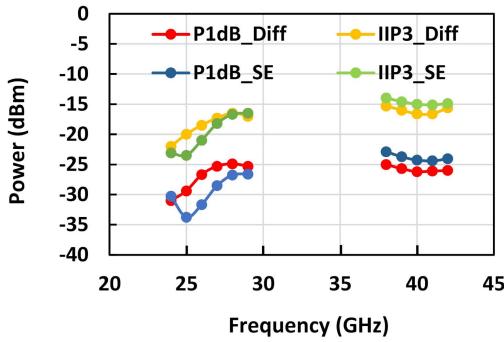


Fig. 13. Simulated input 1-dB compression point, IIP3 of LNA with an active notch, and SE LNA with a passive notch.

D. Noise Analysis

The equivalent noise model of the LNA is shown in Fig. 15 including major noise sources. The simulated noise contribution of major noise sources using Cadence is shown in Fig. 16 and shown in percentage for four different frequencies within the bands of interest. According to the simulated noise contribution within passband frequencies, the noise contribution of notch transistors is very low (less than 1.5% total noise contribution over the entire band), and the following noises are considered in the analysis: the thermal channel noise of the input nMOS M1 modeled as a current source, $\overline{I_{n,M1}^2} = 4kT\gamma g_{m1}$, the thermal channel noise of the cascode

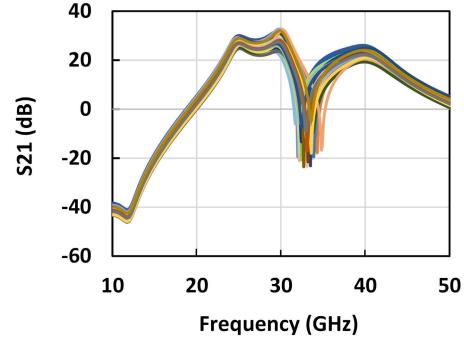
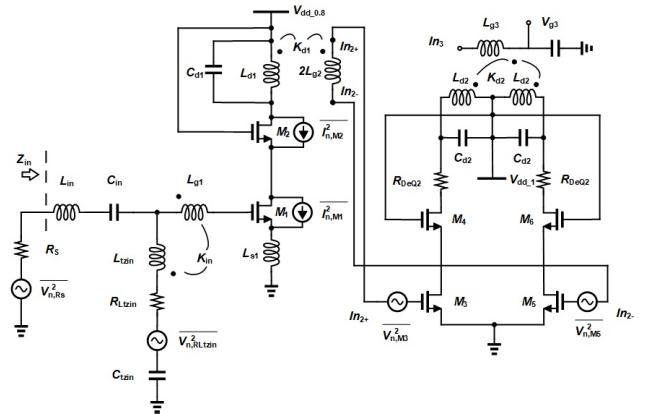
Fig. 14. Simulated S_{21} in schematic-level Monte-Carlo simulation.

Fig. 15. Noise source model of the LNA.

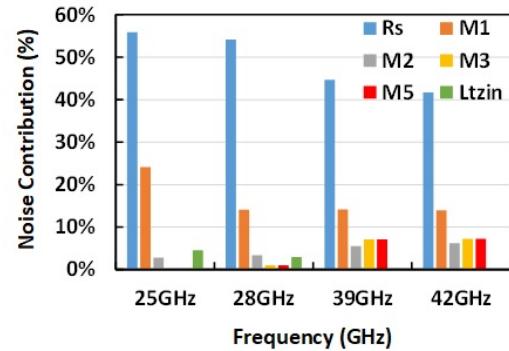


Fig. 16. Simulated noise contribution of major noise sources in the LNA.

nMOS M2 modeled as a current source, $\overline{I_{n,M2}^2} = 4kT\gamma g_{m2}$, the thermal channel noise of the second stage input nMOS M3/5 modeled as a voltage source, $\overline{V_{n,M3}^2} = ((4kT\gamma)/g_{m3})$, and $\overline{V_{n,M5}^2} = ((4kT\gamma)/g_{m5})$, the noise due to parasitic resistances R_{Ltzin} of L_{tizin} , $\overline{V_{n,Ltzin}^2} = 4kT R_{Ltzin}$, and the noise due to input source resistance R_s , $\overline{V_{n,s}^2} = 4kT R_s$ (k is the Boltzmann constant, γ is the excess noise coefficient, and T is the temperature in kelvin).

The noise current at the output of the first-stage $\overline{I_{n,o}^2}$ can be written as

$$\overline{I_{n,o}^2} = \overline{I_{no,M1}^2} + \overline{I_{no,M2}^2} \quad (7)$$

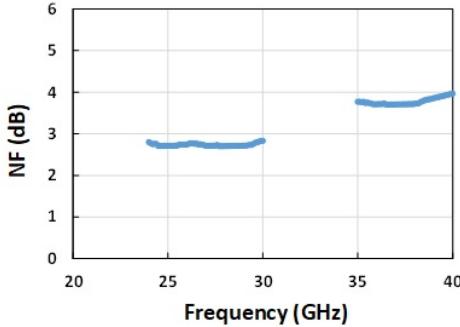


Fig. 17. NF from the analysis versus frequency for two desired subbands.

where

$$\overline{I_{no,M1}^2} \approx \frac{\overline{I_{n,M1}^2}}{[sL_{s1}g_{m1} + 1]^2} \quad (8)$$

$$\overline{I_{no,M2}^2} \approx \frac{\overline{I_{n,M2}^2}}{[1 + g_{m2}r_{o1}(1 + g_{m1}sL_{s1})]^2}. \quad (9)$$

The input-referred noise voltage of the first-stage $\overline{V_{ni,1}^2}$, the second-stage $\overline{V_{ni,2}^2}$ at the gate of the first stage, and the total input-referred noise voltage $\overline{V_{ni,g1}^2}$ at the gate of the first stage due to the noise effect of the transistors can be written as

$$\overline{V_{ni,g1}^2} = \overline{V_{ni,1}^2} + \overline{V_{ni,2}^2} \quad (10)$$

where

$$\overline{V_{ni,1}^2} = \frac{\overline{I_{n,o}^2}}{G_{m1}^2} \quad (11)$$

$$\overline{V_{ni,2}^2} = \frac{\overline{V_{n,2}^2}}{G_{m1}^2 Z_{d21}^2}. \quad (12)$$

Then the input-referred noise voltage $\overline{V_{n,i}^2}$ can be written as the following, assuming $Z_{in} = R_s$

$$\overline{V_{n,i}^2} \approx \overline{V_{n,s}^2} + \overline{V_{n,Ltzin}^2} + \overline{V_{ni,g1}^2}. \quad (13)$$

From simulations $g_{m1} \approx g_{m2}$ and $g_{m3} \approx g_{m5}$, the total NF of the concurrent LNA within the frequency bands of interests is given by the following equation and plotted in Fig. 17. As will be seen later, the calculated NF from (14) is close to the NF from Cadence simulations

$$\begin{aligned} \text{NF}(f) &= \frac{\overline{V_{n,i}^2}}{4kTR_s} \\ &\approx 1 + \frac{R_{Ltzin}}{R_s} + \frac{\gamma}{R_s g_{m1}} \\ &\quad + \frac{\gamma}{R_s g_{m1}^3 r_{o1}^2} + \frac{2\gamma}{R_s G_{m1}^2(f) Z_{d21}^2(f) g_{m3}}. \end{aligned} \quad (14)$$

E. Gain Control Design

In the third stage, a digital gain control subblock is implemented. It has a 3-bit control with a gain step of 1 dB each and a 7-dB gain difference in total. A 3-to-8 decoder with low activity is implemented to convert the 3-bit digital control

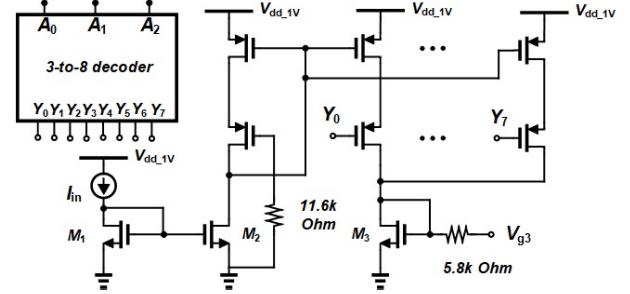


Fig. 18. Schematic of the gain-control-select current mirror.

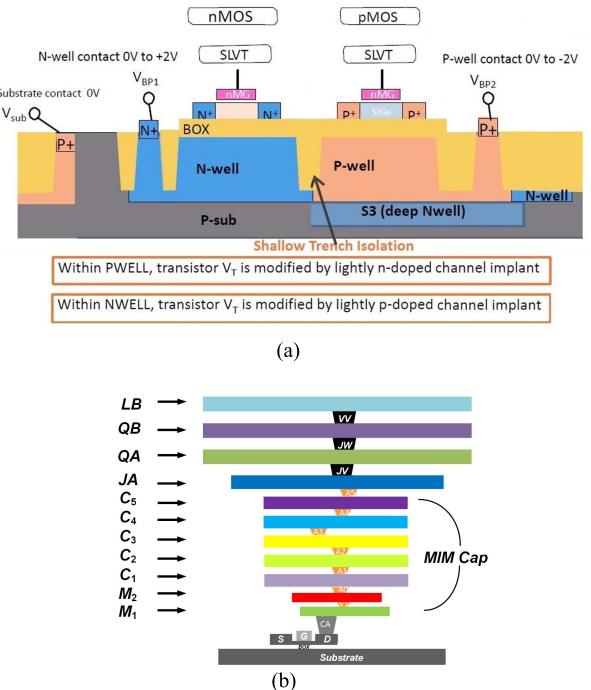


Fig. 19. (a) Cross section of FDSOI flip-well SLVT transistors. (b) Metal stacks of 22-nm FDSOI Option 19 [27].

signals to eight-switch enable signals of a current mirror. The schematic of the gain-control-select current mirror is shown in Fig. 18. The current output of this current mirror is delivered to M3 where its gate is connected to the third-stage input transistor M7 via a large resistor, $5.8\text{k}\Omega$.

III. LAYOUT DESIGN

A. Active Devices

The LNA is implemented in Global Foundries 22-nm FDSOI process. The Super low V_t (SLVT) transistors are used in this design, thanks to their lower noise and better high-frequency performance. Forward body biasing (FBB) technique is applied to SLVT transistors by applying a positive voltage on the body of nMOS and a negative voltage on the body of pMOS, VBP1, and VPB2 in Fig. 19(a), respectively. The threshold voltage is then reduced to increase the drive current. This technology helps to reduce the leakage current and junction capacitances and provides better isolation between devices, thus performing better at mm-wave frequencies.

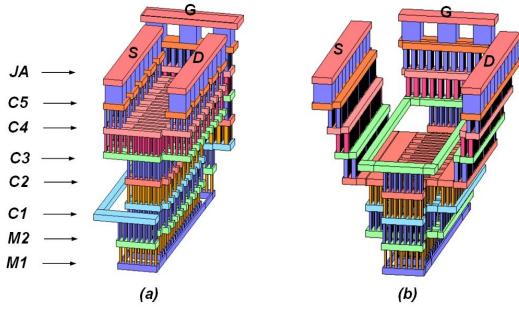


Fig. 20. (a) Layout of standcell for one of the multipliers (out of four) with finger width $W_F = 0.7 \mu\text{m}$ and number of fingers $N_F = 18$ from PDK. (b) Layout of standcell with modification.

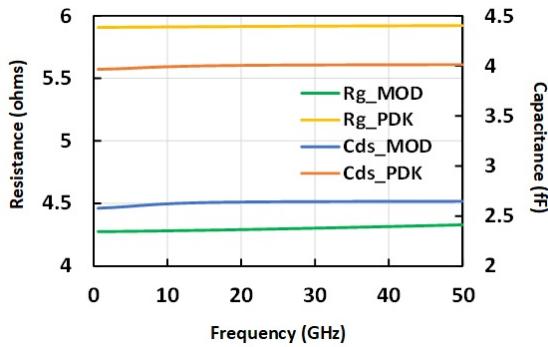


Fig. 21. C_{ds} and R_g due to metal routing.

The metal stack option 19 has been used with 11 layers of metals including the topmost aluminum metal (LB), as shown in Fig. 19(b).

The standcell of the first-stage input nMOS transistor is characterized as follows: A relaxed $2\times$ pitch helps to reduce the parasitic capacitance since the gate, drain, and source have larger separations between each other than standard pitch $1\times$. A multiple of 4, as in 2×2 , helps to reduce the routing resistance and improve matching during fabrications. A multiple finger number is implemented to reduce the gate resistance, which helps to reduce the NF. The layout is modified to a staircase pattern while bringing the metal routing to higher layer metals, as shown in Fig. 20, for one of the multipliers (out of four) with finger width $W_F = 0.7 \mu\text{m}$ and the number of fingers $N_F = 18$. For the gain control transistor (input transistor of the third stage), the connections are routed to the top layers as well. C_{ds} and R_g due to metal routing are EM simulated in Sonnet (version 17), as shown in Fig. 21. The results show that they are reduced, especially the reduced R_g helps to lower the NF which is important for an LNA.

Given the biasing condition of the first stage input nMOS M1 in Fig. 1, $V_{gs} = 0.4 \text{ V}$ and $V_{ds} = 0.39 \text{ V}$, f_t and f_{\max} are around 219 and 273 GHz, respectively. At $f = 30 \text{ GHz}$, the simulated NF_{\min} and V_{gs} with respect to the current density of the drain of the nMOS SLVT transistors, M1 and M2, are shown in Fig. 22. For a current density of $0.1\text{--}0.2 \text{ mA}/\mu\text{m}$, the NF reaches its lowest value. Given this result, the first stage of this LNA is biased at around $0.2 \text{ mA}/\mu\text{m}$ for optimized noise

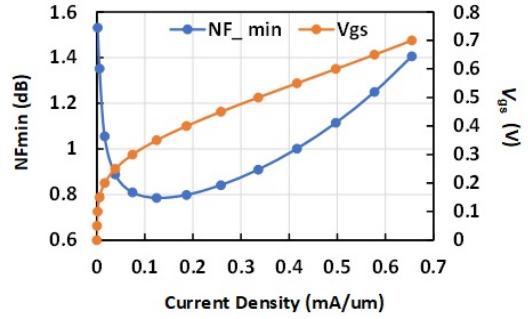


Fig. 22. Simulated NF_{\min} and V_{gs} with respect to current density.

performance. The first stage is sized in a way that the biasing current is at a lower level for NF and enough total width of $51 \mu\text{m}$ ($0.7 \mu\text{m} \times 18 \text{ fingers} \times 4 \text{ multiples}$) to provide the required transconductance.

B. Passive Components

In order to achieve a relatively compact layout and better performance, the inductors are fully customized, and they are simulated and optimized for a better quality factor using Sonnet (version 17). The top three thick layers of metals QA, QB, and LB in Fig. 19 have been used to implement inductors for a better quality factor due to their lower sheet resistance and further distance from the substrate. The top-layer LB metal is preferred due to its farthest distance from the substrate. The inductors are surrounded by ground shielding stacked from the M1 layer to the LB layer to contain their EM field and to minimize the coupling effect to other inductors.

The input inductor ($L_{\text{in}} = 69 \text{ pH}$, $Q = 22$ at 30 GHz), the output inductor ($L_{\text{out}} = 47 \text{ pH}$, $Q = 25$ at 30 GHz), the first-stage source degeneration inductor ($L_{s1} = 55 \text{ pH}$, $Q = 23$ at 30 GHz), and the third-stage source degeneration inductor ($L_{s3} = 20 \text{ pH}$, $Q = 28$ at 30 GHz) are implemented by transmission-line-type inductors. The input-coupled inductor, the interstage matching coupled inductor between the first stage and the second stage, and the interstage matching coupled inductor between the second stage and the third stage are implemented using spiral structures. The input inductor has a coupling factor of 0.07, L_{g1} of 180 pH, and L_{tzin} of 370 pH at 30 GHz, shown in Fig. 23. The low coupling factor is chosen for wideband input matching. The interstage matching coupled inductor between the first and the second stages acts as a balun to convert the SE signal at the output of the first stage to a differential signal for the second-stage differential inputs. It has a coupling factor of 0.58, L_{d1} of 220 pH, L_{g2} of 300 pH, as shown in Fig. 24. This coupling factor value is selected to optimize the gain of the first stage as mentioned in Section II-A. L_{d1} also serves as the Vdd power rail for the first stage. The interstage matching coupled inductor between the second and the third stage also acts as a balun to convert the differential signal of the second stage output to an SE input at the third stage. The QA metal layer is connected to the XCPs for the power supply. It has a coupling factor of 0.15, L_{d2} of 200 pH, and L_{g3} of 240 pH, as shown in Fig. 25. The notch inductor L_{tz} and the third-stage load inductor L_{d3} are

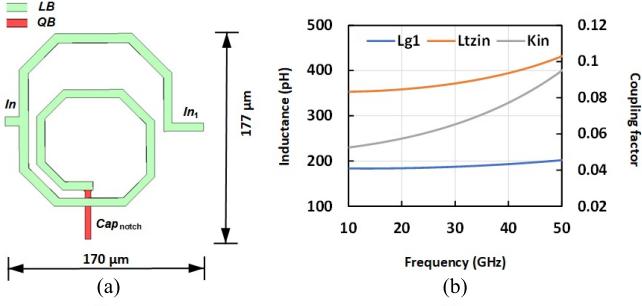


Fig. 23. (a) Layout of the input-coupled inductor. (b) Inductance values of L_{g1} , L_{tzin} , and their coupling factor k_{in} .

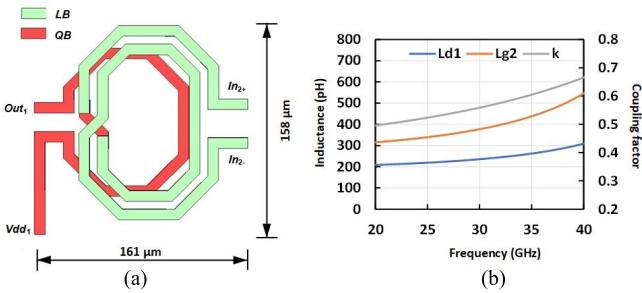


Fig. 24. (a) Layout of the interstage matching-coupled inductor between the first- and second-stage L_{d1g2} . (b) Inductance values of L_{d1} and L_{g2} , and their coupling factor of k_{d1} .

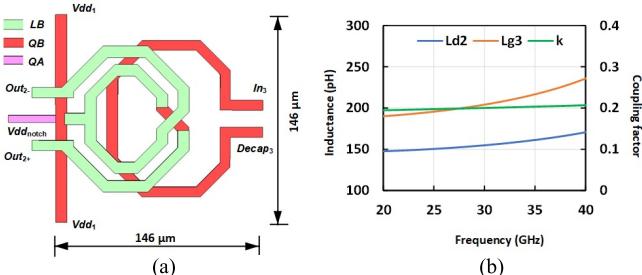


Fig. 25. (a) Layout of the interstage matching-coupled inductor between the second- and the third-stage L_{d2g3} . (b) Inductance values of L_{d2} and L_{g3} , and their coupling factor of k_{d2} .

shaped to fit into their locations for a compact layout. L_{tz} has an inductance value of 335 pH and a quality factor of 13 at 33 GHz, as shown in Fig. 26. L_{d3} has an inductance value of 160 pH and a quality factor of 22 at 30 GHz.

The mm-wave metal oxide metal (MOM) capacitors were carefully selected from the PDK. They have been optimized/modified to improve their quality factors. The lower level of metals, M1, and M2 were avoided to keep the capacitor further away from the substrate to reduce the substrate loss, thus improving the quality factor. For capacitors, type-2.5-V and type-5-V MOM capacitors were implemented which provide a better quality factor due to wider finger width than standard type-1.8-V MOM at the cost of lower capacitance density. All capacitors were modified with more vias and wider routing metal lines of positive and negative nodes to reduce the

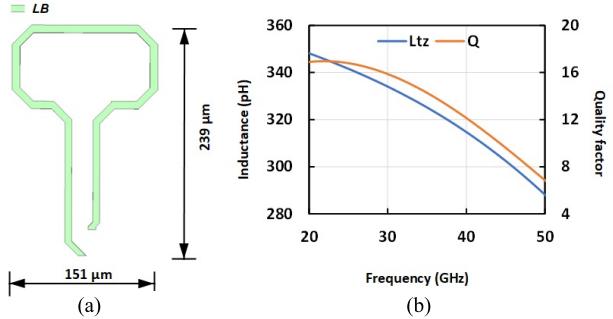


Fig. 26. (a) Layout of the third-stage source degeneration inductor L_{tz} . (b) Inductance value and quality factor of L_{tz} .

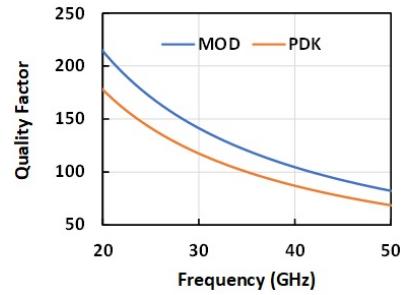


Fig. 27. Comparison of quality factor between the PDK MOM capacitor and modified MOM capacitor with wider metal routings and more vias.

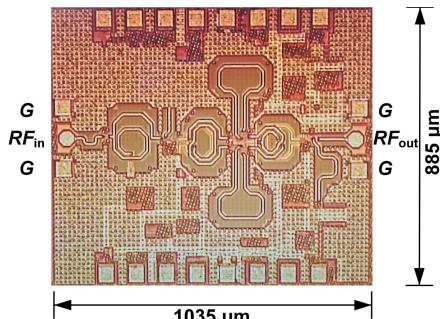


Fig. 28. Die photograph of the concurrent LNA.

series resistance. The improved quality factor and the original quality factor are shown in Fig. 27.

IV. FABRICATION AND MEASUREMENT

This concurrent LNA is fabricated using a 22-nm FDSOI CMOS process from Global Foundries. The photograph of the die under the microscope is shown in Fig. 28. It has a length of 1035 μm, a width of 885 μm, and an area of 0.916 mm² including all dc, RF pads, and decoupling capacitors. This concurrent LNA is measured on a wafer and by probing the dc biasing, RF input, and output. The cables and the RF probes are de-embedded by through, open, short, and matched (TOSM) calibration substrate. The Rohde & Schwarz ZVA67 network analyzer was used to perform S-parameter, 1-dB compression point, and IIP3 measurements. The Rohde & Schwarz FSV40 spectrum analyzer and Keysight 346CK01 noise source performed the NF measurement.

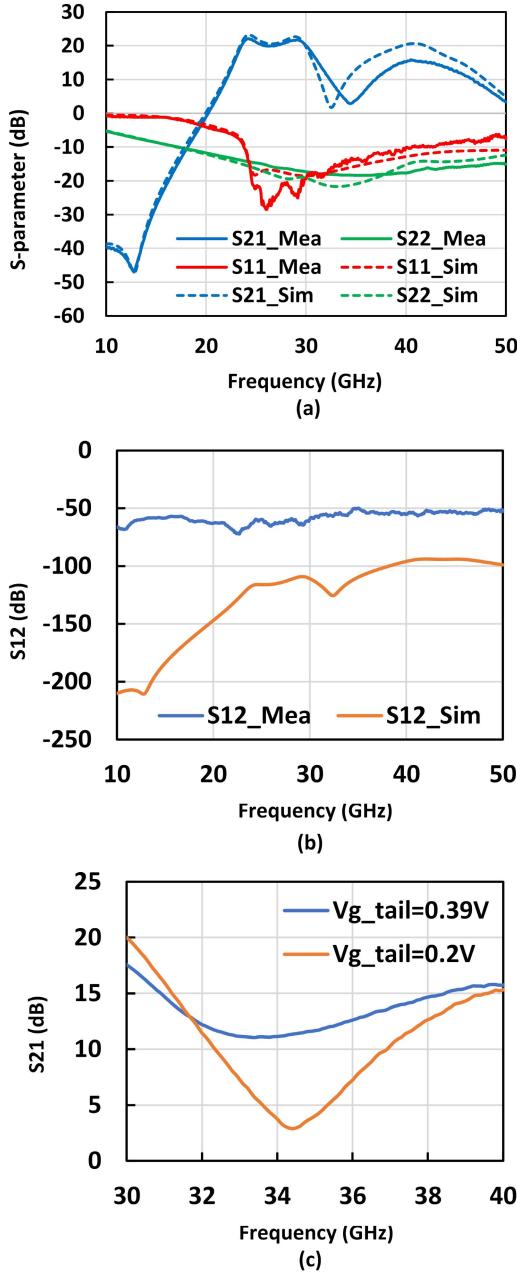


Fig. 29. (a) Measured and simulated results for S_{11} , S_{21} , and S_{22} . (b) Measured and simulated S_{12} . (c) Measured S_{21} of the notch with and without the enhancement effect.

The LNA consumes 18 mW with a supply voltage of 0.8 V for the first stage and 1 V for the second and third stages when the gain control is disabled.

Fig. 29(a) shows the measured and simulated results for S_{21} , S_{11} , and S_{22} versus frequency. The measured 3-dB gain bandwidth of S_{21} is from 23.3 to 30.3 GHz for the low bands with a peak gain of 22 dB at 24 GHz, and 38 to 44.7 GHz for the high bands with a peak gain of 16 dB at 40.5 GHz. The measured S_{11} is better than -10 dB from 23.7 to 42.7 GHz, and better than -9 dB up to 44.6 GHz. The measured S_{22} is better than -10 dB from 17.3 to 50 GHz. The measured S_{12} is better than -50 dB for the entire band as shown in Fig. 29(b). The notch is 2.8 dB at 34.1 GHz, compared to the low band,

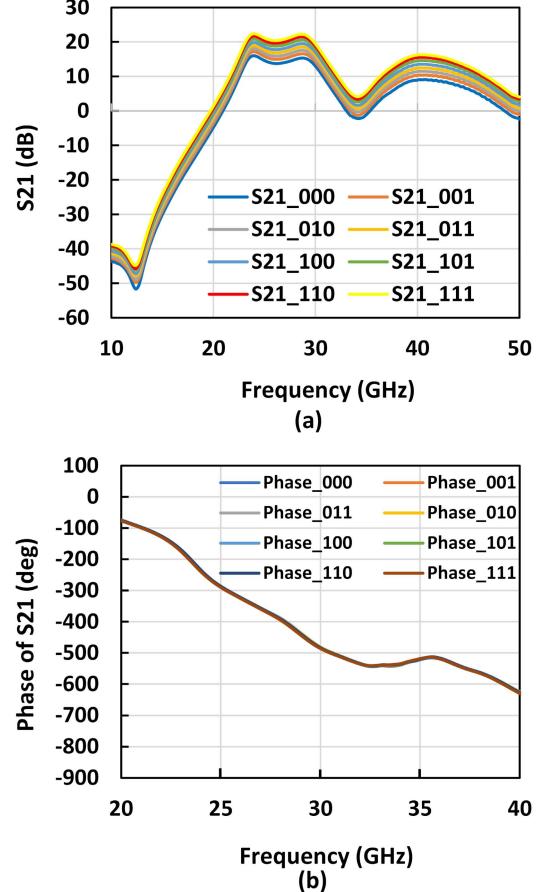


Fig. 30. Measured (a) gain steps and (b) phase steps.

the rejection is around 19.2 dB. The difference between the depth of notches is shown in Fig. 29(c) with and without the enhancement effect by differently tuned $V_{g\text{-tail}} = 0.39$ V and 0.2 V, respectively. The optimal depth notch frequency is different from chip to chip due to variations in fabrication. $V_{g\text{-tail}}$ in Fig. 1 is tuned differently to compensate parasitics so as to maximize the depth of the notch. The peak gain drop for the higher passband is likely due to the cross-coupling effect of passives and the reduced quality factor of customized inductors due to the mandatory metal filling which results in shifting the notch frequency after fabrication. Different gain steps and phase steps are shown in Fig. 30. S_{21} has eight steps with a 7-dB gain difference in total. Fig. 31 shows the measured and simulated stability factors K and $B1$. The measured K is larger than 12 and $B1$ is larger than 0.9 across the entire band. Although the measured stability factors K and $B1$ have some degradation compared to simulations, they still satisfy the necessary and sufficient conditions for unconditional stability $K > 1$ and $B1 > 0$.

In Fig. 32, the measured and simulated results of input IP3 and input 1-dB compression points are shown. The IIP3 is measured with 10-MHz two-tone spacing at each frequency. IIP3 varies from -18.2 to -21.6 dBm, and the input 1-dB compression point varies from -25.7 to -30.6 dBm for the lower band. IIP3 varies from -10.3 to -12.9 dBm, and the input 1-dB compression point varies from -17.2 to -22 dBm for the higher band. At the upper passband, the measured IIP3

TABLE I
PERFORMANCE COMPARISON OF RECENT WIDEBAND/SWITCHING/CONCURRENT LNAs

Reference & Type	Tech	Eff BW* (GHz)	Peak Gain (dB)	NF (dB)	S11/S22 -10dB BW (GHz)	P1dB/IIP3 (dBm)	Power (mW) @ Vdd (V)	Stopband rejection (dB)	Gain control & Range (dB)
JSSC 2020 [28] Wideband	22 nm CMOS FDSOI	22-32 (10)	21.5	1.73-2.87	22.5-32.2 (9.7) /20-32.4 (12.4)	NA/-14.4	17.3@1.05 5.6@1.05	NA	2-step Anlg. 3.6
RFIC 2019 [29] Wideband	22 nm CMOS FDSOI	26-34 (8)	12.6	1.35-1.7 (Limited Mea. BW)	26-34 (8) /25-31 (6)	-7.9/1.4	13@1.3	NA	NA
RFIC 2019 [6] Wideband	22 nm CMOS FDSOI	24-28 (5) 37-42 (5)	23	3.1-4.3	20-28 (8) 34-42 (8) /12.5-35 (22.5)	-20.4to-27 /-13.2to-19	20.5@1/1.6 12.1@0.8	NA	2-step Anlg. 4.8
RFIC 2021 [30] Wideband	28 nm CMOS	22.2-43 (20.8)	21.1	3.5-5.3	22.2-46.8 (24.6) /32.5-48 (15.5)	NA/avg=-3	22.3@0.9	NA	NA
MWCL 2019 [11] Switching	130 nm SiGe BiCMOS	28(Narrowband) 60‡	16.2 15	2.8 3.35	25-30 (5) /-9dB@28GHz -8dB@60GHz	-12/NA -7/NA	21@2.5	8.7 10	NA
TCAS-II 2021 [10] Switching	45 nm CMOS FDSOI	24‡ 28‡ 39‡	9 6 15.5	5.8 4.5 5.5	-8dB@24GHz -8dB@28GHz -5dB@39GHz /NA	-12/NA -13/NA -16.5/NA	20.7@NA	10 NA 5.5	NA
TMTT 2013 [15] Concurrent	180 nm SiGe BiCMOS	14-15.2 (1.2) 22.4-25.8 (3.4) 32.1-35(2.9)	22.4 23.7 20.2	3.4-5 3.2-3.6 3.7-4.1	14-35 (21) /14-15 (1)	-21/-13.5 -26.7/-17.1 -24.1/-16.1	36@1.8	41 30	NA
TCAS-I 2018 [16] Concurrent	180 nm SiGe BiCMOS	21.5‡ 36‡	16.6Se 19.Dif	4.2-5.8 4.3-8	-9dB@26GHz /15-42 (27)	-24.3/-14.9 -26.9/-16.8	73.8@2.5	26Se 37Dif	NA
This work Concurrent	22 nm CMOS FDSOI	23.7-30.3 (6.6) 38-42.7 (4.7)	22 16	2.55-3.8 4.75-6.1**	23.7-42.7 (19) /17.3-50(32.7)	-17.2to-30.6 /-10.3to-21.6	18@0.8/1	19.2 13.2	8-step Digi. 7

*Eff BW is when the gain is within 3-dB BW and the input matching is better than -10dB.

**The NF is measured up to 40 GHz due to the limitation of FSV40 and the peak gain of upper band is beyond 40 GHz.

‡The input matching is worse than -10dB.

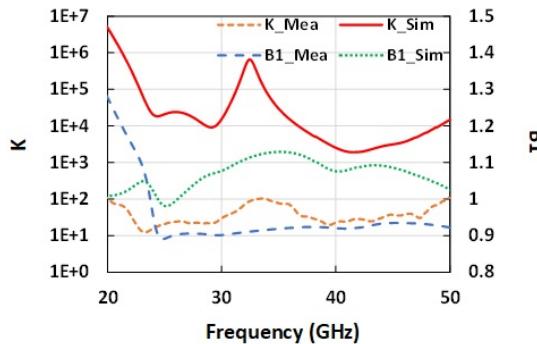


Fig. 31. Measured and simulated stability factors K and $B1$.

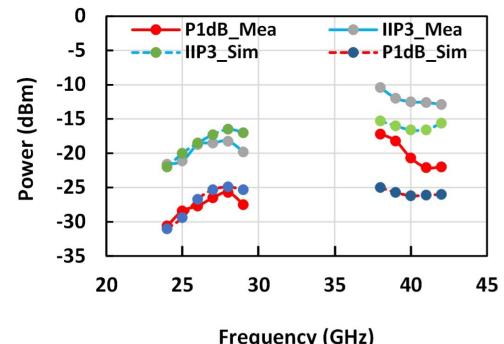


Fig. 32. Measured and simulated input 1-dB compression point and IIP3.

and P1 dB are better than the simulated values due to the reduced gain caused by the cross-coupling effect of passives and the mandatory metal filling. The measured and simulated noise figures (NFs) are shown in Fig. 33. The Y-factor method was used for the NF measurement. The minimum measured NF is 2.55 dB at 28 GHz. The NF is measured up to 40 GHz due to the limitation of the spectrum analyzer, and NF is 4.75 dB at 40 GHz as a result of the reduced gain.

Table I summarizes the measured results of other recently published wideband and switching LNAs. It also includes concurrent LNAs with stopband rejection. The wideband

LNAs have a relatively flat frequency response and can work concurrently while having no stopband rejection. The switching LNAs can provide 5–10 dB of stopband rejection for narrowband operations, but cannot work concurrently. The concurrent LNAs [15], [16] do provide deeper stopband rejection compared to this work but at the cost of worse input–output matching, wider gap between passbands, and considerably narrower frequency response. This work simultaneously achieves wideband input matching from 23.7 to 42.7 GHz, wideband output matching from 17.3 to 50 GHz, a gain of 22 dB with 3-dB BW from 23.3 to 30.3 GHz,

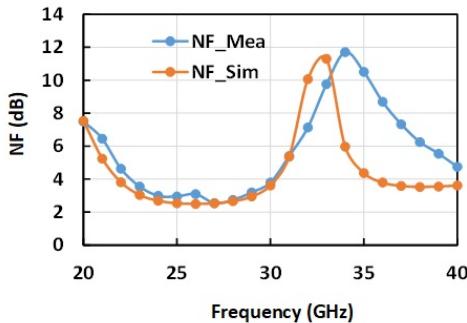


Fig. 33. Measured and simulated NF.

and a gain of 16 dB with 3-dB BW from 38 to 44.7 GHz, a 19.2-dB stopband rejection, a 2.55-dB minimum NF performance, as well as 18-mW power consumption at the same time.

V. CONCLUSION

A concurrent dual-band LNA is introduced using the 22-nm FDSOI process. It covers 23.3–30.3-GHz and 38–44.7-GHz 5G bands with low NF, low power consumption, and wideband matching. Two notches are implemented at 12.8 and 34.1 GHz, respectively, to attenuate unwanted blocker signals. The XCP-enhanced notch is implemented to enhance the notch depth by overcoming the limited quality factor of passives at mm-wave frequency.

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