

Certificate

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Class: I T E - 2

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Exam No:

Institution _____

*This is certified to be the bonafide work of the student in the
Laboratory during the academic
year 20 / 20 .*

No. of practicals certified _____ out of _____ in the
subject of STLD

.....
Teacher In-charge

.....
Examiner's Signature

.....
Principal

Date:

Institution Rubber Stamp

(N.B: The candidate is expected to retain his/her journal till he/she passes in the subject.)

I n d e x

S. No.	Name of the Experiment	Page No.	Date of Experiment	Date of Submission	Remarks
1.	Exp-1 Verification & realization of truth table for AND, OR, NOT, NOR, NAND, XOR, XNOR		11/10/21		J G 10/10/21
2.	To verify all gates using NAND and NOR gates		18/10/21		J Ph G 13/12/21
3.	To realize half adder and full adder.		25/10/21		J G 10/10/21
4.	To realize half subtractor and full subtractor.		1/11/21		J Ph 10/10/21
5.	To realize priority encoder using basic gates.		8/11/21		J Ph 13/12/21
6.	To design binary grey code converter.		15/11/21		J G 10/10/21
7.	To realize multiplexer and demultiplexer using NAND gates only.		22/11/21		J Ph 13/12/21
8.	To realize 1 bit magnitude comparator		29/11/21		J Ph 13/12/21

EXPERIMENT - 1

AIM: Verification & interpretation of truth table for AND, OR, NOT, NOR, XOR, X-NOR gates.

Apparatus: Breadboards, IC's, logic gates

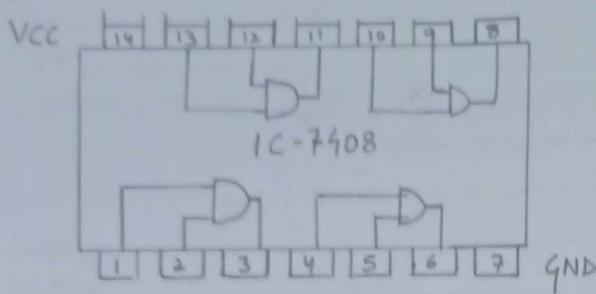
Theory:

1. AND gate - produces output as 1 only when both of the inputs are 1 otherwise 0.
2. OR gate - produces output when any input is 1 otherwise 0.
3. NOT gate - It has 1 input and 1 output as when any, if input is 1 output is 0 and vice versa.
4. NAND GATE - The output is 1 when any or both inputs are 0, otherwise it is 0.
5. NOR GATE - The output is 0 when any or both inputs are 1, otherwise it is 1.
6. X-OR GATE - produces output as 1 if no. of 1's in input is odd otherwise 0.
7. X-NOR gate - produces output as 1, when no. of 1's at input is even otherwise zero.

PROCEDURE

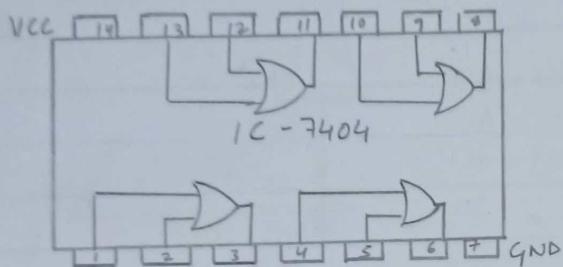
1. Connect to the power supply
2. Connect the input of any logic gates to the logic source of output to the logic indicators.

1. AND Gate



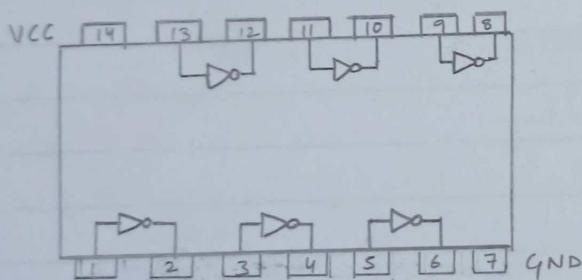
A	B	$Y = AB$
0	0	0
0	1	0
1	0	0
1	1	1

2. OR GATE



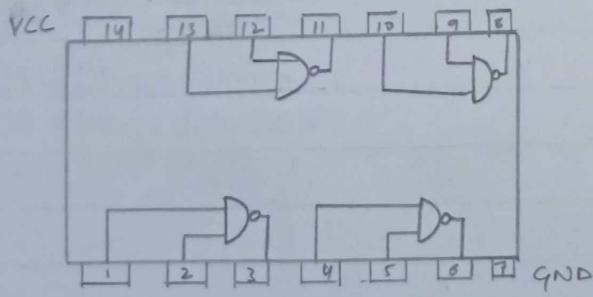
A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT-GATE



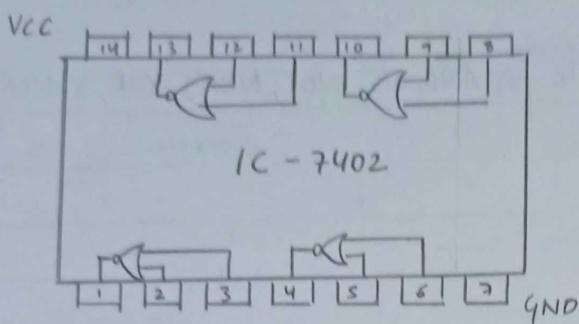
A	$Y = \bar{A}$
0	1
1	0

4. NAND GATE



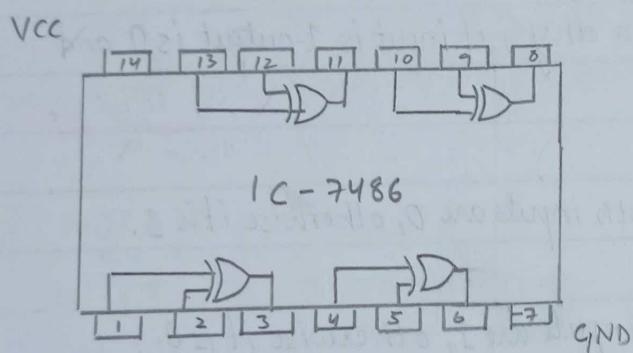
A	B	$Y = A \cdot \bar{B}$
0	0	1
0	1	1
1	0	1
1	1	0

5. NOR GATE :-



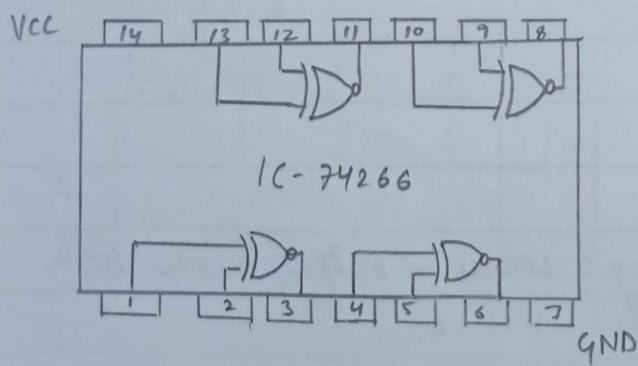
A	B	$Y = \bar{A} + \bar{B}$
0	0	1
0	1	0
1	0	0
1	1	0

6. X-OR GATE :-



A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

7. X-NOR GATE :



A	B	$Y = A \bar{\oplus} B$
0	0	1
0	1	0
1	0	0
1	1	1

3. Verify the truth table for each input and output.

PRECAUTIONS :

1. Take care while supplying voltage to IC.
2. Keep in mind the number of pins.

RESULT :

All the given gates were studied & verified by truth table.

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Teacher's Signature _____

EXPERIMENT-2

AIM → To verify all gates using NAND and NOR gate.

Apparatus → Breadboard, IC 7400 (NAND), IC (7402'NOR), LED, Connecting wires

Theory:

- I. NAND gate represents complement of the AND operation. It's name is an abbreviation of NOT-AND. The graphic symbol of NAND gates consist of an AND symbol with bubble on the output.
- II. NOR gate: The NOR gate represents the complement of the OR operation. It's name is the abbreviation of NOT-OR. The graphic symbol of NOR gate consists of an OR symbol with bubble on the output.

Procedure:

1. Connections are made as per circuit diagram.
2. Switch on the power supply.
3. Apply different combination of input with observation of output. Compare output with the truth table.

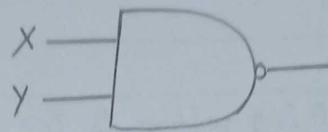
Precautions:

- All IC's should be checked before starting the experiment.
- All the connection should be tight.

Result:

NAND and NOR gates have been studied as universal gates.

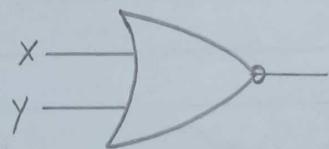
FOR NAND



$$Z = \overline{X \cdot Y}$$

X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

FOR NOR GATE

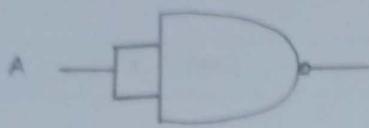


$$Z = \overline{X + Y}$$

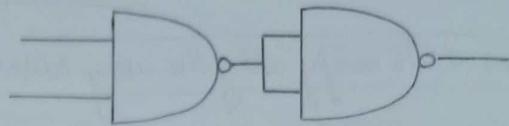
X	Y	NOR
0	0	1
0	1	0
1	0	0
1	1	0

NAND AS UNIVERSAL GATES!

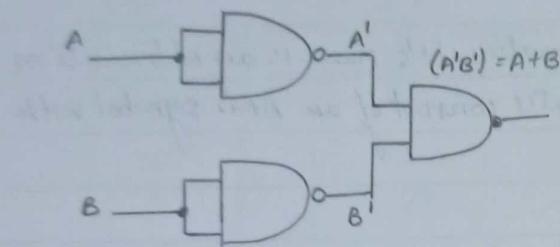
(a) NAND as NOT GATE



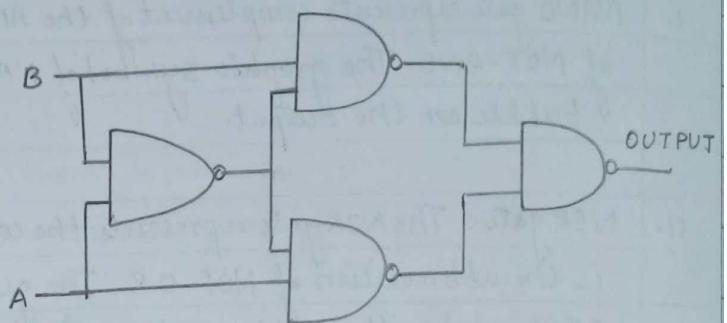
(b) NAND as AND GATE



(c) NAND as OR GATE

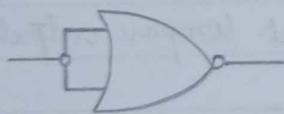


(d) NAND as

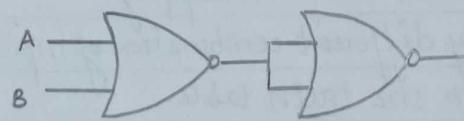


NOR GATE AS UNIVERSAL GATES:

(a) NOR \rightarrow NOT

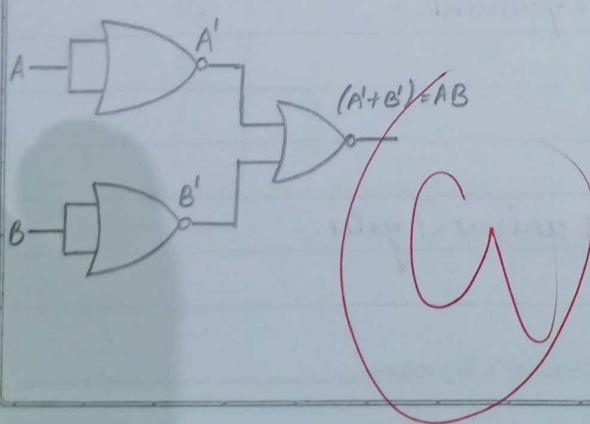


(b) NOR \rightarrow OR

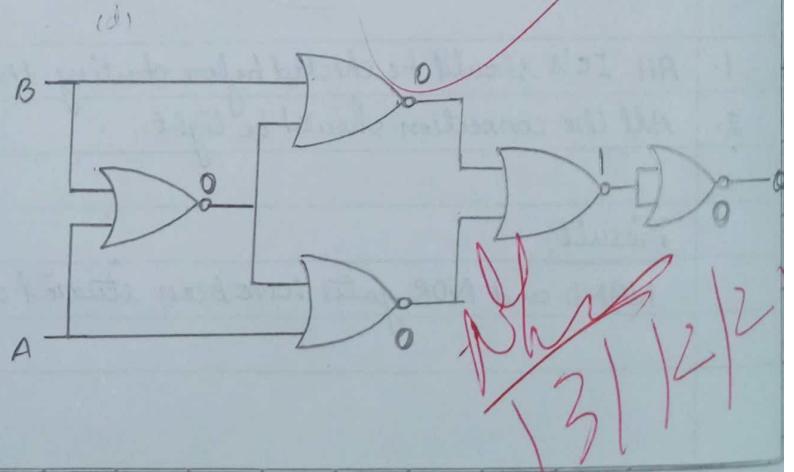


(c) NOR \rightarrow AND

(c) NOR \rightarrow AND



(d) NOR \rightarrow XOR



EXPERIMENT-3

AIM: To realize half adder and full adder.

Apparatus: Bread board, IC - 7486 (X-OR), IC - 7408 (AND), IC - 7432 (OR), Led's.

Theory:

1. Half Adder: A combinational circuit that perform the addition of two bits A & B is called half adder.
Addition will give two output bits one of which is the sum bit S and the other is carry bit.

$$S = A \oplus B$$

$$C = AB$$

2. Full Adder: The half adder does not take the carry bit from its previous stage into account. This carry bit from previous stage is called carry-in bit. A combinational logic-circuit that adds two bits A & B and a carry-in bit C_{in} is called full adder.

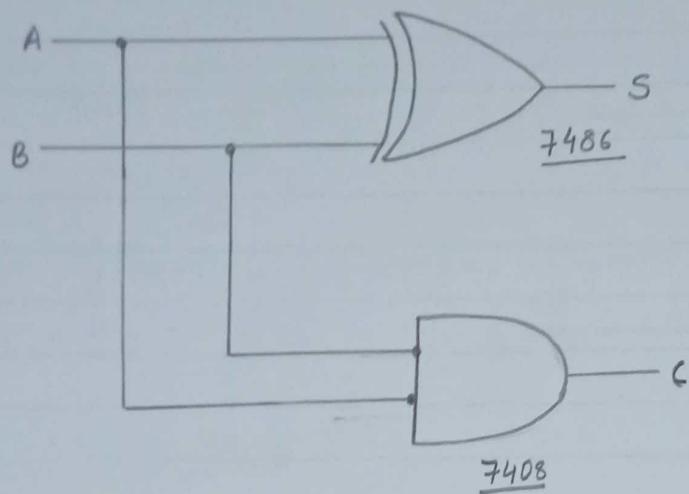
$$\rightarrow S = (X \oplus Y) \oplus C_{in}$$

Procedure:

1. Verify the gates.
2. Make connection as per circuit diagram.
3. Switch on V_{cc} & apply various combinations.
4. Note the output reading.

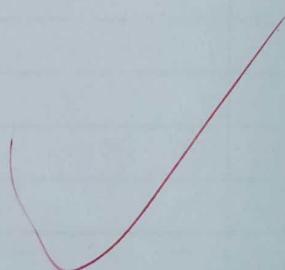
Teacher's Signature _____

HALF ADDER



TRUTH TABLE

INPUTS		OUTPUTS	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Precautions:

1. All IC's should be checked before.
2. All connection should be tight.
3. Always connect ground first & then the supply.

Result

Half adder and Full adder have been realized using basic gates & their truth table has been verified.

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FULL ADDER

TRUTH TABLE

INPUTS			OUTPUTS	
A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

X	YZ	00	01	11	10
0			1		1
1		1		1	

$$S = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XY\bar{Z}$$

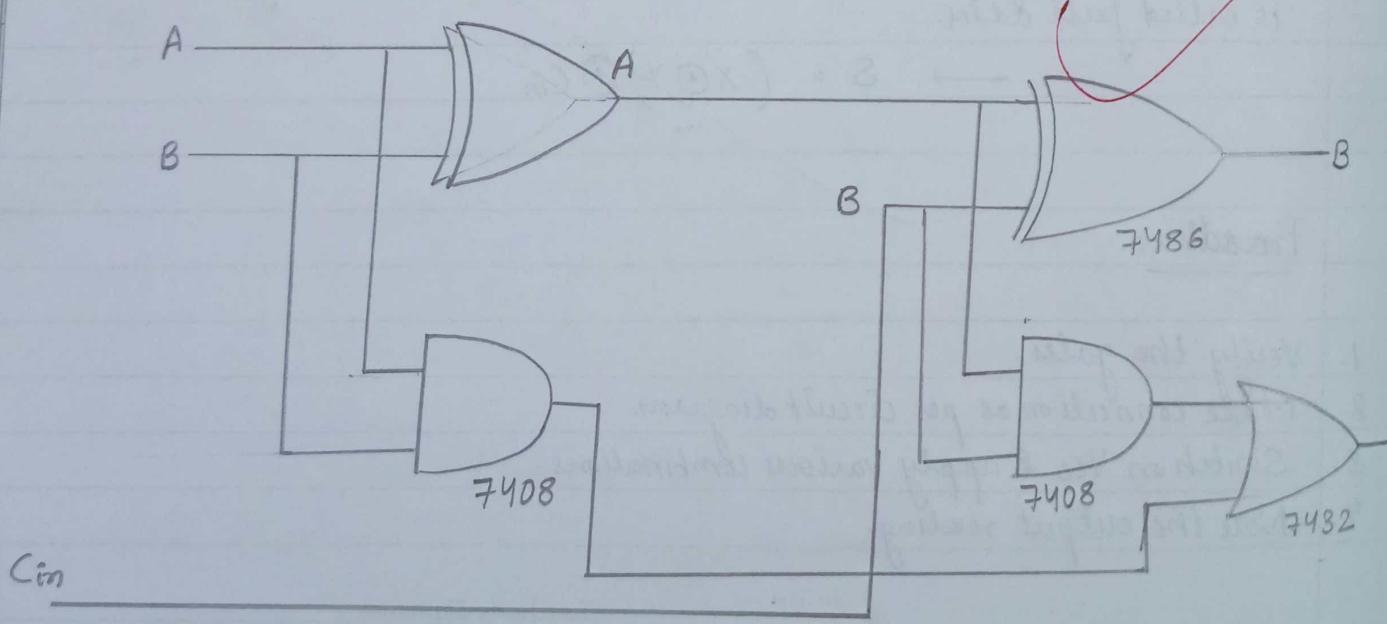
$$= X \oplus Y \oplus Z$$

X	YZ	00	01	11	10
0				1	
1			1	1	1

$$C = XY + XZ + YZ$$

$$= XY + Z(\bar{X}Y + \bar{X}Y)$$

$$= XY + Z(X \oplus Y)$$



EXPERIMENT-4

AIM: To realize Half subtractor and full subtractor.

Apparatus: Breadboard, IC-7486 (XOR), IC-7408 (AND), IC-7432 (OR), Leds, Power Supply.

Theory:

1. **Half Subtractor**

Subtracting a single bit binary value B from another produces a different bit D and a borrow bit out B . This is called half subtractor.

$$S = A \oplus B$$

$$C = A'B$$

2. **Full Subtractor**

Subtracting two bit binary values B , Cin from single bit value. It produces a different bit D & a borrow out B_{out} bit. This is called full subtractor.

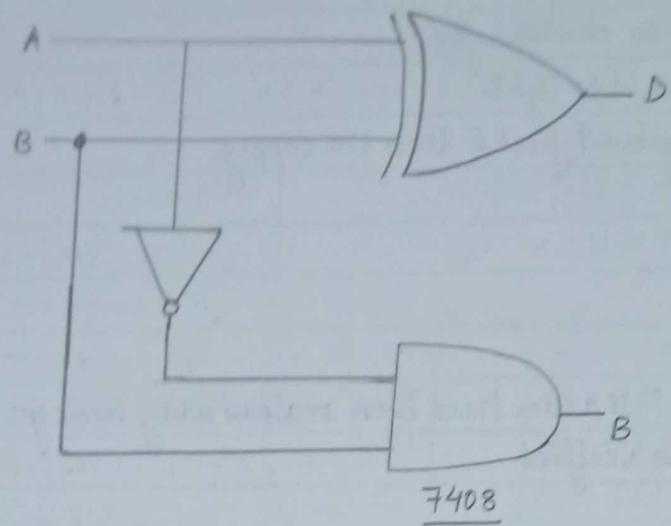
$$D = (X \oplus Y) \oplus Cin$$

$$B_{out} = A'B + A'Cin + BCin$$

Procedure:

1. Check the components for their working.

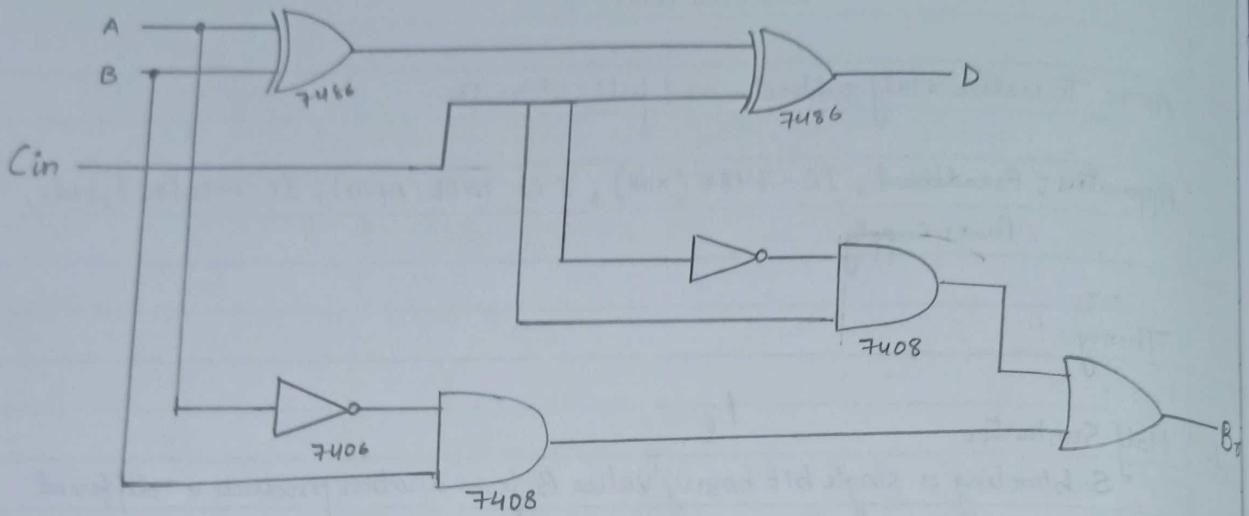
Half Subtractor



TRUTH TABLE

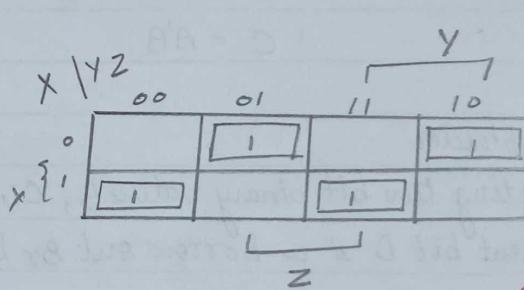
INPUTS		OUTPUTS	
A	B	D	B̄
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

FULL SUBTRACTOR

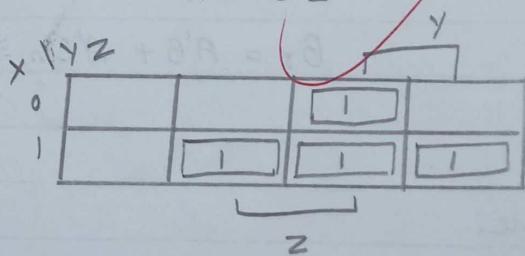


TRUTH TABLE

INPUTS			OUTPUTS	
A	B	Cin	D	B̄
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



$$\begin{aligned} S &= \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XY\bar{Z} \\ &= X \oplus Y \oplus Z \end{aligned}$$



$$\begin{aligned} C &= XY + XZ + YZ \\ &= XY + Z(X\bar{Y} + \bar{X}Y) \\ &= XY + Z(X \oplus Y) \end{aligned}$$

2. Insert the appropriate IC into IC base.
3. Make connections as shown.
4. Verify the result.

Precautions :

1. All the connection should be tight.
2. Always connect ground first & then the supply.

Result

Half subtractor & full subtractor have been verified.

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EXPERIMENT - 5

AIM: To realize priority encoder using basic gates.

Apparatus: Bread Board, IC-7408 (AND), IC-7404 (NOT)

Theory:

The priority encoder circuit that includes the priority function. The operation of priority encoder is such that if two or more inputs are equal to 1 at the same time the input having the highest priority will take precedence.

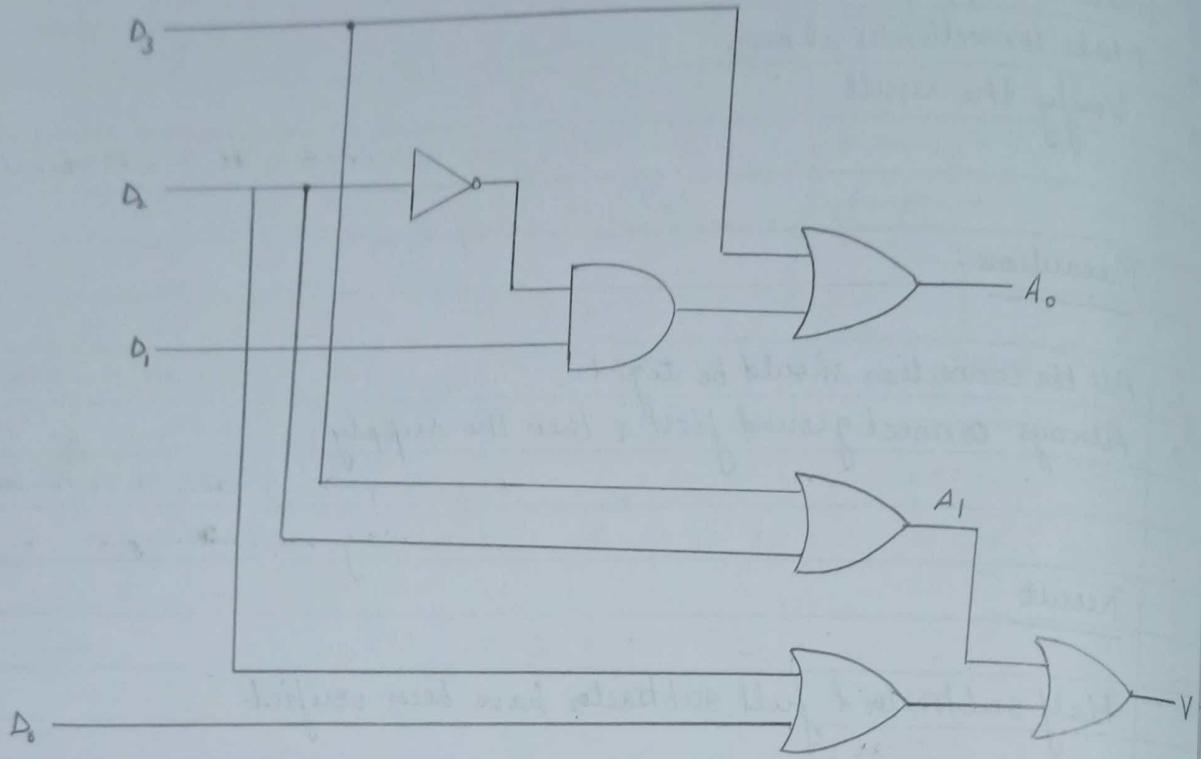
The 4-input priority encoder has 4 inputs and 3 outputs. 'V' is valid-bit indicator that is set to 1 when one or more inputs are equal to 1. If all inputs are zero, there is no valid input and V is equal to 0. The other two outputs are not specified when V equals 0 and are specified as don't care conditions.

Procedure:

1. Check the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections.
4. Verify the results.

Precautions:

1. All connection should be tight.
2. Always connect ground first & then supply.
3. Switch off the power supply.



TRUTH TABLE:

D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	x	x	1
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	0	x	x	1	0	1
1	x	x	x	1	1	1



$D_3 D_2$	$D_1 D_0$	00	01	11	10
00	X				
01		1	1	1	1
11		1	1	1	1
10		1	1	1	1

$$A_1 = D_2 + D_3$$

$D_3 D_2$	$D_1 D_0$	00	01	11	10
00	X				
01					
11		1	1	1	1
10		1	1	1	1

$$A_0 = D_3 + D_1 D_2$$

$D_3 D_2$	$D_1 D_0$	00	01	11	10
00					
01					
11		1	1	1	1
10		1	1	1	1

D_2

$$V = D_0 + D_1 + D_2 + D_3$$

Result

Priority Encoder has been studied & its truth table has been verified.

✓ G
W 2
B 1 | 2 |

EXPERIMENT - 6

AIM: To design binary to grey code converter.

Apparatus: Breadboard, connecting wires, IC

Theory:

It is very important & useful code converter in which a decimal number is converted to a binary form in such a way that each grey code differs from other than preceding & succeeding number by single bit.

Procedure:

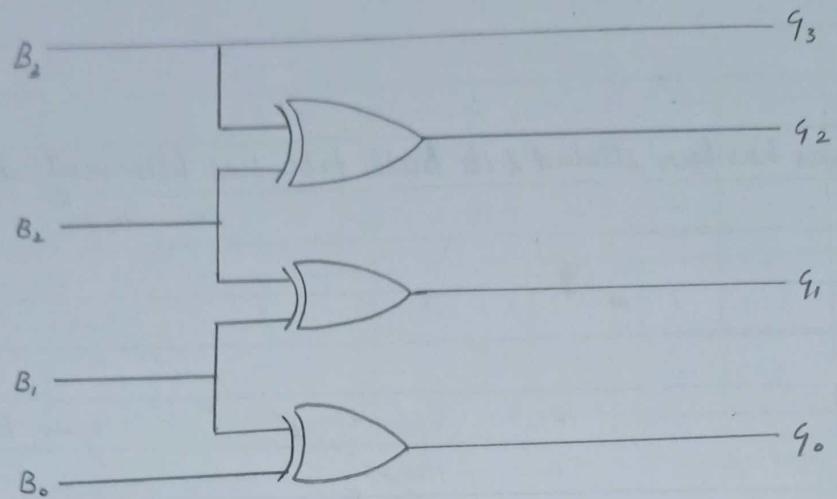
1. Connect circuit as per given diagram.
2. Insert IC on breadboard.
3. Give Vcc & ground to all ICs.
4. Specify the output of binary to grey code converter.
5. Verify output with truth table.

Result:

Binary code to grey code has been converted.

Precautions:

1. Make neat & tight connections.
2. Insert all IC without damaging breadboard



TRUTH TABLE

K-MAP

1. For G_0

		$B_1 B_0$	00	01	11	10
		$B_2 B_3$	00	1	1	1
		00	1	1	1	1
		01	1	1	1	1
		11	1	1	1	1
		10	1	1	1	1

$$G_0 = B_0 \bar{B}_1 + B_1 \bar{B}_2 \\ = B_0 \oplus B_1$$

2. For G_1

		$B_1 B_0$	00	01	11	10
		$B_3 B_2$	00	1	1	1
		01	1	1	1	1
		11	1	1	1	1
		10	1	1	1	1

$$G_1 = B_2 \bar{B}_1 + B_1 \bar{B}_2 \\ = B_1 \oplus B_2$$

3. For G_2

		$B_1 B_0$	00	01	11	10
		$B_2 B_3$	00	1	1	1
		01	1	1	1	1
		11	1	1	1	1
		10	1	1	1	1

$$G_2 = B_2 \bar{B}_3 + B_3 \bar{B}_2 \\ = B_2 \oplus B_3$$

4. For G_3

		$B_1 B_0$	00	01	11	10
		$B_3 B_2$	00	1	1	1
		01	1	1	1	1
		11	1	1	1	1
		10	1	1	1	1

$$G_3 = B_3$$

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EXPERIMENT - 7

Aim: To realize Multiplexer & Demultiplexer using NAND gates only.

Apparatus: Breadboard, IC-7400 (NAND), IC-7410 (3 Input NAND), LED's, 5 V power supply.

Theory:

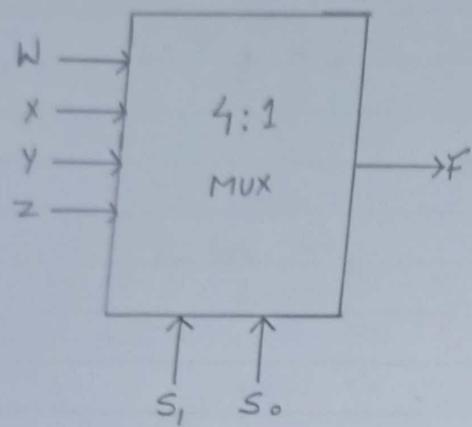
Multiplexers are very useful components in digital system. They transfer a large number of information units over a small number of channels. Multiplexer means many to one output. By using control signals we can select any input but only one output. The general multiplexer has 2^n input signals or control signal & 1 output signal.

Demultiplexer performs opposite function of multiplexer. They transfer a small number of units over large number of channels under control of single unit signals.

Procedure:

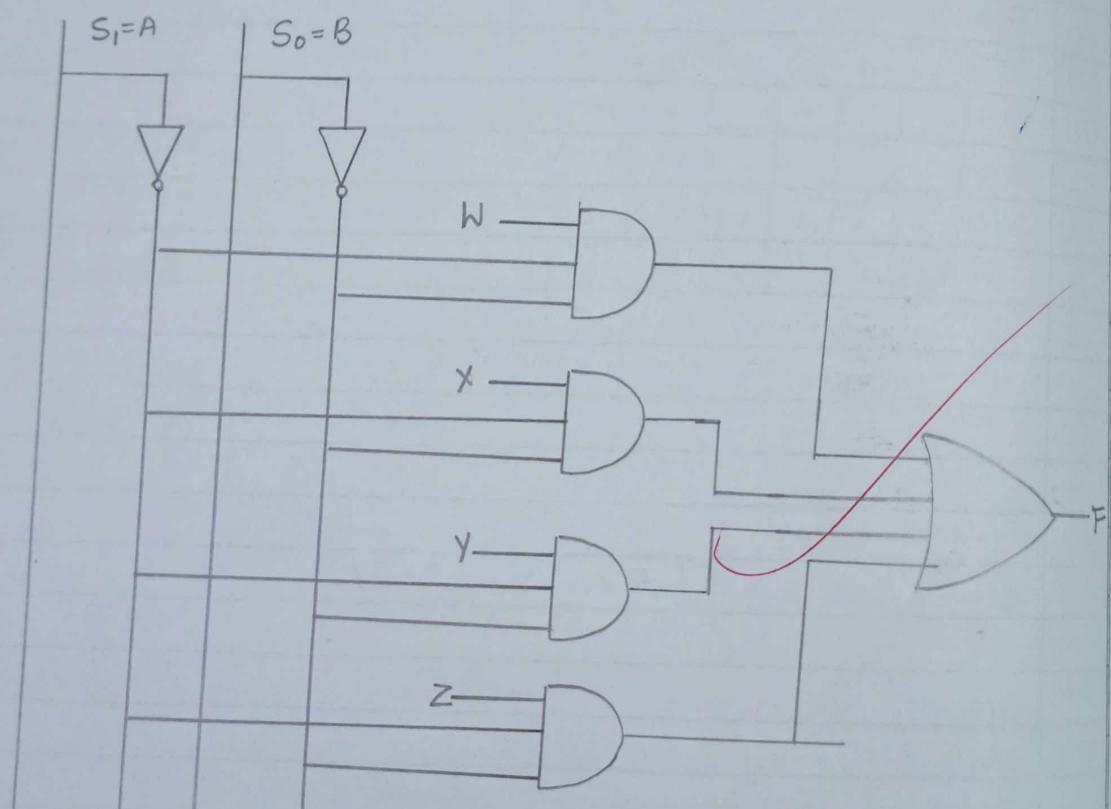
1. Check the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connection shown in the diagram.
4. Verify the result.

Logic diagram And truth table for 4:1 multiplexer

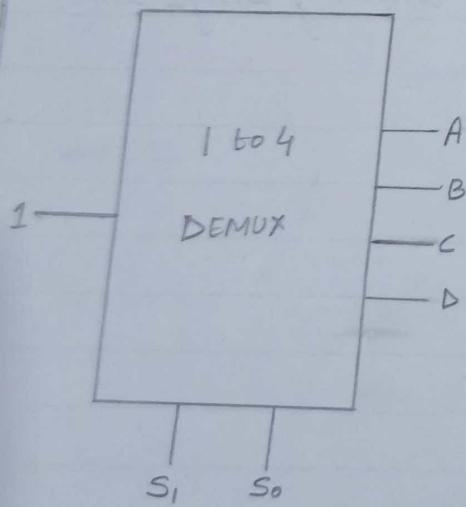
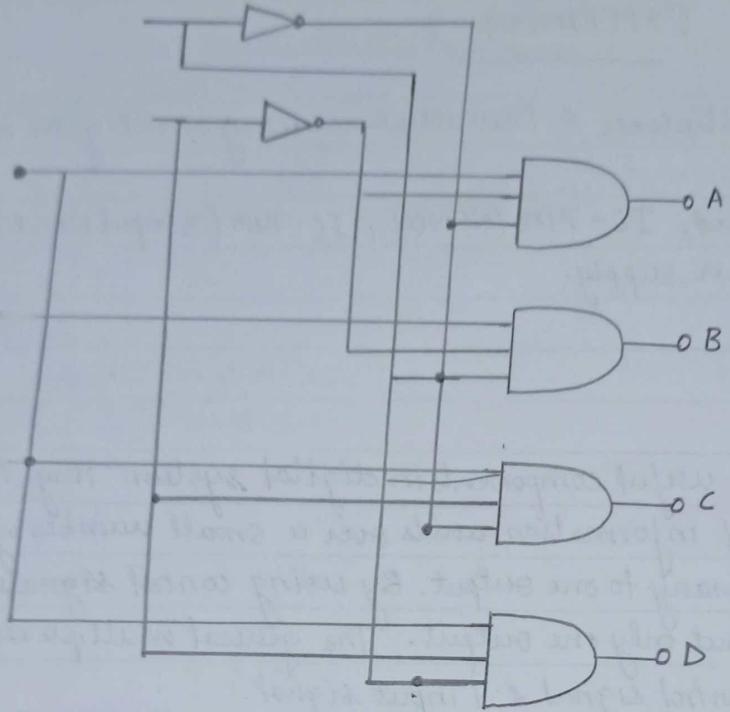


$$S_1 = A$$

$$S_0 = B$$



Logic diagram and Truth table of 1:4 DEMUX



	SELECT		O/P				
	S ₁	S ₀	A	B	C	D	
	1	0	0	1	0	0	0
	1	0	1	0	1	0	0
	1	1	0	0	0	1	0
	1	1	1	0	0	0	1

Precautions:

1. All the connection should be tight.
2. Always connect ground first & then supply.
3. Switch off the power supply after completion.

Result

Multiplexer & De-Multiplexer is being verified.

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EXPERIMENT - 8

AIM → To realize 1 bit magnitude comparator.

Apparatus → Bread board, IC's (7400) NAND, 7403 - (3ip NAND), LED's, Wires

Theory:

Magnitude comparator is a logical circuit which compares two signals A & B and generate three logical output whether $A > B$, $A = B$ or $A < B$. The outcome of the comparison is specified by three binary variables that indicate whether $A > B$, $A = B$, $A < B$. A comparator used to compare two bits is called single bit. It consists of two inputs each ~~for~~ for two single bit numbers of three output to generate less than, equal to & greater than between two binary numbers.

Procedure:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base
3. Make the connection as shown in circuit diagram.
4. Verify the result and observe the output

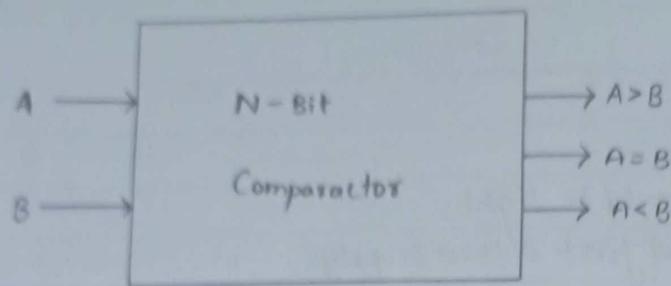
Result

1-bit comparator has been studied & its truth table is also verified.

Precautions:

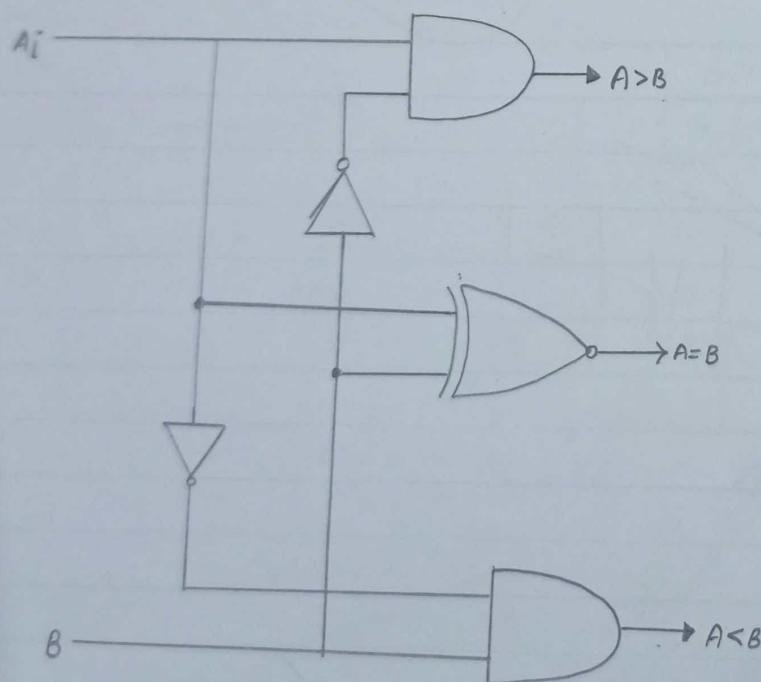
1. All the connections should be tight.

1.



TRUTH TABLE

<i>A</i>	<i>B</i>	$A < B$	$A = B$	$A > B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0



• $A > B$ only if $A_i = 1, B_i = 0$

• $A < B$ only if $A_i = 0, B_i = 1$

• $A = B$ only if $A_i = B_i = 0 \text{ or } 1$

4. K map for 1 bit comparator

(a)

	B	0	1
A	0	1	0
0	1	0	0
1	0	0	0

$(A > B)$

$$\text{Equation is } A > B = A \cdot \bar{B}$$

(b)

	B	0	1
A	0	0	1
0	0	1	0
1	0	0	0

$(A < B)'$

$$\text{Equation is } A < B = A \cdot \bar{B}$$

(c)

	B	0	1
A	1	1	0
0	0	0	1

$(A = B)$

$$\begin{aligned} \text{Equation is } (A = B) &= \bar{A} \cdot \bar{B} + A \cdot B \\ &= A \times \text{XNOR } B \end{aligned}$$

→ From truth table

$$\rightarrow (A < B) + (A > B) = A' B + B' A$$

$A > B : AB'$ $A < B : A'B$ $A = B : A'B' + AB$

{ Take complement both sides }

$$\begin{aligned} ((A < B) + (A > B))' &= (A'B)' \cdot (\bar{A}B')' \\ &= (AA' + AB' + BA' + BB')' \\ &= (AB + A'B')' \end{aligned}$$

$$((A < B) + (A > B))'$$

$$((A < B) + (A > B))'$$

Thus,

$$((A < B) + (A > B))' = (A = B)$$

2. Always connect ground first & then the supply.
3. Switch off the power supply after completion of experiment.

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