8086 16-bit

R.

- 8086 - 1978
- DIP ⊙ Dual Inline package (having two rows of pins)

8086 ← 8086 (5MHz)
8086-2 (8MHz)
8086-1 (10 MHz)

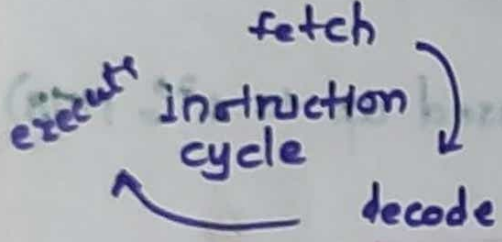
- 29,000 transistors
- 16 line data bus
- 20 line address bus (addressed up to 2^{20} = 1MB)

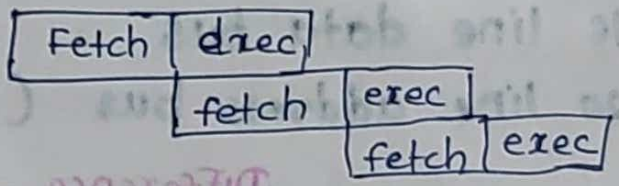
Difference

8085		8086
8-bit	data	16-bit
16-bit (64 kB)	address / Memory	20-bit (1 MB)
No	Instruction queue	6-byte
No	Pipelining / Multi Processor	Yes
2^8 = 256	IO	2^{16} = 65536
No	Co-processor	8087
No	Mul / Div	Yes

Integer only	— Arithmetic —	Integer / Real arithmetic.
3-5 MHz	— clk speed —	5-8-10 MHz
single	— operating mode —	Min / Max mode
6 - addressing mode	— addressing mode —	24 - addressing mode
8-vectored	— Interrupts —	256 vectored
No	— Memory seg mentation —	Yes

Pipelining : fetching 2nd instruction during execution of first.





Adv Throughput increase
Pipline stage ↑ execution ↑

Through put : clk required to execute instruction

difference

8086		8088
16-bit	— data bus —	8-bit
20 - bit	— address —	8-bit
2 banks < 512 kb, 512 kb	— Bank —	single memory bank
5-8-10 MHz	— clk speed —	5-8 MHz
M/$\overline{IO}$	— Min mode —	IO/$\overline{M}$
$\overline{BHE}$ for higher byte	— data width 20 pin —	only 1 byte

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यश हॉस्पिटल व प्रसूती गृह

(अॅडव्हान्सड् लॅपरोस्कोपीक सेंटर)

कॉलेज रोड, रावळगांव नाक्याजवळ, मालेगांव कॅम्प – ४२३ १०५

फोन नं. (०२५५४) २५१३१४

डॉ.तुषार पी.झांबरे

M.B.B.S., D.G.O.

R. Features of 8086 : 40 pins (20 - 20)

16-bit up, 20-bit address bus (2^{20} = 1MB), 10 ports (2^{16} = 64)

Registers (14, 16-bits), word size 2 byte (16-bits) double size 4 bytes (32 bits).

Multiplexed address & data buses (AD0 - AD15) & (A16-A19)

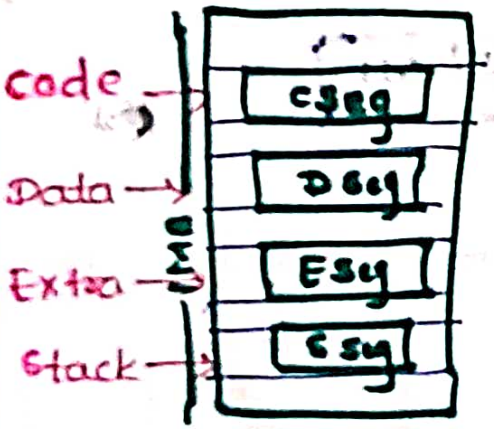
Operates in two mode (Min / Max)

having 6-byte instruction queue.

+5 Volts power supply.

Address ranges = 00000H - FFFFFH

Segment Memory



Memory divided into logical segments. (each 64 kB) data, code, extra, stack. they may be overlapped or non-overlapped

There are four registers (Segment registers)

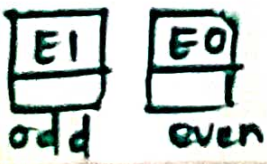
DS, SS, ES, CS

They holds upper 16-bit data address of four memory segment (it is starting address of each segment)

1MB divided into two parts (banks) each

odd bank (contains odd address) lower bank

Even bank (contains even address) Higher bank



Segment discriptions : associated Register (16-bit each)

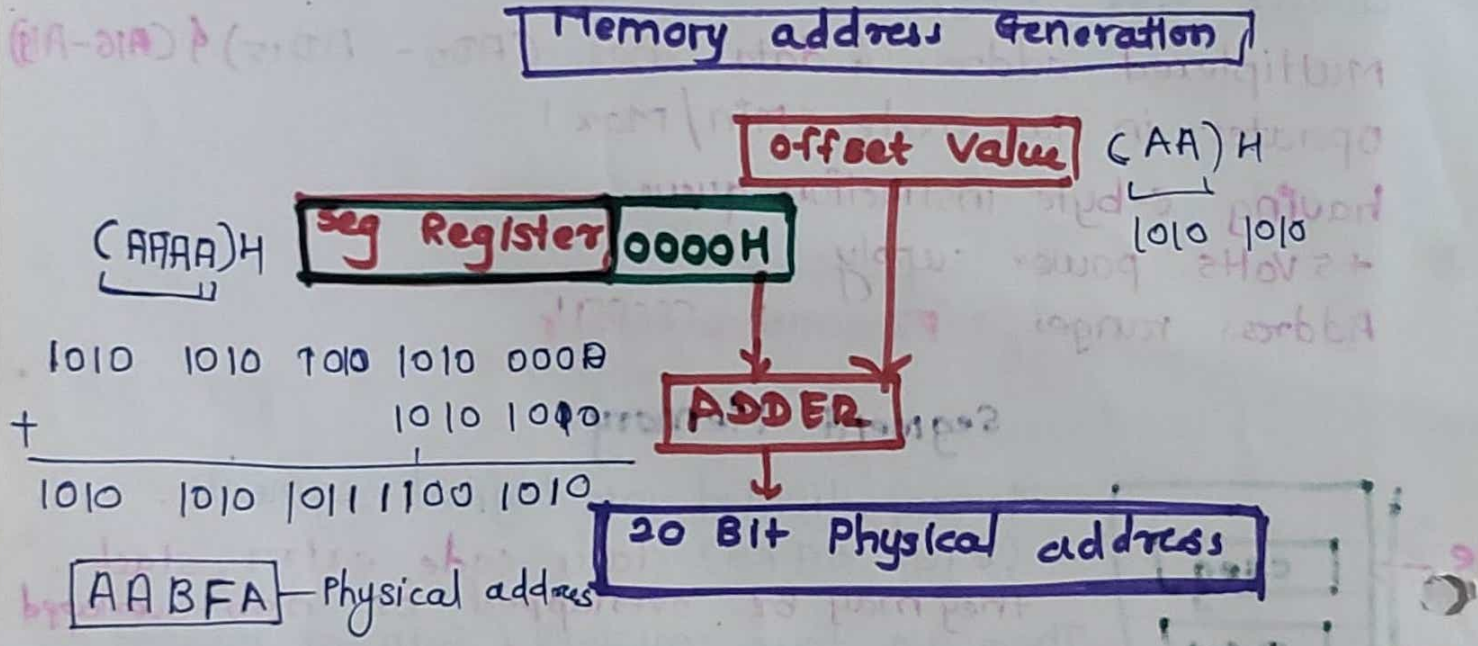
code segment — stores instruction (CS Register)

stack segment — used as stack (can store or return address) (stack seg reg)

data segment, extra segment } — store data byte (data seg reg) (extra seg reg)

Segment Registers : they points to starting location of particular seg.

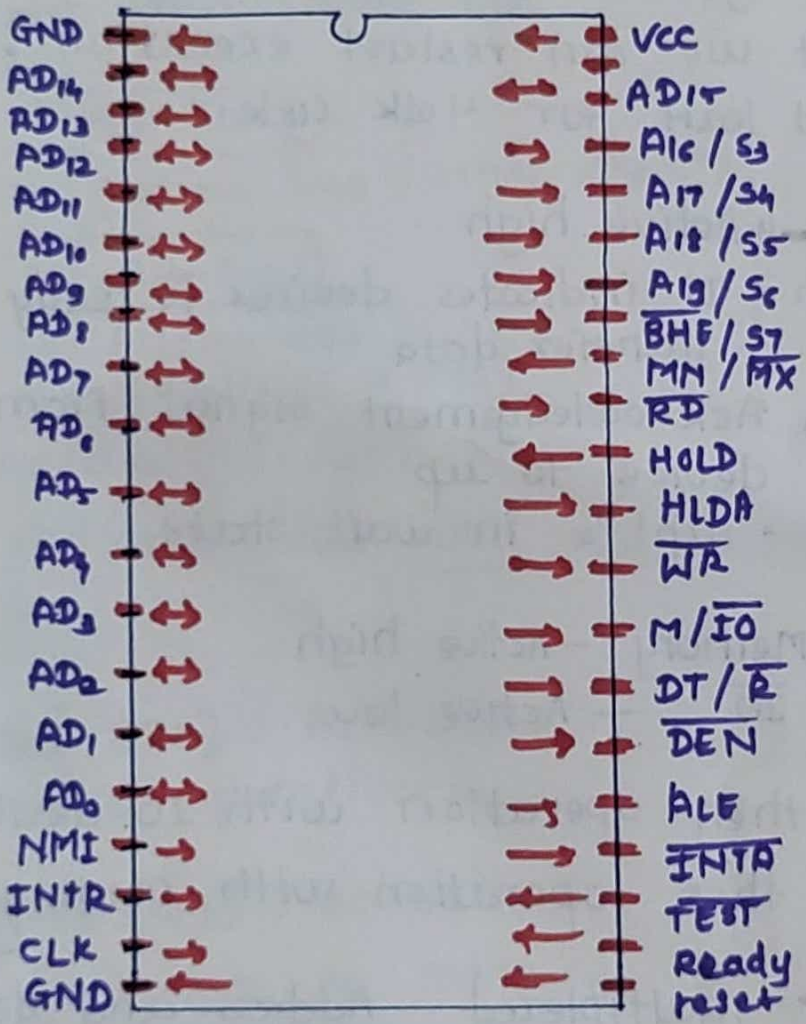
EACH segment reg stores upper 16-bits of starting address of each corresponding segments.



logical address : combination of base reg + index reg.

16 bits — Effective address : base reg + index reg + offset

R. Pin discription :



(Pin) If there is bar then it is active low

(Pin) If —11— no bar —11— active high

← output
↔ bidirectional
→ input

(i) **GND** – 2 ground: pins apply ground signal

(ii) **Vcc** – +5V is applied (power supply signal)

(iii) **Clk signal (19)** – provides timing to processor operation

33% duty cycle

5 - 8 - 10 MHz frequency.

(iv) **RESET (21)** – Active high.
- System reset (set all to 0)
- by applying it we can restart execution.
Must active at least for 4 clk cycle.

(v) **Ready (22)** – Active high.
- when high = It indicates devices is ready to transfer data.
- Acknowledgement signal from slower device to up
- when low - up is in wait state.

(vi) **M/$\overline{IO}$** – Memory – Active high
$\overline{IO}$ – Active low

$\overline{IO}/M = 0$, then operation with IO devices
$\overline{IO}/M = 1$, then operation with memory.

(vii) **$AD_0 - AD_{15}$** – multiplexed Address and data bus.
In 1st clock cycle = carries address
remaining — 11 — = carries data

$AD_0 - AD_7$ = lower data byte } 16-bit
$AD_8 - AD_{15}$ = higher —11— }

(viii) **$A_{16} - A_{19}$** / – remaning 4 bits carried out by A16 - A19 bus.

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डॉ.तुषार पी.झांब
M.B.B.S., D.C

R. ix) ALE : Min mode

↳ Address latch Enable pin.

ALE Pin → octal latch 8282 (3 latches)

A0-A15
Address bus (carries 16-bits)

A16-A19
Address bus (carries 4-bits)

} this 20 bit address is store in octal latc

↳ connected to latch

↳ It indicates that valid address is available.

x) Read (32) : Active low

→ read operation

Max mode xi) Write (29) : Active low

It write to memory or device depending upon $M/\overline{IO}$ signal

xii) $\overline{DEN}$ (26) Max mode :

↳ Data Enable signal.
↳ used to enable transceiver
↳ used to seprate data from address / data bus
↳ Active low.

up → 8286 octal → memory

Bus transceiver (Buffer IC's)

12) $DT/\overline{R}$ (27)

- Data transfer / Receive signal
- It decides direction of data flow

$DT/\overline{R} \rightarrow 1 \rightarrow$ transmit data

$DT/\overline{R} \rightarrow 0 \rightarrow$ Recieves. data

13) **INTR** (18) : Interrupt request signal
- active high

14) **NMI** (17) : Non-maskable interrupt (we can't disable)
- Active high

15) **$\overline{INTA}$** (Min) : interrupt acknowledge signal.
- Active
- Indicates that up is ready for executing interrupt.

16) **HOLD** (Min) : when DMA controller needs bystem buses control it send request 1 to up.

HLDA (Min)

As soon as up receives 1 as Hold then it sends HLDA signal as 1 to DMA for accessing control of buses.
- Hold acknowldegement

17) **$\overline{RQ}/\overline{GT_1}$ and $\overline{RQ}/\overline{GT_0}$ (Max) :**

- Request / Grant pins :
- when other processor wants control of sys. buses.

$\overline{RQ}/\overline{GT_0} = 0 \leftarrow$ Recieving then it will send control of buse

$\overline{RQ}/\overline{GT_0} = 0 \rightarrow$ sends that take control of buses

R. $\overline{RQ}/\overline{GT_0}$ has high priority than $\overline{RQ}/\overline{GT_1}$

18) **LOCK (Max):**
Active low,
It indicates that other processor should not ask cpu to leave the sys. bus.
↓
because in that case up in not condition for releasing sys. buses.

19) **TEST** : Active low
↳ If test pin low then execution continous else up in wait state.
↳ checks status of maths co-processor. 8087

20) **QS1 & QS0 = (Max)**
(only check status of queue

QS_0	QS_1	
0	0	No operation
0	1	1 byte opcode
1	0	Empty
1	1	Subsequent byte from queue

$\overline{S0}, \overline{S1}, \overline{S2}$ (Max) :

- Indicates operation being done by up.
- Info is required by bus controller 8288 to generated memory & I/O control.

$\overline{S0}$	$\overline{S1}$	$\overline{S2}$	
0	0	0	INTA
0	0	1	I/O Read
0	1	0	I/O write
0	1	1	Halt
1	0	0	opcode fetch
1	0	1	memory read
1	1	0	—11— write
1	1	1	Passive

MN / $\overline{MAX}$

- Pins 24 to 31 are two set one set works in min mode & another in max mode.
- 8086 works in two mode < Max / Min

MN/$\overline{MX}$ = 1 then works in min mode

MN/$\overline{MX}$ = 0 then works in max mode

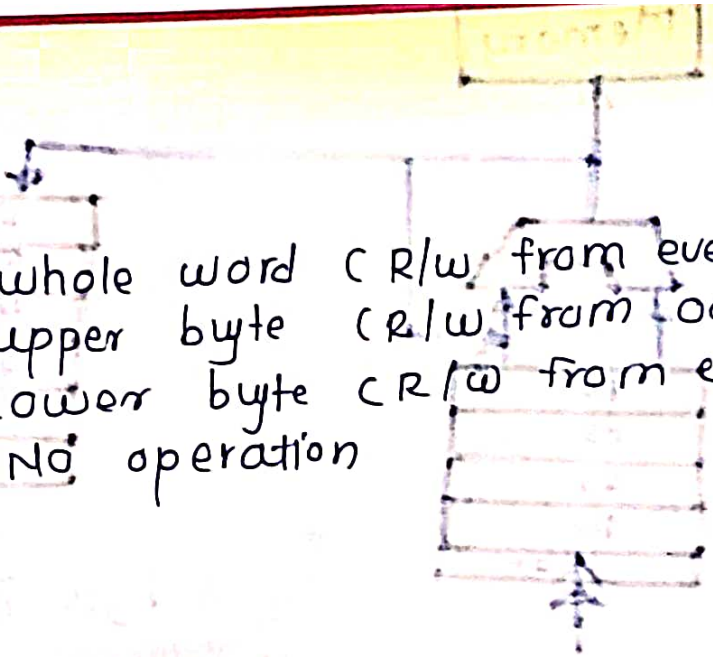
$S6, S5, S4, S3$ — S5 (contain IF value)

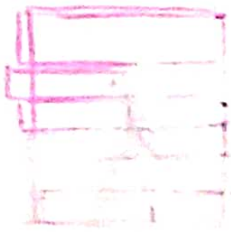
Tells which segment is used

S_4	S_3	
0	0	Alternate data (ES)
0	1	SS
1	0	CS
1	1	DS

R. BHE / S7

BHE	A0 (S7)	
0	0	whole word (R/W from even address)
0	1	upper byte (R/W from odd -11-)
1	0	lower byte (R/W from even -11-)
1	1	No operation

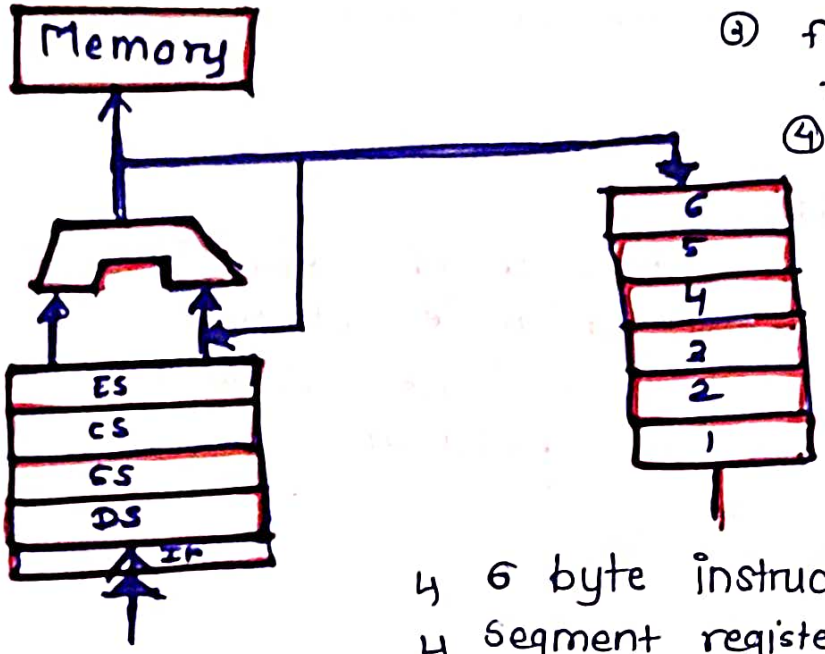




Architecture of 8086 :

① BIU (Bus interface Unit)
② EU (Execution unit)

BUS Interface Unit (BIU) :



Funtions BIU

① Handles transaction of data/address on buses for EU
② It sends address
③ fetches instruction from memory
④ R/W to memory or I/O ports.

queue
⑤ transfer instruction bytes to queue.

- 6 byte instruction queue
- Segment register (CS, DS, SS, ES)
- Instruction pointer (IP)
- Address summing block (Σ)

BIU : For implimenting pipeling BIU uses-

Instruction queue { Instruction stream queue..
(As this queue prefetch up to 6 bytes of instruction. code)

whenever, 2 bytes of queue are getting free then and then only BIU can fetches next instruction into queue (as instructions are of 16-bits or more than it)

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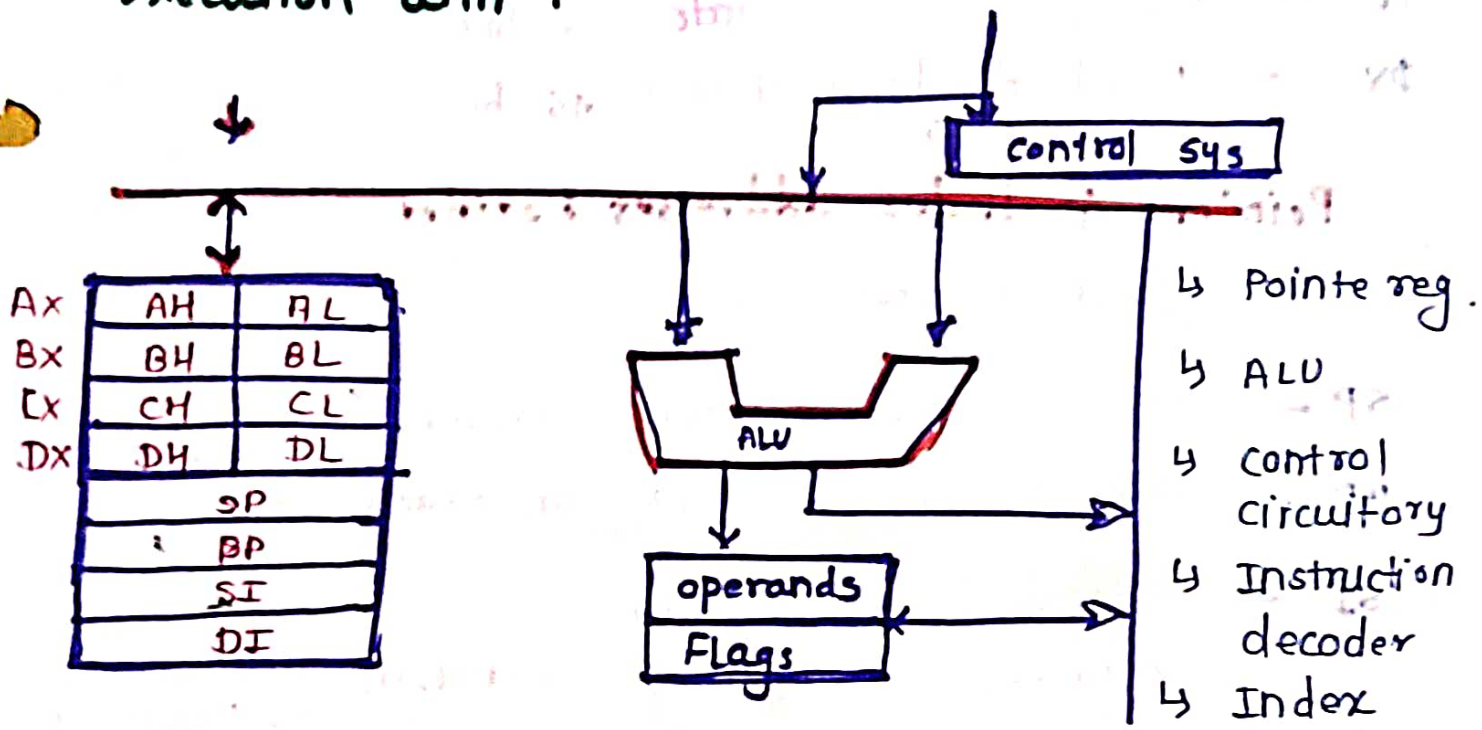
~~BIU~~ EU

R. Execution unit :



Functions :

① Tells BIU from where to fetch data
② decodes instruction fetched by BIU
③ Generates control signals.
④ Executes instructions from queue.

AX - Accumulator
BX - Base
CX - count
DX - data reg.
} Registers

SP — stack pointer
BP — Base pointer
} pointer

SI - Source index
DI - destination index
} Index register.

General Purpose Register.

AX – Accumulator [word multiply / divide] 16-bit
AL – 8-bit (Byte multiply / divide)
HL – 8-bit (byte multiply / divide)
BX – Stores address info 16-bit
CX – String operation / loops 16-bit
CL – Variable. shift rotate 8-bit
DX – Word divide/ multiply 16-bit

Pointer & index ~~addresses~~ Register

keeps offset addresses.

SP – use to access stack segment
BP – use to access data on stack.
SI – Source index register required for string operation.
DI – Destination index reg. required for string operation.

used for data access-ment from array.

Flag register:

16-bit
9 active flags
7 undefined (U)
③ control flags.
⑥ Status/ conditions