ROLL NO. _____

THEORY EXAMINATION

Question Paper

Month and Year of the Examination: **MAY-2019**

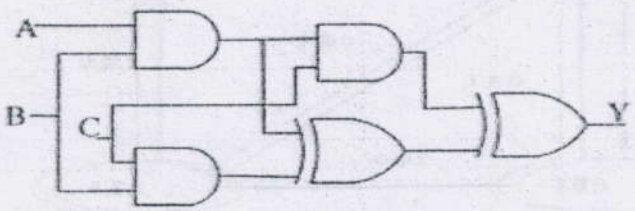
Programme: **B.Tech** Semester: **2nd**

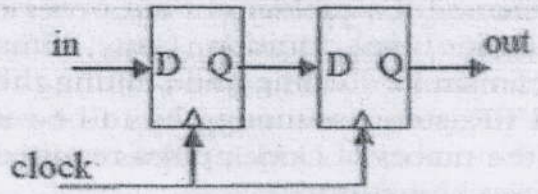
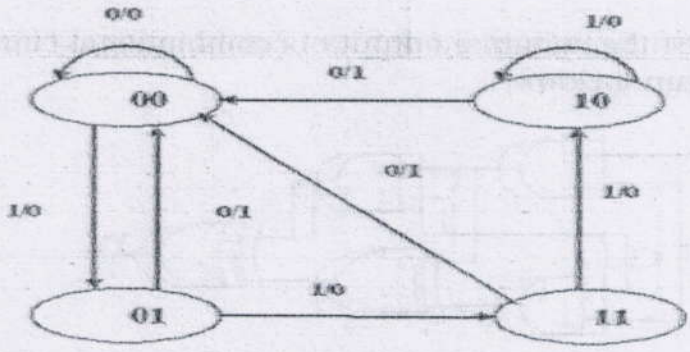
Subject: **Digital System Design.** Course No: **CSPC-10**

Total number of questions given: **6** Maximum Marks: **50**

Number of Questions to be Attempted: **5** Time allowed: **3 hrs**

Note: Assume suitably and state, additional data required, if any. For the better understanding of the answers draw suitable diagram, wherever necessary.

1. (a)	The message below coded in the 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each word. 1001001, 0111001	**06 Marks**
(b)	Reduce the following expressions to their simplest forms using laws of Boolean Algebra. At each step, state the law used for simplification. i) $f1(A, B, C) = \overline{(A + \overline{BC})}(A\bar{B} + ABC)$ ii) $f2(A, B, C, D) = A+B[AC+(B+\bar{C})D]$	**04 Marks**
2. (a)	How can we overcome the problem of data over-riding in the registers for specific time duration (say, 25msec)? Also, suggest the mechanism for loading and shifting the bits 1011 in the PISO Shift Register, assuming bits to be zero initially. What would be the number of clock pulses required to receive all the bits in a given bit pattern?	**05 Marks**
(b)	Using the Quine-McCluskey Method of tabular reduction, minimize the given combinational single output function $f(W, X, Y, Z) = \sum m(0,1,5,7,8,10,14,15)$. Also, identify an Essential Prime Implicants for the given function.	**05 Marks**
3 (a)	What would be the minimized output of combinational circuit given in the figure below? 	**04 Marks**

(b)	Why do we need Priority encoders? Draw the truth table and minimized expressions for Decimal-to-BCD Priority Encoder, while considering inputs and outputs to be active-low signal.	06 Marks
4 (a)	In a certain application, four inputs A, B, C, D (both true and complement forms available) are fed to logic circuit, producing an output F which operates a relay. The relay turns on when F(ABCD)=1 for the following states of the inputs (ABCD): '0000','0010','0101','0110','1101' and '1110'. States '1000' and '1001' do not occur, and for the remaining states, the relay is off. Minimize F with the help of a Karnaugh Map and realize it using a minimum number of 3-input NAND Gates.	05 Marks
(b)	Design and implement a 4-bit BCD to Excess-3 code converter. Explain the steps involved in performing the conversion.	05 Marks
5 (a)	How can we draw a ripple counter other that MOD-2^n? Illustrate your answer by designing a MOD-14 Ripple Counter using J-K Flip-Flop, suggesting the terminal count for the same.	06 Marks
(b)	Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops.  Draw the state transition diagram depicting all the states and their transitions on some value of "in".	04 Marks
6 (a)	Design the sequential circuit specified by the state diagram below using D-Flip-Flops 	06 Marks
(b)	Use a Multiplexer to implement the logic function F=A⊕B⊕C.	04 Marks