comp – 5

ROLL NO. _____

THEORY EXAMINATION

Question Paper

Month and Year of the Examination: **DEC-2019**

Programme: **B.Tech** Semester: **Re-Appear**

Subject: **Digital System Design.** Course No: **CSPC-10**

Total number of questions given: **5** Maximum Marks: **50**

Number of Questions to be Attempted: **5** Time allowed: **3 hrs**

Total Number of Pages used: **2**

Note: Assume suitably and state, additional data required, if any. For the better understanding of the answers draw suitable diagram, wherever necessary.

1. (a)	Given F=A(B+C)+D. Obtain i) minimal SOP ii) minimal POS iii) canonical SOP iv) canonical POS.	**05 Marks**
(b)	Implement 8×1 Multiplexer using 4×1 Multiplexer. Elaborate the steps involved.	**05 Marks**
2. (a)	If the Hamming code sequence 1100110 is transmitted and due to error in one position, is received as 1110110, locate the position of the error bit using parity checks and give the method for obtaining the correct sequence.	**05 Marks**
(b)	Solve the function F(ABCD) = ∑m (0, 1, 2, 3, 5, 7, 8, 10, 14, 15) using Q-M method. Identify an Essential Prime Implicants, if any.	**05 Marks**
3 (a)	A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations A is False, B is True A is False, C is True A, B, C are False A, B, C are True (i) Write the Truth table for F. Use the convention True=1 and False = 0. (ii) Draw logic circuit using minimum number of 2-input NAND Gates.	**05 Marks**
(b)	Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram	**05 Marks**
4. (a)	Derive and draw logic circuit for BCD to Excess-3 Code converter.	**05 Marks**

(b) Obtain the reduced state table for the following state table of an asynchronous sequential circuit. **05 Marks**

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
a	d	b	0	0
b	e	a	0	0
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

5 (a) Design 2-bit magnitude comparator and draw its logic circuit. **05 Marks**

(b) With neat logic diagram and timing diagram, explain the operation of a 3-bit ripple up/down counter. **05 Marks**

OR

5 (a) Why do we need the concept of Look-Ahead Carry? Draw a 4-bit adder with look-ahead carry **05 Marks**

(b) Explain SIPO and PISO shift registers with relevant logic diagrams. **05 Marks**