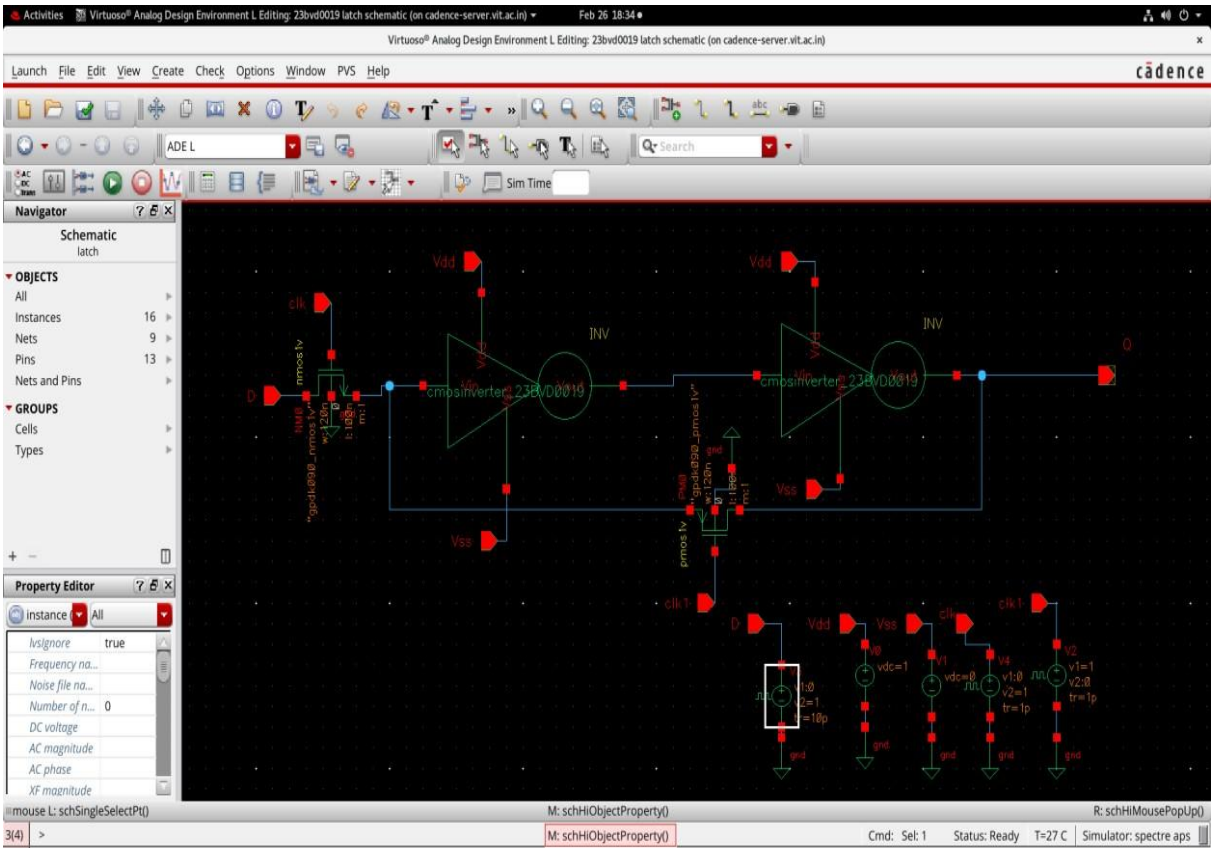
IMPLEMENTATION OF D-LATCH, D-FLIP FLOP, SISO REGISTER, AND D TO T FLIP FLOP USING CADENCE VIRTUOSO

D-LATCH

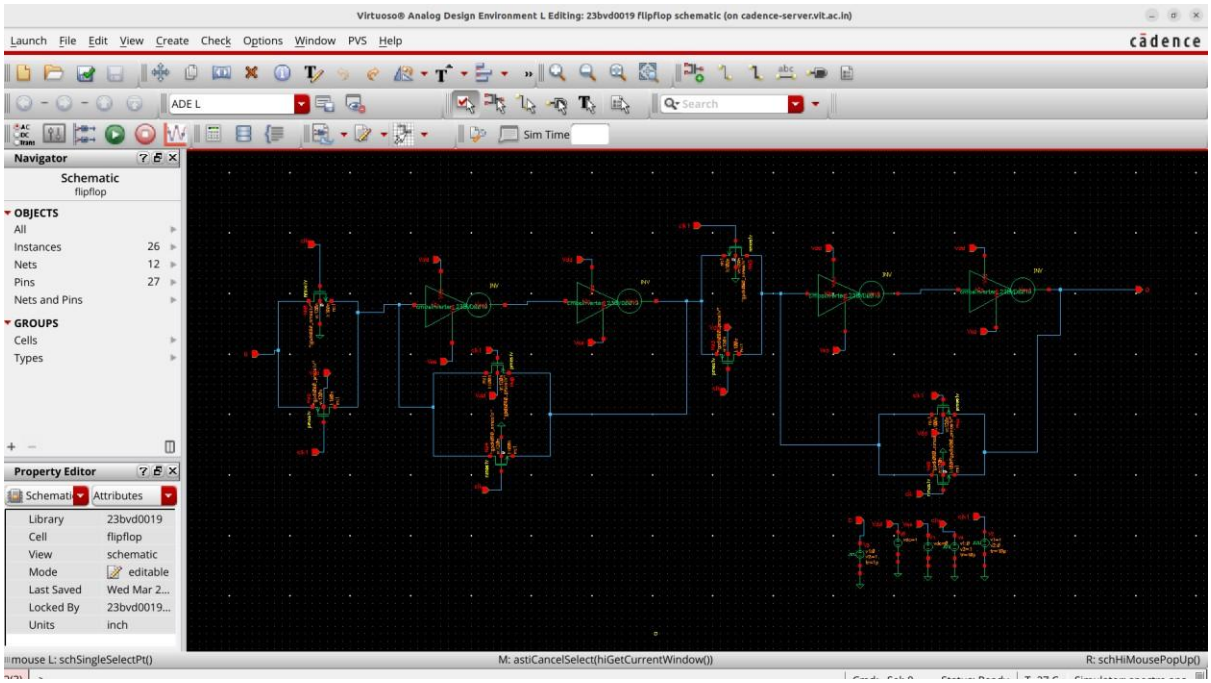
Circuit Diagram:



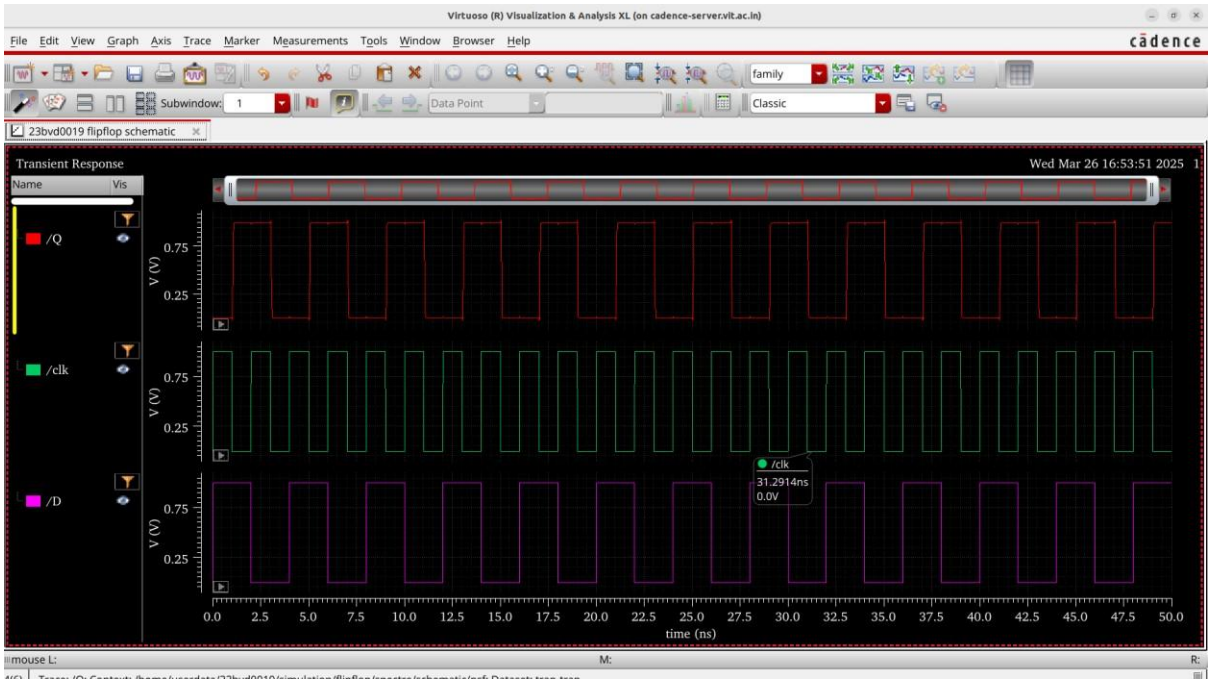
Output Waveform:


Activities
Virtuoso (R) Visualization & Analysis XL (on cadence-server.vit.ac.in)
Feb 26 18:34
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindow: 1
Data Point
Classic
23bvd0019 latch schematic
Transient Response
Wed Feb 26 18:38:38
Name
Vis
/clk1
/clk
/Q
/D
V (V)
V (mV)
1.1
-0.1
735.8
-126.9
/Q
15.572ns
219.33mV
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0 14.0 15.0 16.0 17.0 18.0 19.0 20.0
time (ns)
mouse L:
M:
R:
15(26)
Trace: /Q; Context: /home/userdata/23bvd0019/simulation/latch/spectre/schematic/psf; Dataset: tran-tran

D-FLIP FLOP:

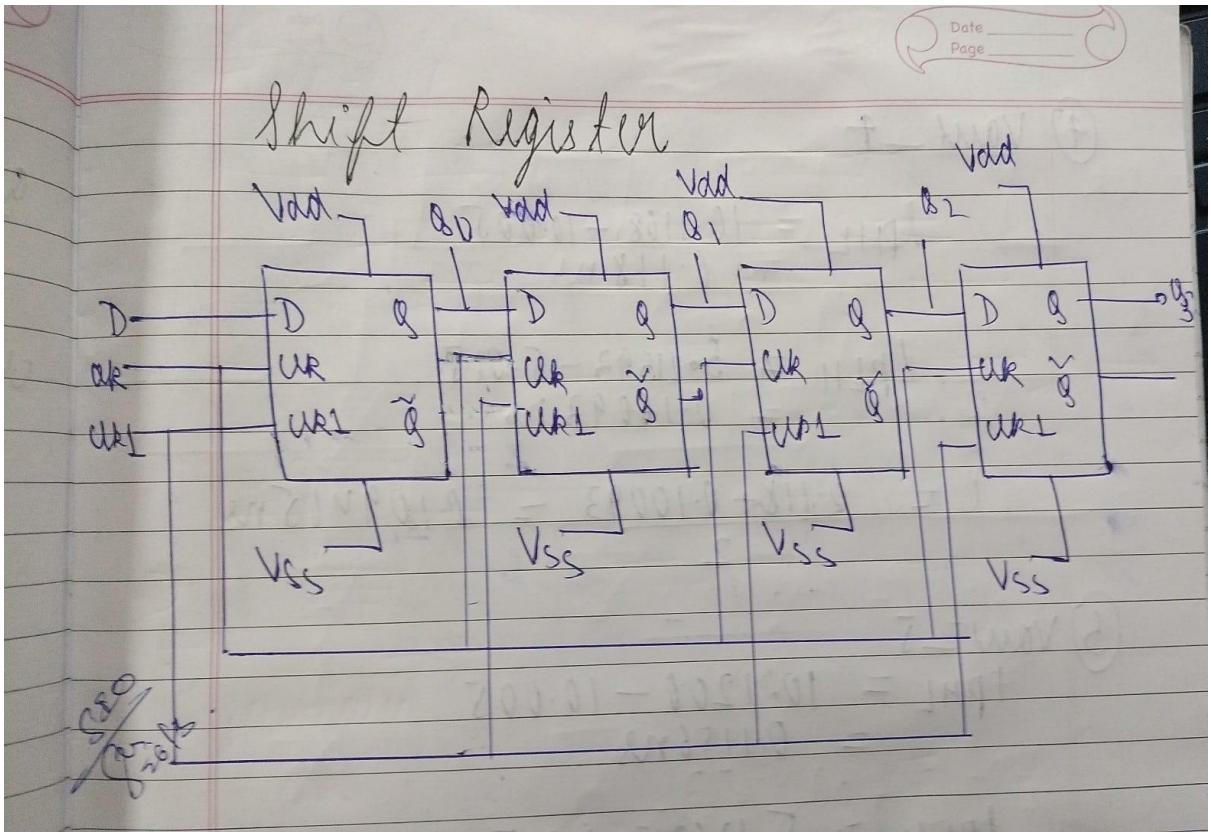


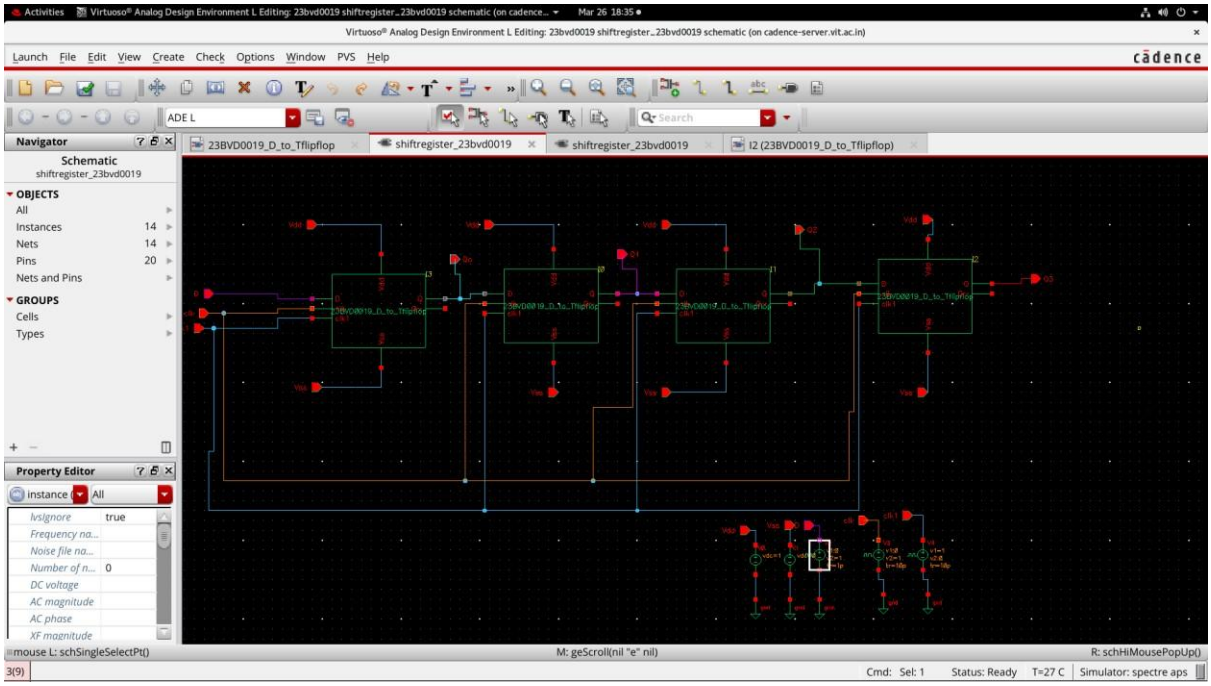
Output Waveform:



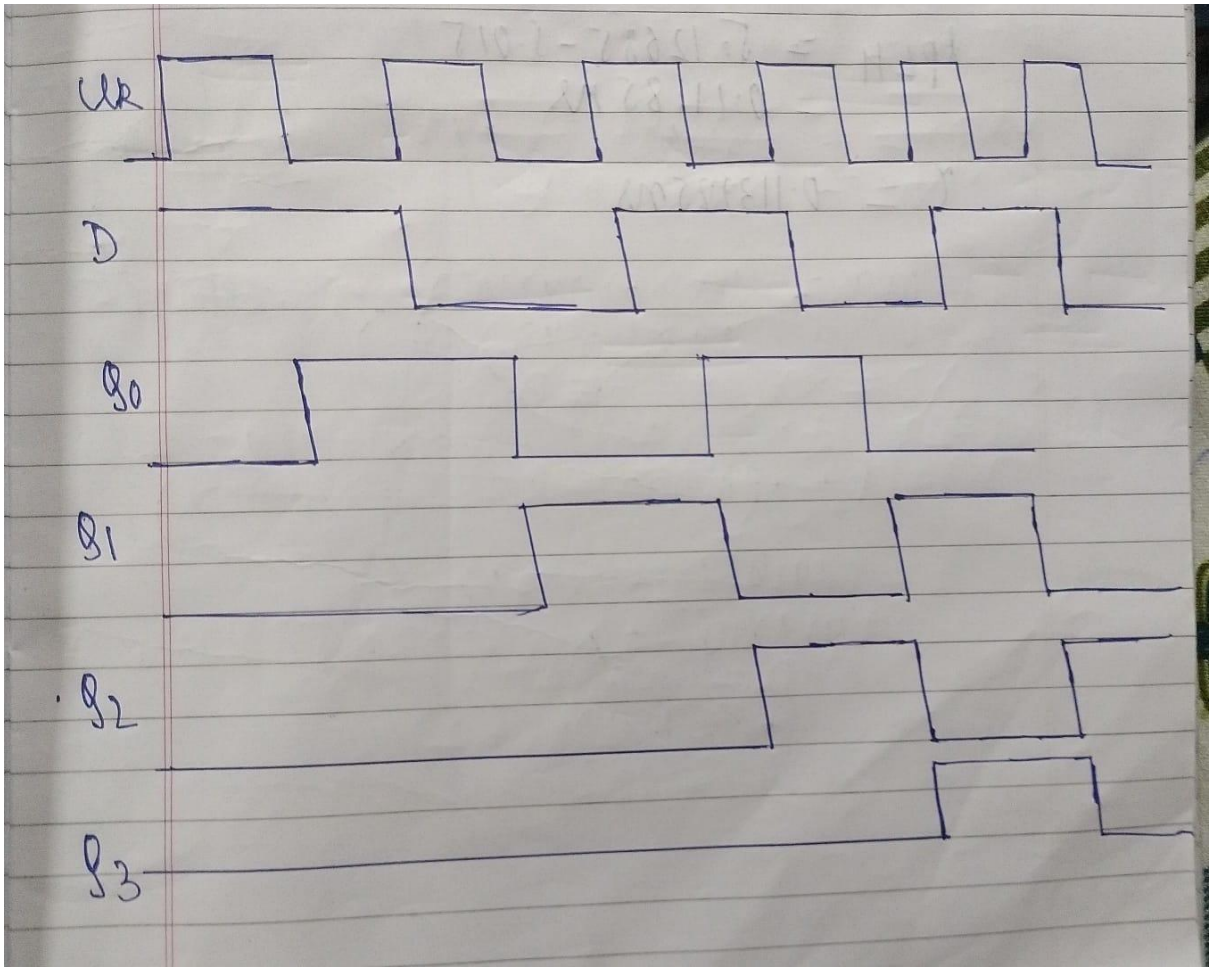
SERIES IN SERIES OUT:

Schematic:

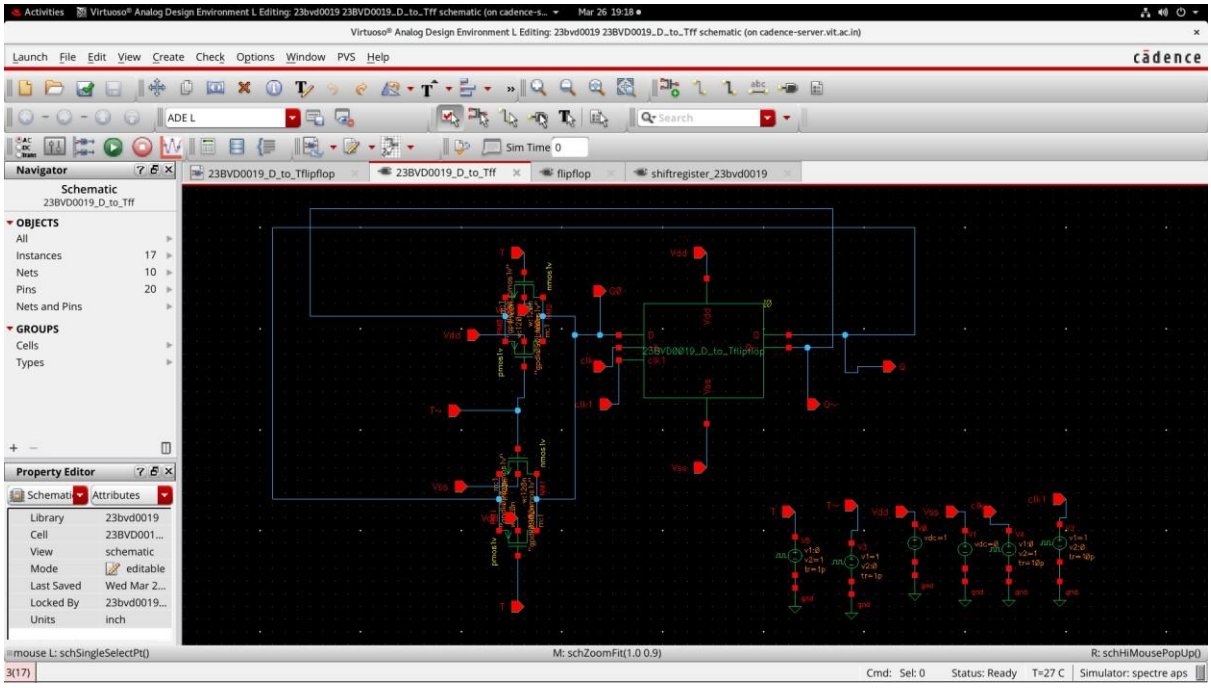




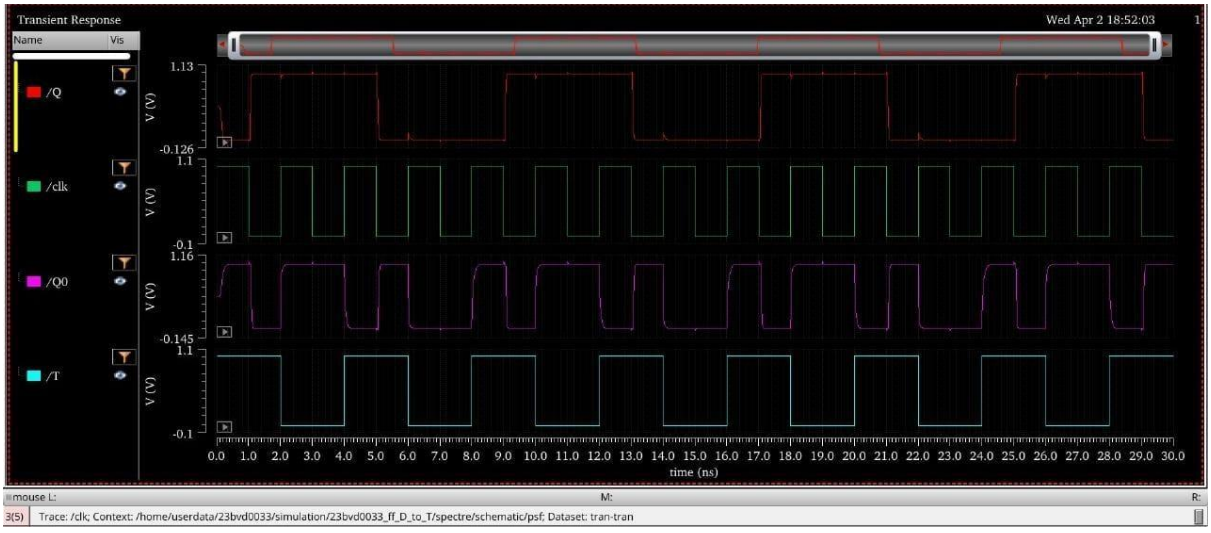
Output Waveform :

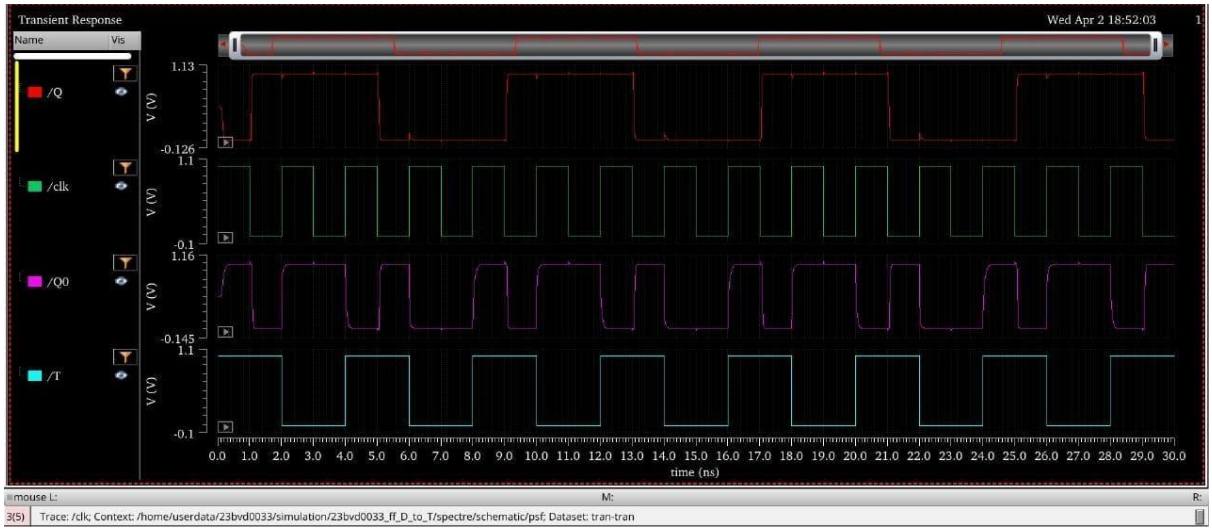


D TO T – FLIP FLOP Schematic:



Waveform Generation:




Transient Response
Wed Apr 2 18:52:03
1
Name
Vis
/Q
/clk
/Q0
/T
1.13
-0.126
1.1
-0.1
1.16
-0.145
1.1
-0.1
V (V)
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0 14.0 15.0 16.0 17.0 18.0 19.0 20.0 21.0 22.0 23.0 24.0 25.0 26.0 27.0 28.0 29.0 30.0
time (ns)
mouse L:
M:
R:
3(5)
Trace: /clk; Context: /home/userdata/23bvd0033/simulation/23bvd0033_ff_D_to_T/spectre/schematic/psf; Dataset: tran-tran