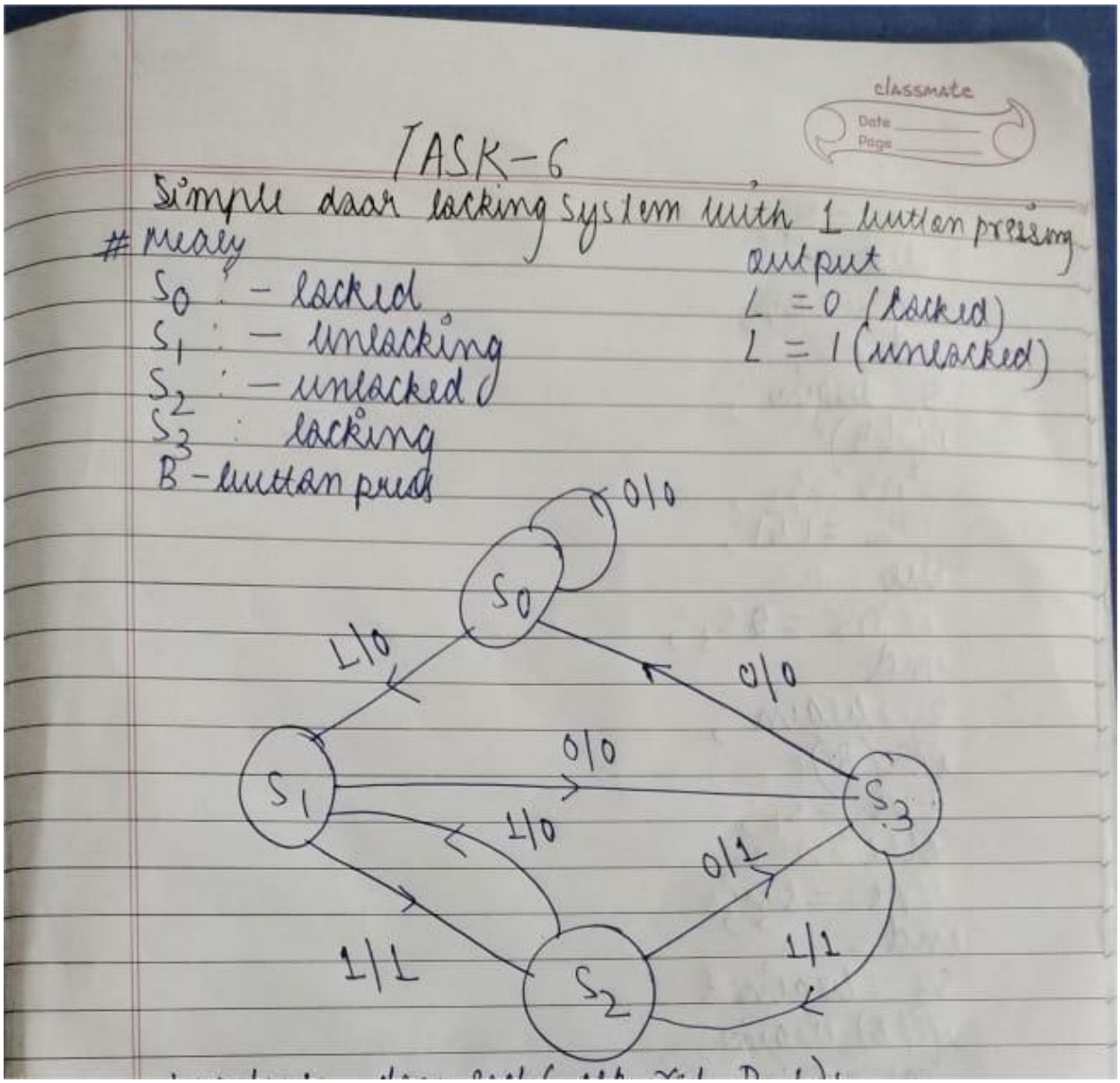
PROJECT ON FINITE STATE MACHINE

Implementation of A simple Door clock system

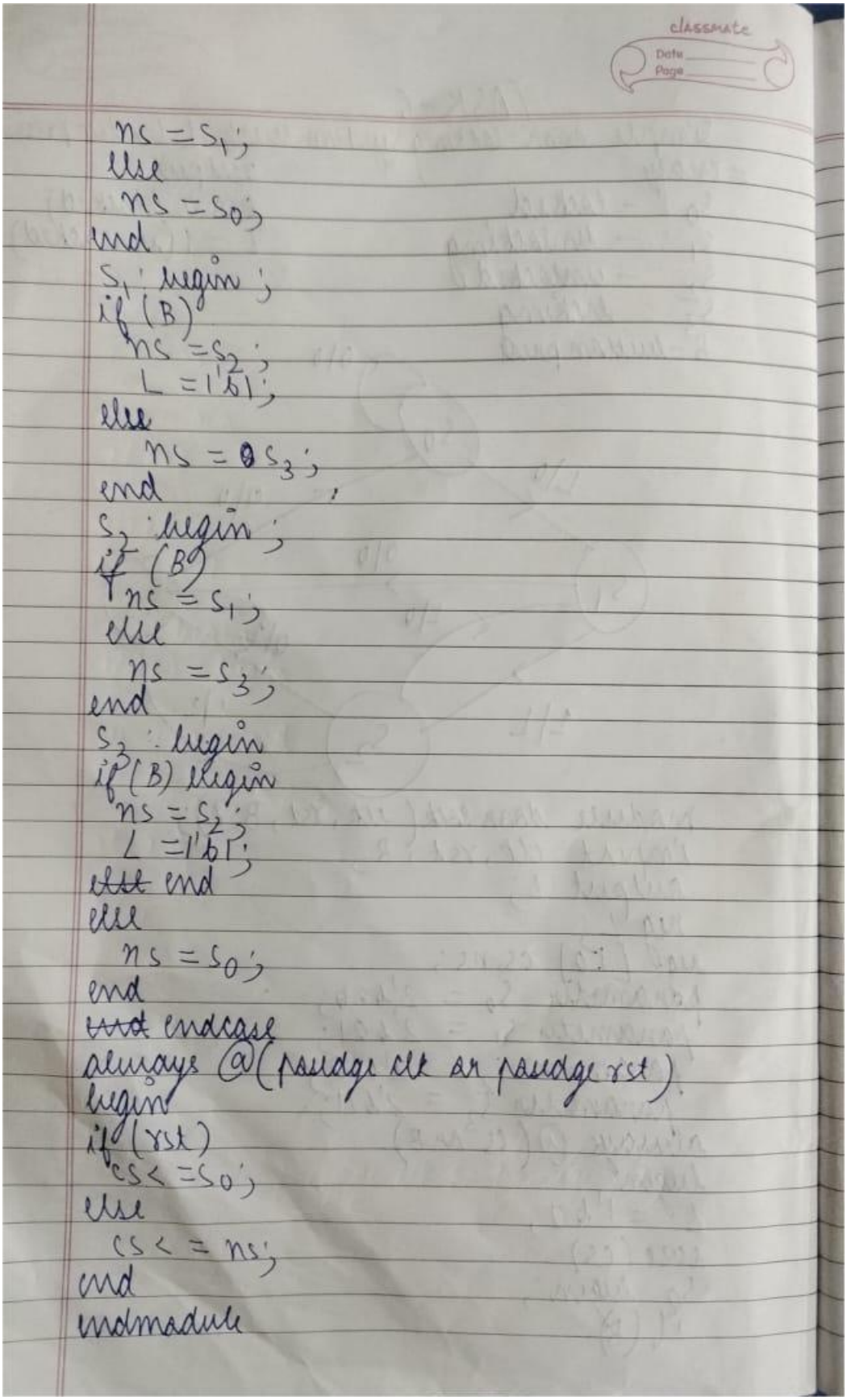
IMPLEMENTED USING MODELSIM AND FPGA

Machine on FPGA State diagram**:**



Verilog Code:

```
module door lock( clk, rst, B, L);
input clk, rst; B;
output L;
reg L;
reg [1:0] cs, ns;
parameter S0 = 2'b00;
parameter S1 = 2'b01;
parameter S2 = 2'b10;
parameter S3 = 2'b11;
always @(cs or B)
begin
L = 1'b0;
case (cs)
S0: begin;
if (B)
```


ns = S1;
else
ns = S0;
end
S1: begin;
if (B)
ns = S2;
L = 1'b1;
else
ns = S3;
end
S2: begin;
if (B)
ns = S1;
else
ns = S3;
end
S2: begin
if (B) begin
ns = S2;
L = 1'b1;
end
else
ns = S0;
end
endcase
always @(posedge clk or posedge rst)
begin
if (rst)
cs <= S0;
else
cs <= ns;
end
endmodule

Output:

Pin configuration:

LEDG [0]-L

Switch [0]-B

Switch [1]- rst

Key [0]-clk

Input:

B=101

State transition:

S0 –S1—S3—S2

L=1 (door unlock)

FPGA Implementation: