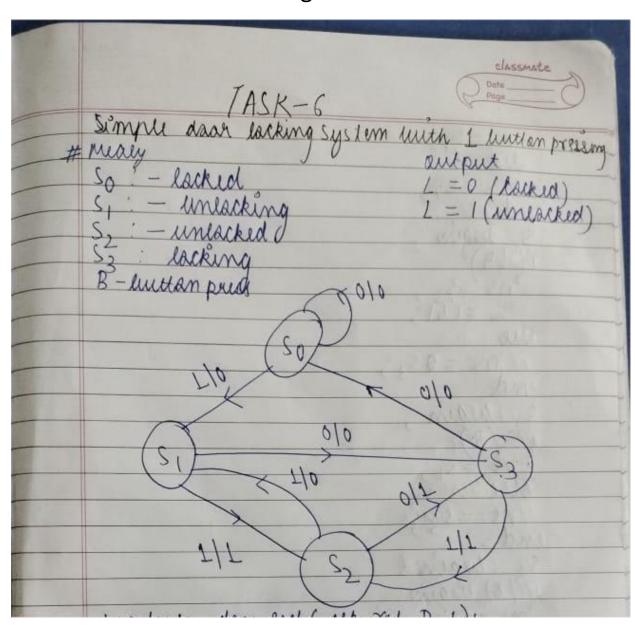
PROJECT ON FINITE STATE MACHINE

Implementation of A simple Door clock system

IMPLEMENTED USING MODELSIM AND FPGA

Machine on FPGA State diagram:



Verilog Code:

madule doan lack (alk, rst, B, L);

injust clk, rst, B;

output L;

rig L;

rig L;

reg [1:0] cs, ns;

parameter So = 2!600;

parameter S1 = 2!601;

parameter S2 = 2!610;

parameter S2 = 2'611;

always (a) (cs ar B)

lugin

L = 1'60;

case (cs)

so: lugin;

	Classmate Doth Page
nc = s,:	
llse	MANYA.
001	MINEY - TORKER
ms = so)	Acrida Call
S, ' hearn ',	In heat rateous -
il (B)	partition of
nc=c.	S-hubbar and
L=121?	
else	
MS = 050;	
end 3,	9/2/
s. lugin	
it (B)	1/0
The = s.	(3)
une 1	41-70
ns = s,	
end 3)	111
Sz. lugin	2 4 41-
iP(B) lligin	1
ns=s,	a Nacanah suhaw
1=1/67:	I day all daylors
elet end	1 Juglin
elle	The state of the s
ns = 50'	12425 (691) Vari
ena	ale - 2 standal
und endrase	Language S = 240
almays (a) psuda	i all ar paudge ret).
lugin	AC = Planting
1 (xx)	afosour (D) (C) AND
es<=so;	I THE SEAL THE PROPERTY.
CASE	rd letter
(S < = NS;	(35) 1111
Md	to have
molmadule	Xa I Pa

Output:

Pin configuration:

LEDG [0]-L

Switch [0]-B

Switch [1]- rst

Key [0]-clk

Input:

B=101

State transition:

S0-S1-S3-S2

L=1 (door unlock)

FPGA Implementation:

