# EW2 PROJECT - 1 Report
## Audio Amplifier

Khyathi Sri Basireddy
*2023102065*
*International Institute of Information Technology*
Hyderabad
khyathisri.basireddy@students.iiit.ac.in

Sanjana Sheela
*2023102027*
*International Institute of Information Technology*
Hyderabad
sanjana.sheela@students.iiit.ac.in

***Abstract*—This project focuses on amplifying audio from a microphone circuit. It includes a pre-amplifier stage to provide a small gain and reduce noise. The gain stage then significantly amplifies the signal, followed by a filter stage that ensures only audible frequencies pass through. Finally, a power amplifier stage increases the signal power to drive the speaker effectively, ensuring a clear and noise-free output.**

***Index Terms*—Microphone, Preamp Stage, Gain Stage, Band-Pass Filter, Power Amplifier**

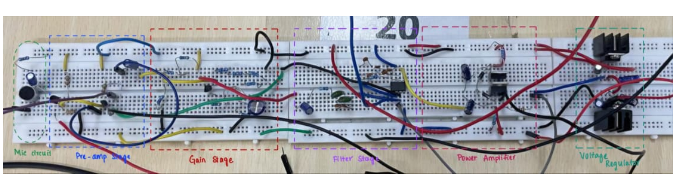
## I. Introduction

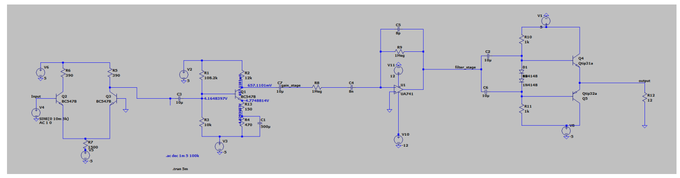
This project focuses on designing a low-power audio amplifier with a 0–5V supply and an input signal range of 10–20 mV peak-to-peak. The design includes a pre-amplifier for initial signal amplification, a gain stage with a target voltage gain of 500, a band-pass filter for signal integrity, and a Class AB power amplifier for efficiency and low distortion. Key performance metrics such as total harmonic distortion (THD) and slew rate are analyzed to ensure high-fidelity audio output. This paper presents the design, implementation, and performance evaluation of the amplifier.

## II. Specifications

- Supply Voltage: +5V, -5V
- Input Voltage Range (VPP): 10mV - 20mV
- Gain: $G_1 \times G_2 \geq 500$
- $G_1$ = Gain of Preamp Stage
- $G_2$ = Gain of Gain Stage
- Frequency Range: 20Hz to 20KHz (Audible Range)
- Power: 1.5W
- Note: The Filter Stage and the Power Amp Stage do not provide any gain.

FINAL CIRCUITS



The input with which all the results in the entire project are projected is 20mV peak to peak.

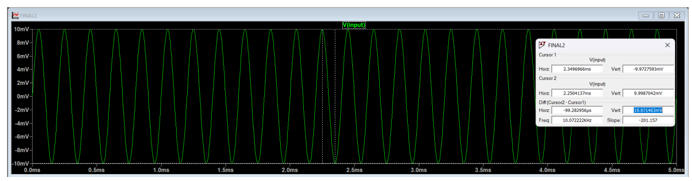


Fig. 1. Input to the circuit with 20mV Peak-to-Peak

## III. Mic Circuit

We will need a simple microphone circuit to take the input from the user. This specific circuit is designed to interface a mic with an amplifier. The circuit uses a 10 Kohm resistor (R1) to provide biasing voltage to the microphone from a 5V supply. The mic converts sound waves into an electrical signal, which is then coupled through a 1μF capacitor (C1) to block DC components while allowing the AC audio signal to pass to the amplifier.

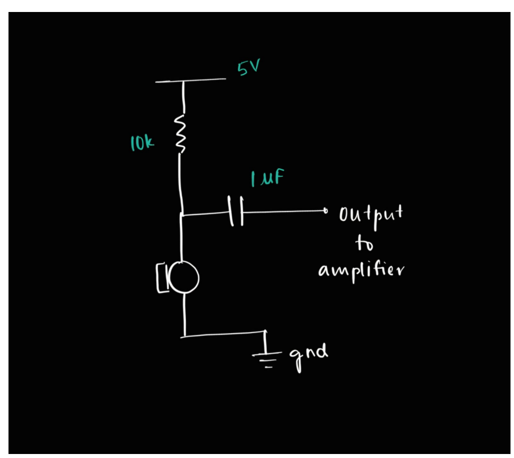



Fig. 2. Mic Circuit


Fig. 3. Mic Circuit - Hardware

## IV. Pre-Amplifier Stage

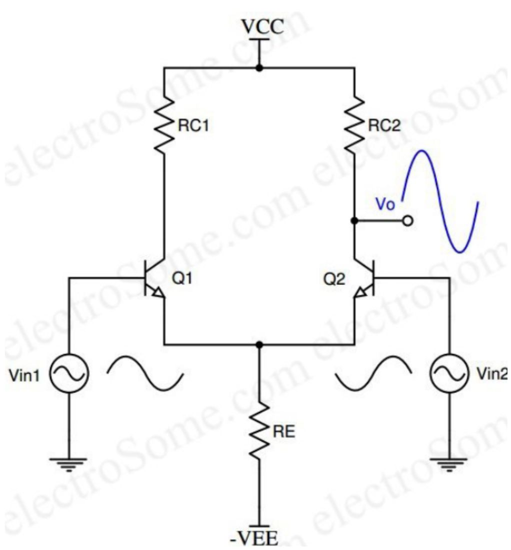



Fig. 4. Pre-amp stage circuit

The pre-amplifier is the first amplification stage in the circuit. It takes a weak electrical signal and boosts it to a level suitable for further processing.

In this stage, we aim at getting a gain of 10. The parameters of the circuit are set according to that.

The pre-amplifier is a differential amplifier designed to amplify the difference between two input signals while maintaining a low common-mode gain to filter noise. That is, the Common Mode gain is set below 0, to reduce the noise in the circuit. Then, using the Differential gain, we amplify the input to achieve a gain of 10.

The common-emitter differential amplifier can be used as it has a high input and low output impedence, with good noise performance, This is the reason to use the differential amplifier as a pre-amp

Even with a single-ended output, a differential amplifier cancels most common-mode noise due to its symmetrical design and current source, reducing noise compared to a standard single-ended amplifier.

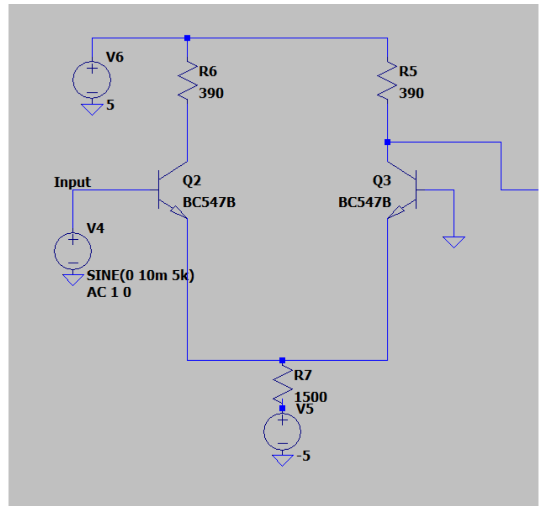



Fig. 5. Pre-Amplifier Stage Circuit

### *1. Differential Mode Gain ($A_d$)*

$$V_{in1} - V_{\pi 1} = V_p = V_{in2} - V_{\pi 2}$$

$$V_{in1} - V_{in2} = V_{id}$$

$$V_{in1} - V_{in2}$$

$$g_{m1} V_{\pi 1} + g_{m2} V_{\pi 2} + \frac{V_{\pi 1}}{r_{\pi 1}} + \frac{V_{\pi 2}}{r_{\pi 2}} = \frac{V_p}{R_e}$$

$$\left(g_m + \frac{1}{r_\pi}\right)(V_{\pi 1} + V_{\pi 2}) = \frac{V_p}{R_e}$$

$$\left(g_m + \frac{1}{r_\pi}\right)(V_{in1} - V_p + V_{in2} - V_p) = \frac{V_p}{R_e}$$

$$(-2V_p)\left(g_m + \frac{1}{r_\pi}\right) = \frac{V_p}{R_e}$$

$$V_{in1} - V_{in2} = V_{\pi 1} - V_{\pi 2}$$

$$V_{o1} - V_{o2} = -g_m V_{\pi 1} R_C + g_m V_{\pi 2} R_C$$

$$= -g_m R_C (V_{\pi 1} - V_{\pi 2})$$

$$= -g_m R_C (V_{in1} - V_{in2})$$

$$\frac{V_{out}}{V_{in}} = -g_m R_C$$

*2. Common-mode gain ($A_c$)*

For common-mode input:

$$V_1 = V_2 = V_{in,cm}$$

Since both bases move together, the emitter voltage follows:

$$V_E = V_{in,cm}$$

The small-signal resistance looking into the emitter is as follows:

$$2(r_e + R_E)$$

Emitter current:

$$i_E = \frac{V_E}{2(r_e + R_E)}$$

Using:

$$V_{out} = -g_m R_C V_E$$

Substituting $V_E$:

$$V_{out} = -g_m R_C \cdot \frac{V_{in,cm}}{1 + g_m R_E}$$

Thus, the Common-Mode gain is:

$$A_c = -\frac{g_m R_C}{1 + g_m R_E}$$

*3. Calculation of Circuit Parameters*

Assuming the collector current:

$$I_C = 1.5 \text{ mA}$$

Since,

$$I_{EE} = 2 \times I_C = 3 \text{ mA}$$

The voltage gain is given by:

$$\text{Gain} = 10$$

We use the transconductance relation:

$$\text{Gain} = g_m R_C$$

where,

$$g_m = \frac{I_C}{V_T}$$

Given,

$$V_T \approx 26 \text{ mV}$$

$$g_m = \frac{1.5 \text{ mA}}{26 \text{ mV}} = 0.0577 \text{ S}$$

Solving for $R_C$,

$$R_C = \frac{\text{Gain}}{g_m} = \frac{10}{0.0577} \approx 175\,\Omega$$

Since we are taking input only from a voltage source and grounding the other, all resistor values are doubled:

$$R_C \approx 2 \times 175 = 350\,\Omega$$

For the emitter resistance:

$$I_{EE} = \frac{V_{EE} - V_{BE}}{R_E}$$

Solving for $R_E$:

$$R_E = \frac{5 - 0.7}{3 \text{ mA}} = \frac{4.3}{3 \text{ mA}} \approx 1400\,\Omega$$

To achieve the required gain, slight adjustments were made to resistor values.

In the simulation and hardware setup results below, we can see that Pre-amp stage has achieved a gain of 10.

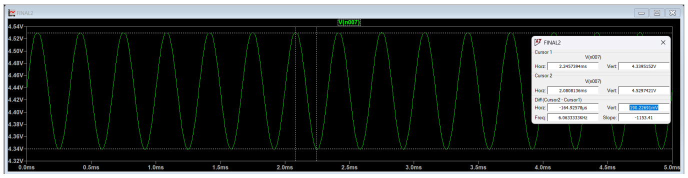


Fig. 6. Output of the Pre-Amp Stage (Input = 19.9mV , Output = 190.22mV)

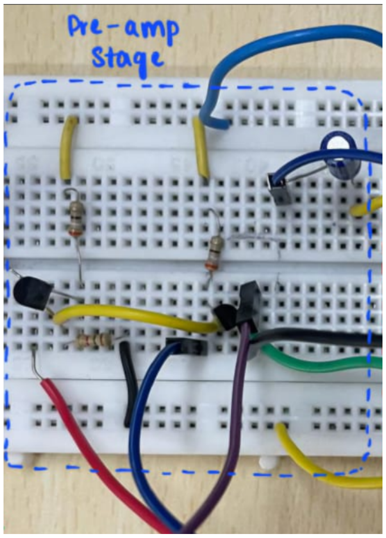



Fig. 7. Pre-Amp Hardware Circuit

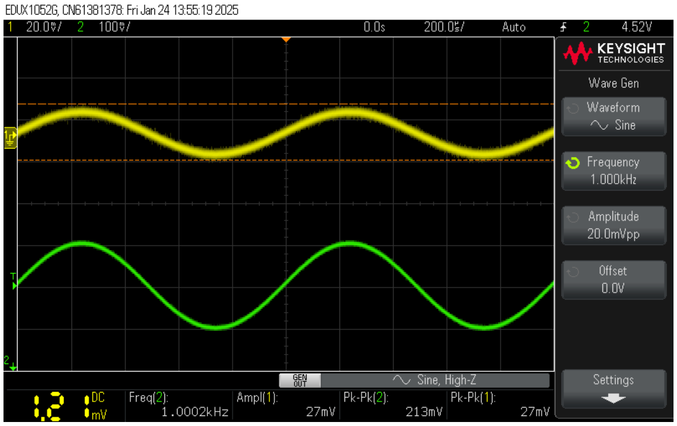



Fig. 8. Hardware Result of Pre-Amp Stage

### 4. CMRR

The ability of the amplifier to minimize common-mode signals while amplifying differential signals is measured by the Common-Mode Rejection Ratio (CMRR).

The CMRR is calculated by supplying a common mode signal to the differential amplifier and measuring common mode gain $A_c$ and by supplying another differential mode signal to the diff amp and measuring the differential gain $A_d$.

Then, the CMRR is found using:

$$CMRR = 20\log\left(\frac{A_d}{A_c}\right)$$

A higher CMRR indicates better rejection of unwanted noise and improved signal accuracy, making differential amplifiers essential in applications like sensor signal processing and communication systems.

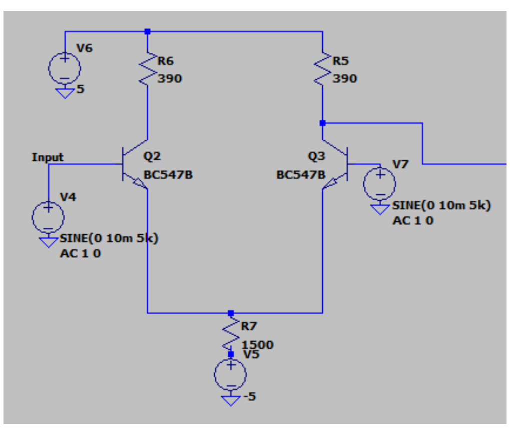



Fig. 9. Commom Mode Stage of Pre-Amp

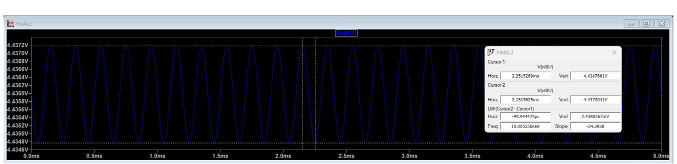


Fig. 10. Output of Commom Mode Signal

The Common Mode Gain, $A_c = \frac{2.44\text{mV}}{20\text{mV}} = 0.122$

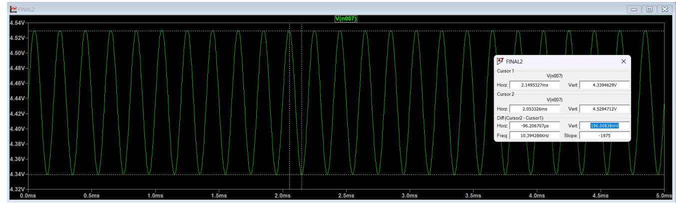


Fig. 11. Output of Differential Signal

The Differential Gain, $A_d = \frac{190\text{mV}}{20\text{mV}} = 9.5$
Hence, CMRR can be calculated as:

$$CMRR = 20\log\left(\frac{A_d}{A_c}\right) = 20\log\left(\frac{9.5}{0.122}\right) = 37.827$$

### 5.Reason why single ended differential amplifier is able to cancel noise

Let's define the input signals:

$$V_1 = V_{sig} + V_{noise} \tag{1}$$

$$V_2 = -V_{sig} + V_{noise} \tag{2}$$

where:

- $V_{sig}$ is the actual signal.
- $V_{noise}$ is the common-mode noise present in both inputs.

A differential amplifier has a differential-mode gain $A_d$, which amplifies the difference between inputs:

$$V_{out,diff} = A_d(V_1 - V_2) \tag{3}$$

Substituting $V_1$ and $V_2$:

$$V_{out,diff} = A_d[(V_{sig} + V_{noise}) - (-V_{sig} + V_{noise})] \tag{4}$$

$$V_{out,diff} = A_d[V_{sig} + V_{noise} + V_{sig} - V_{noise}] \tag{5}$$

$$V_{out,diff} = A_d(2V_{sig}) \tag{6}$$

Since the noise terms cancel out, the differential amplifier completely rejects the common-mode noise.

In a typical differential amplifier circuit, the two output voltages are:

$$V_{out1} = A_dV_{sig} + A_cV_{noise} \tag{7}$$

$$V_{out2} = -A_dV_{sig} + A_cV_{noise} \tag{8}$$

where:

- $A_d$ is the **differential gain**.
- $A_c$ is the **common-mode gain** (ideally very small).

If we take a **single-ended output** (say, $V_{out1}$):

$$V_{out1} = A_dV_{sig} + A_cV_{noise} \tag{9}$$

Even though the common-mode noise is not completely eliminated as in a fully differential output, the circuit still suppresses it because $A_c$ is much smaller than $A_d$ (due to the differential pair design), meaning noise is greatly attenuated.

## V. Gain Stage

The primary function of the gain stage is to amplify the signal after it has been filtered by the pre-amplifier. This stage uses a common-emitter (CE) amplifier configuration to achieve significant gain.

Consider a Common Emitter amplifier where the transistor operates in active mode, with the following assumptions:

- The input signal is applied to the base.
- The emitter is grounded.
- The output is taken from the collector through a load resistor $R_C$.

For small-signal analysis, the transistor is modeled with a transconductance $g_m$, where:

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}}$$

Here, $I_C$ is the collector current, and $V_{BE}$ is the base-emitter voltage. The small signal collector current is given by:

$$i_c = g_m v_{be}$$

where $v_{be}$ is the small-signal base-emitter voltage.

The output voltage $v_{out}$ across the load resistor $R_C$ is given by:

$$v_{out} = -i_c R_C$$

Substituting for $i_c$, we get:

$$v_{out} = -g_m v_{be} R_C$$

### Relationship Between Input and Base-Emitter Voltage

The input voltage $v_{in}$ is applied to the base. Assuming the base current is small, the input voltage $v_{in}$ is related to the base-emitter voltage $v_{be}$ by:

$$v_{in} = v_{be} + i_b R_b$$

where $i_b$ is the base current and $R_b$ is the base resistance. For small-signal analysis, we approximate the base current as:

$$i_b = \frac{v_{in}}{R_b}$$

Thus, the base-emitter voltage is approximately:

$$v_{be} \approx v_{in}$$

### Voltage Gain

The voltage gain $A_v$ of the amplifier is defined as the ratio of the output voltage to the input voltage:

$$A_v = \frac{v_{out}}{v_{in}}$$

Substitute the expression for $v_{out}$ from earlier:

$$A_v = \frac{-g_m v_{be} R_C}{v_{in}}$$

Since $v_{be} \approx v_{in}$, we obtain the final expression for the voltage gain:

$$A_v = -g_m R_C$$

Thus, the voltage gain of the Common Emitter amplifier is:

$$A_v = -g_m R_C$$

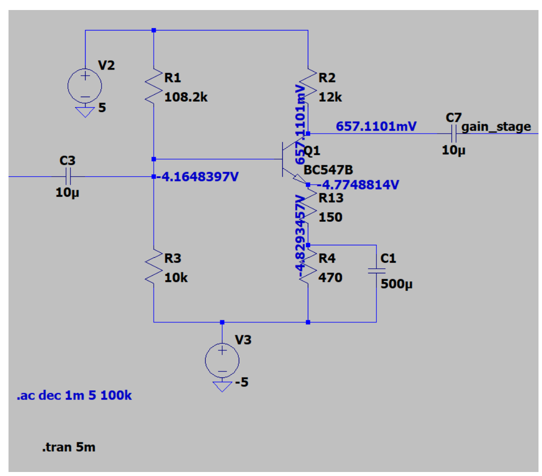



Fig. 12. Gain Stage Circuit

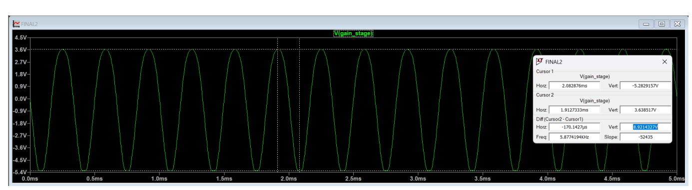


Fig. 13. Output of the Gain Stage (Input = 190.2mV, Output = 8.92V)

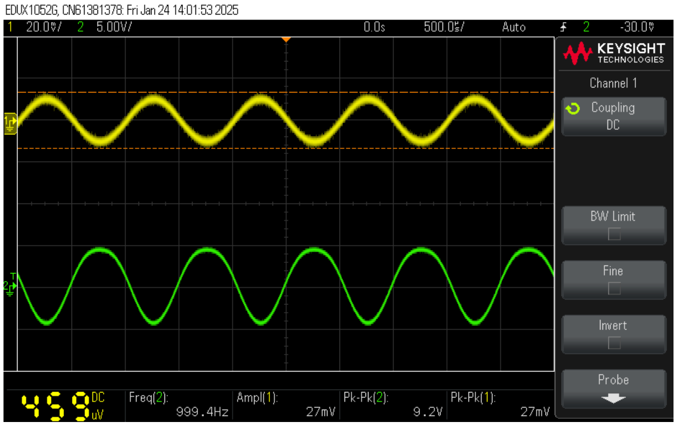



Fig. 14. Hardware Result of Gain Stage

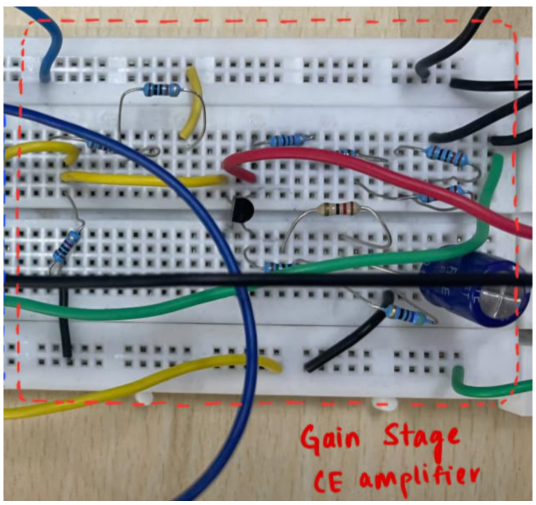



Fig. 15. Gain Stage Hardware Circuit

## VI. Filter Stage

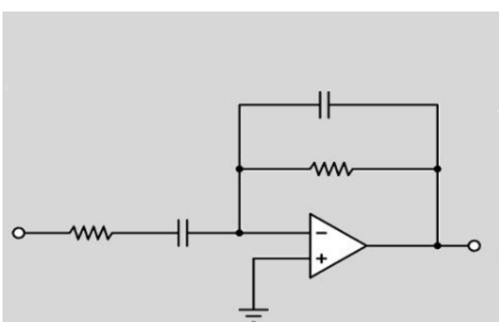


Fig. 16. Active Bandpass Filter

The filter stage in an audio amplifier refines the signal by removing unwanted frequencies, improving sound clarity and reducing distortion. A band-pass filter is used to allow only frequencies in the human-audible range (20Hz to 20KHz) to pass through. An active filter is chosen for its low distortion and enhanced performance.

Derivation of the Gain Equation for an Active Band-Pass Filter

The circuit consists of resistors $R_1$, $R_2$ and capacitors $C_1$, $C_2$. Using voltage division and impedance analysis, we derive the gain equation.

Transfer Function

Applying Kirchhoff's Voltage Law (KVL) and using impedance of capacitors $X_C = \frac{1}{j\omega C}$:

$$\frac{V_{\text{out}} - 0}{R_2 \parallel X_{C2}} = \frac{0 - V_{\text{in}}}{R_1 + X_{C1}} \tag{10}$$

Solving for $V_{\text{out}}/V_{\text{in}}$:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_1 + X_{C1}}{R_2 \parallel X_{C2}} \tag{11}$$

Expanding the parallel impedance:

$$R_2 \parallel X_{C2} = \frac{R_2 X_{C2}}{R_2 + X_{C2}} = \frac{R_2 \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} \tag{12}$$

Substituting,

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_1 + \frac{1}{j\omega C_1}}{\frac{R_2}{1 + j\omega C_2 R_2}} \tag{13}$$

Simplifying,

$$A_v = -\frac{j\omega C_1 R_2}{(1 + j\omega C_2 R_2)(j\omega C_1 R_1 + 1)} \tag{14}$$

*Magnitude Response*

The magnitude of the transfer function is:

$$|A_v| = \left| \frac{\omega C_1 R_2}{\sqrt{(1 + (\omega C_2 R_2)^2)(1 + (\omega C_1 R_1)^2)}} \right| \tag{15}$$

### Cutoff Frequencies

The cutoff frequencies $f_L$ and $f_H$ are determined from the high-pass and low-pass behaviors.

*Lower Cutoff Frequency*

The lower cutoff frequency occurs when the denominator term $j\omega C_1 R_1 + 1$ is dominant. Setting its magnitude to $\sqrt{2}$:

$$1 + (\omega_L C_1 R_1)^2 = 2 \tag{16}$$

Solving for $\omega_L$:

$$\omega_L = \frac{1}{R_1 C_1} \tag{17}$$

$$f_L = \frac{1}{2\pi R_1 C_1} \tag{18}$$

The low cutoff frequency $f_L$ is determined by the high-pass filter formula:

$$f_L = \frac{1}{2\pi R_8 C_4}$$

Substituting the given values:

$$f_L = \frac{1}{2\pi(1 \times 10^6)(8 \times 10^{-9})}$$

$$f_L \approx 19.89 \text{ Hz}$$

*Upper Cutoff Frequency*

The upper cutoff frequency is determined by the term $1 + j\omega C_2 R_2$. Setting its magnitude to $\sqrt{2}$:

$$1 + (\omega_H C_2 R_2)^2 = 2 \tag{19}$$

Solving for $\omega_H$:

$$\omega_H = \frac{1}{R_2 C_2} \tag{20}$$

$$f_H = \frac{1}{2\pi R_2 C_2} \tag{21}$$

the high cutoff frequency $f_H$ is determined by the low-pass filter formula:

$$f_H = \frac{1}{2\pi R_9 C_5}$$

Substituting the values:

$$f_H = \frac{1}{2\pi(1 \times 10^6)(8 \times 10^{-12})}$$

$$f_H \approx 19.89 \text{ kHz}$$

*Bandwidth*

The bandwidth of the band-pass filter is given by:

$$BW = f_H - f_L \tag{22}$$

Thus, the filter operates as a band-pass filter with a frequency range of approximately **20 Hz to 20 kHz**.

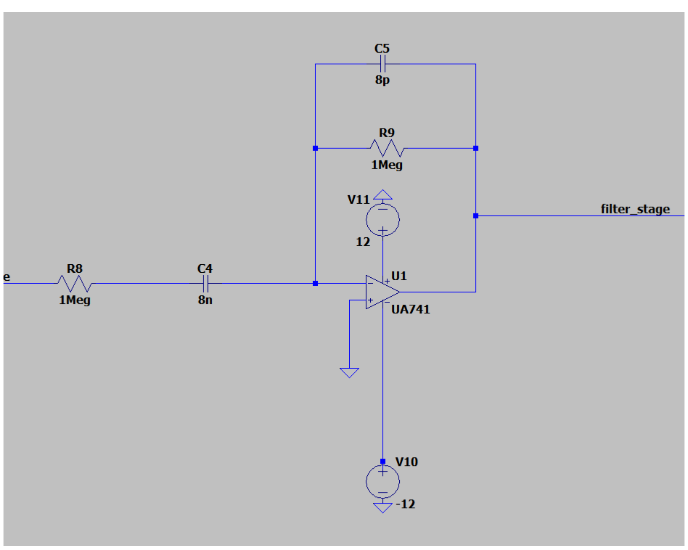



Fig. 17. Filter Stage Circuit

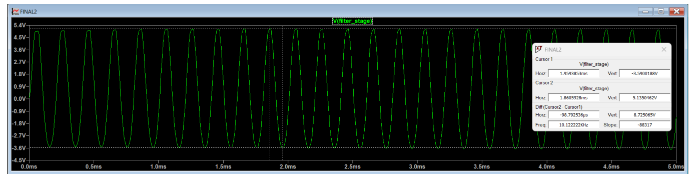


Fig. 18. Filter Stage Output

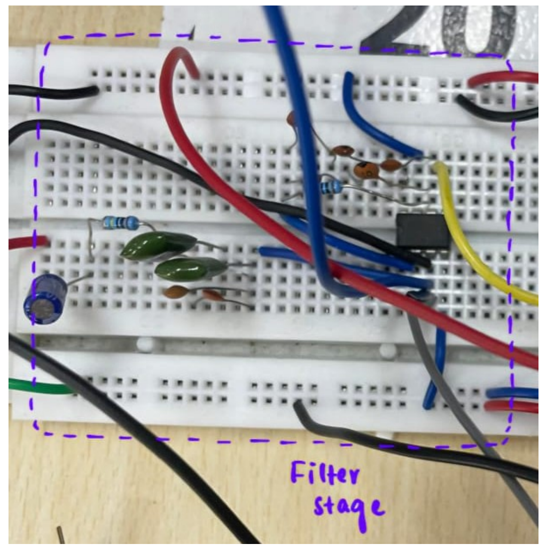



Fig. 19. Fliter Stage Hardware Circuit

## VII. Power Amplifier Stage

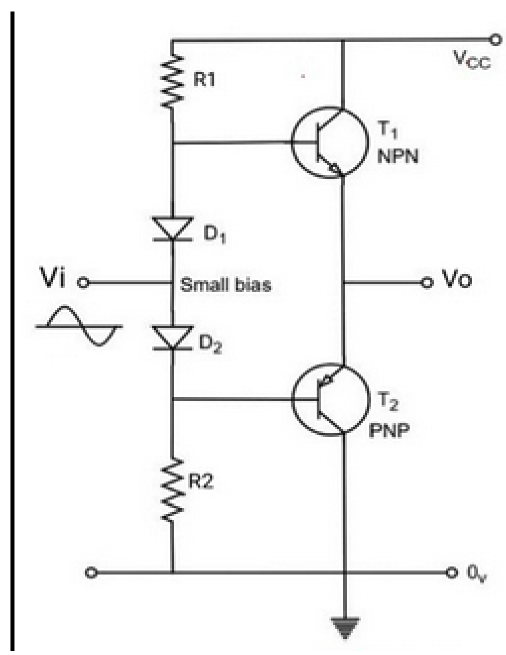



Fig. 20. Power Amplifier Stage

The power amplifier stage is responsible for increasing the power of the signal. The output of the filter stage has very low current, which is insufficient to drive a speaker. The power amplifier boosts the current, ensuring sufficient power to produce audible sound.

- **Diodes in Biasing**: Diodes (or a biasing network) ensure both transistors conduct for a small part of the cycle, preventing distortion at the zero crossing of the waveform.
- **Current Amplification**: A small base current in the transistors controls a much larger collector current, allowing significant current gain.
- **Voltage Gain $\approx$ 1**: The circuit typically follows a common-collector (emitter follower) configuration, where the output voltage closely follows the input voltage, resulting in unity voltage gain.
- **Push-Pull Operation**: The two transistors handle different halves of the waveform, ensuring continuous signal conduction with minimal distortion.

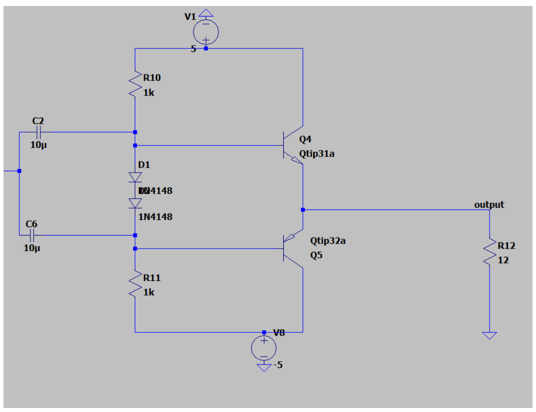



Fig. 21. Power Amplifier Circuit

### Voltage Gain Derivation

The voltage gain is 1 due to the following reasons:

$$V_{out} = I_E R_L = I_E R_L V_{in}$$

$$V_{in} - V_\pi = V_{out}$$

$$V_{in} - \frac{I_C}{g_m} = V_{out}$$

$$V_{in} - I_e r_e = V_{out}$$

$$V_{in} = I_e R_L + I_E r_e$$

$$V_{in} = (R_L + r_e) I_E$$

$$\frac{V_{out}}{V_{in}} = \frac{R_L}{R_L + r_e}$$

Since $r_e$ is negligible:

$$\frac{V_{out}}{V_{in}} \approx 1$$

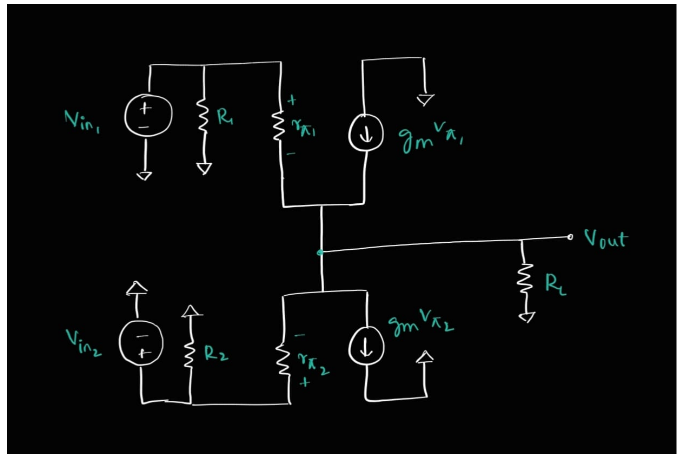



Fig. 22. Small signal Analysis of the Power Amplifier

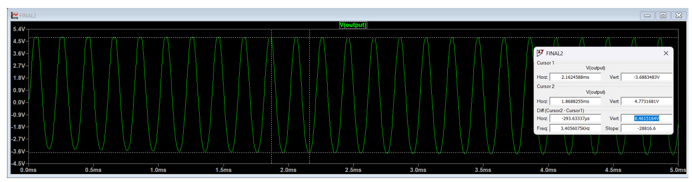


Fig. 23. Power Amplifier Output

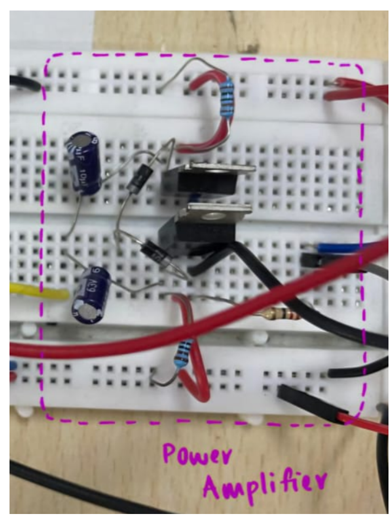
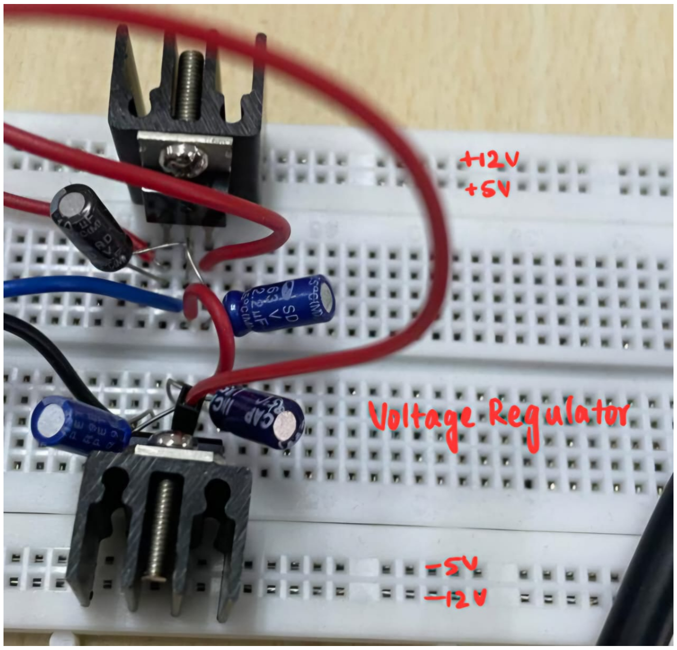



Fig. 24. Power Amplifier Hardware Circuit

## VIII. Voltage Regulator

Two voltage regulators are used to generate $\pm 5V$ from $\pm 12V$. The $+12V$ supply is used for the filter stage, while the rest of the circuit operates on $\pm 5V$. This ensures stable operation and proper voltage levels for different sections of the circuit.




## IX. Final Circuit

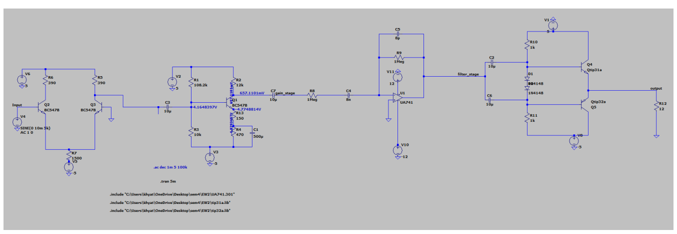


Fig. 25. Final circuit in Simulation

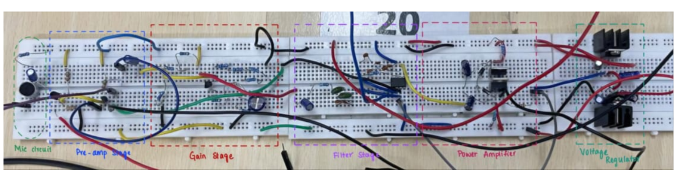



Fig. 26. Final hardware circuit

## X. Results

The designed amplifier successfully achieves a gain of approximately 430 within the frequency range of 1 kHz to 10 kHz. However, beyond this range, the amplitude gradually attenuates due to the non-ideal nature of the filter. The filter does not exhibit a sharp cutoff, resulting in a gradual roll-off as the frequency approaches 20 Hz and 20 kHz. This behavior is evident in the frequency response, where the gain remains linear within the specified bandwidth but begins to decline outside this range. Future improvements could involve designing a sharper filter to maintain a more consistent gain over a wider frequency spectrum.

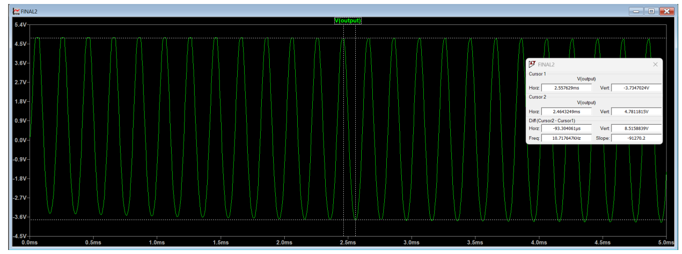


Fig. 27. Final Simulation Result

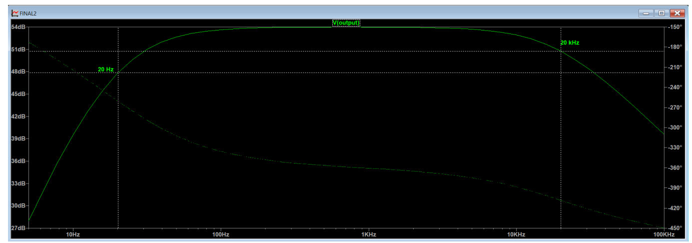


Fig. 28. Frequency Response of the Final Circuit

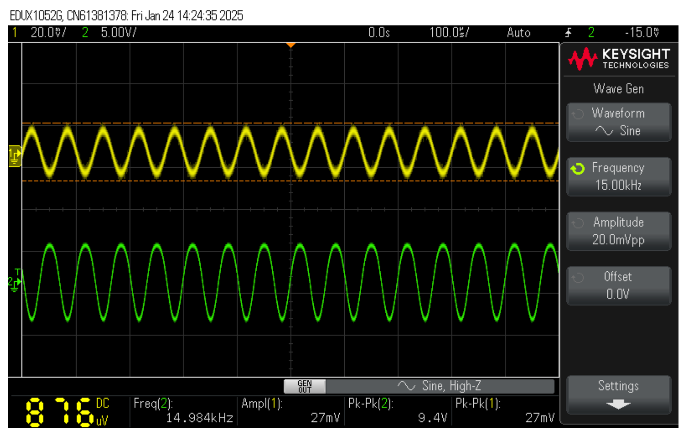



Fig. 29. Final Hardware Result

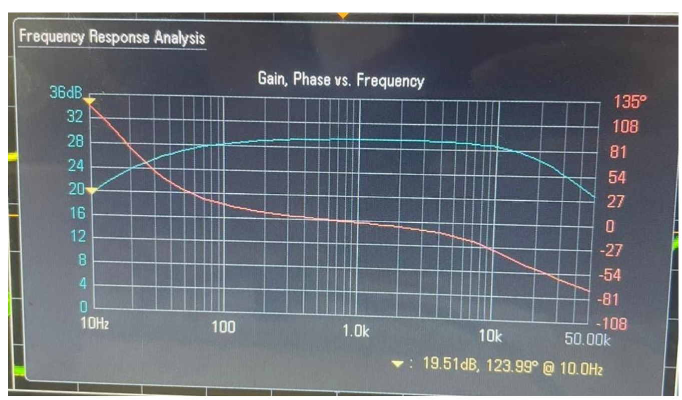



Fig. 30. Hardware Frequency Response

The final circuit successfully amplifies the audio signal while maintaining clarity and minimizing noise.

## XI. Distortion Analysis

Distortion Analysis is done to figure out the amount of unwanted harmonic content in the frequency content of a signal. It can further elaborate on the behaviour of the circuit at different frequencies.

The main formula used was -

$$THD = \sqrt{\frac{\sum_{n=2}^{\infty} V_{n\_RMS}^2}{V_{f\_RMS}}}$$

- *THD* is the total harmonic distortion present in the signal.
- $V_{n\_RMS}$ is the RMS voltage of the $n$th harmonic.
- $V_{f\_RMS}$ is the RMS voltage of the fundamental frequency.

The voltages can be found using the FFT of a sine signal in the *wavegen*, which can be plugged into the formula accordingly.

Having a large THD leads to distortion in the output amplified signal, which can be manifested in the form of skewed or flat regions in the signal. This is disastrous for an audio signal as any skewing or slewing in the input signal can lead to complete destruction of the quality of the audio of the output.

A lower THD also means higher efficiency magnification of the signal, and a higher quality output.

THD can be improved by trying to minimise the circuit interference and by adding filters to shut down higher unwanted harmonic currents in the system. Resistive-capacitive filters (low pass in our case) effectively kill the higher order harmonics, improving the THD of the circuit.

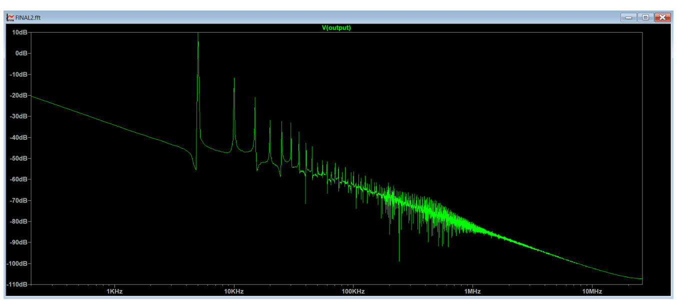


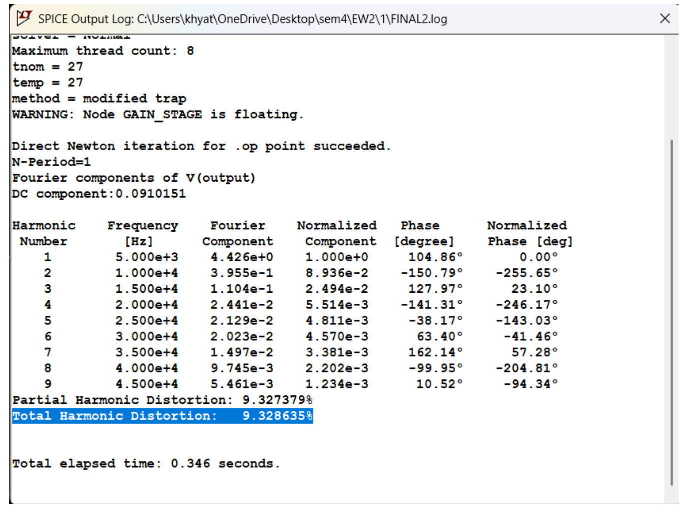
Fig. 31. Fast Fourier Transform of the Output

Let's take Fundamental Frequency = 5KHz.
Considering the first five harmonics,

| Harmonic | Frequency (Hz) | $V_{\text{RMS}}$ (V) |
|---|---|---|
| 1st | 5000 | 3.12 |
| 2nd | 10 000 | 0.239 |
| 3rd | 15 000 | 0.209 |
| 4th | 20 000 | 0.0342 |
| 5th | 25 000 | 0.0320 |

TABLE I
Harmonic Analysis Data

On substituting the values in the above formula, we can find the THD. Further, the THD percentage is shown in the Spice Ouput Log File which is below.



```
SPICE Output Log: C:\Users\khyat\OneDrive\Desktop\sem4\EW2\1\FINAL2.log
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
WARNING: Node GAIN_STAGE is floating.

Direct Newton iteration for .op point succeeded.
N-Period=1
Fourier components of V(output)
DC component:0.0910151

Harmonic  Frequency   Fourier    Normalized   Phase    Normalized
 Number     [Hz]     Component   Component   [degree]  Phase [deg]
    1     5.000e+3   4.426e+0    1.000e+0     104.86°     0.00°
    2     1.000e+4   3.955e-1    8.936e-2    -150.79°  -255.65°
    3     1.500e+4   1.104e-1    2.494e-2     127.97°    23.10°
    4     2.000e+4   2.441e-2    5.514e-3    -141.31°  -246.17°
    5     2.500e+4   2.129e-2    4.811e-3     -38.17°  -143.03°
    6     3.000e+4   2.023e-2    4.570e-3      63.40°   -41.46°
    7     3.500e+4   1.497e-2    3.381e-3     162.14°    57.28°
    8     4.000e+4   9.745e-3    2.202e-3     -99.95°  -204.81°
    9     4.500e+4   5.461e-3    1.234e-3      10.52°   -94.34°
Partial Harmonic Distortion: 9.327379%
Total Harmonic Distortion:   9.328635%


Total elapsed time: 0.346 seconds.
```

Fig. 32. THD result in LtSpice

## XII. Slew Rate

Slew Rate is defined as the maximum change in output voltage divided by the change in time.

Ideally, the slew rate for a circuit should be infinitely high, so that even for high-frequency applications, the circuit does not produce a distorted output. If the slew rate is not high enough, it will not be able to catch up with the input (say high frequency), which will cause distortion and the output will not be as required.

$$\text{S.R.} = \max\left(\frac{\delta V_{\text{out}}}{\delta t}\right)$$

Slew Rate can be increased by increasing the maximum operating voltage or by making the capacitive impedances of the subcircuits smaller. This will allow that particular subcircuit to operate at a higher frequency.

From the below graph, we can see that,
Slew Rate = 389.1 K/Vs

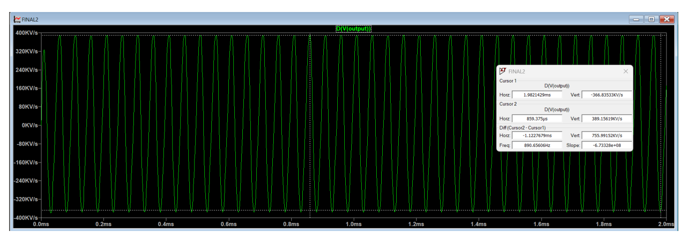


Fig. 33. Derivative of the Output

## XIII. Key Findings

1) The circuit utilizes a two-stage amplification approach. The preamplifier stage provides initial noise attenuation and moderate gain, ensuring a cleaner signal before passing it to the main gain stage, which amplifies the signal to the desired level.
2) Noise reduction is achieved by designing the circuit with a common-mode gain close to zero, effectively minimizing unwanted interference and external noise.

3) Impedance matching between different stages is crucial to ensure efficient signal transfer and to prevent signal degradation, thereby maintaining the integrity of the amplified signal.
4) The filter stage attenuates frequencies below 1 kHz and above 10 kHz due to its non-ideal characteristics. Instead of a sharp cutoff, it exhibits a gradual roll-off, leading to reduced gain at extreme frequency ranges.
5) A Class AB amplifier is chosen for the final amplification stage as it offers an optimal balance between efficiency and linearity. It provides high power efficiency without significant distortion, making it suitable for high-fidelity signal amplification.