***AEC* *LAB REPORT – 8***

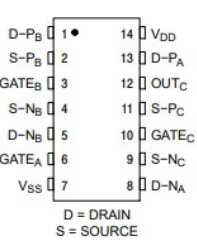
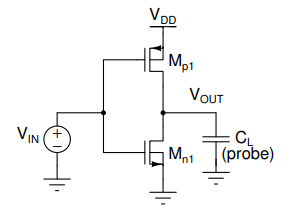
***Operational Amplifiers***

***NAME:*** *Khyathi Sri Basireddy*

***ROLL NO****: 2023102065*

***TABLE NO: 9***

***1.*** ***CMOS Inverter with feedback***

***Pins Used***

Pin 1 – PMOS Drain 

Pin 2 – PMOS Source

Pin 3 – Common Gate

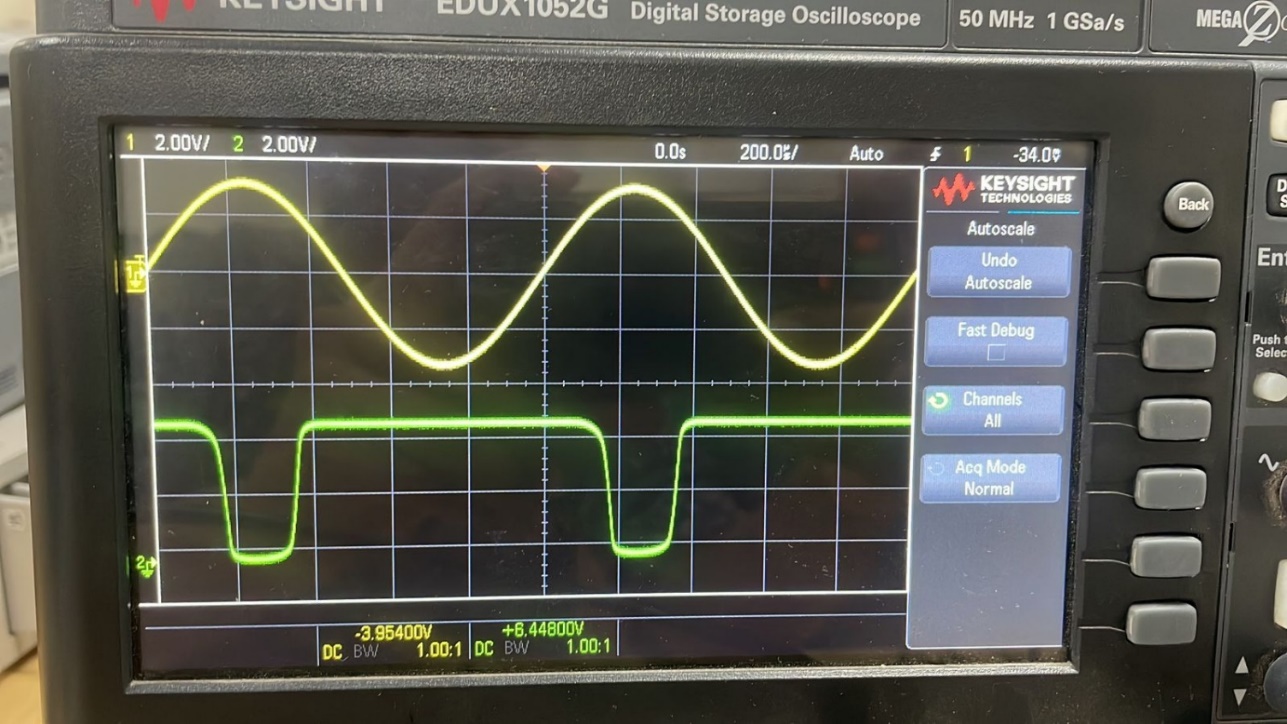
Pin 4 – NMOS Source

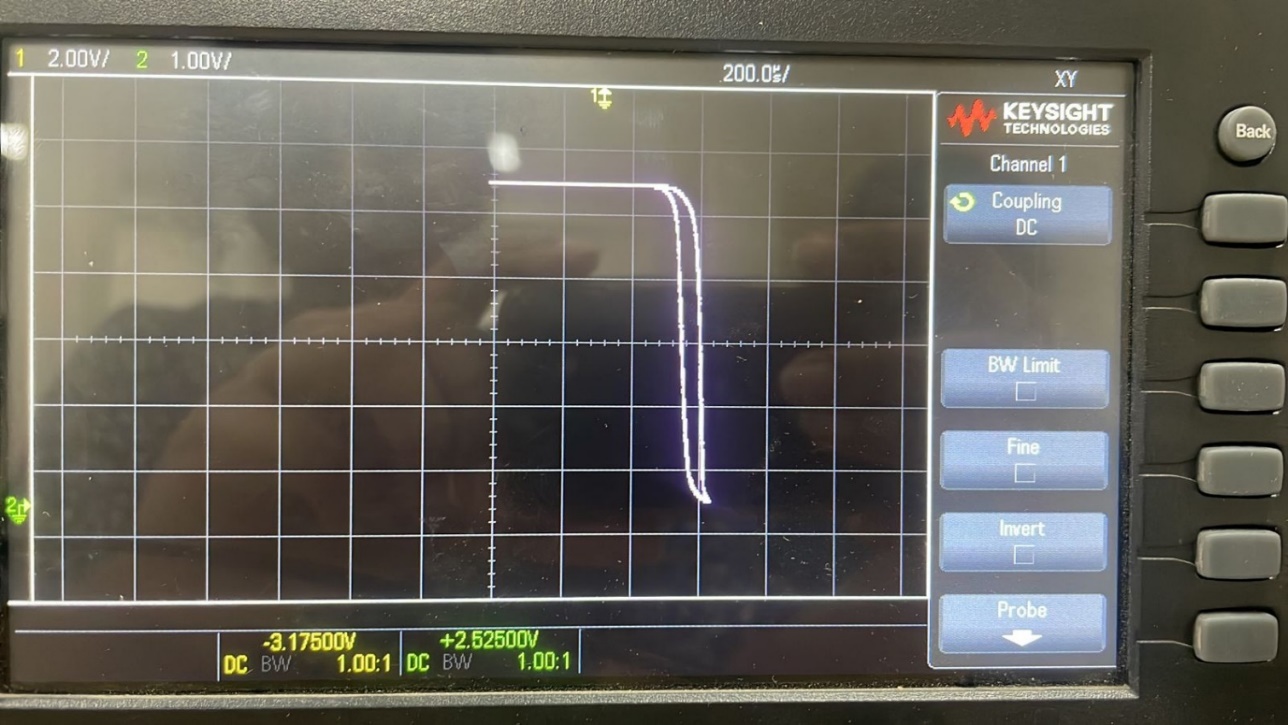
Pin 5 – NMOS Drain

Pin 7 – Vss

Pin 14 – VDD

**(a)Voltage Transfer Characteristics (VOUT vs VIN)**

****

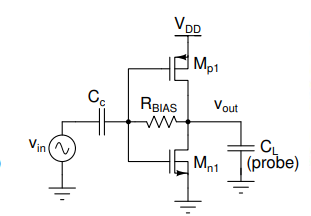
****

**Valid input and output region lies where slope of the curve, i.e, VOUT/VIN is greater than 1.**

Valid Input Range – 1.67V to 3.22V

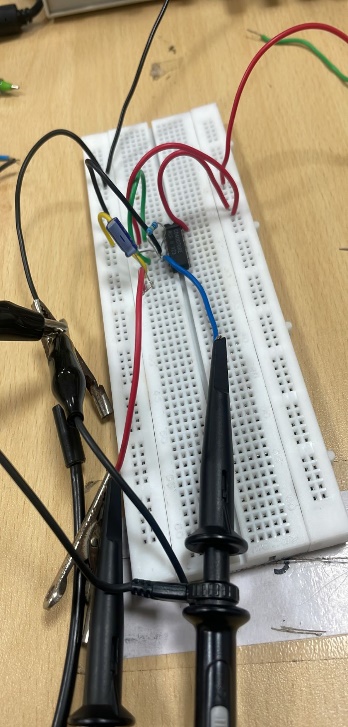
Valid Output Range – 12.5mV to 4.96V

**(b) With RBIAS**



DC Value at Gate = OV (Since the Capacitor there doesn’t allow the DC signal to pass through)

DC Value at Drain of CMOS = OV



**Input Parameter:**

Wave – Sin Wave

Amplitude – 100mV

Frequency – 1kHz

RBIAS = 1M ohm

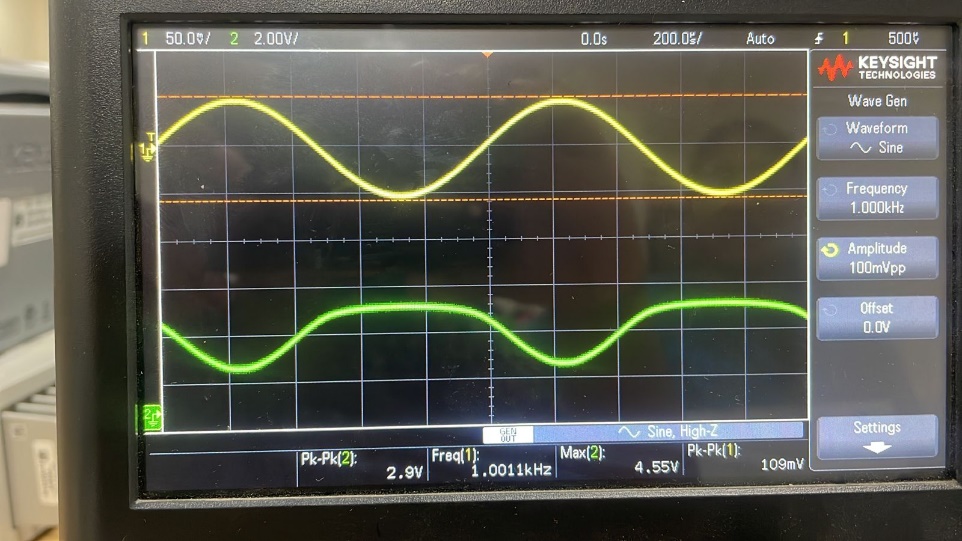
CC = 10 u F

VDD = 5V

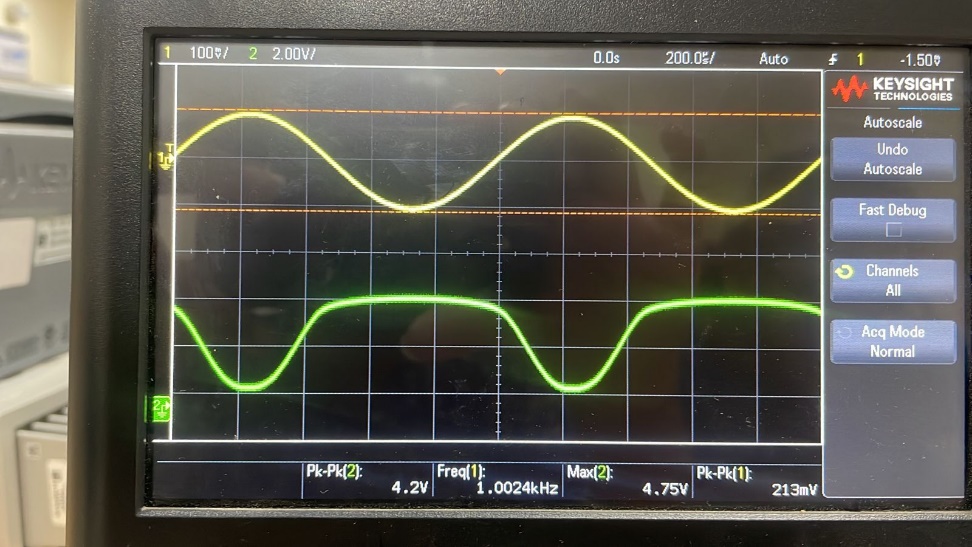
Given below are the gains for different values of VGS:

|  |  |  |
| --- | --- | --- |
| ***VIN*** | ***VOUT*** | ***GAIN*** |
| 100mV | 2.9V | 29 |
| 200mV | 4.2V | 21 |
| 300mV | 4.6V | 15.34 |
| 400mV | 4.7V | 11.75 |
| 500mV | 4.8V | 9.6 |
| 600mV | 5.0V | 8.34 |

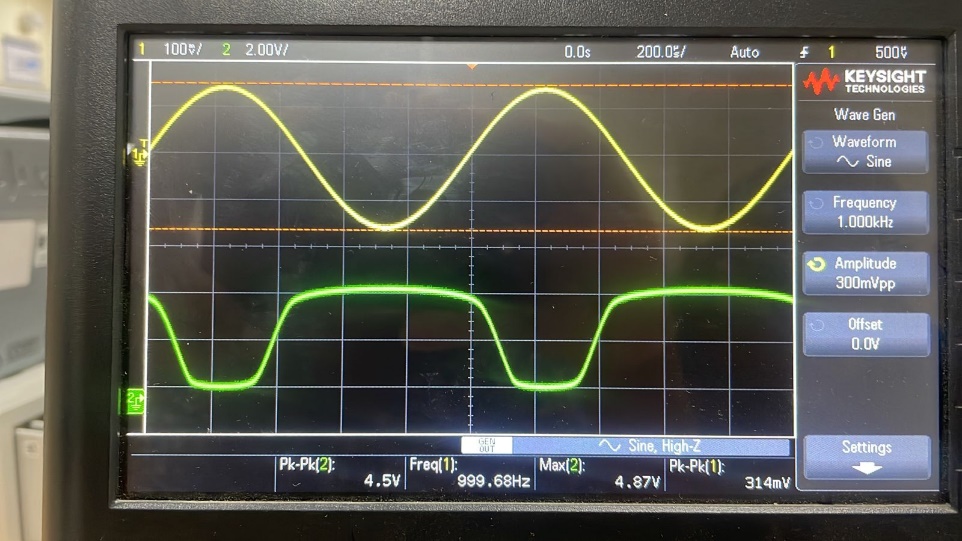
**VIN = 100mV**

****

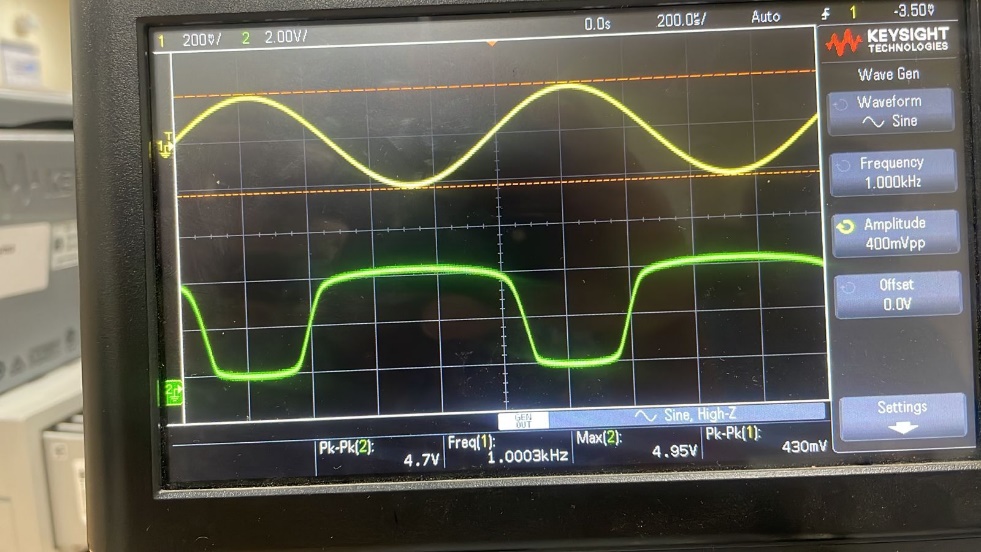
**VIN = 200mV**



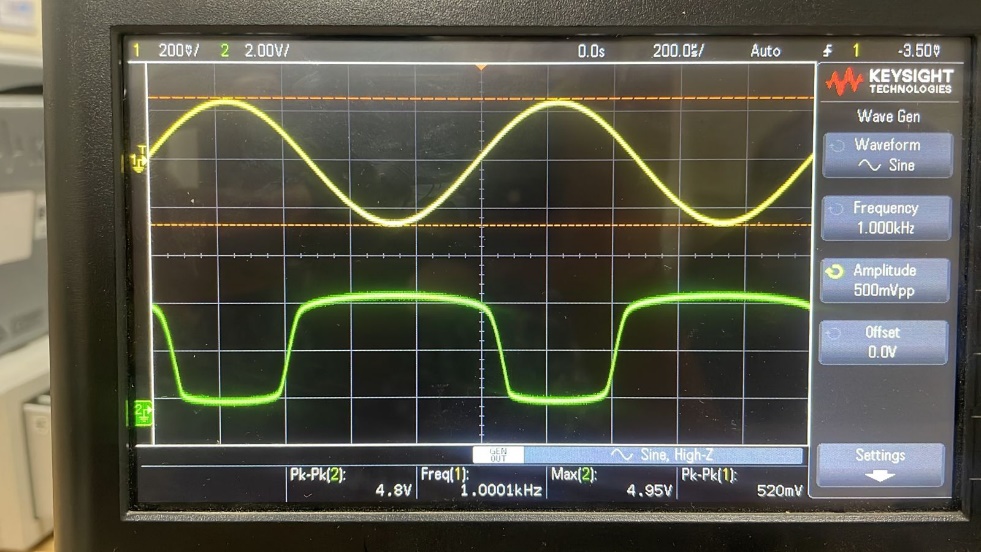
**VIN = 300mV**



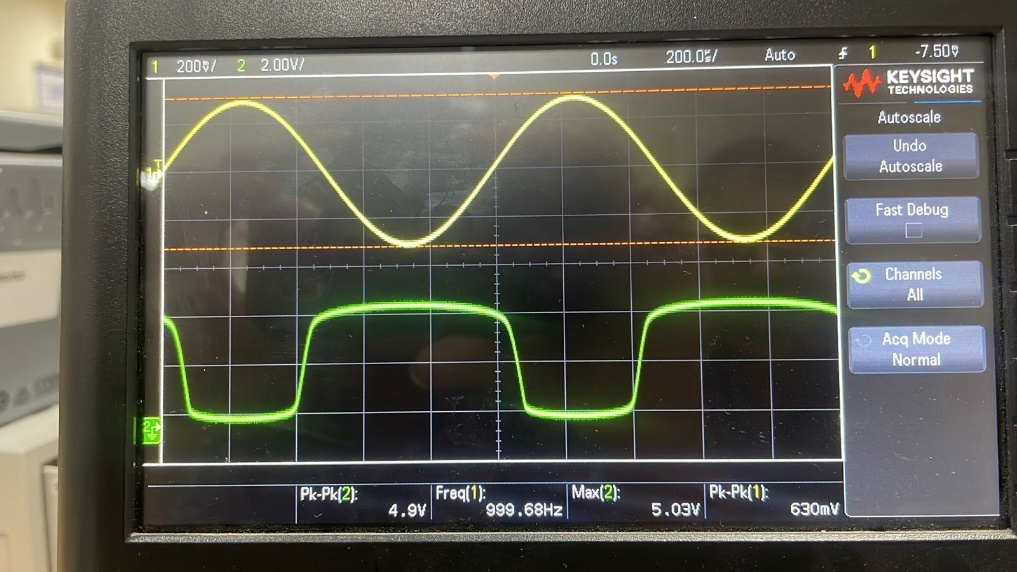
**VIN = 400mV**

****

**VIN = 500mV**



**VIN = 600mV**

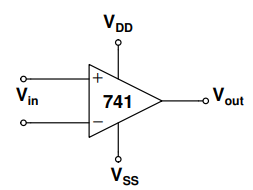
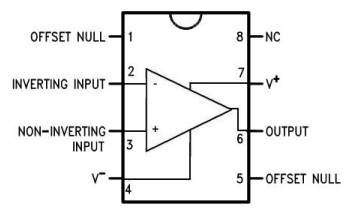


**Reason for Clipping:**

This is so because a signal point that is higher than the swing range would go beyond the saturation zone, which is the point at which amplification doesn't happen. When the input amplitude is increased, a   
  
More clipping occurs when a bigger percentage of the output signal leaves the saturation area. Because the circuit cannot efficiently amplify signals that exceed the saturation limits, this results in a loss in gain.

***2.*** ***Characterization of an operational amplifier***

**(a) OpAmp Open Loop Characteristics**

**Input Parameter:**

VIN – 12 Vpp

Frequency – 100Hz

VDD = 5V

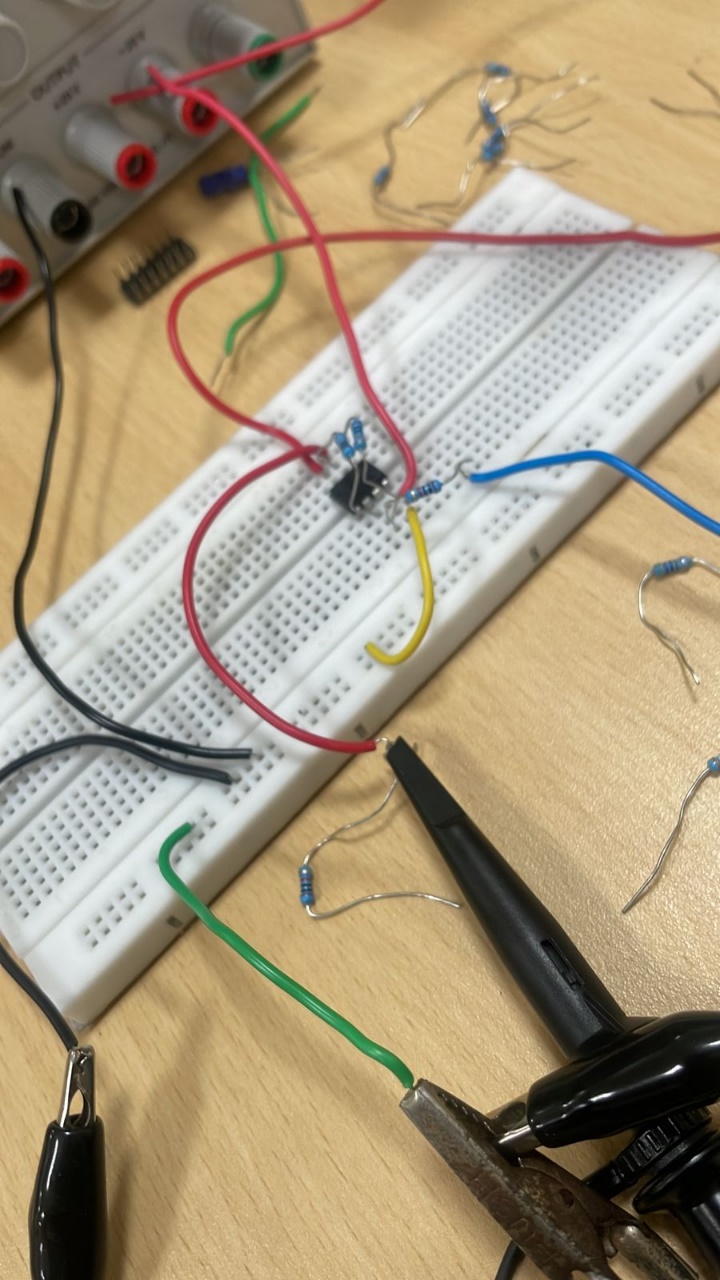
**Input Parameter:**

VIN = 12V

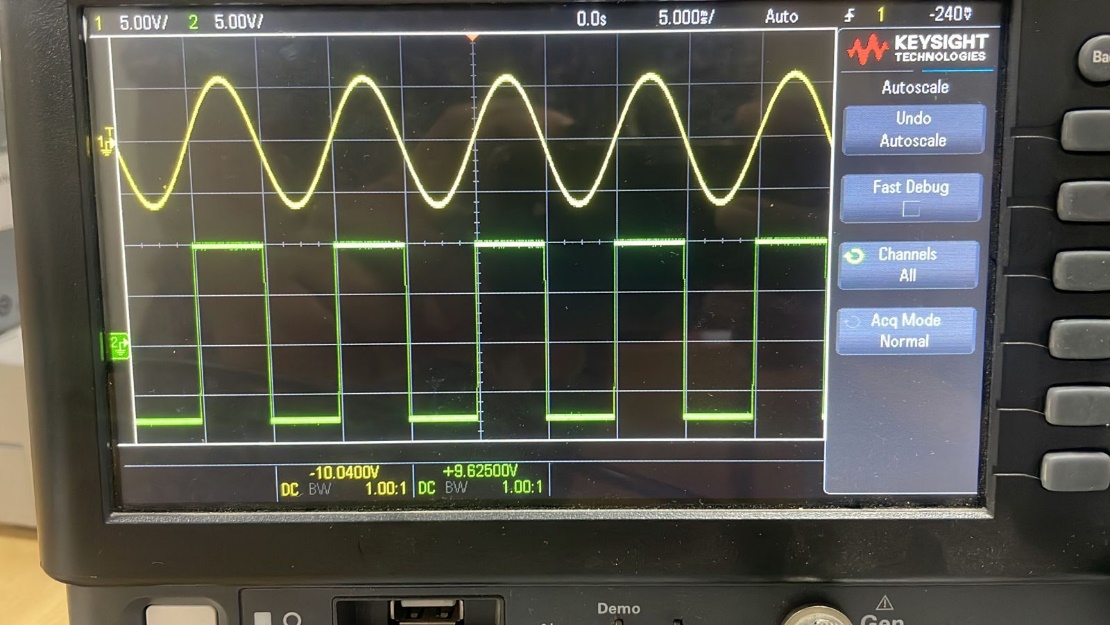
Frequency – 100Hz

VDD = 5V

VSS = -10V



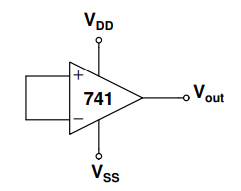
**Voltage Transfer Characteristics (VOUT vs VIN)**



**VOUT and VIN with time:**

****

**(b) Offset Measurement**



Based on the ideal behaviour of a differential amplifier, we predict an output of 0V in this experiment when we short both of the Op Amp's input terminals. Instead, we see a saturated output because of flaws in the device itself, such as an intrinsic DC offset at the input. This happens as a result of the Op Amp is practically extremely high and potentially unlimited gain, which amplifies even the smallest input offsets and produces an output voltage that is not zero.

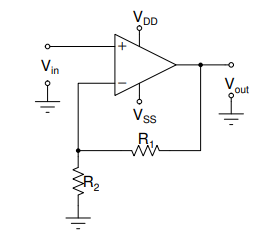


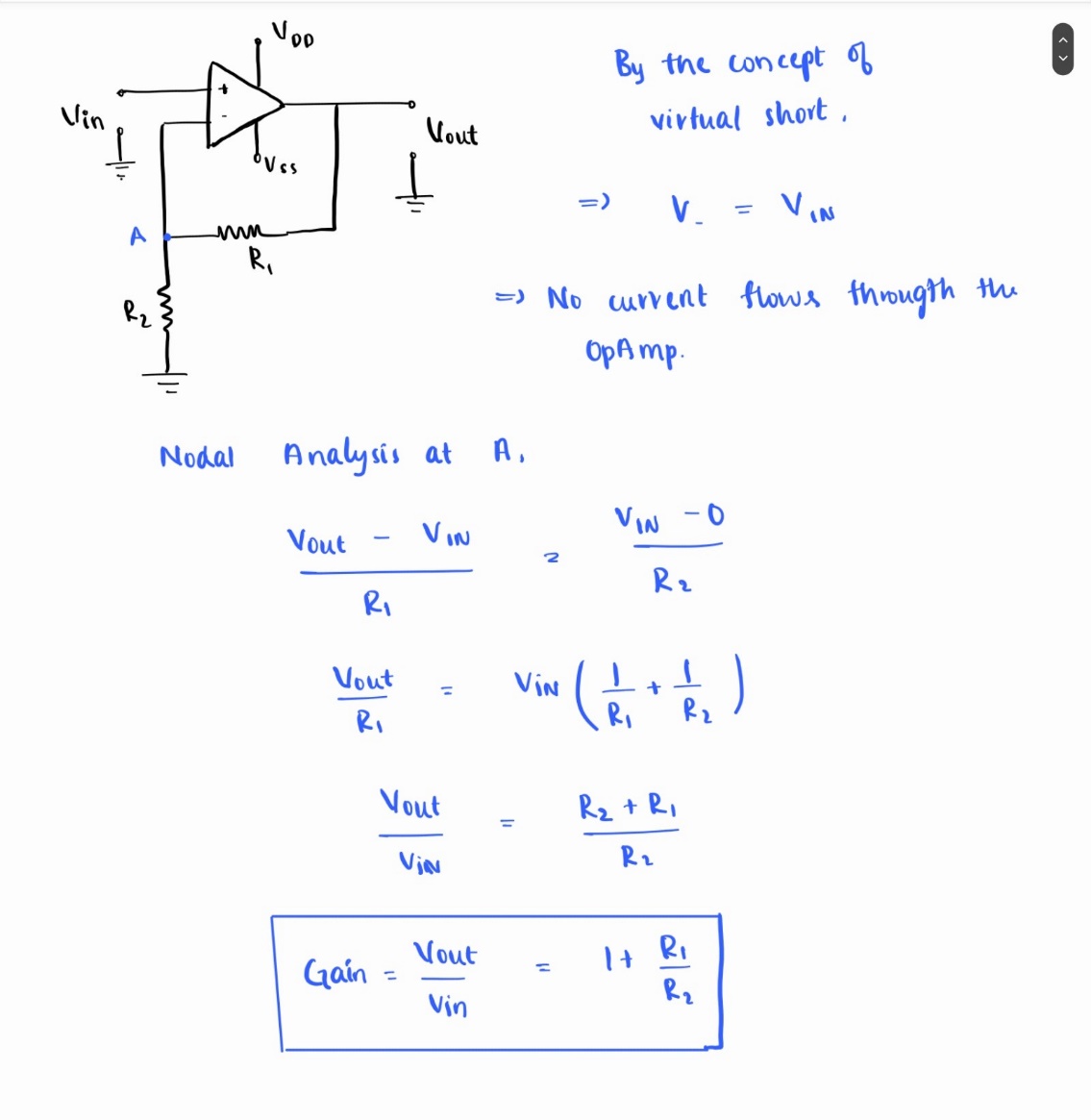
However, when the input voltage is maintained at about 0.47V, we can achieve an output of 0V.

This change basically compensates foe the inherent DC offset in the OpAmp, allowing us to nullify the output voltage and get it back to the desired zero level.

***3.*** ***Non inverting amplifier***

**(a) Derivation of Gain**





**(b)**

**Input Parameter:**

VIN = 250 mV (peak to peak)

Frequency = 5kHz

VDD = 12V

VSS = -12V

**Calculated Gain = 1 + R1/R2**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **R1** | **R2** | **VOUT** | **Calculated Gain** | **Obtained Gain** |
| 10k ohm | 10k ohm | 520 mV | 2 | 2.08 |
| 10k ohm | 4.7k ohm | 810 mV | 3.128 | 3.24 |

**R1 = 10k ohm , R2 = 10k ohm**



**R1 = 10k ohm , R2 = 4.7k ohm**

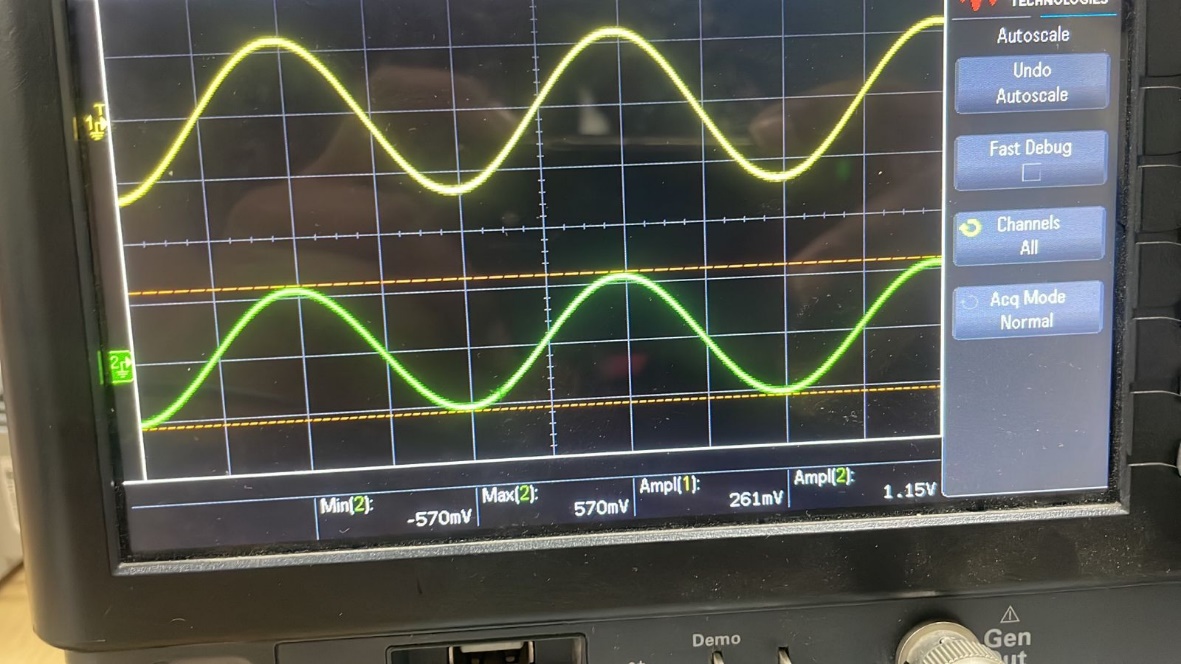


**(c)**

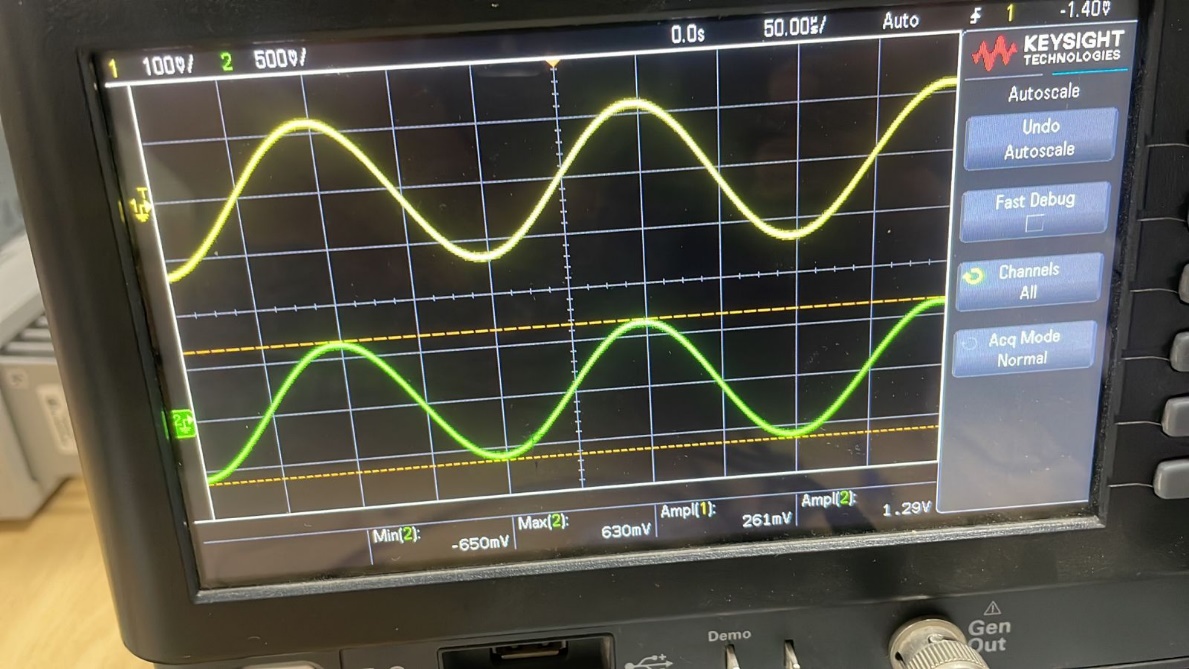
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Expected Gain** | **R1** | **R2** | **VOUT** | **Obtained Gain** |
| 4 | 33k | 10k | 1.15V | 4.4 |
| 5 | 39k | 10k | 1.29V | 4.942 |

Generally exact expected gain can be obtained by using 30k and 40k respectively, but we do not have the exact resistors of that value, so consider the approx..

**R1 = 33k ohm , R2 = 10k ohm**



**R1 = 39k ohm , R2 = 10k ohm**



**(d)**

Now, when we remove R1 and R2 and directly connect the VOUT to the inverting input terminal directly, we observe the following



VIN = 261 mV (Vpp)

VOUT = 261 mV (Vpp)

GAIN = VOUT / VIN

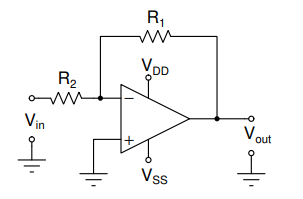
= 261 mV / 261 mV

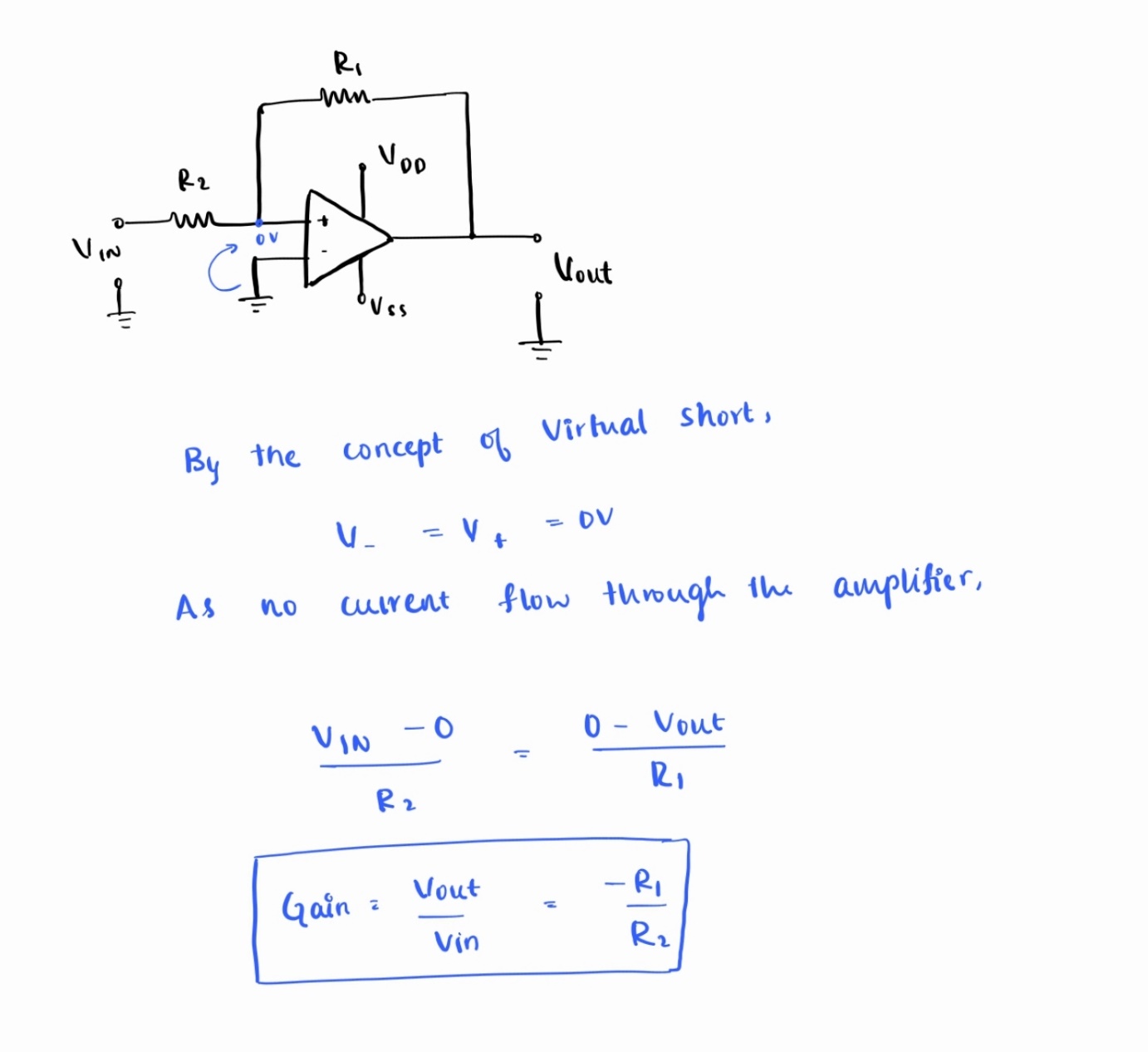
= 1

With this configuration, we can obtain a gain of 1.

***4.*** ***Inverting amplifier***

**(a) Derivation of Gain**





**(b)**

**Input Parameter:**

VIN = 250 mV (peak to peak)

Frequency = 5kHz

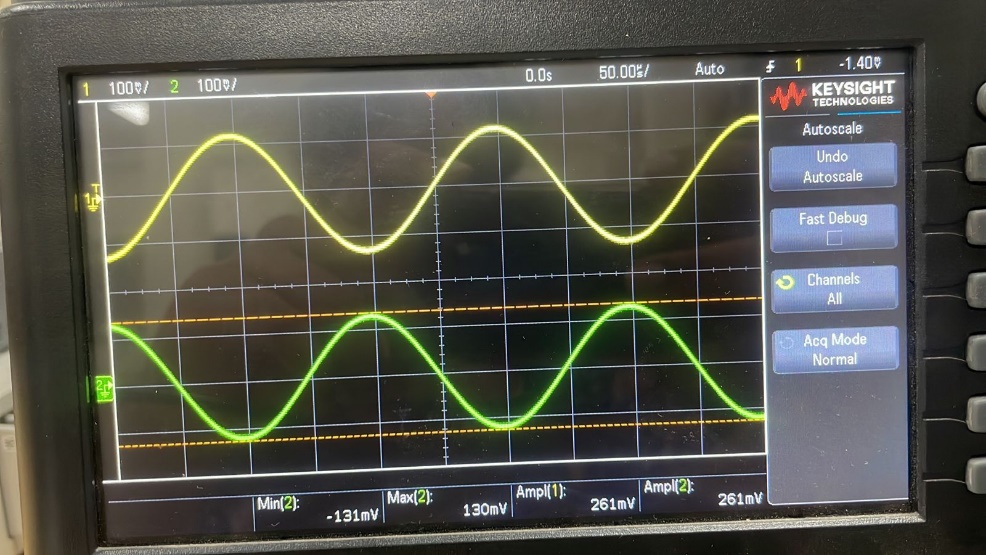
VDD = 12V

VSS = -12V

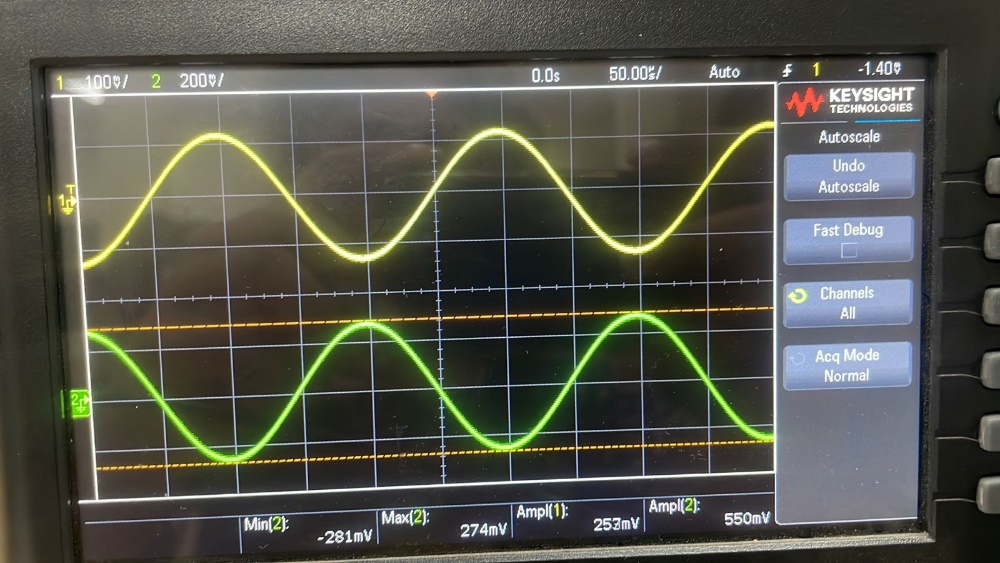
**Calculated Gain = - R1/R2**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **R1** | **R2** | **VOUT** | **Calculated Gain** | **Obtained Gain** |
| 10k ohm | 10k ohm | 261 mV | 1 | 1.044 |
| 10k ohm | 4.7k ohm | 550 mV | 2.127 | 2.2 |

**R1 = 10k ohm , R2 = 10k ohm**



**R1 = 10k ohm , R2 = 4.7k ohm**

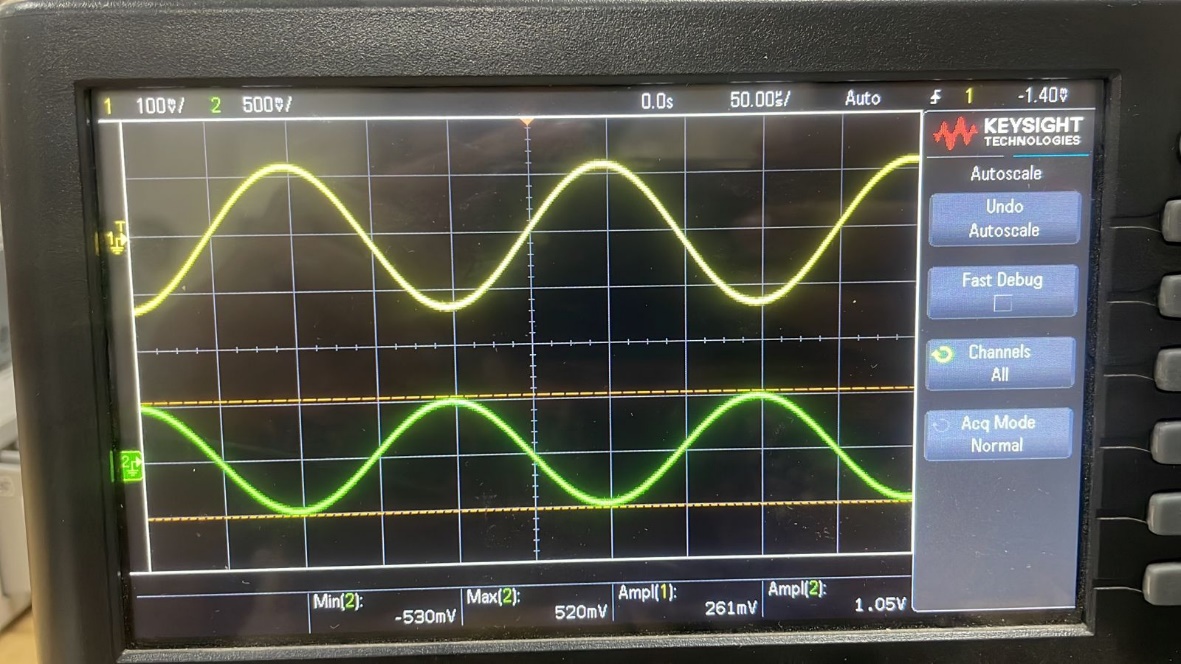


**(c)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Expected Gain** | **R1** | **R2** | **VOUT** | **Obtained Gain** |
| 4 | 39k | 10k | 1.05V | 4.022 |
| 5 | 50k | 10k | 1.31V | 5.019 |

Generally exact expected gain can be obtained by using 30k and 40k respectively, but we do not have the exact resistors of that value, so consider the approx..

**R1 = 39k ohm , R2 = 10k ohm**



**R1 = 50k ohm , R2 = 10k ohm**

