PATRIoT lab

Lecture 18 – Sequential circuits 3

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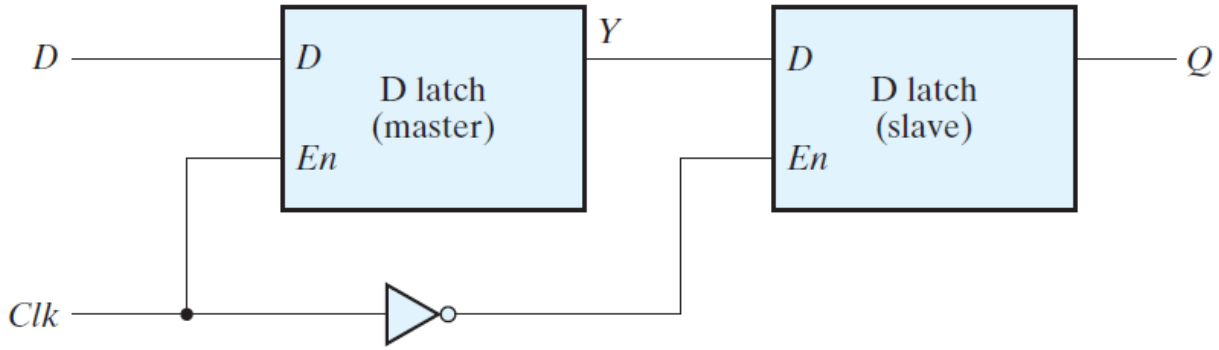
Chapter 5

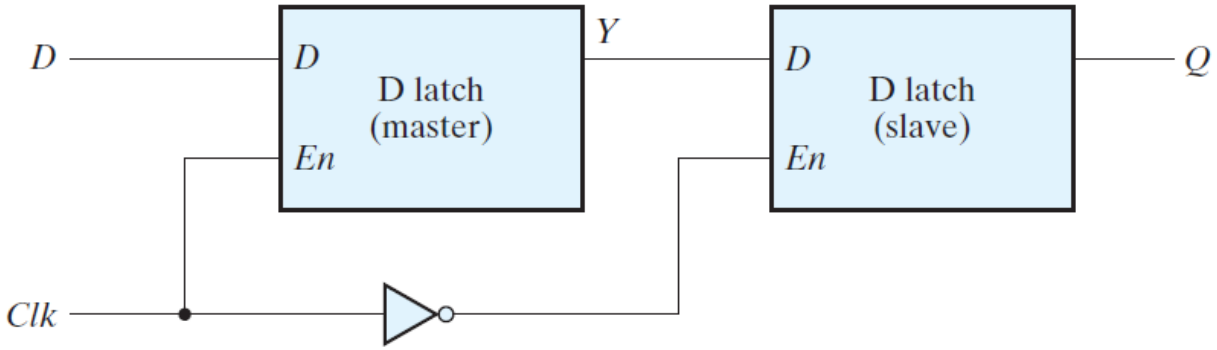
Flip flops

- We can implement flip flops using two latches
- The first latch is called the master and the second the slave
- The circuit samples the *D* input and changes its output *Q* only at the negative edge of the synchronizing or controlling clock (designated as *Clk*)
- When the *Clk = 0*, the slave latch is enabled, and its output *Q* is equal to the master output *Y*
- When the input pulse changes, the data from the external *D* input are transferred to the master

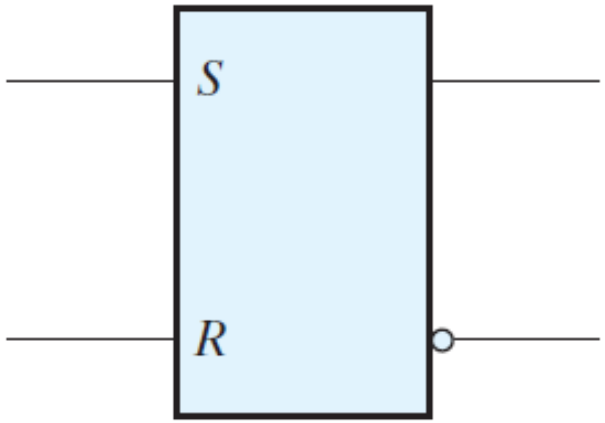


Flip flops

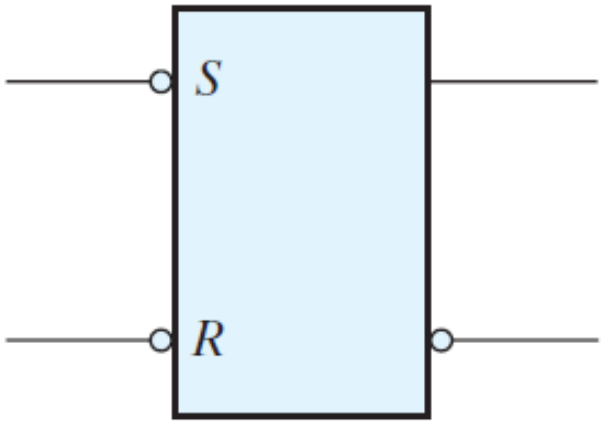
- The slave, however, is disabled as long as the clock remains at the 1 level, because its *enable* input is equal to 0
- Any change in the input changes the master output at *Y*, but cannot affect the slave output
- When the clock pulse returns to 0, the master is disabled and is isolated from the *D* input
- At the same time, the slave is enabled and the value of *Y* is transferred to the output of the flip-flop at *Q*
- Thus, *a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0 (-ve edge)*



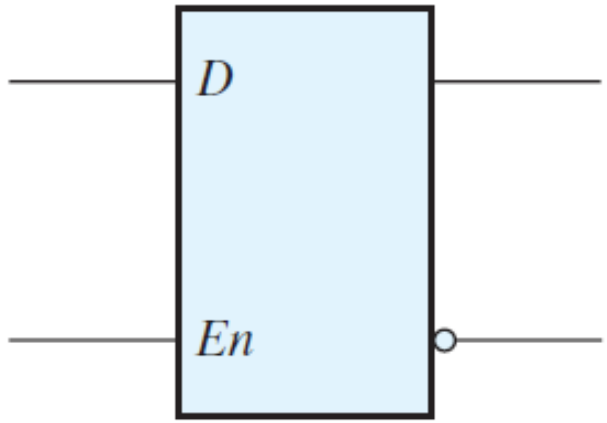
Graphical symbols



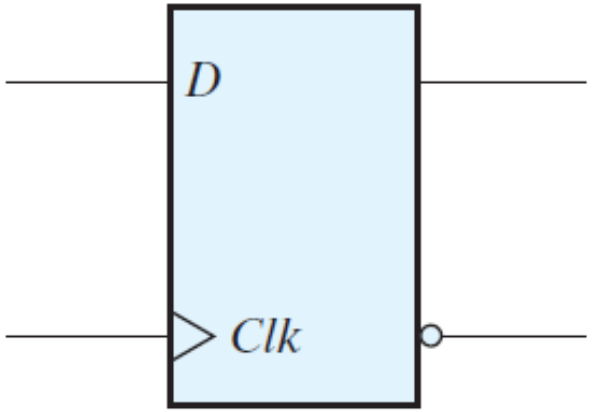
SR



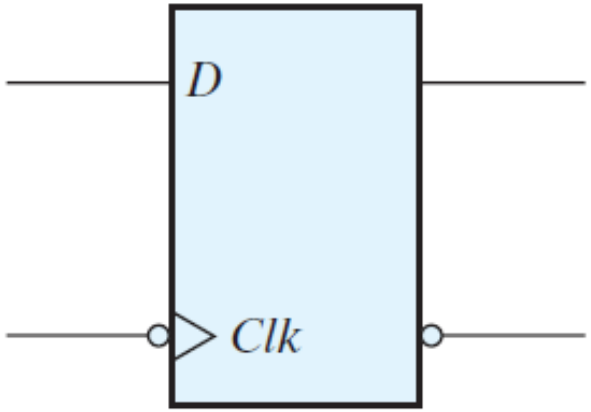
$\overline{S}\overline{R}$



D



(a) Positive-edge

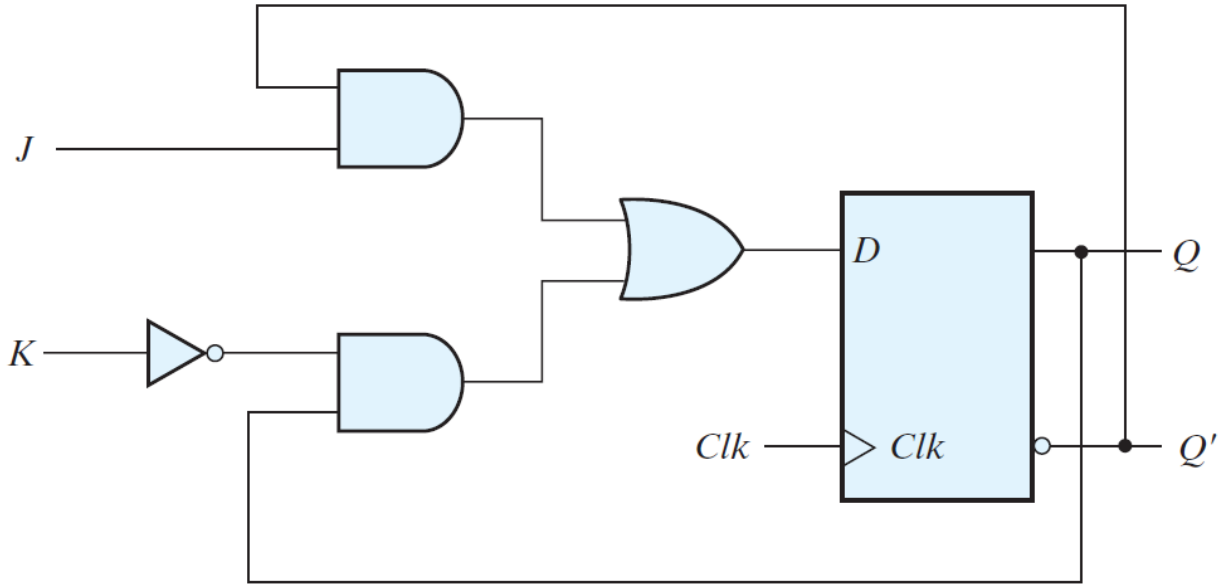


(a) Negative-edge

JK Flip Flop

- There are four operations we are looking to perform in a flip-flop: Set it to 1, reset it to 0, retain or complement its output
- With only a single input, the *D* flip-flop can set or reset the output, depending on the value of the *D* input immediately before the clock transition
- Synchronized by a clock signal, the *JK* flip-flop has two inputs and performs all four operations
- The *J* input sets the flip-flop to 1, the *K* input resets it to 0, and when both inputs are enabled, the output is complemented
- This can be obtained if the *D* input is:

$$D = JQ' + KQ$$



(a) Circuit diagram

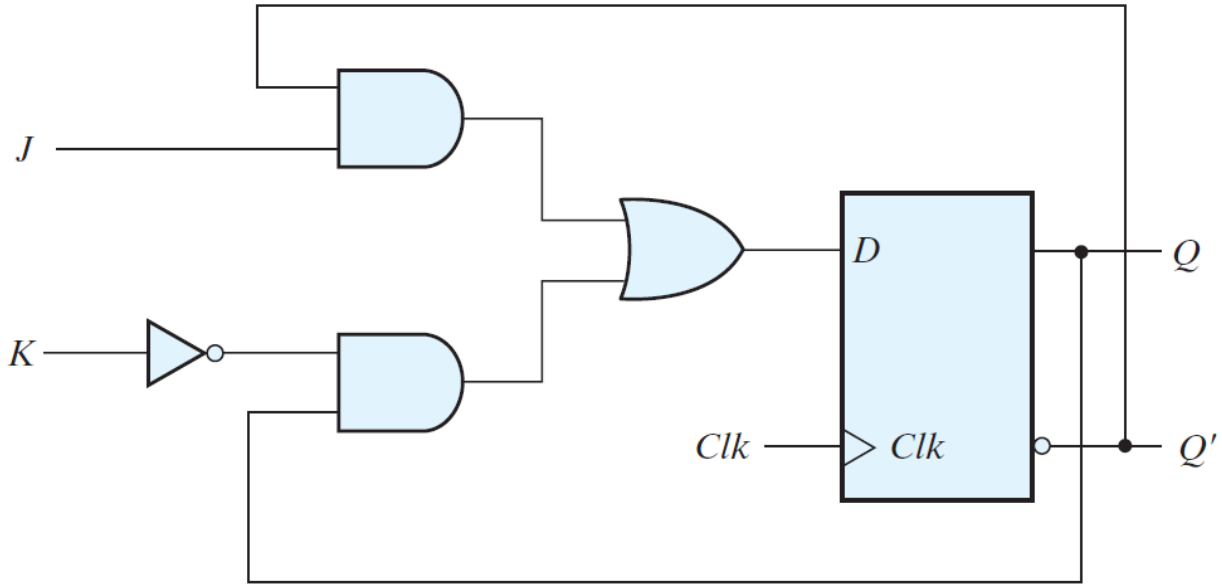
JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

JK Flip Flop

$$D = JQ' + K'Q$$

- When $J = 1$ and $K = 0$, $D = Q' + Q = 1$, so the next clock edge sets the output to 1
- When $J = 0$ and $K = 1$, $D = 0$, so the next clock edge resets the output to 0
- When both $J = K = 1$ and $D = Q'$, the next clock edge complements the output
- When both $J = K = 0$ and $D = Q$, the clock edge leaves the output unchanged
- Because of their versatility, JK flip-flops are called *universal flip-flops*



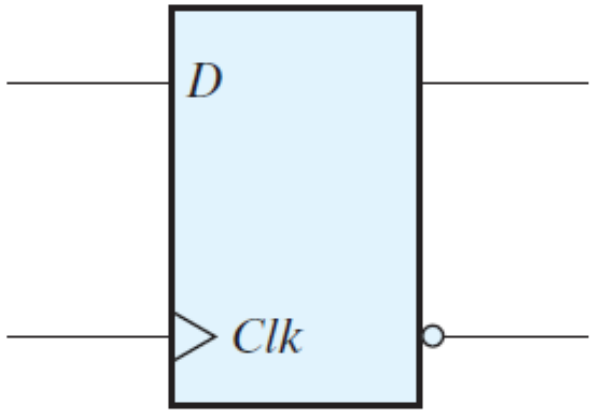
(a) Circuit diagram

JK Flip-Flop

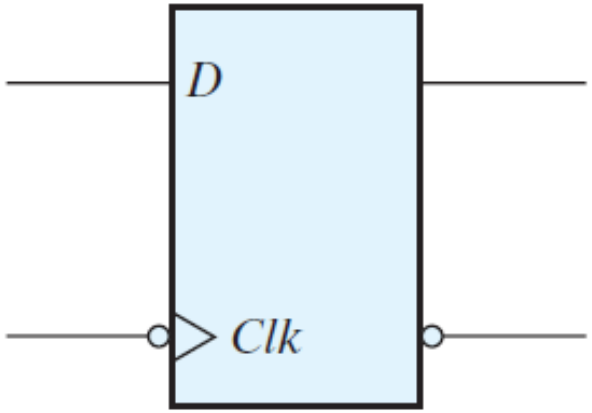
J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip Flop

- Transparent flip-flop
- The bit at D is transferred to Q at the edge of the clock
- The information is retained upto the next edge of the clock



(a) Positive-edge

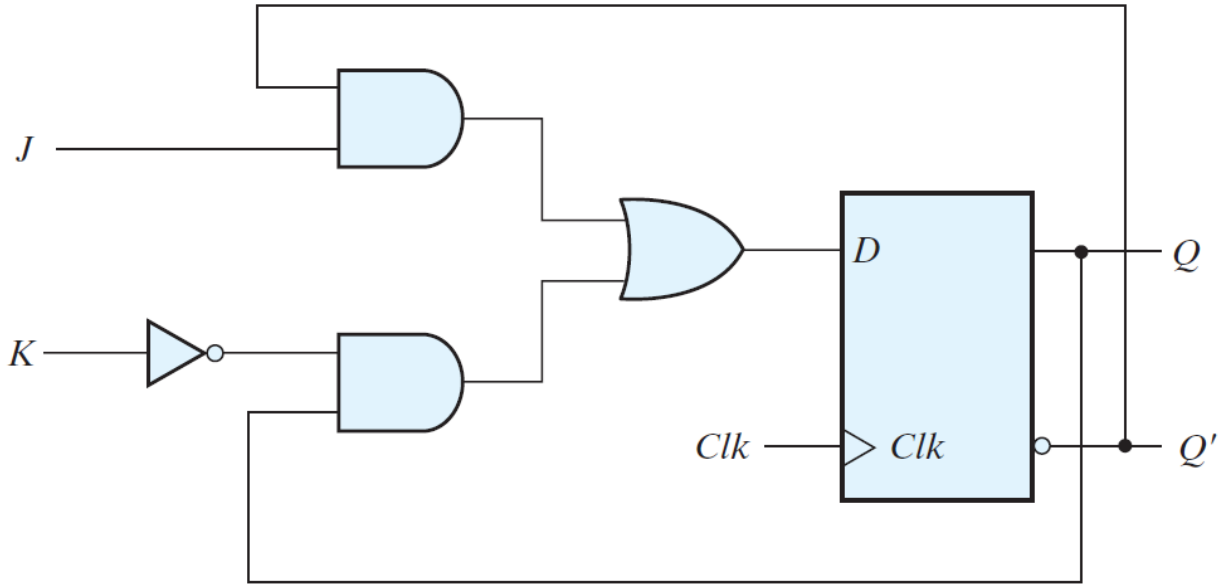


(a) Negative-edge

JK Flip Flop

$$D = JQ' + K'Q$$

- When $J = 1$ and $K = 0$, $D = Q' + Q = 1$, so the next clock edge sets the output to 1
- When $J = 0$ and $K = 1$, $D = 0$, so the next clock edge resets the output to 0
- When both $J = K = 1$ and $D = Q'$, the next clock edge complements the output
- When both $J = K = 0$ and $D = Q$, the clock edge leaves the output unchanged
- Because of their versatility, JK flip-flops are called *universal flip-flops*



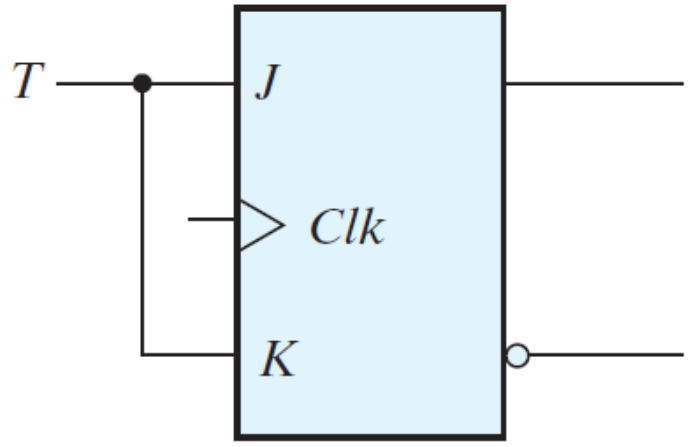
(a) Circuit diagram

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

T Flip Flop

- The *T* (toggle) flip-flop is a complementing flip-flop and can be obtained from a *JK* flip-flop when inputs *J* and *K* are tied together
- When *T* = 0 (*J* = *K* = 0), a clock edge does not change the output
- When *T* = 1 (*J* = *K* = 1), a clock edge complements the output
- The complementing flip-flop is useful for designing binary counters



(a) From *JK* flip-flop

T Flip-Flop

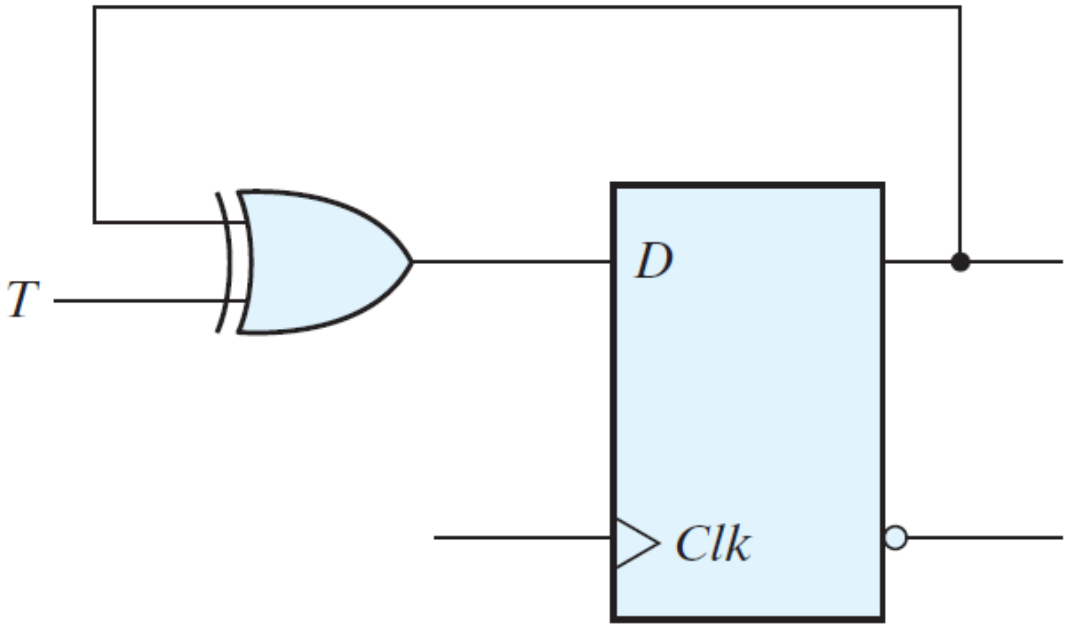
T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

T Flip Flop

- The *T* flip-flop can also be constructed using a *D* flip-flop
- The expression for the *D* input is:

$$D = T'Q + TQ'$$

- When *T* = 0, *D* = *Q* and there is no change in the output
- When *T* = 1, *D* = *Q'* and the output complements
- The graphic symbol for this flip-flop has a *T* symbol in the input

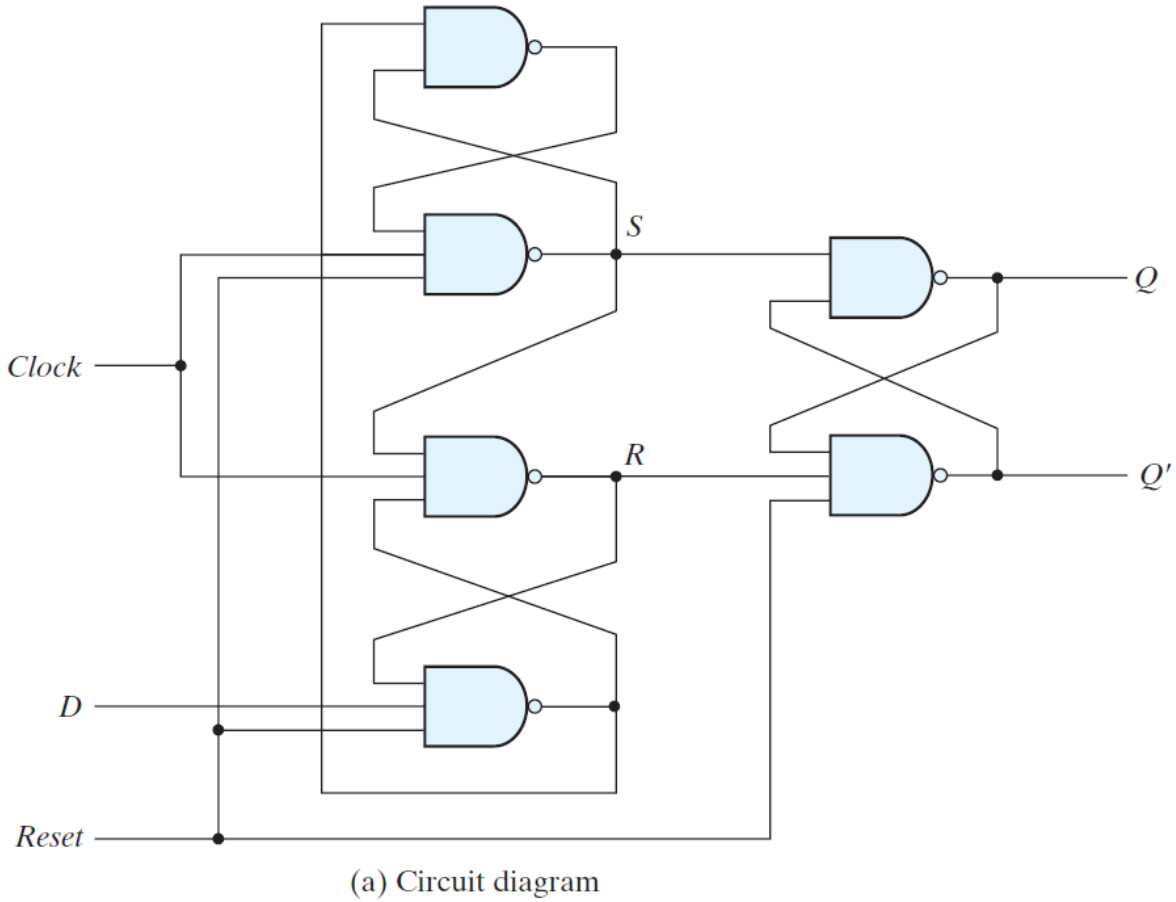


T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Asynchronous inputs

- Some flip-flops have asynchronous inputs that are used to force the flip-flop to a particular state independently of the clock
- The input that sets the flip-flop to 1 is called *preset* or *direct set*
- The input that clears the flip-flop to 0 is called *clear* or *direct reset*
- When power is turned on in a digital system, the state of the flip-flops is unknown
- The direct inputs are useful for bringing all flip-flops in the system to a known starting state prior to the clocked operation.
- When the reset input is 0, it forces output *Q'* to stay at 1, which, in turn, clears output *Q* to 0, thus resetting the flip-flop



(a) Circuit diagram