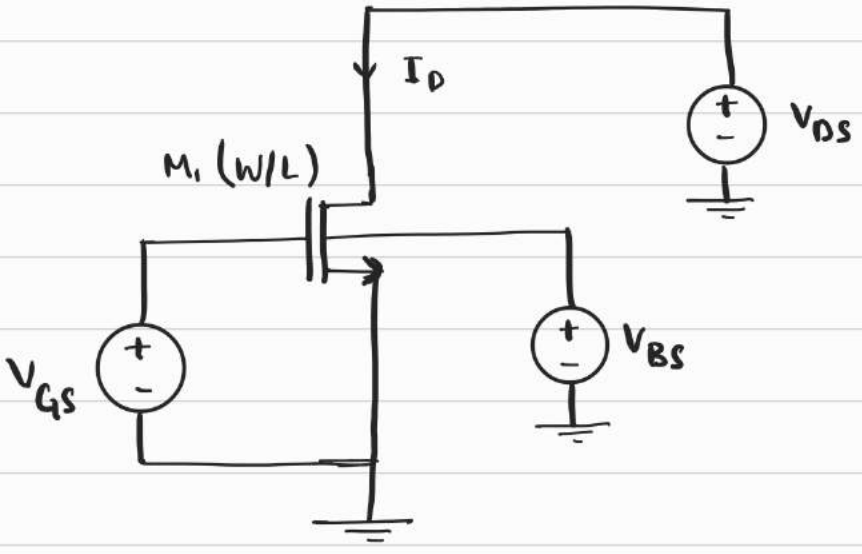
AEC Assignment -5

- B. Khyathi Sri
2023102068

Question -1

Given, $\frac{W}{L} = \frac{1.8\,\mu}{0.18\,\mu}$



V_{BS} = 0 Volt (No Body Effect)

V_{DS} = 0 to 0.18 V step size = 0.01 V

V_{GS} = 0 to 1.8 V step size = 0.3 V

Technology Parameters :

λ (LAMBDA) = $\frac{L}{2}$ = 0.09 μ

width_N = 1.8 μ

Source Area (AS) = (5)(1.8μ)(0.09μ) = 0.81 pm^2

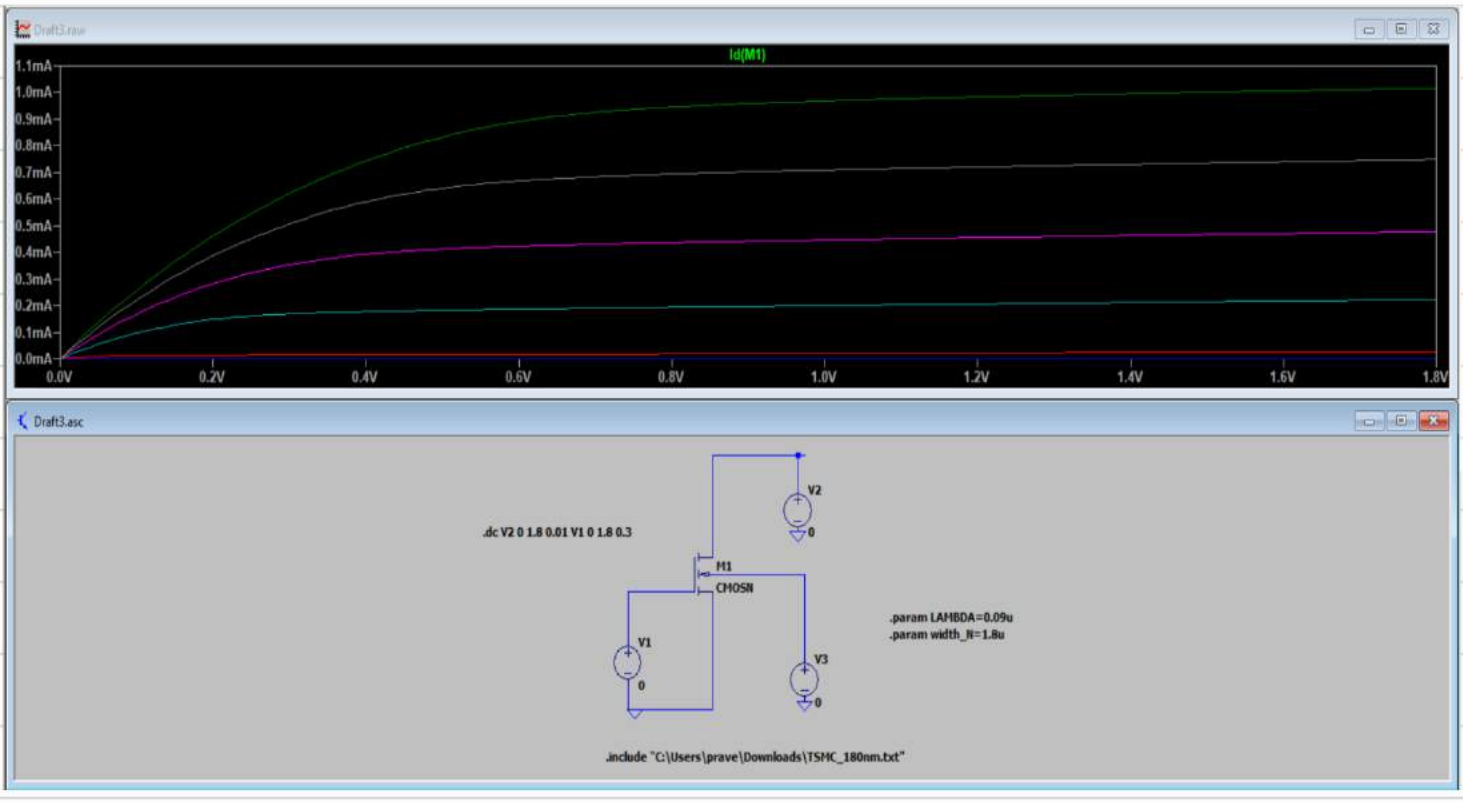
Drain Area (AD) = (5)(1.8u)(0.09u) = 0.81 pm

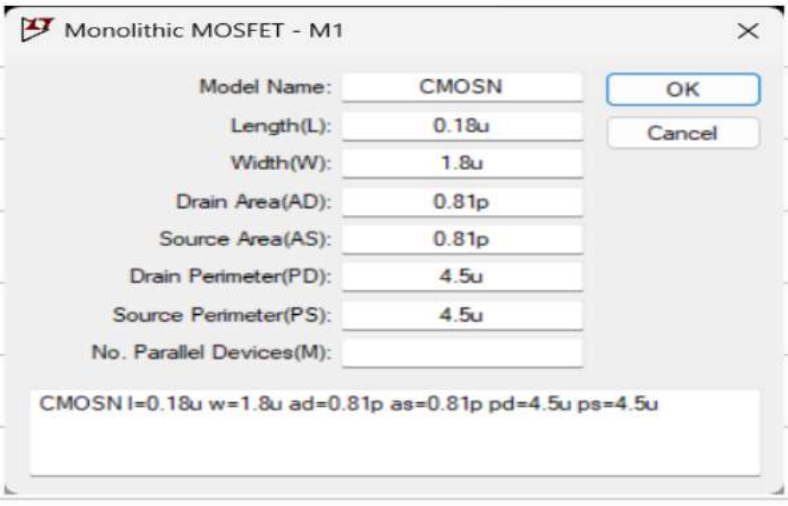
Source Perimeter (PS) = $10\lambda + 2w$ = 4.5 µm

Drain Perimeter (PD) = $10\lambda + 2w$ = 4.5 µm

The plot of I_D vs V_{DS} is given below:

Here we sweep V_{DS} first and then the V_{GS}.





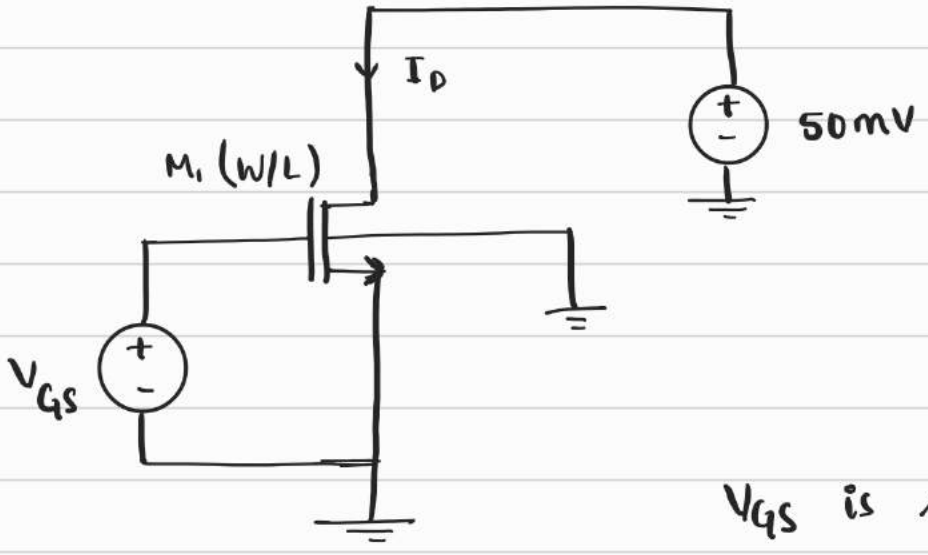
Question - 2

Question 2

Given, $W = 1.8u$; $L = 0.18u$

$V_{DS} = 50\ mV$

$V_{BS} = 0\ V$ (No body effect)



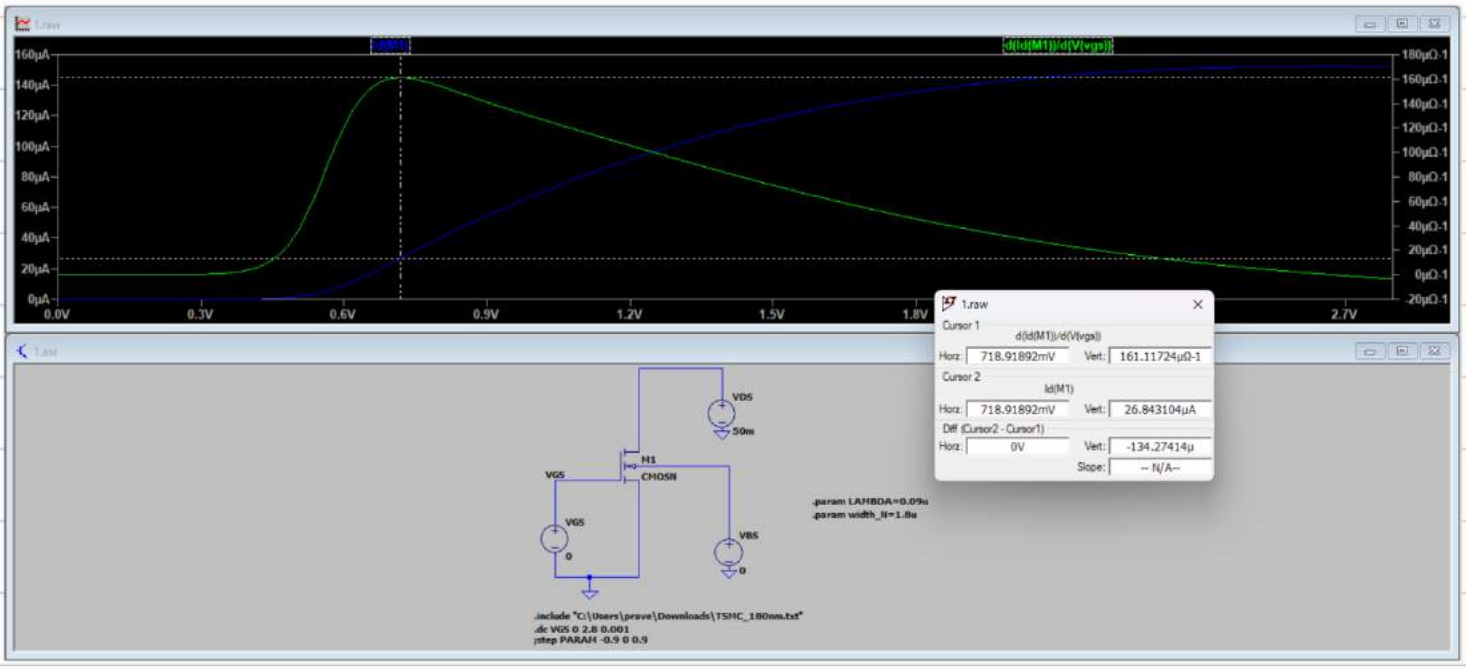
V_{GS} is sweeped from

0 to 2.8V with step of 0.001

(a) Estimation of V_T

To calculate the value V_T, we find a find where the slope of I_{DS} vs V_{GS} is maximum.
(It generally occurs in the linear mode).

Now, use the linear relation between I_D, V_{GS} and slope of the line.



Blue graph — I_D

Green graph — slope $\frac{dI_D}{d V_{GS}}$

Max slope = 161.11 μ ohm^{-1}

Point at which max slope is obtained = (718.418 mV, 26.843 µA).

In Linear Mode, $I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$

$$I_D \propto (V_{GS} - V_T)$$

$$\Rightarrow \quad I_D = (V_{GS} - V_T) \frac{d(I_D)}{d(V_{GS})}$$

$$26.843 \times 10^{-6} = (718.418 \times 10^{-3} - V_T) \times 161.11 \times 10^{-6}$$

$$\Rightarrow \quad V_T = 718.418 \times 10^{-3} - 0.1666$$

$$\boxed{V_T = 0.55138 \text{ V}}$$

∴ The threshold voltage when $V_{DS} = 50mV$ is 0.551 volt

Estimation of μC_{ox} :

Let, $V_{GS} = 1V$

Here $V_{GS} - V_T = 1 - 0.551$

$= 0.449 > 0.05$

$V_{GS} - V_T > V_{DS}$

∴ MOSFET is in Linear Mode.

Drain current in Linear Mode is given by

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

At $V_{GS} = 1V$, $I_D = 68.385\ \mu A$

$$\Rightarrow 68.385 \times 10^{-6} = \mu_n C_{ox} \frac{10}{0.18} \left[(1 - 0.551)\, 0.05 - \frac{(0.05)^2}{2} \right]$$

$$\mu_n C_{ox} = \frac{68.385 \times 10^{-6}}{10 \times (0.02248 - 0.00125)}$$

$$68.385 \times 10^{-6}$$

$$0.212$$

$$\mu_n C_{ox} = 322.570\ \mu A/V^2$$

(b) At $V_{DS} = 1.8V$

Here, the transistor is clearly in Saturation Mode.

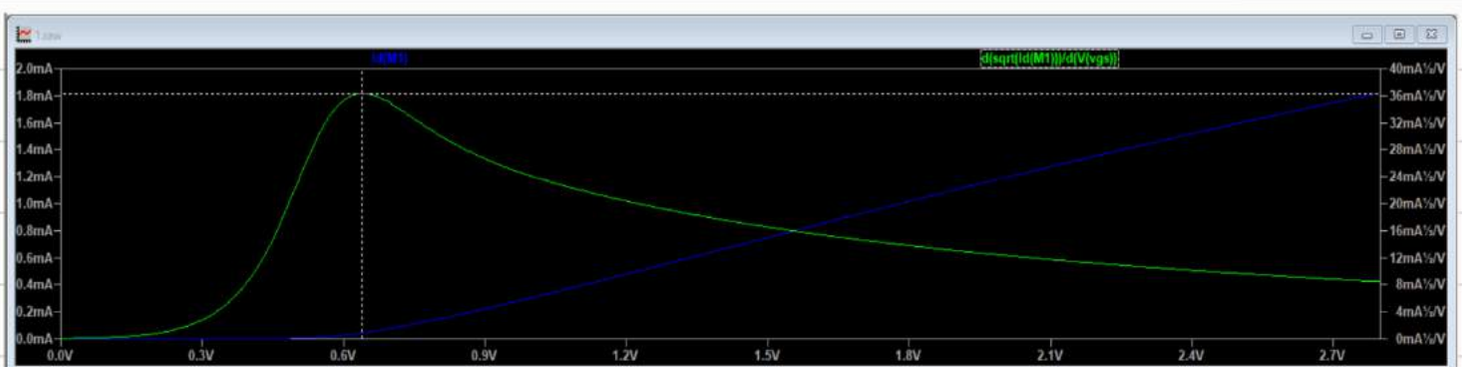
Then, the current equation is like

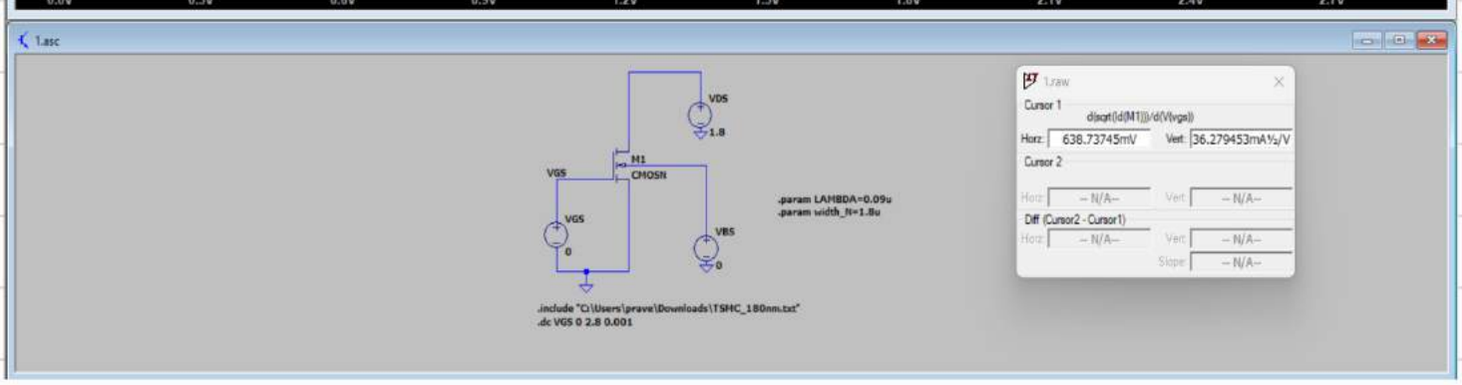
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_D \propto (V_{GS} - V_T)^2$$

$$\sqrt{I_D} \propto (V_{GS} - V_T) \quad \text{—— (1)}$$

Now obtain the maximum slope from the below plot of $\frac{\partial \sqrt{I_D}}{\partial V_{GS}}$ vs V_{GS} plot.





From the plot,

$$\frac{\partial \sqrt{I_D}}{\partial (V_{GS})} = 36.27945 \quad mA^{1/2}/V$$

The maximum slope is obtained at a point where

$I_D = 31.92352 \ \mu A$ and,

$V_{GS} = 638.73745 \ mV$

As, $\sqrt{I_D} \propto (V_{GS} - V_T)$

$$\sqrt{I_D} = (V_{GS} - V_T) \frac{\partial \sqrt{I_D}}{\partial V_{GS}}$$

$$\sqrt{31.9235 \times 10^{-6}} = (0.6387 - V_T)\ 36.279 \times 10^{-3}$$

$$0.15579 = 0.6387 - V_T$$

$$\therefore \boxed{V_T = 0.48296 \ V}$$

V_{DS}	V_T
50mV	0.551 V
1.8V	0.482 V

We can clearly see that there is a decrease in the threshold voltage (V_T) as V_{DS} increases.

Reason:

When V_{DS} is increased, there is an occurrence of a second-order effect called Drain-Induced Barrier Lowering (DIBL) in transistors.

* In saturation region, the velocity of the charge carriers gets saturated and for higher drain voltage pinch off region is effective as a result, we don't need much energy for inversion.
  Hence, V_T is reduced.

* Also, as $V_{DS} \uparrow$, it is like increasing the reverse bias voltage to an already reverse biased diode. This results in expansion of width of the depletion region, causing the voltage required to form an inversion layer to decrease.
  Hence, V_T decreases.

Question - 3 :

Given $\frac{W}{L} = \frac{0.18\ \mu m}{0.18\ \mu m}$

For NMOS Transistor,

Vary the value of V_{BS} from $-0.9V$ to $0.9V$.

V_{BS}	V_T
-0.9 V	612.45 mV
0	488.86 mV
0.9 V	225.60 mV

In an NMOS Transistor,

When the Body Voltage is less than zero $V_{BS} < 0$ i.e, the p-substrate is negetively charged.

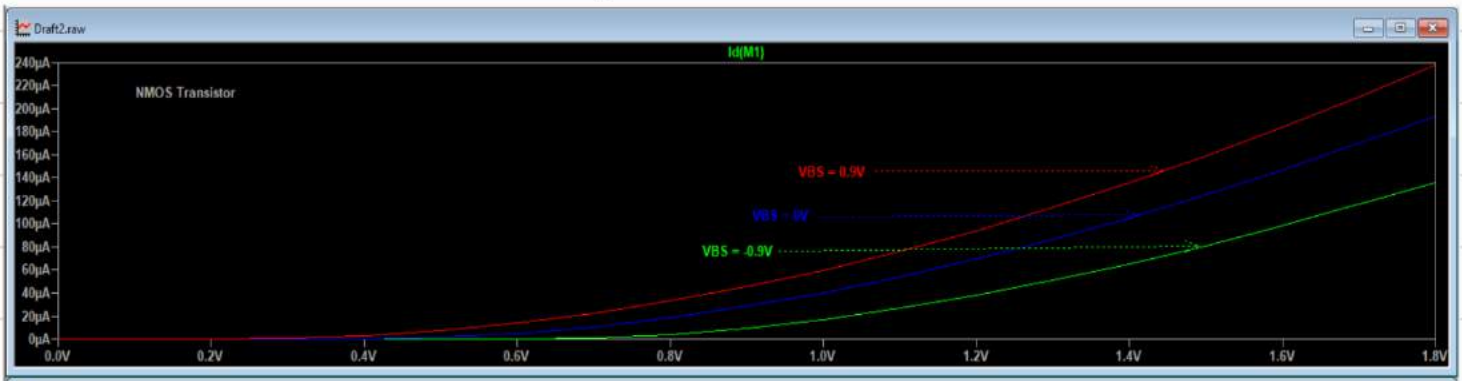
Here, the n^+ regions and the p-substrate in the MOSFET are in reverse-bias.

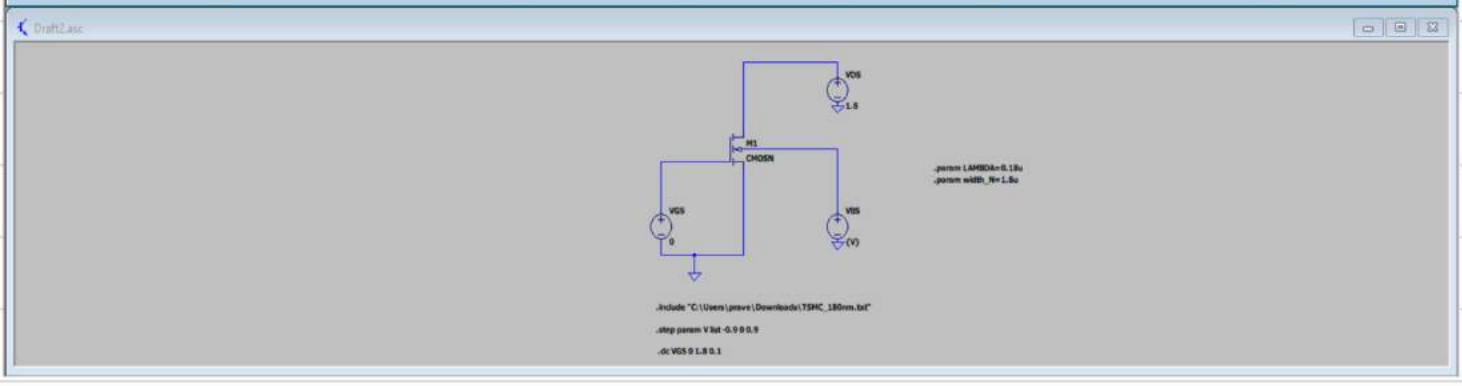
As a result of this, the $e^{\ominus}$ are further pushed into the n^+ regions. This makes it difficult for the channel formation and thus V_T increases.

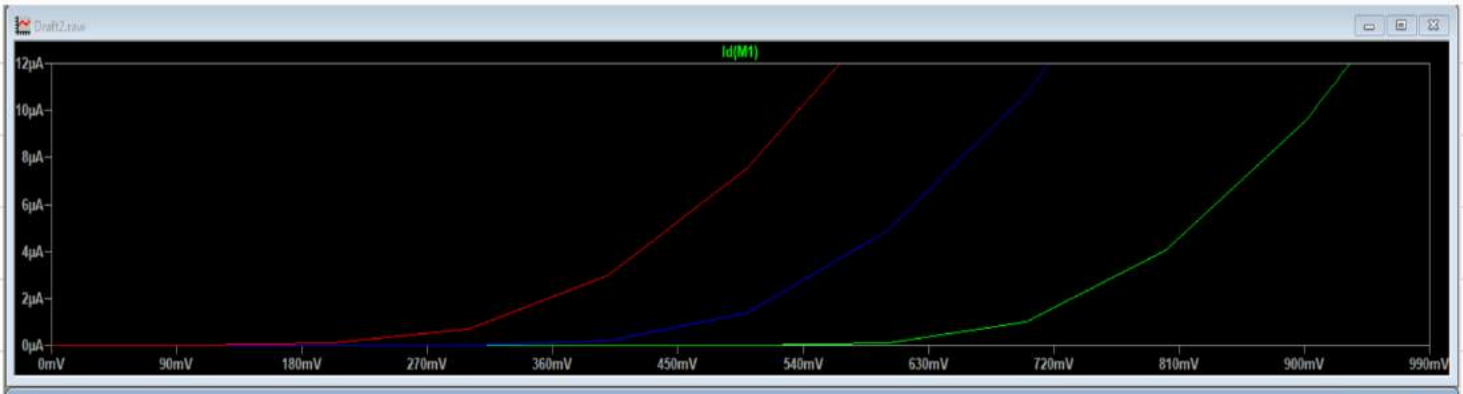
Conversely, when $V_{BS} > 0$, the substrate and the n^+ region are in forward bias. This makes more electrons being drawn out of the n^+ substrate due to the positive charge accumulation at the substrate's bottom. As a result, to enable conduction and fill the channel with $e^{\ominus}$, a lower threshold value is needed. Thus,

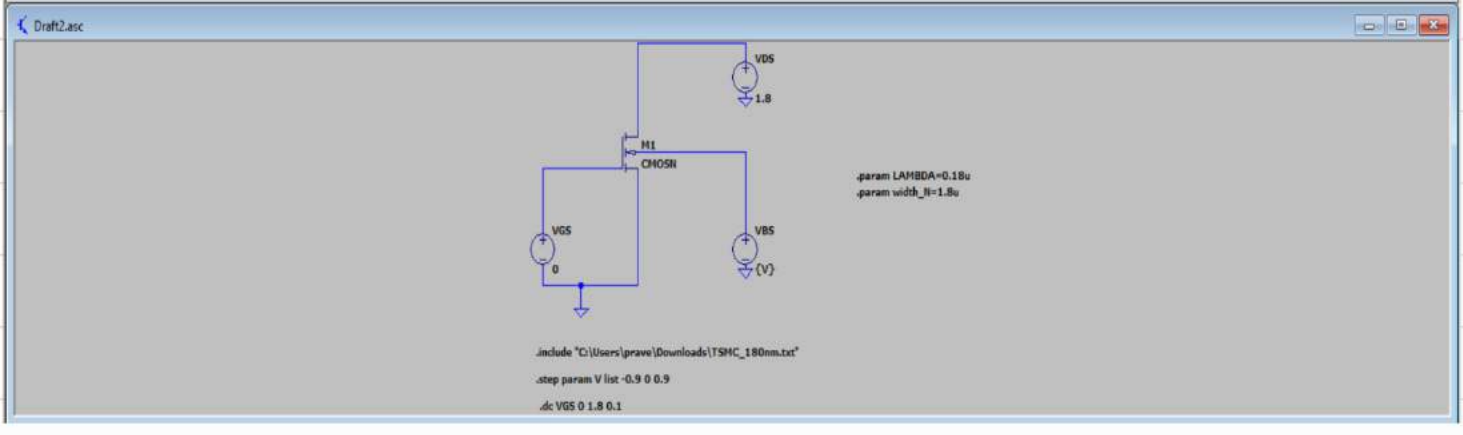
V_T decreases.

$$V_T = V_{T_0} + \gamma\left[\sqrt{2\phi_s + V_{SB}} - \sqrt{2\phi_s}\right]$$







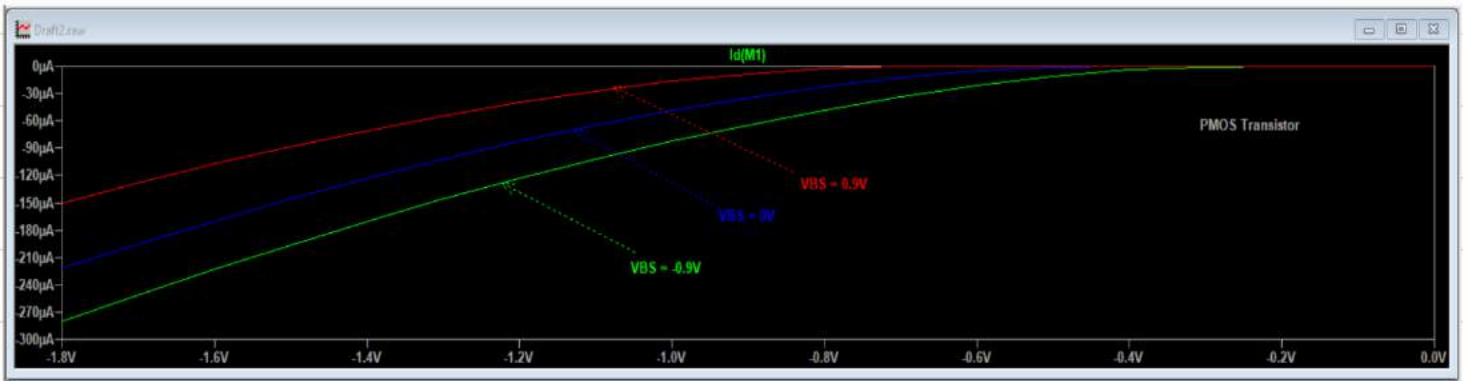


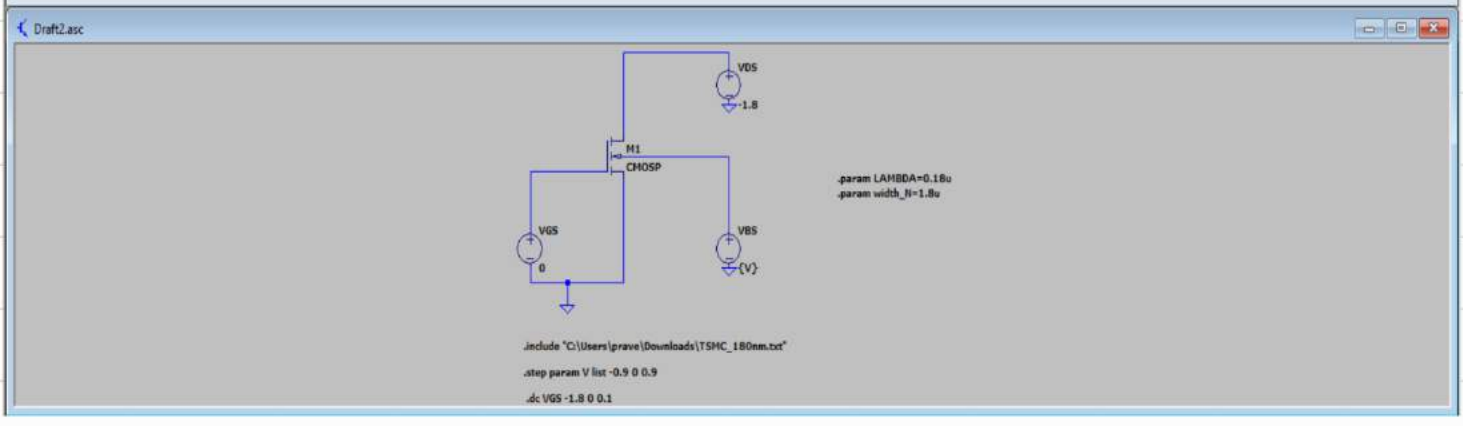
For PMOS Transistor,

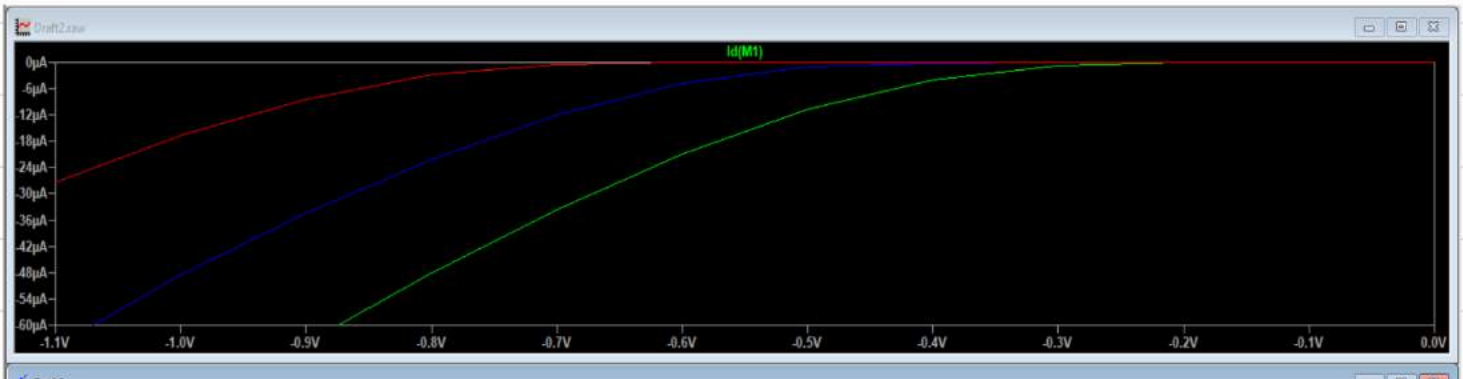
Vary the value of V_{BS} from $-0.9V$ to $0.9V$.

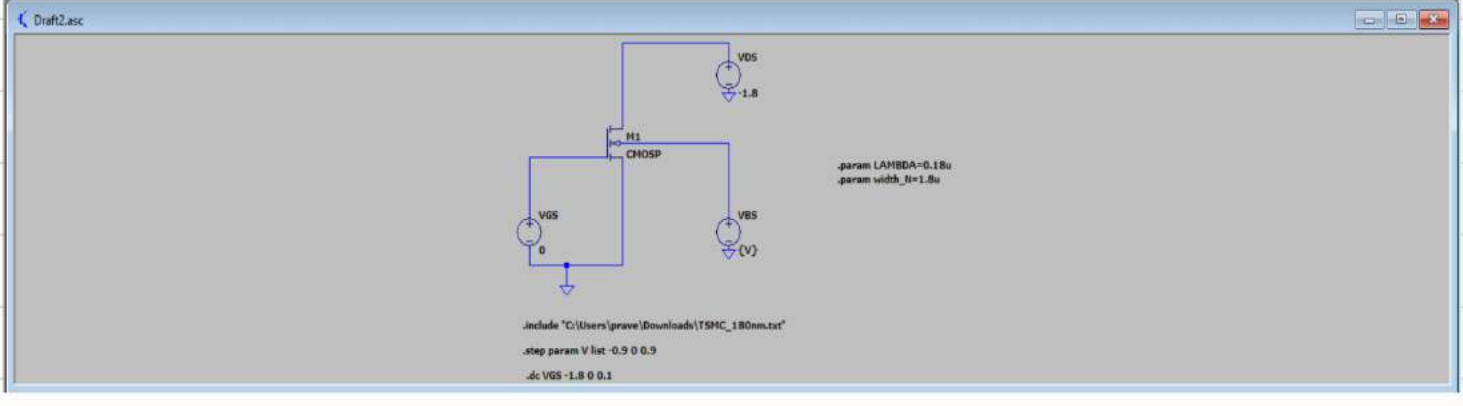
V_{BS}	V_T

−0.9 V	−229.23 mV
0	−486.850 mV
0.9 V	−649.8 mV









Explanation :

Here, we observe that as body-source voltage becomes more +ve, the

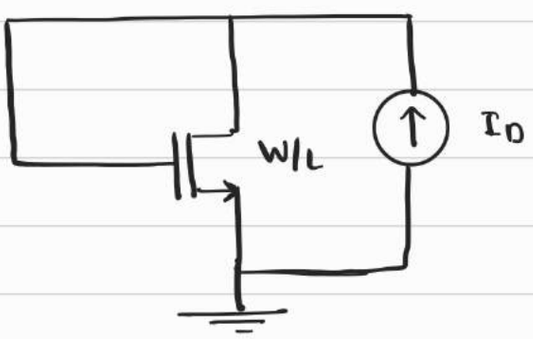
magnitude of V_T increases (for PMOS). This means that a more -ve voltage at the gate terminal is required to achieve the conduction in PMOS.

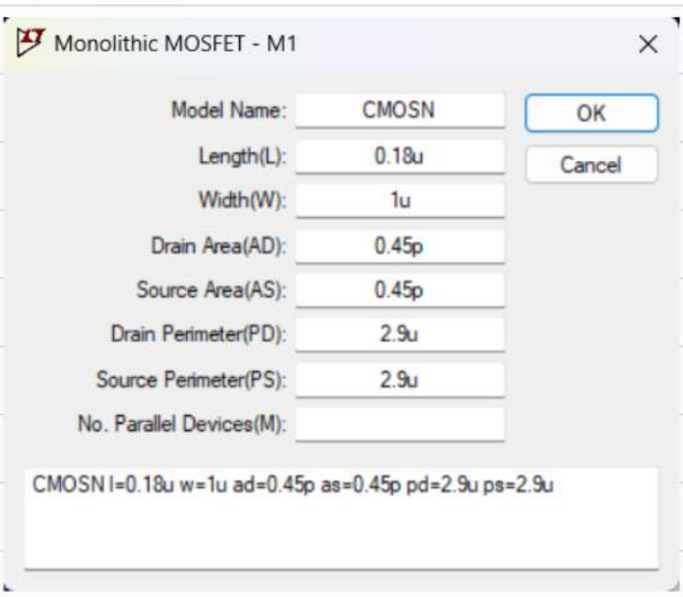
Let's consider the same capacitance as in NMOS, but now polarities are reversed. The gate and body terminals act as the negative plates of their respective capacitors, while the channel acts as positive plate. This reversal is due to the fact that PMOS transistors utilize holes as charge carriers.

When V_{BS} ↑ (becomes more +ve), the conc of holes in the channel decreases since it acts as the positive plate of the capacitor. Consequently, a more -ve charge at the gate terminal is needed to attract more holes into the channel and achieve state of inversion.

Question 4 :

Given,





Here,

$$\frac{W}{L} = \frac{1\ \mu m}{0.18\ \mu m}$$

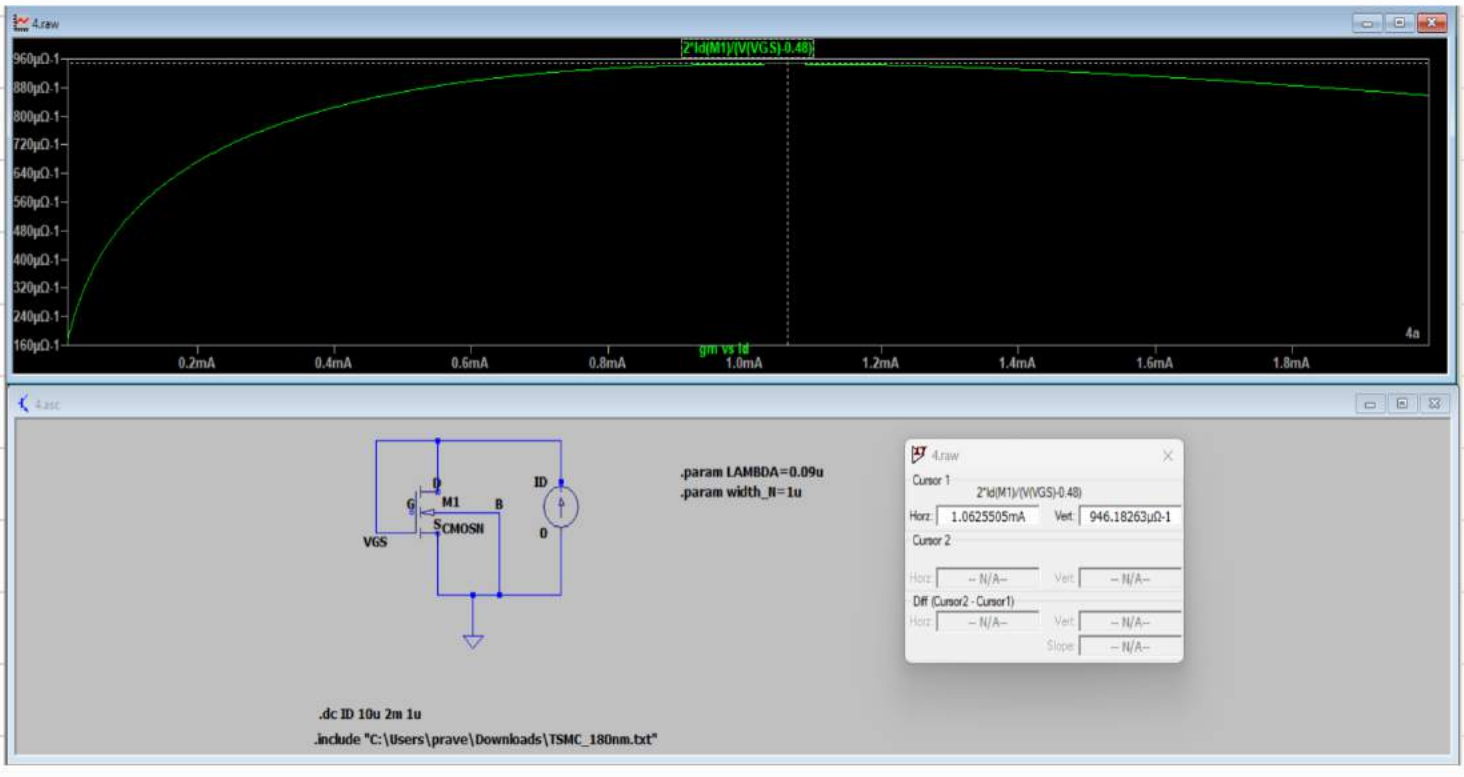
$V_T = 0.48\ V$

(from Q3 NMOS)

$$g_m = \frac{2I_D}{(V_{GS} - V_T)}$$

The plot of g_m vs I_D is given below

The $g_{m_{max}}$ is also plotted below.



Here, $g_{m_{max}} = 946.18263\ \mu\Omega^{-1}$

To achieve $4 \times g_{max}$:

The parameters that we can change are W and L.

$$g_m = \mu_N C_{ox} \frac{W}{L} (V_{GS} - V_T)$$

* But making a change in 'L' will also effect the V_T (threshold)

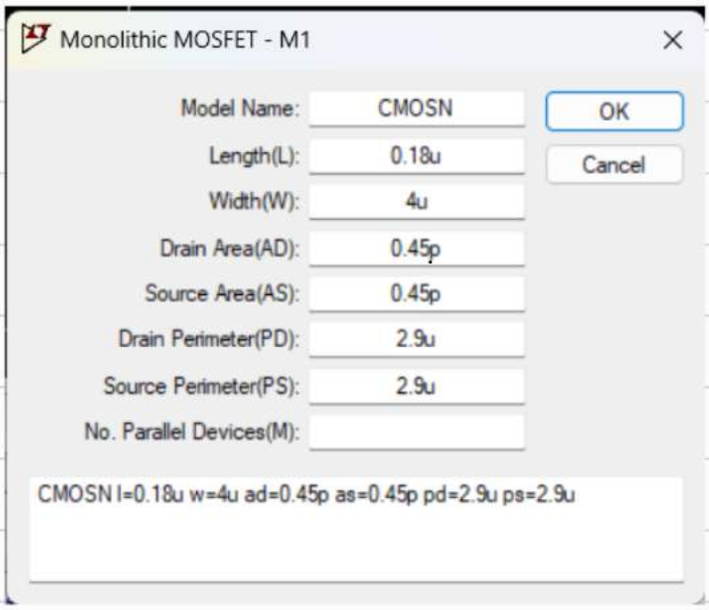
* Hence, we can modify width of transistor

Here, as $g_m \propto W$

To increase g_m by 4 times, width is increased by 4 times.

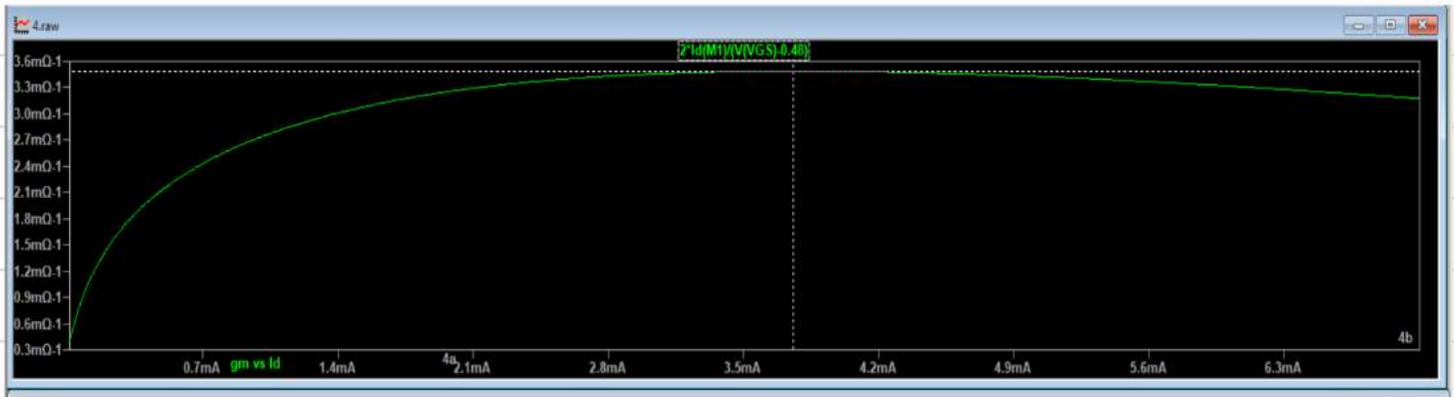
* Hence, $\boxed{W_{new} = 4\,\mu m}$

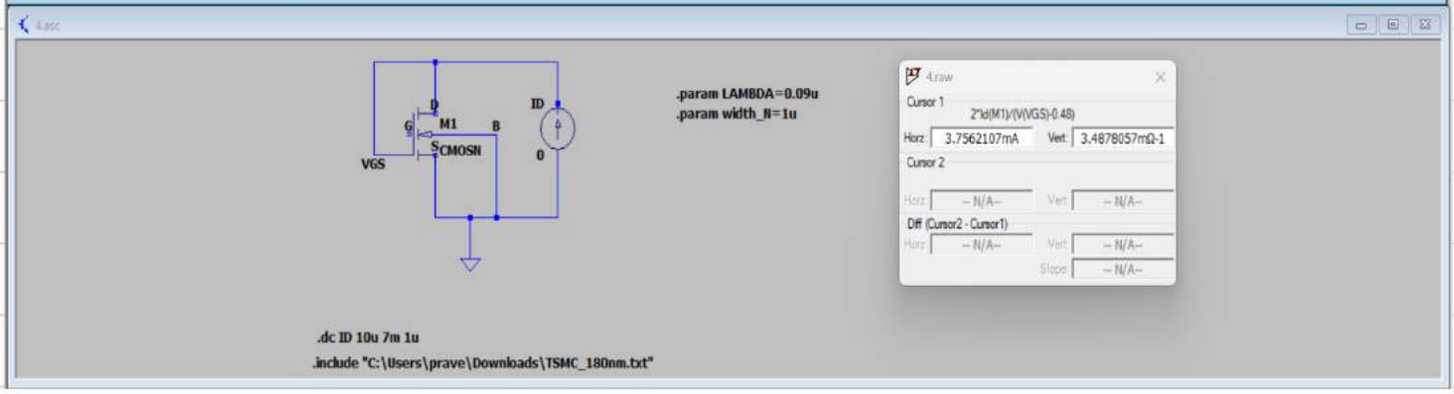
$$\left(\left((g_m)_{max} \right)_{New} \right)_{calculated} = 4 \times 946.182\ \mu\Omega^{-1}$$
$$= 3.784\ m\Omega^{-1}$$



$L = 0.18\,\mu m$

$W = 4\,\mu m$





Experimental Result :

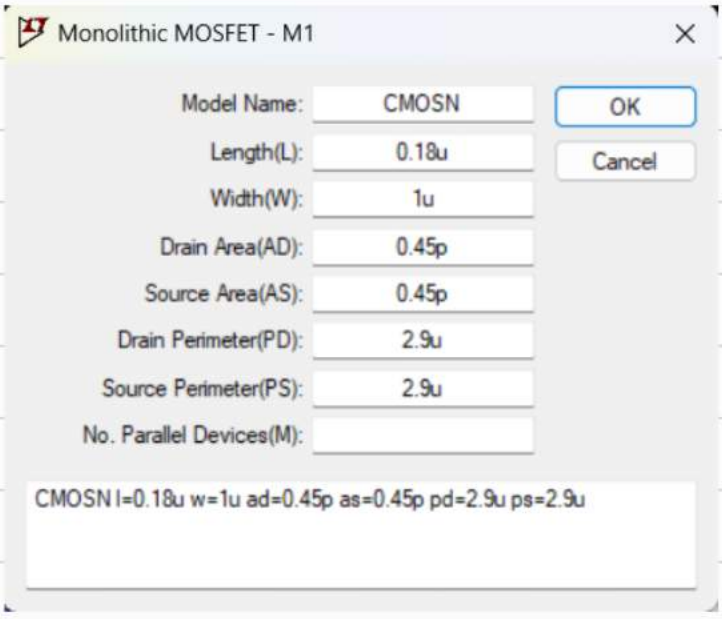
$$\left[(g_m)_{max}\right]_{New} = 4 \times g_{m_{max}}$$

$$\boxed{\left[(g_m)_{max}\right]_{New} = 3.4878 \ m\Omega^{-1}} \quad \text{(experimental)}$$

The calculated and experimental results are almost similar.

Question 5 :

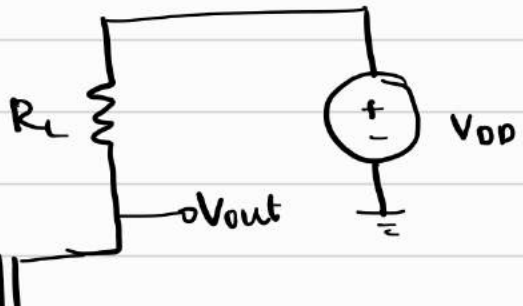
Given,

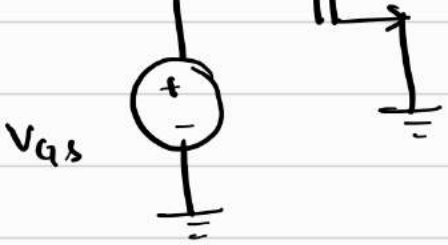


$$\frac{W}{L} = \frac{1\,\mu m}{0.18\,\mu m}$$

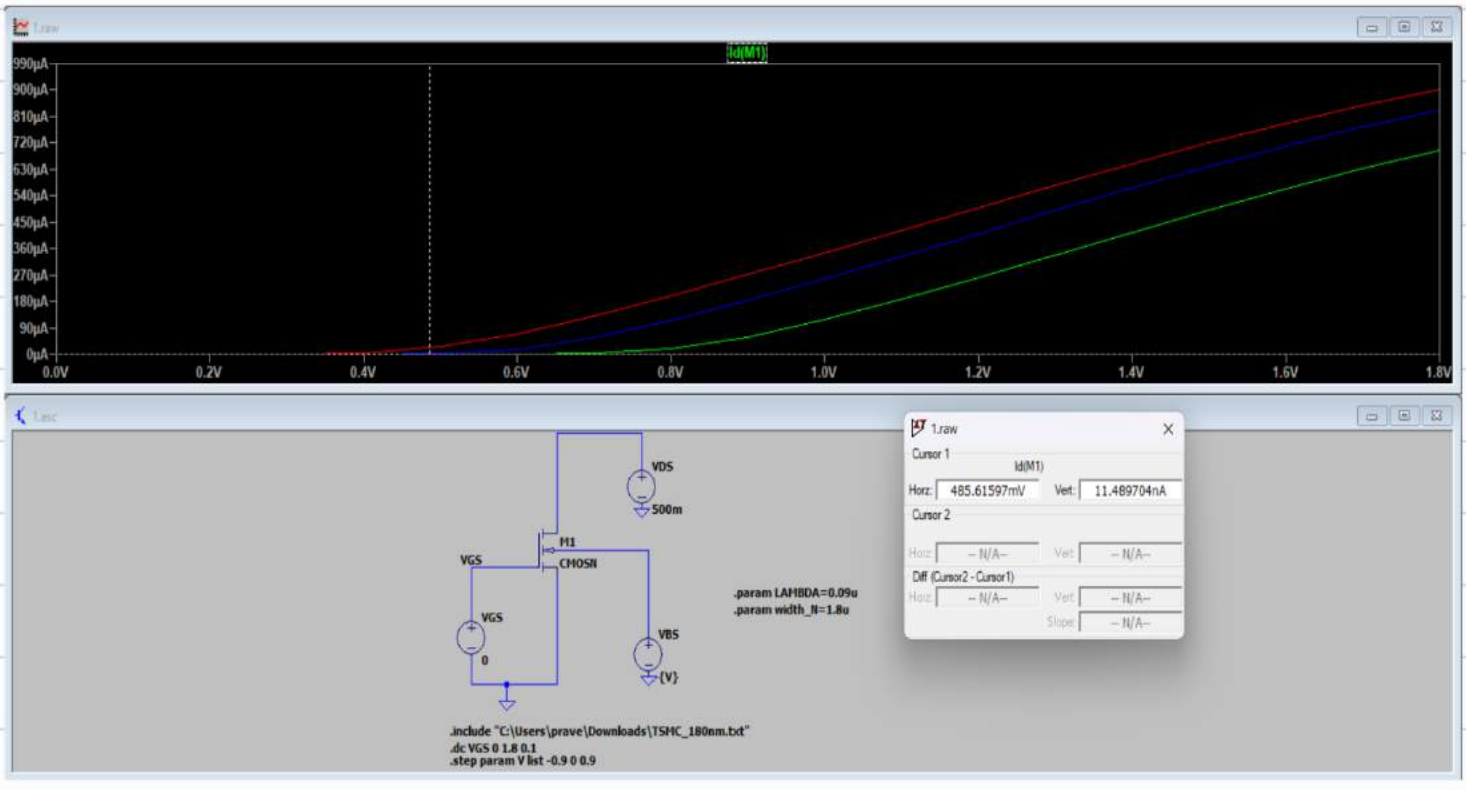
$$V_{DD} = 500\ mV$$

$$R_L = 1k\Omega$$

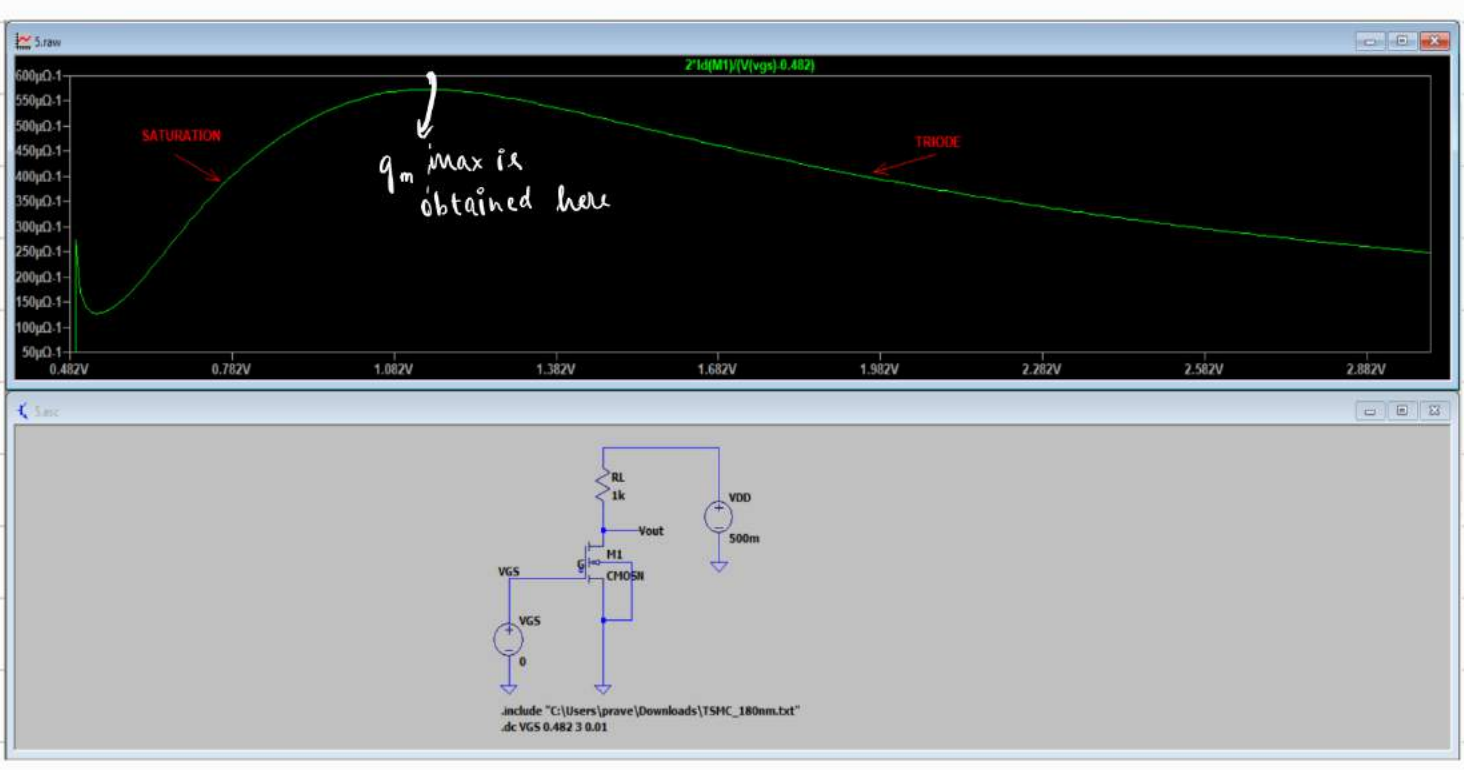


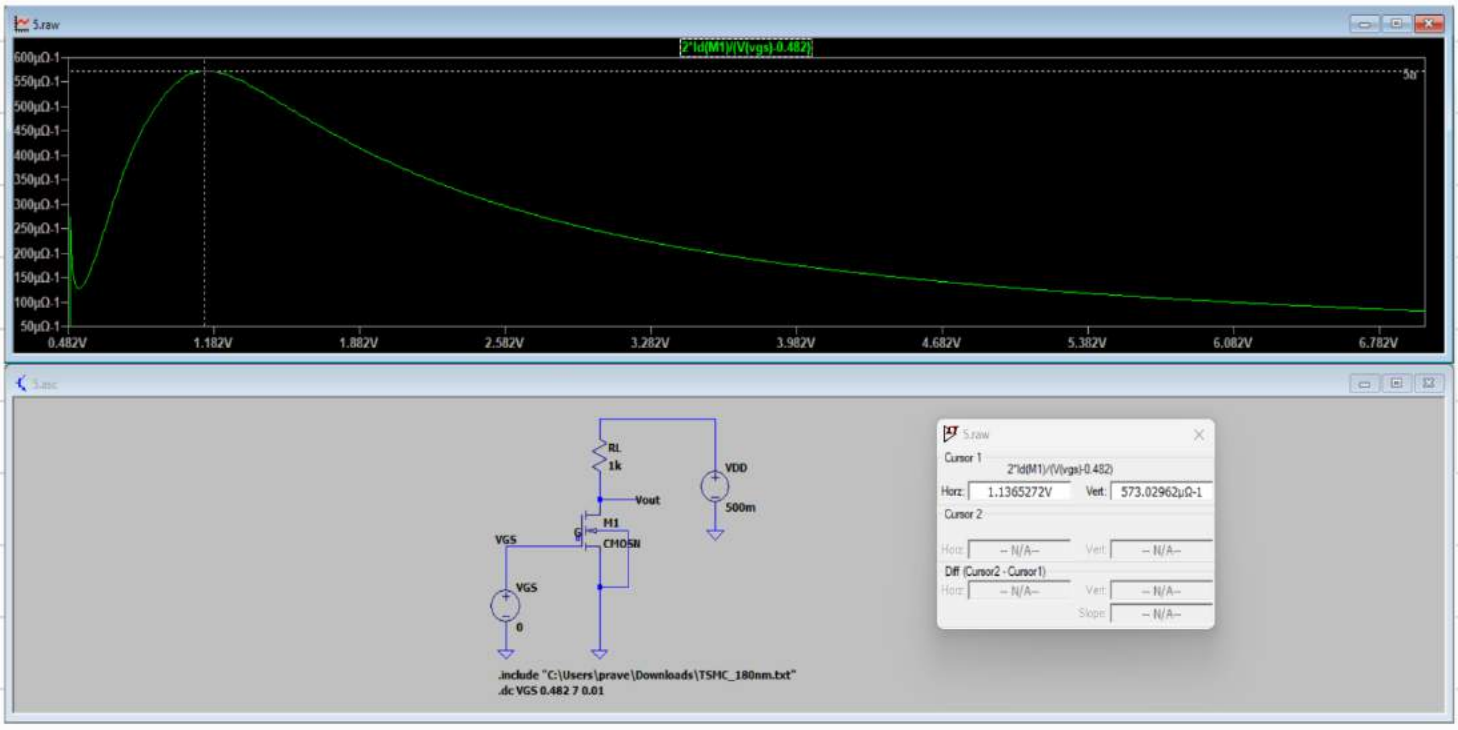

VGS

$V_T = 0.485\ V$


Id(M1)
990µA
900µA
810µA
720µA
630µA
540µA
450µA
360µA
270µA
180µA
90µA
0µA
0.0V
0.2V
0.4V
0.6V
0.8V
1.0V
1.2V
1.4V
1.6V
1.8V
VDS
500m
M1
CMOSN
VGS
VGS
0
VBS
{V}
.param LAMBDA=0.09u
.param width_N=1.8u
.include "C:\Users\prave\Downloads\TSMC_180nm.txt"
.dc VGS 0 1.8 0.1
.step param V list -0.9 0 0.9
1.raw
Cursor 1
Id(M1)
Horz: 485.61597mV
Vert: 11.489704nA
Cursor 2
Diff (Cursor2 - Cursor1)
Slope

(a)


2*Id(M1)/(V(vgs)-0.482)
600µΩ-1
550µΩ-1
500µΩ-1
450µΩ-1
400µΩ-1
350µΩ-1
300µΩ-1
250µΩ-1
200µΩ-1
150µΩ-1
100µΩ-1
50µΩ-1
0.482V
0.782V
1.082V
1.382V
1.682V
1.982V
2.282V
2.582V
2.882V
SATURATION
TRIODE
g_m max is obtained here
RL
1k
VDD
500m
Vout
M1
CMOSN
VGS
VGS
0
.include "C:\Users\prave\Downloads\TSMC_180nm.txt"
.dc VGS 0.482 3 0.01



From the above graph, we can see that

$$(g_m)_{max} = 573.0296 \ \mu\Omega^{-1}$$

at $V_{GS} = 1.136\ V$

Cut-off Region:

The condn' for cut-off is

$$V_{GS} < V_{TH}$$

But here $V_{GS} = 1.136 > V_{TH} = 0.48\ V$

Thus, cut off region can't be seen.

Saturation Region:

For $V_{GS} < 1.1365272\ V$

the transistor is in saturation.

→ In saturation, the MOSFET is active, where drain current is very high and varies linearly with V_{GS}. As a result, transconductance increases, with high sensitivity.

Triode Region:

For $V_{GS} > 1.1365272\ V$

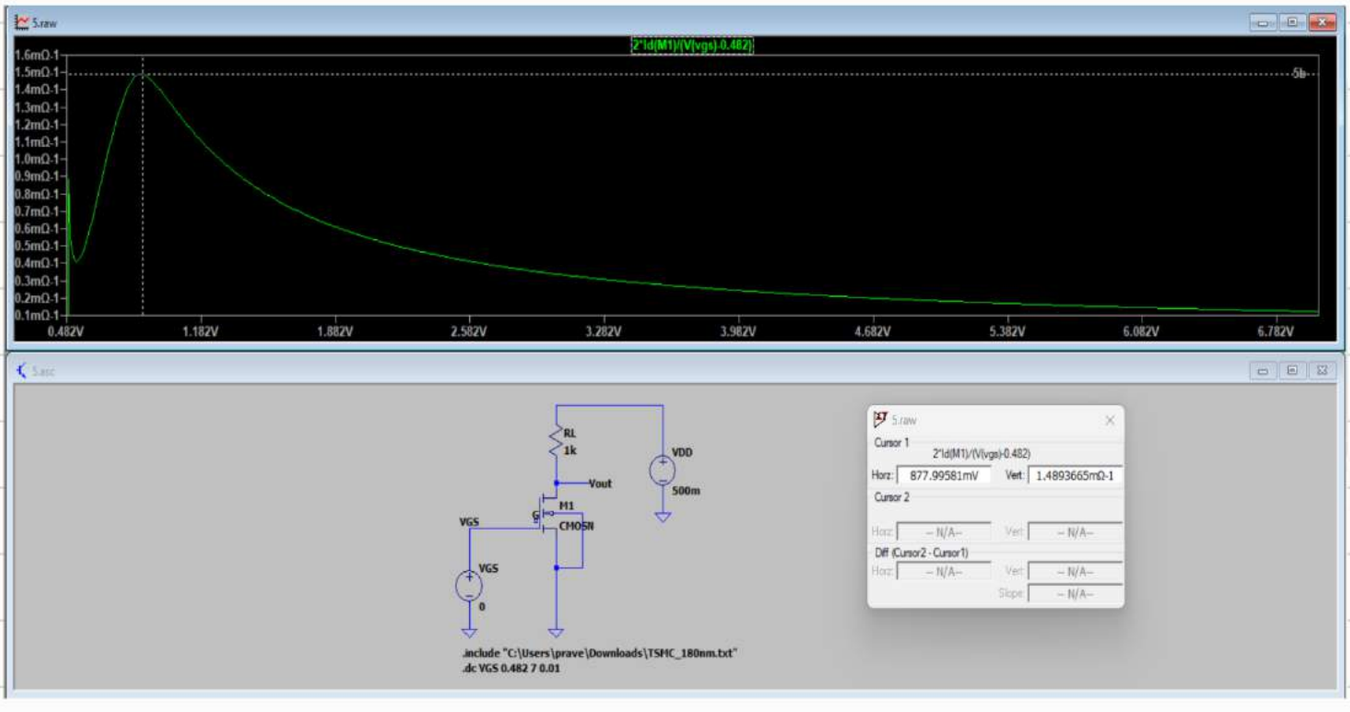
the transistor is in Linear Mode.

→ Generally, when MOSFET is in Linear mode, it has low drain currents.

In this region, MOSFET operates as a voltage-controlled resistor, and its transconductance is lower than when in saturation, since I_D is less.

Here,
$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

(b) Now, $\frac{W}{L} = \frac{4\mu m}{0.18\mu m}$



Now, g_m value is obtained at $V_{GS} = 877.9958$ mV

$$\boxed{g_m = 1.4893 \text{ m}\Omega^{-1}}$$

For $V_{GS} < 877.9958$ mV

└ transistor is in Saturation Mode

$V_{GS} > 877.9958$ mV

└ transistor is in Linear Mode

Trade-Offs :

Gain :

We know that gain $\propto g_m$

$$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}}$$

$$g_m \propto \sqrt{W}$$

$$\Rightarrow \text{gain} \propto \sqrt{W}$$

Thus, as width ↑, gain also ↑.

∴ For $W = 4\mu m$, the amplifier gain will be higher than at $W = 1\mu m$.

Swing :

The input AC swing trade-off is impacted by the

changes in MOSFET's parameters.

Bias points may be encountered as the gain of the amplifier is increased, where the amplified sinusoidal signals crosses the MOSFET's ability to handle.

As a result, the MOSFET can switch to linear mode, which is inappropriate for an amplifier. To maintain amplifier performance, this trade-off between transconductance and AC swing needs to be carefully maintained.

→ Clipping occurs when output signal exceeds the upper or lower bounds of the amplifier, resulting in distortion.

Here, swing is more when $W = 1\,\mu m$.

Bandwidth:

When width of MOSFET is increased, the gain increases, along with this there is also an increase in the capacitance.

$$W\uparrow \Rightarrow A\uparrow \Rightarrow C = \frac{\varepsilon_0 A}{d}$$

$$\Rightarrow C\uparrow$$

∴ Overdrive Capacitance increases

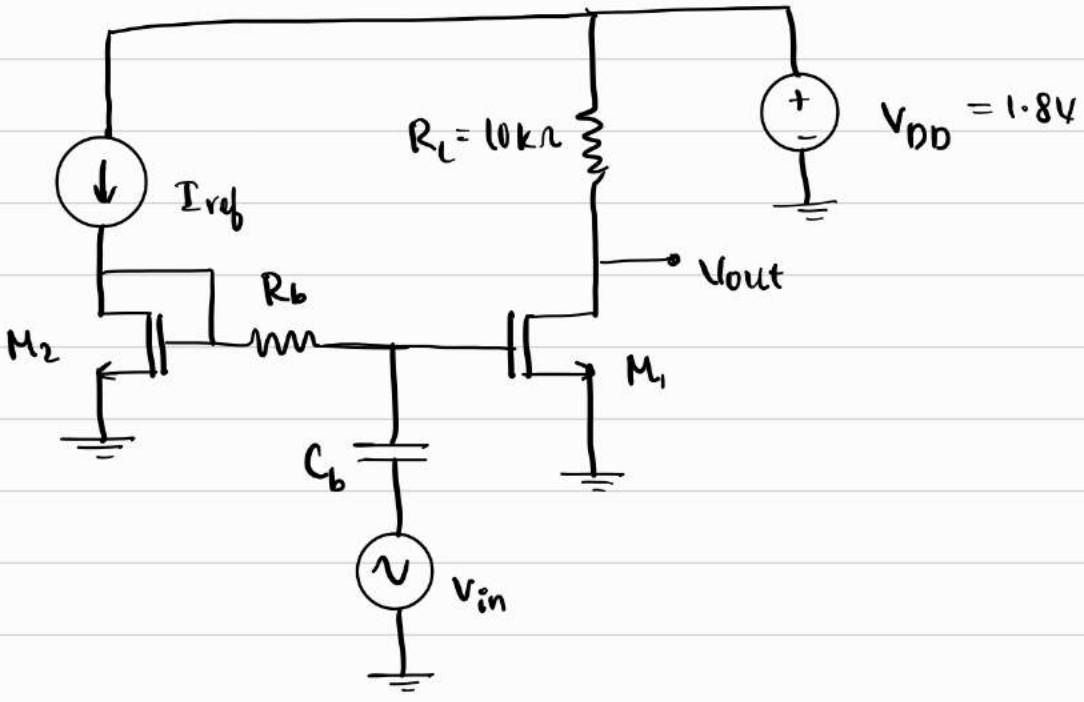
⇒ As $C\uparrow$, the bandwidth decreases, which limits the range of frequencies over which

the amplifier can amplify the signals.

∴ In such a way, there is a trade-off between gain, swing and bandwidth when width of the MOSFET is adjusted.

Question -6

Given,



$R_L = 10\,k\Omega$

Voltage gain, $A_v > 5$

$V_{GS} - V_T = 200\,mV$ (overdrive voltage)

$f = 100\,Hz$

Let us begin by assuming

Gain, $A_V = 10$ — Assumption 1

then $g_m R_L = 10$

$$g_m = \frac{10}{10K\Omega}$$

$$\boxed{g_m = 1m\Omega^{-1}}$$

For MOSFET M_2 :

$$V_{GS} = V_{DS}$$

$$V_{DS} - V_{GS} = 0 \geq -V_{TH}$$

$\therefore$ M_2 is always in saturation Mode.

$$I_{D_2} = I_{ref} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS_2} - V_T)^2$$

For MOSFET M_1 :

$$V_{GS} - V_T = 200mV$$

Even M_1 is in saturation as

$$V_{DS} = V_{DD} - I_{ref} R_L$$

$$I_{D_1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS_1} - V_T)^2$$

Since gate current of both Mosfets is 0

$$\Rightarrow V_{GS_1} = V_{GS_2}$$

Now,

$$\frac{I_{D_1}}{I_{ref}} = \frac{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS_1} - V_T)^2}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right) (V_{GS_2} - V_T)^2}$$

(considering same technology parameters)

$$\Rightarrow \quad \frac{I_D}{I_{ref}} = \frac{(W/L)_1}{(W/L)_2}$$

Consider that both MOSFETs are identical

└ Assumption 2

Then, $\boxed{I_{D_1} = I_{ref}}$

Now, $$g_m = \frac{2 I_D}{V_{GS} - V_t}$$

$$I_D = \frac{(1 m\Omega^{-1}) \times (200 mV)}{2}$$

$$= 100 \times 10^{-6} \text{ A}$$

$$= 10^{-4} \text{ A}$$

$$\boxed{I_{ref} = I_D = 0.1 \text{ mA}} = 100 \mu A$$

Now, to find the technology parameters, let us take the value of $\mu_n C_{ox}$ from previous question,

$$\mu_n C_{ox} = 322.570 \ \mu A/V^2$$ — Assumption 3

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_t)$$

$$\frac{W}{L} = \frac{g_m}{\mu_n C_{ox} (V_{GS} - V_t)}$$

$$\mu_n C_{ox} (V_{GS} - V_t)$$

$$= \frac{10^{-3}\, 10^{3}}{322.570 \times 10^{-6} \times 0.2}$$

$$\boxed{\frac{W}{L} = 15.5}$$

Let us take $\boxed{L = 0.18\ \mu m}$ — Assumption 4

$$\Rightarrow \boxed{W = 2.79\ \mu m}$$

Next, Minimum input frequency, $f = 100$ Hz

$$f \geq \frac{1}{2\pi R_b C_b}$$

let $C = 10$ nF

$$R_b C_b < \frac{1}{2\pi f}$$

$$R_b < \frac{1}{200\pi (10n}$$

$$R_b < \frac{5 \times 10^{7}}{\pi}$$

let $\boxed{R_b = 5M\Omega}$

Total power consumed = $V_{DD}\, I$

$$= V_{DD}\left(I_{ref} + I_D\right)$$

$$= V_{DD}\left(2 I_D\right)$$

$$= 1.8\left(2(0.1)\,m\right)$$

$$\boxed{P_D = 0.36\ mW}$$

(a) Finally,

$$W = 2.79\ \mu m$$

$$L = 0.18\ \mu m$$

$$\lambda = \frac{L}{2} = 0.09\ \mu m$$

$$AS = AD = SW\lambda = 1.25\ pm^2$$

$$PS = PD = 10\lambda + 2W = 6.48\ \mu m$$

$$I_{ref} = 0.1\,mA$$

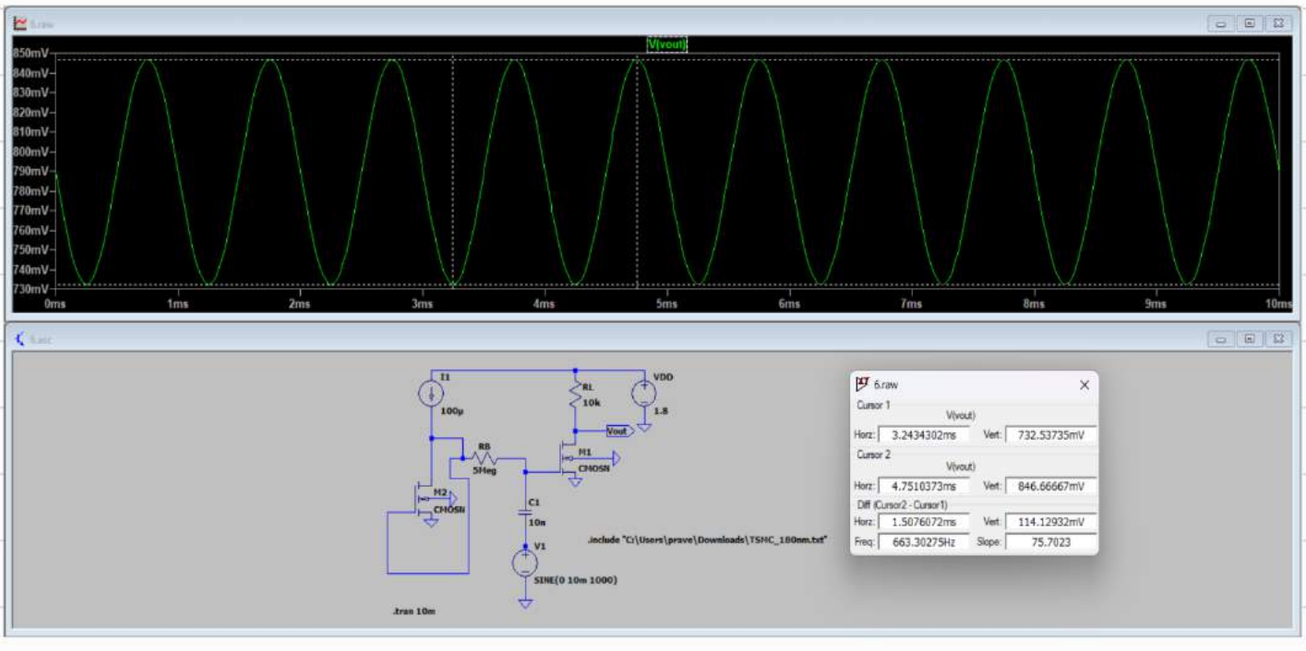
$$C_b = 10\,pF$$

$$R_b = 5\,M\Omega$$

Power consumed = 0.36 mW

(b) $v_{in} = 10\sin\left(2\pi(1000)t\right)$

Given below is the plot of V_{out} vs time



Calculate the value of V_{out} :

$$V_{out} = 846.66\ mV - 732.53\ mV$$
$$= 114.1293\ mV$$

$$V_{in} = 10mV \quad (given)$$

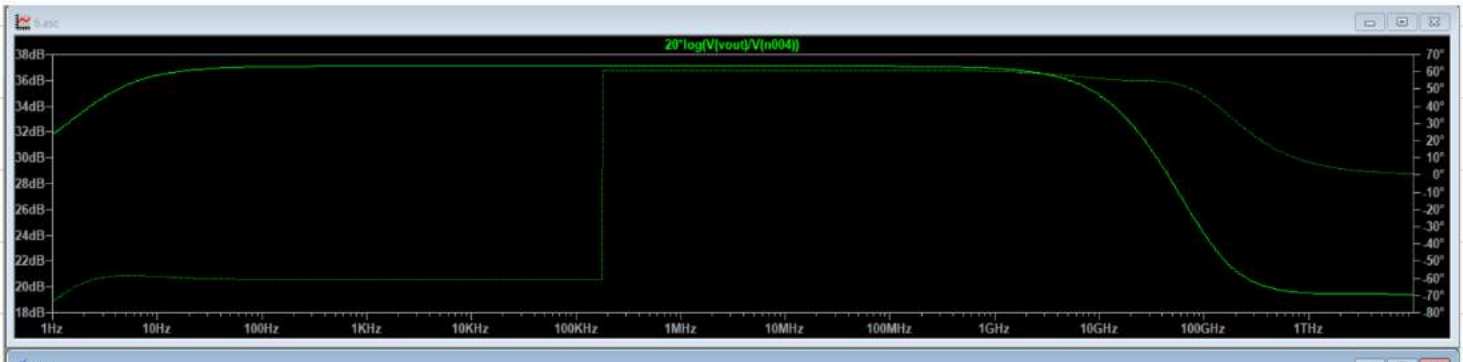
$$Gain = \frac{V_{out}}{V_{in}} = \frac{114.12\ mV}{10\ mV}$$

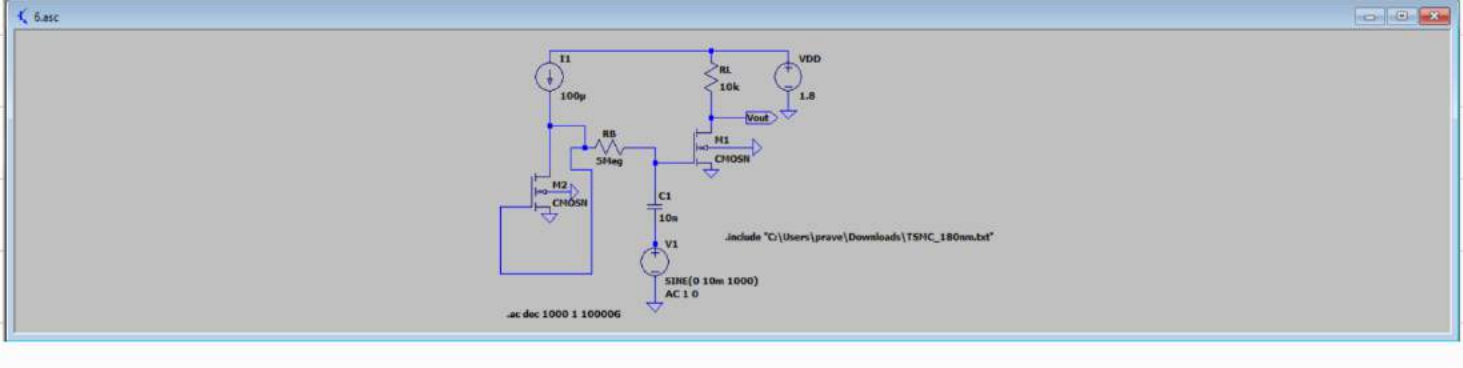
$$Gain = 11.4$$

$$Gain \approx 10$$

which is almost closer to the gain value we have assumed.

(d) Plot of AC response $(20\log|A_V|$ vs freq$)$





Unity bandwidth frequency:

→ The is a frequency where gain = 1

→ This means that $20\left(\log\left|\frac{V_{out}}{V_{in}}\right|\right) = 0$

→ But the above graph is never seen to be 0.

→ Therefore, unity bandwidth frequency does not exist.