Analog Electronic Circuits Lab (EC2.103, Spring 2023)

TAs: Adithya, Swarnim, Deeksha, Nitin, Prasanth; Lab Admin: Prashant Instructor: Prof. Abhishek Srivastava, CVEST, IIIT Hyderabad

Instructions:

- 1. Systematically record all your observations in the lab book (mandatory)
- 2. Save results in USB or take pictures
- 3. Make meaningful tables to summarize your findings and show it to the instructor(s) during the lab session only
- 4. Bring your calculators and DMM (if available)
- 5. Handle equipment carefully and report in case of any incidence
- 6. Enjoy your time in lab and strengthen your understanding about circuits

Experiment-6

MOSFET: I-V and Voltage transfer characteristics (VTC)

1. I_D vs V_{DS} characteristics

As shown in Fig. 1, in this experiment we will use operational amplifier to plot the required NMOS characteristics. The MOSFET you are going to use is an n-channel device (NMOS), having its Gate, Source, and Drain terminals available at pins 3, 4 and 5 of the IC CD4007BE in figure 2. All NMOS devices in the IC have a common substrate (pin 7). In Fig. 1, $V_2 = V_{DS}$ and $V_0 = -I_2 \times R_0 = -I_D \times R_0$, where $R_0 = 1 \ k\Omega$ (between node 2 and 6). Therefore plot of I_D will be proportional to V_0 . We will sweep $V_2 = V_{DS}$ using the function generator and plot $V_0 (\propto -I_D)$.

(a) Connect the NMOS and other components in the configuration as shown in Fig. 1, with pin 7 of MOS IC connected to ground. The internal configuration of the NMOS is also shown in Fig. 2(a). The PIN diagram of the operational amplifier and MOS IC used is as shown in Fig. 2(b) and 2(c), respectively . Verify the potentiometer output using the multimeter or DSO and observe that the output voltage varies between -4 V and 4V. Please note that potentiometer is a variable resistor, which is used here to vary the V_{GS} . Also note that opamp uses dual supply $(\pm 12\ V)$.

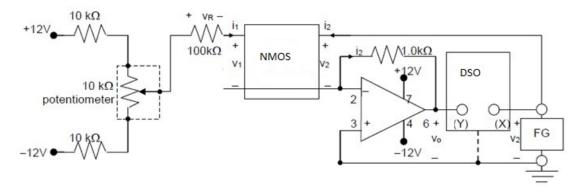


Figure 1: Circuit for displaying the output i-v characteristics of MOSFET

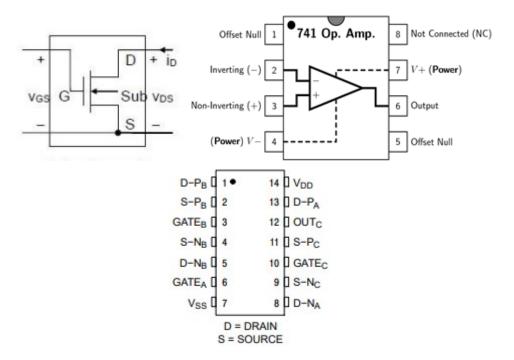


Figure 2: (a) NMOS, (b) opamp pin configuration (c) MOS Pin configuration

(b) Provide a 100 Hz sine wave input with peak to peak voltage of 8 V and offset of 4 V at the D terminal of the NMOS using the function generator. Channel 1 of the DSO is also connected to D terminal and channel 2 is connected at the output of the opamp (V_0) . Observe the characteristic waveform obtained using the acquire function of the DSO by varying the V_{GS} (potentiometer resistance) and report parameters shown in Table 2 from the measured results for $V_{GS} = \{0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1, 1.2, 1.4, 1.6, 1.8, 2, 3 and 4\} V, where <math>V_{GS}$ is the voltage at potentiometer output.

V_{GS}	V_{DS}	V_o	I_D

Table 1

2. I_D vs V_{GS} characteristics and parameter extraction $(V_T \& \mu_n C_{ox} \frac{W}{L})$

- (a) To sweep V_{GS} , connect the function generator across the gate terminal and the potentiometer across the drain terminal. Give a sinusoidal signal from function generator to the gate to sweep similar to the 1st question. Plot I_D vs V_{GS} for $V_{DS}=0.1,\ 0.5,\ 1,\ 2,\ 3,\ 4\ V$ and tabulate similar to table 2.
- (b) To determine the value of V_T of the given NMOS, bias the MOSFET in linear region by using sufficiently smaller value of $V_{DS} (= 100 \ mV)$ and plot I_D vs V_{GS} by sweeping V_{GS} from 0 to 4 V. Find the point (P) of maximum slope $(\frac{dI_D}{dV_{GS}})$ (by inspection use cursors) on the plot. Find the point (V_T) on V_{GS} axis, where the tangent drawn at 'P' will intersect.
- (c) To find the value of $\mu C_{ox} \frac{W}{L}$, use the current equation of NMOS in linear region (Eq. 1) at point 'P'.

$$I_D \approx \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS} \tag{1}$$

3. Large signal analysis and voltage transfer characteristic (VTC) of MOS based amplifier Consider the NMOS based amplifier with a resistive load as shown in figure 3.

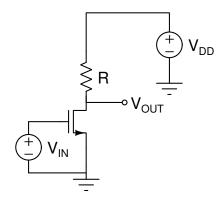


Figure 3: Circuit for large signal analysis and to plot VTC (V_{OUT} vs V_{IN}) of MOS based amplifier

- (a) Refer to pin diagram of IC CD4007BE in figure 2. Use any one NMOS in IC (example: Use pin number 3,4,5). Connect the resistor (1 k Ω), input signal and V_{DD} in the circuit.
- (b) Use WaveGen to provide input signal which should be between 0 to 5V (hint: use offset). Plot V_{OUT} vs V_{IN} using acquire function in DSO.
- (c) In the obtained VTC plot, mark the modes of operation (cut-off/linear/saturation) of MOS-FET. Report any 3 values of input and output voltages corresponding to these different modes.
- (d) For each input DC voltage (V_{DC}) obtained in previous step, apply an ac signal (v_{in}) with 10 mV amplitude and 10 kHz frequency) on top of it and measure the amplitude of output ac signal. Report gain $(\frac{v_{out}}{v_{in}})$. Repeat it for $v_{in} = 50, 100, 500, 1000 \ mV$. (hint: Use WaveGen to get Sinusoidal signal with a offset for input DC value)
- (e) Make a table using the above data and clearly mention your observations and trends. (hint: gain and voltage swing)

V_{DC}	v_{in}	v_{out}	Gain

Table 2