Analog Electronic Circuits (EC2.103) : Assignment-5

Spring 2024, IIIT Hyderabad, Due date : Fri 29 Mar, 2024 (18:00 hrs)

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Instructions:

1. Submit your assignment as a single pdf (Name_RollNo.pdf) at moodle on or before the due date
2. Hand-written/typed (latex/word/notion/others) submissions are allowed
3. Report should be self explanatory and must carry complete solution - Answers with schematics, SPICE directives, annotated waveforms, inference/discussion on results
4. Use the given technology file TSMC_180nm.txt for simulations
5. Specify MOSFET parameters W, L, AS, AD, PS, PD for all simulations

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1. As shown in Fig. 1, plot I_D vs V_{DS} for an NMOS transistor having $\frac{W}{L} = \frac{1.8\mu}{0.18\mu}$ by sweeping V_{DS} from 0 to 1.8 V in a step of 0.01 V and sweeping V_{GS} 0 to 1.8 V in a step of 0.3 V. Assume $V_{BS} = 0\ V$.
   (Hint: *Use NMOS4 from library, edit and change model name to CMOSN, enter W, L, drain/source area (AD/AS), drain/source perimeter (PD/PS) as follows:* $AS = \{5 * width\_N * LAMBDA\},\ PS = \{10 * LAMBDA + 2 * width\_N\},\ AD = \{5 * width\_N * LAMBDA\},\ PD = \{10 * LAMBDA + 2 * width\_N\},\ where\ \{width\_N\} = W,\ \&\ \{2 * LAMBDA\} = L$. *Use ".include TSMC_180nm.txt" in the spice directive.)*

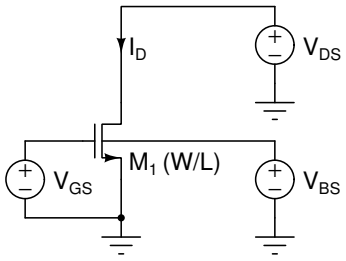

Figure 1

2. Plot I_D vs V_{GS} for $\frac{1.8\mu}{0.18\mu}$ NMOS transistor for V_{DS} = 50 mV and $V_{BS} = 0\ V$.
   (a) Estimate the technology parameter μC_{ox} and V_T from the graph for V_{DS} = 50 mV.
   (b) Plot I_D vs V_{GS} for V_{DS} = 1.8 V and extract V_T from the graph. Compare the obtained V_T with V_{DS} = 50 mV case. Do you observe any difference in V_T values for the two cases? If yes, explain why. *(Hint :DIBL)*
3. From the simple MOS models discussed in class, find out V_T for NMOS and PMOS devices ($\frac{W}{L} = \frac{1.8\mu m}{0.18\mu m}$) with the help of I_D vs V_{GS} simulations for i) Body to source voltage (V_{BS}) of $0\ V$, ii) $V_{BS} = 900\ mV$ and ii) $V_{BS} = -900\ mV$. Overlay the three graphs. Do you observe any difference in V_T for the three cases? Briefly discuss.
   (Hint :I_D *vs* V_{GS} *simulation with* V_{BS} *list, body effect. For PMOS based simulations, use PMOS4 component and use model name : CMOSP, define AS/AD/PS/PD.)*

4. Fig. 2 depicts a diode connected NMOS. Sweep I_D from 10 μA to 1 mA in steps of 1 μA and plot g_m vs I_D curve using $g_m = 2I_D/(V_{GS} - V_T)$ for $\frac{W}{L} = \frac{1\mu m}{0.18\mu m}$. Report maximum $g_{m_{max}}$. How can you achieve $4 \times g_{m_{max}}$, show the circuit modification and simulation results. *(Hint : Run DC, use V_T extracted from previous question)*

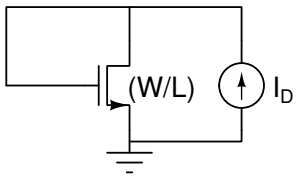

Figure 2

5. (a) Consider the CS amplifier shown in Fig. 3. It is given that $\frac{W}{L} = \frac{1\mu m}{0.18\mu m}$, $V_{DD} = 500\ mV$ and $R_L = 1\ k\Omega$. Sweep V_{GS} from V_T (calculated earlier) to V_{DD} in step size of 0.01 V and plot g_m vs V_{GS} curve using $g_m = 2I_D/(V_{GS} - V_T)$. Clearly mark region of MOSFET operations on the curve. What is the maximum value of $g_{m_{max}}$ and corresponding V_{GS} value.

   (b) Plot g_m vs V_{GS} for $\frac{W}{L} = \frac{4\mu m}{0.18\mu m}$. As compared to the previous case, which amplifier parameters (gain, swing, bandwidth) gets affected? Briefly discuss the trade-offs.

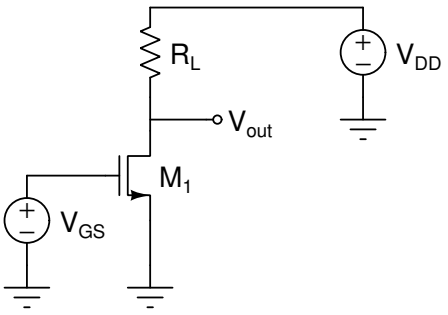

Figure 3

6. Design a common source amplifier (shown in Fig. 4) with a resistive load of 10 kΩ for a voltage gain > 5 and an overdrive voltage (of input transistor) of 200 mV. The minimum input signal frequency is 100 Hz. Design for the minimum power consumption. Clearly write your assumptions (if any).

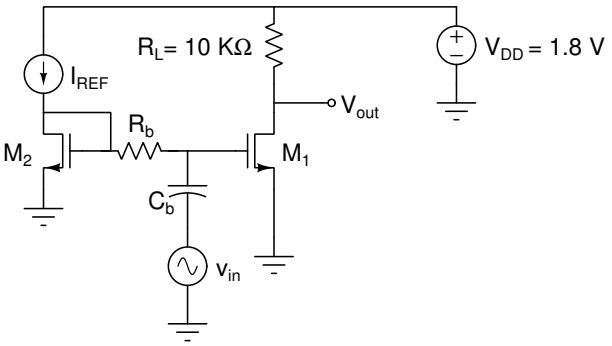

Figure 4

   (a) Show the design procedure with calculations for sizes of transistors, I_{REF}, C_b and R_b. What is the overall power consumed by your amplifier.

   (b) Give the transient (4-5 cycles) simulations plots showing the gain and considering $v_{in} = 10sin(2\pi(1000)t)$ mV.

(c) Show the AC response plots ($20log|A_v|$ vs frequency) and find unity bandwidth frequency (f_u). Vary the frequency from 1 Hz to 1 GHz for AC simulations.

(d) **Bonus problem: (Not mandatory to submit)** Replace the load resistor with a PMOS current source load as shown in Fig. 5 and redesign the circuit for a voltage gain > 15. Show the design procedure, transient and AC response of this amplifier also.

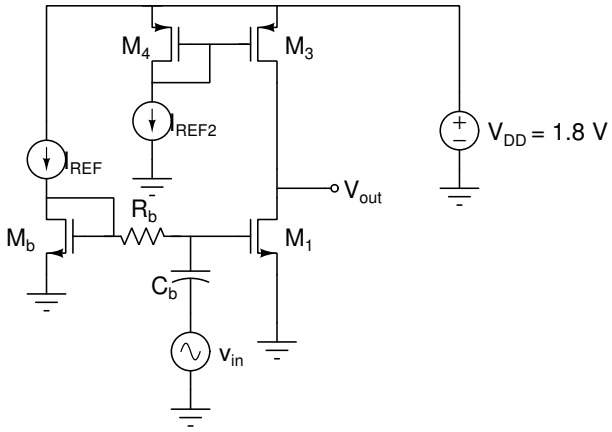

Figure 5

7. **Suggested practice problems: Single stage amplifiers (Razavi).** (No need to submit it.)
