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/*
 * Department of Computer Science and Software Engineering
 * Auburn University
 * COMP 3500 - Project 5
 * Time-driven Simulation: A high-level algorithm.
 *
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 */

begin simulation

load task information from an input file;
initialize the CPU scheduling simulator;

while (simulation not done) /* see next slide */
  handle new arrivals from task_list; /*module 4.1*/
  run first_task in ready_queue; /* module 4.2 */
  clock++;
}

compute statistical information; /* module 7 */
display statistical information; /* module 8 */

end simulation
```

```
/*
 * Time-driven Simulation: Implementation Details
 */

/* initialize the simulator */
begin simulation

clock = 0;
ready_queue = Empty;
finish_task_list = Empty

/* run the command-line parser */
(policy, quantum, file_name) <- commandline_parser();

/* load task information from an input file */
future_task_list = load_task_information(file_name);

while (future_task_list != empty or ready_queue != empty) {
      /* handle new arrivals: module 4.1 */
      for (all tasks in future_task_list) {
            if (task.arrival_time <= clock) {
                  task.remaining_time = task.burst_time;
                  remove task from task_list;
                  place task into ready_queue;
            }
            else break; /* all tasks after this are future */
      } /* end for */
```

```
      /* run first task in the ready queue: module 4.2 */
      get first_task from ready_queue;

      /* determine task's start_time ?*/
      if (first_task.remaining_time == first_task.burst_time)
            first_task.start_time = clock;

      /* run first_task */
      first_task.remaining_time --;

      /* check if first_task finishes or not */
      if (first_task.remaining_time == 0) {
            first_task.finish_time = clock;
            remove first_task from ready_queue;
            place first_task to finish_task_list;
      }

      /* clock is moving forward by one step */
      clock++;
} /* end while */

stat_info = comp_stat_info(finish_task_list); /* module 7 */

display_stat_info(stat_info); /* module 8 */

end simulation
```