Instruction Set Architecture (ISA)

Instruction Set

Instruction	Type	Operation	Binary Encoding
ADD	RRR	regA = regB + regC	0000 regA regB regC
SUB	RRR	regA = regB - regC	0001 regA regB regC
OR	RRR	regA = regB OR regC	0010 regA regB regC
AND	RRR	regA = regB AND regC	0011 regA regB regC
LI	RI	load IM into regA	0100 regA IM
SW	RRS	store word of regC into address of regB	0101 regB regC
LW	RRL	load word at address of regB into regA	0110 regA regB
BEQ	RRS	branch to address of regB if regC == CMP-bit	0110 regB regC
B	I	branch to immediate address	0111 IM
SLR	RRR	regA = regB >> regC	1000 regA regB regC
SLL	RRR	regA = regB << regC	1001 regA regB regC
CMP	RRR	compare regB == regC and write to regA	1010 regA regB regC
NOP	-	No operation	-
HALT	-	Halt execution	-

Table 1: ISA Instructions

Instruction Format Details

RRR Type

4-bit opcode	3-bit regA	1-bit F	3-bit regB	3-bit regC	2-bit unused

RRL Type

4-bit opcode	3-bit regA	1-bit F	3-bit regB	5-bit unused

RRS Type

4-bit opcode	3-bit unused	1-bit F	3-bit regB	3-bit regC	2-bit unused

RI Type

4-bit opcode	3-bit regA	1-bit F	8-bit immediate

I Type

4-bit opcode	3-bit unused	1-bit F	8-bit immediate

Schaltbild

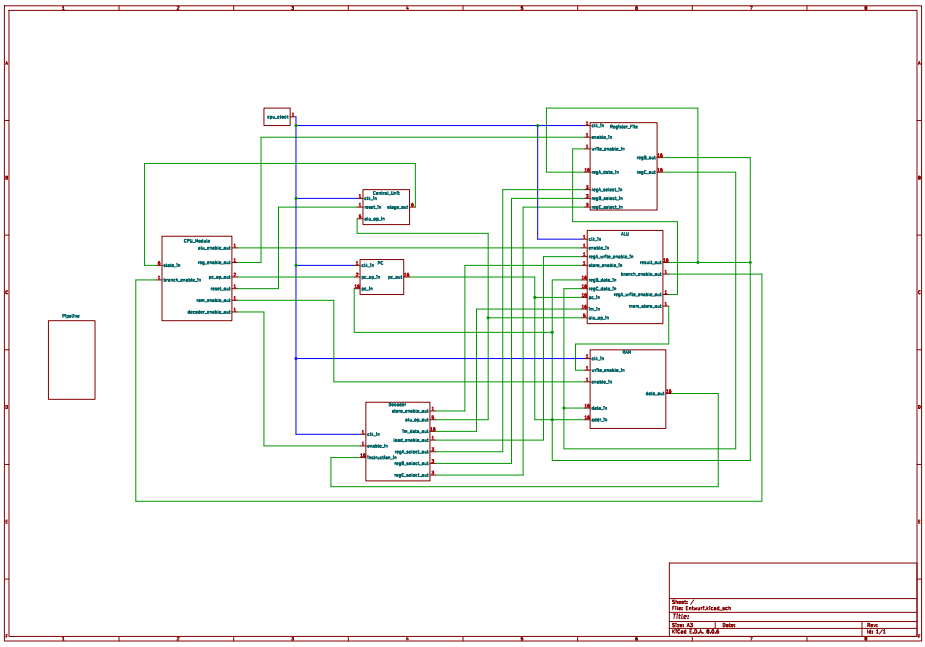

Figure 1: Schaltbild