**18F25K80 Support Information**

**#pragma config Settings**

**Register: CONFIG1L @ 0x300000**

|  |  |  |
| --- | --- | --- |
| RETEN = | VREG Sleep Enable bit |  |
| ON | Ultra low-power regulator is Enabled (Controlled by SRETEN bit) |  |
| OFF | Ultra low-power regulator is Disabled (Controlled by REGSLP bit) |  |
|  |  |  |

|  |  |  |
| --- | --- | --- |
| INTOSCSEL = | LF-INTOSC Low-power Enable bit |  |
| HIGH | LF-INTOSC in High-power mode during Sleep |  |
| LOW | LF-INTOSC in Low-power mode during Sleep |  |

|  |  |  |
| --- | --- | --- |
| SOSCSEL = | SOSC Power Selection and mode Configuration bits |  |
| HIGH | High Power SOSC circuit selected |  |
| LOW | Low Power SOSC circuit selected |  |
| DIG | Digital (SCLKI) mode |  |

|  |  |  |
| --- | --- | --- |
| XINST = | Extended Instruction Set |  |
| ON | Enabled |  |
| OFF | Disabled |  |

**Register: CONFIG1H @ 0x300001**

|  |  |  |
| --- | --- | --- |
| FOSC = | Oscillator |  |
| RCIO | External RC oscillator |  |
| RC | External RC oscillator, CLKOUT function on OSC2 |  |
| EC1 | EC oscillator (Low power, DC - 160 kHz) |  |
| EC1IO | EC oscillator, CLKOUT function on OSC2 (Low power, DC - 160 kHz) |  |
| EC2 | EC oscillator (Medium power, 160 kHz - 16 MHz) |  |
| EC2IO | EC oscillator, CLKOUT function on OSC2 (Medium power, 160 kHz - 16 MHz) |  |
| INTIO1 | Internal RC oscillator, CLKOUT function on OSC2 |  |
| INTIO2 | Internal RC oscillator |  |
| EC3 | EC oscillator (High power, 16 MHz - 64 MHz) |  |
| EC3IO | EC oscillator, CLKOUT function on OSC2 (High power, 16 MHz - 64 MHz) |  |
| HS1 | HS oscillator (Medium power, 4 MHz - 16 MHz) |  |
| HS2 | HS oscillator (High power, 16 MHz - 25 MHz) |  |
| XT | XT oscillator |  |
| LP | LP oscillator |  |

|  |  |  |
| --- | --- | --- |
| PLLCFG = | PLL x4 Enable bit |  |
| ON | Enabled |  |
| OFF | Disabled |  |

|  |  |  |
| --- | --- | --- |
| FCMEN = | Fail-Safe Clock Monitor |  |
| OFF | Disabled |  |
| ON | Enabled |  |

|  |  |  |
| --- | --- | --- |
| IESO = | Internal External Oscillator Switch Over Mode |  |
| OFF | Disabled |  |
| ON | Enabled |  |

**Register: CONFIG2L @ 0x300002**

|  |  |  |
| --- | --- | --- |
| PWRTEN = | Power Up Timer |  |
| OFF | Disabled |  |
| ON | Enabled |  |

|  |  |  |
| --- | --- | --- |
| BOREN = | Brown Out Detect |  |
| SBORDIS | Enabled in hardware, SBOREN disabled |  |
| NOSLP | Enabled while active, disabled in SLEEP, SBOREN disabled |  |
| ON | Controlled with SBOREN bit |  |
| OFF | Disabled in hardware, SBOREN disabled |  |

|  |  |  |
| --- | --- | --- |
| BORV = | Brown-out Reset Voltage bits |  |
| 3 | 1.8V |  |
| 2 | 2.0V |  |
| 1 | 2.7V |  |
| 0 | 3.0V |  |

|  |  |  |
| --- | --- | --- |
| BORPWR = | BORMV Power level |  |
| ZPBORMV | ZPBORMV instead of BORMV is selected |  |
| HIGH | BORMV set to high power level |  |
| MEDIUM | BORMV set to medium power level |  |
| LOW | BORMV set to low power level |  |

**Register: CONFIG2H @ 0x300003**

|  |  |  |
| --- | --- | --- |
| WDTEN = | Watchdog Timer |  |
| SWDTDIS | WDT enabled in hardware; SWDTEN bit disabled |  |
| ON | WDT controlled by SWDTEN bit setting |  |
| NOSLP | WDT enabled only while device is active and disabled in Sleep mode; SWDTEN bit disabled |  |
| OFF | WDT disabled in hardware; SWDTEN bit disabled |  |
|  |  |  |
|  |  |  |

|  |  |  |
| --- | --- | --- |
| WDTPS = | Watchdog Postscaler |  |
| 1048576 | 1:1048576 |  |
| 524288 | 1:524288 |  |
| 262144 | 1:262144 |  |
| 131072 | 1:131072 |  |
| 65536 | 1:65536 |  |
| 32768 | 1:32768 |  |
| 16384 | 1:16384 |  |
| 8192 | 1:8192 |  |
| 4096 | 1:4096 |  |
| 2048 | 1:2048 |  |
| 1024 | 1:1024 |  |
| 512 | 1:512 |  |
| 256 | 1:256 |  |
| 128 | 1:128 |  |
| 64 | 1:64 |  |
| 32 | 1:32 |  |
| 16 | 1:16 |  |
| 8 | 1:8 |  |
| 4 | 1:4 |  |
| 2 | 1:2 |  |
| 1 | 1:1 |  |

**Register: CONFIG3H @ 0x300005**

|  |  |  |
| --- | --- | --- |
| CANMX = | ECAN Mux bit |  |
| PORTB | ECAN TX and RX pins are located on RB2 and RB3, respectively |  |
| PORTC | ECAN TX and RX pins are located on RC6 and RC7, respectively |  |

|  |  |  |
| --- | --- | --- |
| MSSPMSK = | MSSP address masking |  |
| MSK7 | 7 Bit address masking mode |  |
| MSK5 | 5 bit address masking mode |  |

|  |  |  |
| --- | --- | --- |
| MCLRE = | Master Clear Enable |  |
| ON | MCLR Enabled, RE3 Disabled | |  |
| OFF | MCLR Disabled, RE3 Enabled | |  |

**Register: CONFIG4L @ 0x300006**

|  |  |  |
| --- | --- | --- |
| STVREN = | Stack Overflow Reset |  |
|  |
|  |

|  |  |  |
| --- | --- | --- |
| BBSIZ = | Boot Block Size |  |
| BB2K | 2K word Boot Block size |  |
| BB1K | 1K word Boot Block size |  |

**ON/OFF CONFIGURATION SECTION**

**ON Disabled**

**OFF Enabled**

**Register: CONFIG5L @ 0x300008**

|  |  |  |  |
| --- | --- | --- | --- |
| CP0 = | | Code Protect 00800-01FFF |  |
|  |
|  |

|  |  |  |  |
| --- | --- | --- | --- |
| CP1 = | | Code Protect 02000-03FFF |  |
|  |
|  |

|  |  |  |  |
| --- | --- | --- | --- |
| CP2 = | | Code Protect 04000-05FFF |  |
|  |
|  |

|  |  |  |
| --- | --- | --- |
| CP3 = | Code Protect 06000-07FFF |  |

**Register: CONFIG5H @ 0x300009**

|  |  |  |  |
| --- | --- | --- | --- |
| CPB = | | Code Protect Boot |  |
|  |
|  |

|  |  |  |  |
| --- | --- | --- | --- |
| CPD = | | Data EE Read Protect |  |
|  |

**Register: CONFIG6L @ 0x30000A**

|  |  |  |
| --- | --- | --- |
| WRT0 = | Table Write Protect 00800-01FFF |  |
|  |
|  |

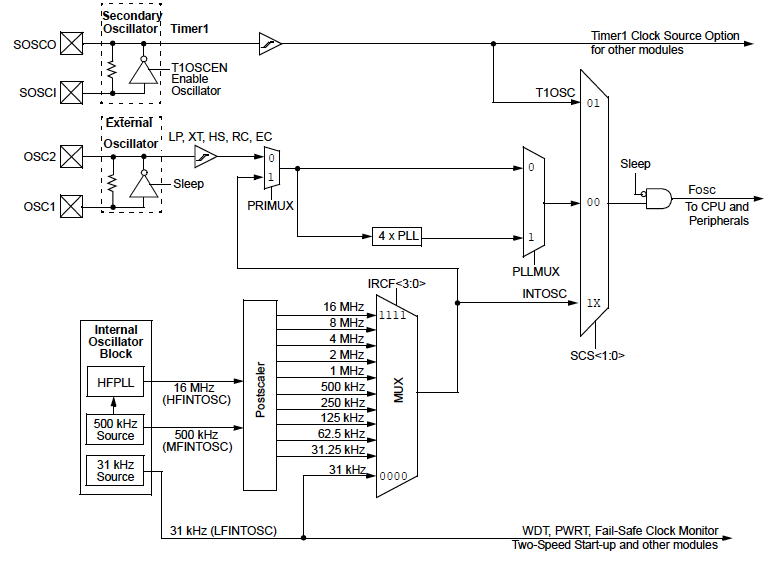
|  |  |  |
| --- | --- | --- |
| WRT1 = | Table Write Protect 02000-03FFF |  |
|  |
|  |

|  |  |  |
| --- | --- | --- |
| WRT2 = | Table Write Protect 04000-05FFF |  |
|  |
|  |

The **ECH**, **ECM**, and **ECL** clock modes rely on an external logic level signal as the device clock source.

The **LP**, **XT**, and **HS** clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range.

The **EXTRC** clock mode requires an external resistor and capacitor to set the oscillator frequency.



The **INTOSC** internal oscillator block produces low, medium, and high-frequency clock sources, designated **LFINTOSC**, **MFINTOSC** and **HFINTOSC**. A wide selection of device clock frequencies may be derived from these three clock sources.