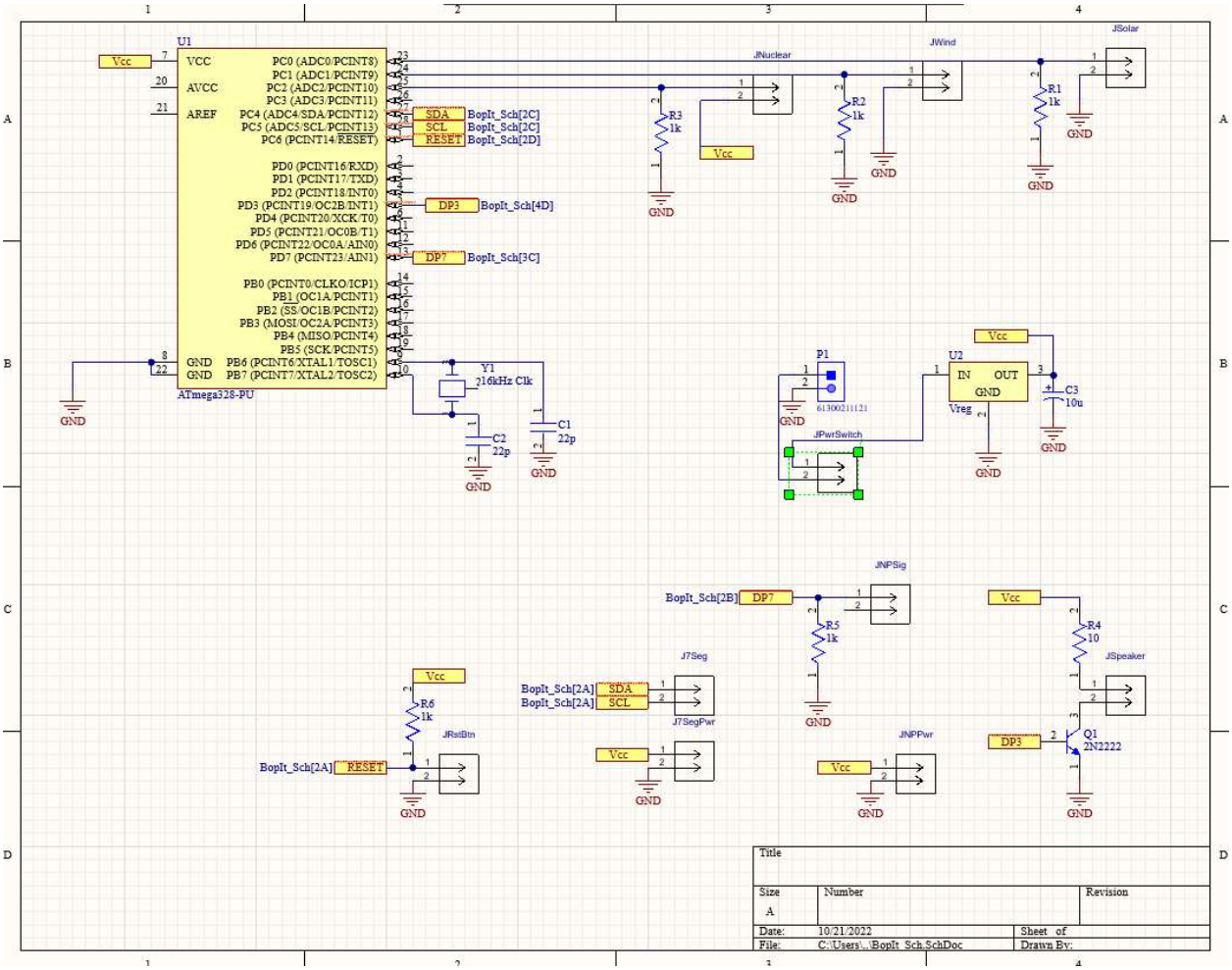
Killian Rush, Bronco York, Jack Carnovale

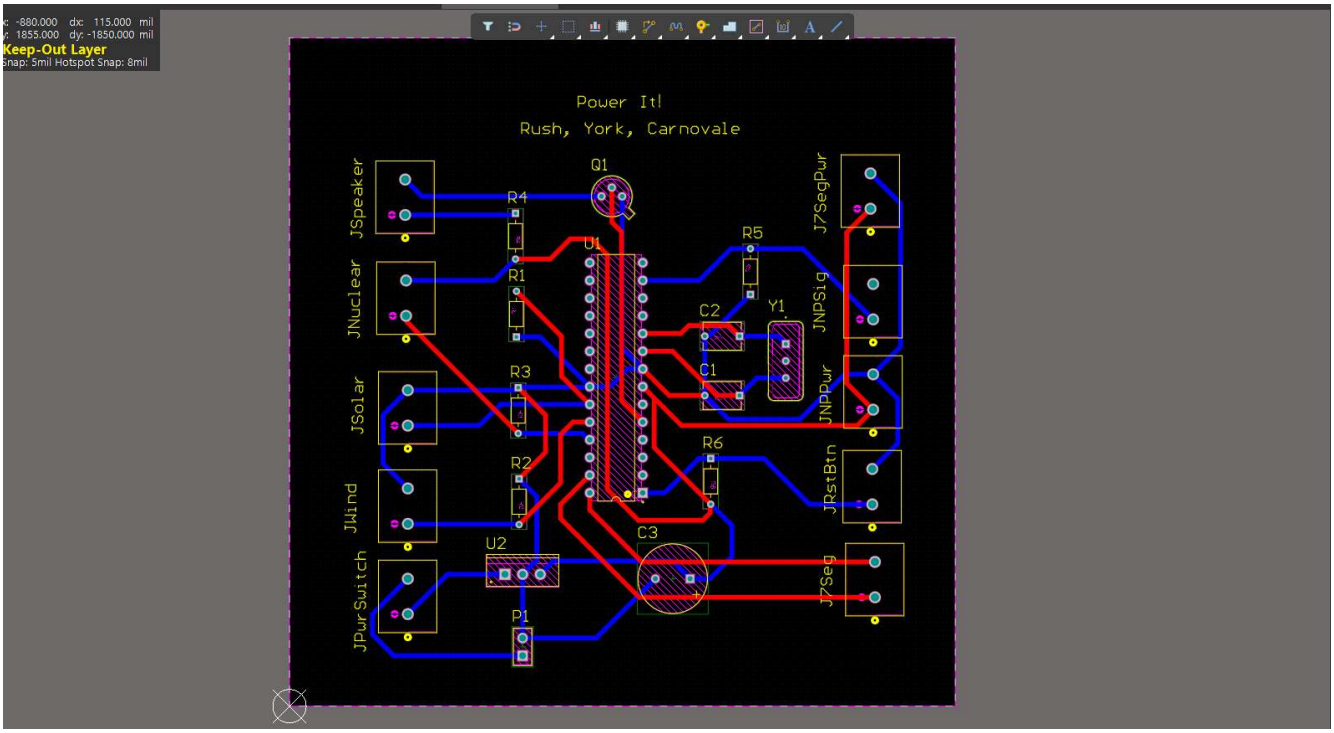
Assignment 16: Bop It Final Gerber Submission

Here are screenshots for the final board for our Bop It project: Power It!

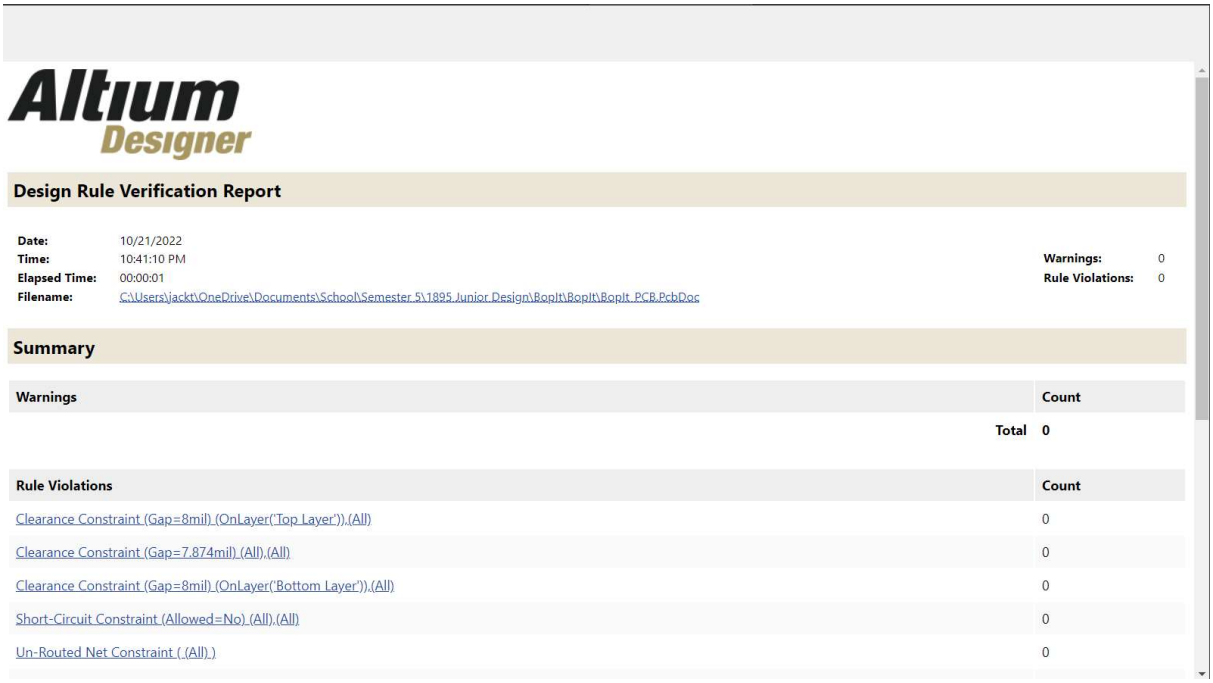
Schematic:



Board Layout:



Design Rule Test:



Altium Designer

Design Rule Verification Report

Date:	10/21/2022		
Time:	10:41:10 PM	**Warnings:**	0
Elapsed Time:	00:00:01	**Rule Violations:**	0
Filename:	C:\Users\jackt\OneDrive\Documents\School\Semester 5\1895 Junior Design\BopIt\BopIt\BopIt_PCB.PcbDoc		

Summary

Warnings	Count
Total	0

Rule Violations	Count
Clearance Constraint (Gap=8mil) (OnLayer('Top Layer')),(All)	0
Clearance Constraint (Gap=7.874mil) (All),(All)	0
Clearance Constraint (Gap=8mil) (OnLayer('Bottom Layer')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0