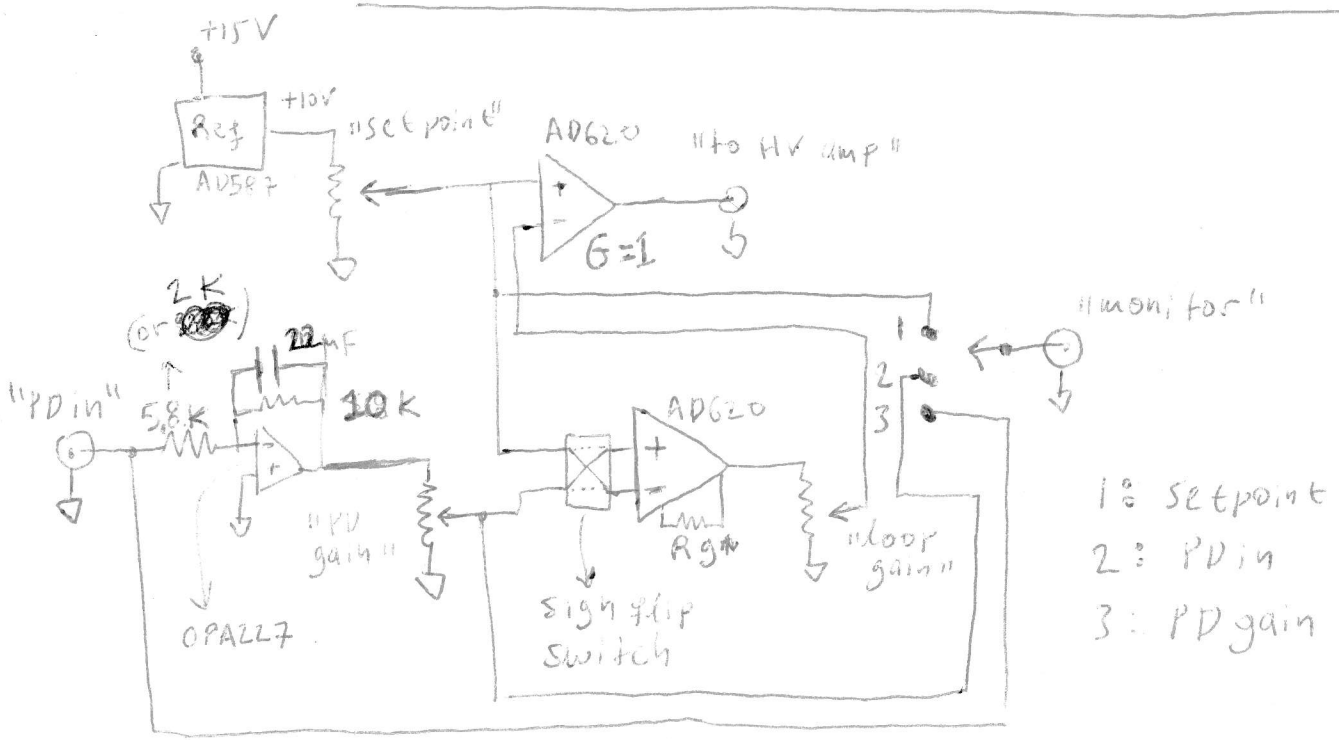
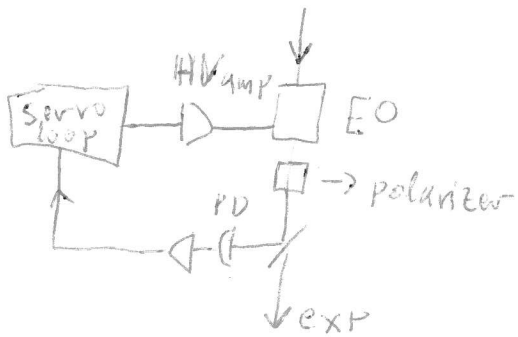
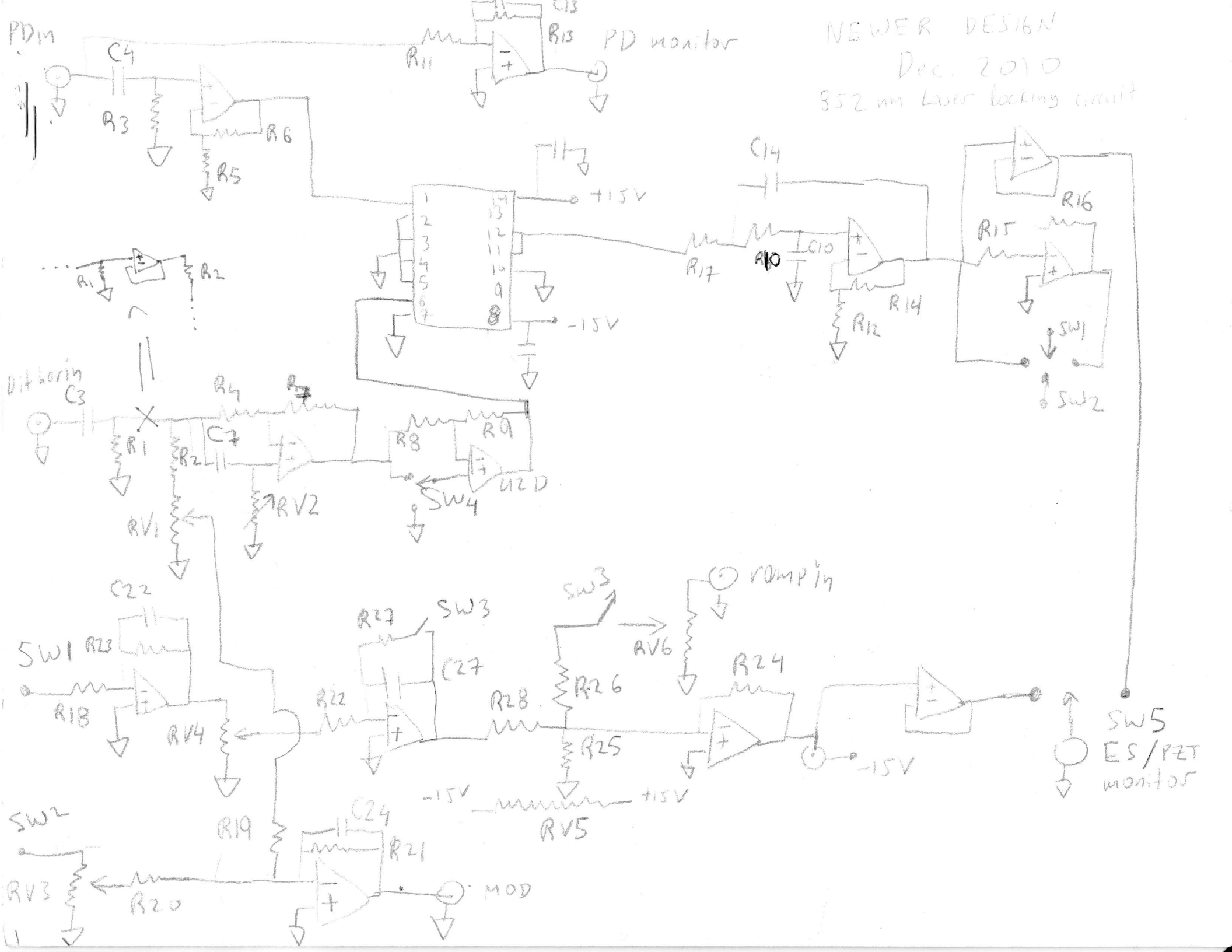
Laser intensity stabilization circuit 03/13/13





* $R_g = 180\,\Omega$, $\text{Gain} = 1 + \frac{50k\Omega}{R_g} = 2778$


NEWER DESIGN
Dec. 2010
852 nm Laser locking circuit
PDin
C4
R3
R5
R6
R11
C13
R13
PD monitor
+15V
-15V
C14
R17
C10
R14
R12
R16
R15
SW1
SW2
R1
R2
Dithering in
C3
R4
C7
RV1
RV2
R8
R9
U2D
SW4
SW1
R23
C22
R18
RV4
R19
SW2
RV3
R20
C24
R21
MOD
R27
SW3
C27
R22
R28
R26
SW3
RV6
ramp in
R24
R25
RV5
-15V
+15V
SW5
ES/PZT
monitor

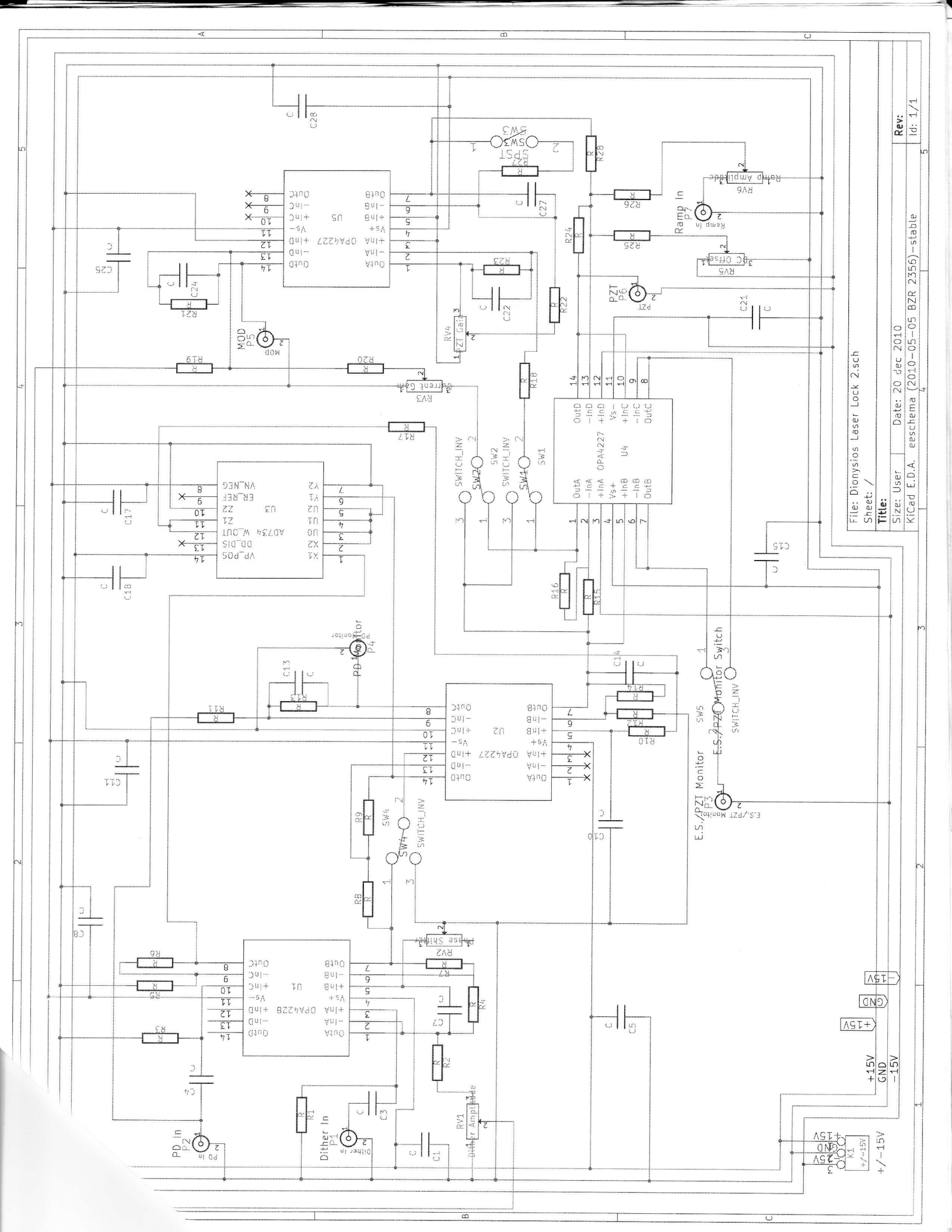
In current configuration LP filter is 1st order, R12 = nothing
R14 = shorted
R17 = shorted
C14 = nothing

" there is no SW4, opamp U2D is configured as inverting amp. with a jumper

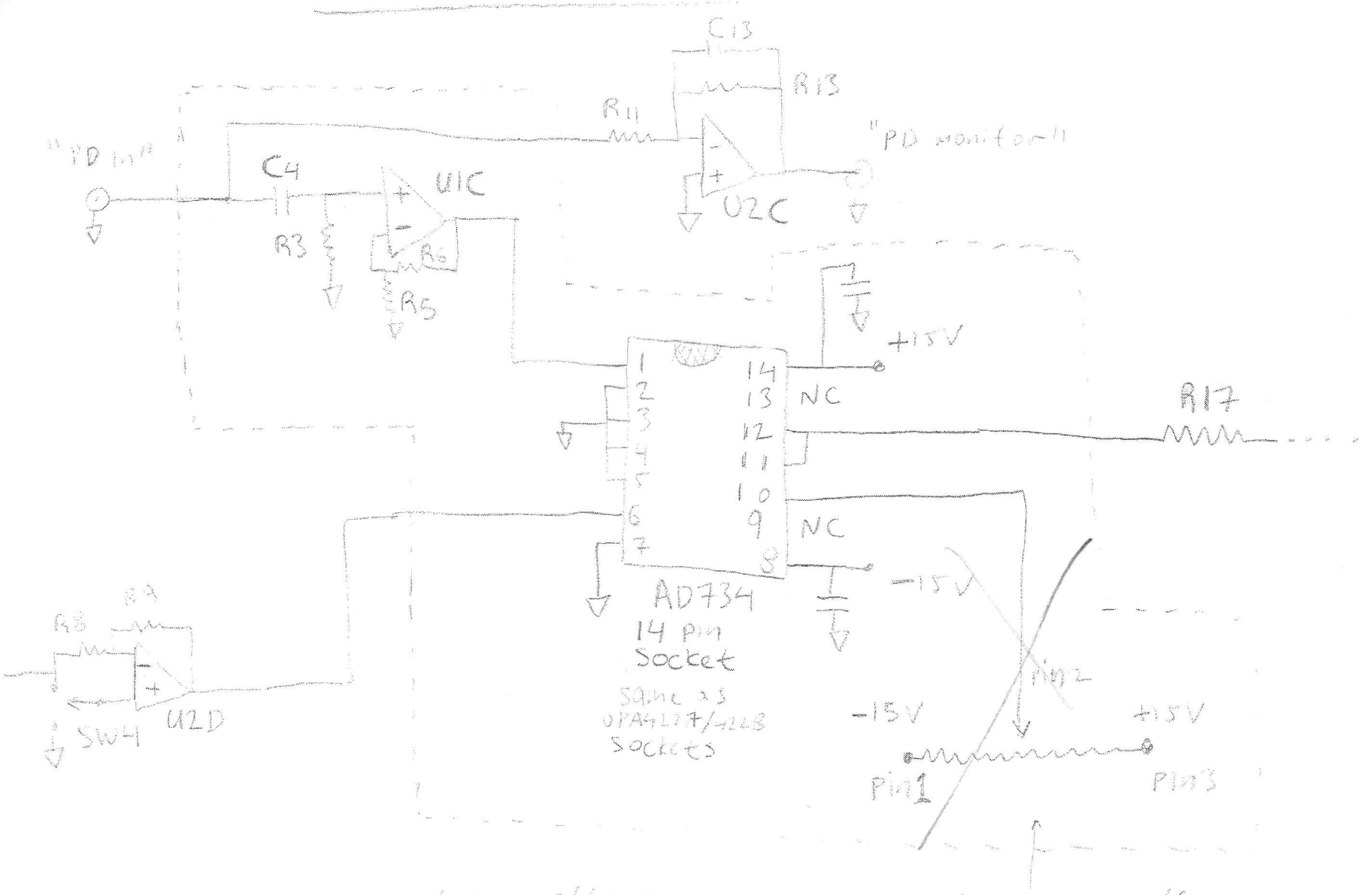
R1	100k	R24	10k	C4	10 nF
R2	10k	R25	10k	C13	nothing
R3	3.2k	R26	1k	C14	nothing
R4	10k	R27	220k	C10	33nF
R5	3.2k → 56k July 2011	R28	10k	C3	0.1 µF
R6	100k	RV1	10k	C7	1uF
R7	10k	RV2	50k	C22	nothing
R8	10k	RV3	10k	C27	220nF
R9	100k	RV4	10k	C24	~ 20pF
R10	10k	RV5	10k		
R11	10k	RV6	1k		
R12	nothing				
R13	10k				
R14	shorted				
R15	10k				
R16	10k				
R17	shorted				
R18	10k				
R19	10k → replaced by 20k July 2011				
R20	10k				
R21	10k				
R22	3.2k				
R23	20k				

July 2011 removed → limits bandwidth

All other caps → 0.1µF bypass
(Also, a pair of 4.7 µF tantalum at power supply pins)
↳ no board pins for these

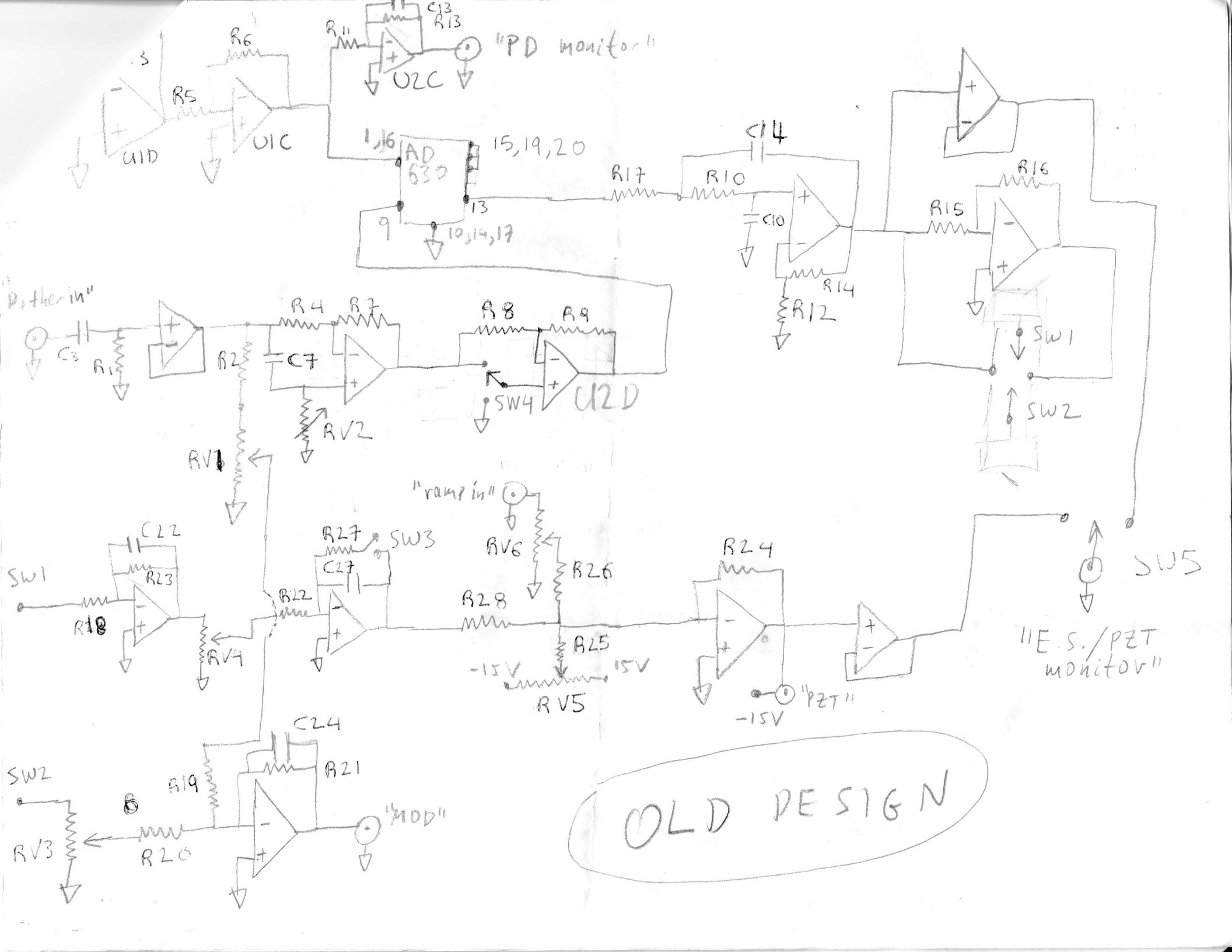

File: Dionysios Laser Lock 2.sch
Sheet: /
Title:
Size: User
Date: 20 dec 2010
KiCad E.D.A. eeschema (2010-05-05 BZR 2356)-stable
Rev:
Id: 1/1
OPA4227
OPA4228
AD734
SWITCH_INV
Ramp In
PZT
MOD
PD Monitor
PD In
Dither In
E.S./PZT Monitor
Monitor Switch
+15V
GND
-15V
+/-15V

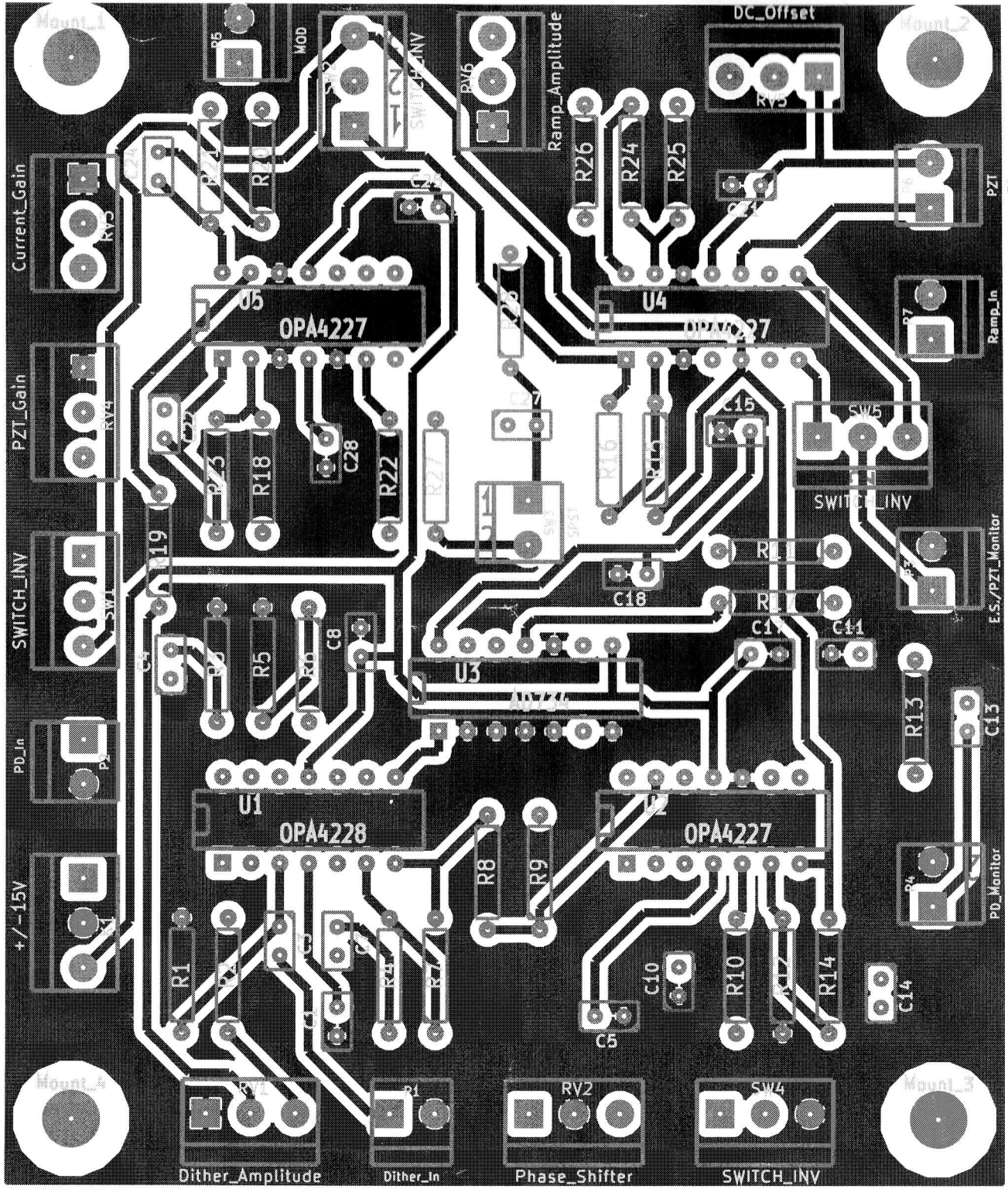
MODIFIED SCHEMATIC



- The dashed box includes all changes we need to make

- this pot will be connected to the board with a 3 pin connector, same as all other 3 pin connectors on the board


R6
R5
U1D
U1C
R11
C13
R13
U2C
"PD monitor"
1,16
AD
630
15,19,20
13
9
10,14,17
C14
R17
R10
C10
R14
R12
R16
R15
SW1
SW2
"Dither in"
C3
R1
R2
R4
R7
C7
RV2
R8
R9
SW4
U2D
RV1
"ramp in"
RV6
R26
R27
SW3
C27
R22
R28
R25
-15V
15V
RV5
R24
"PZT"
-15V
SW5
"E.S./PZT monitor"
C22
R23
SW1
R18
RV4
C24
R21
SW2
R19
RV3
R20
"MOD"
OLD DESIGN



Dec 2010

pcb layout