W74M00AV

3V RPMD
REPLAY PROTECTED MEMORY DEVICE
WITH SPI INTERFACE

Publication Release Date: August 31, 2016
Preliminary - Revision A

winbond

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1. GENERAL DESCRIPTIONS

The W74M series is an enhanced authentication security feature by Replay Protected Memory Device (RPMD). It provides a high level secured communication between the flash device and the controller to reduce the system vulnerabilities to hardware attacks.

2. FEATURES

- **Highest Performance**
  – 80MHz
  – SPI Flash interface
- **Low Power, Wide Temperature Range**
  – Single 2.7V to 3.6V power supply
  – -40℃ to +85℃ operating range
- **Advanced Security Features**
  – Replay Protected Memory Device(RPMD)
  – Volatile Status Register Bits
- **Space Efficient Packaging**
  – 8-pin SOIC 150-mil
  – 8-pin SOIC 208-mil
  – Contact Winbond for other options

3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1 Pin Configuration SOIC 150-mil/208-mil

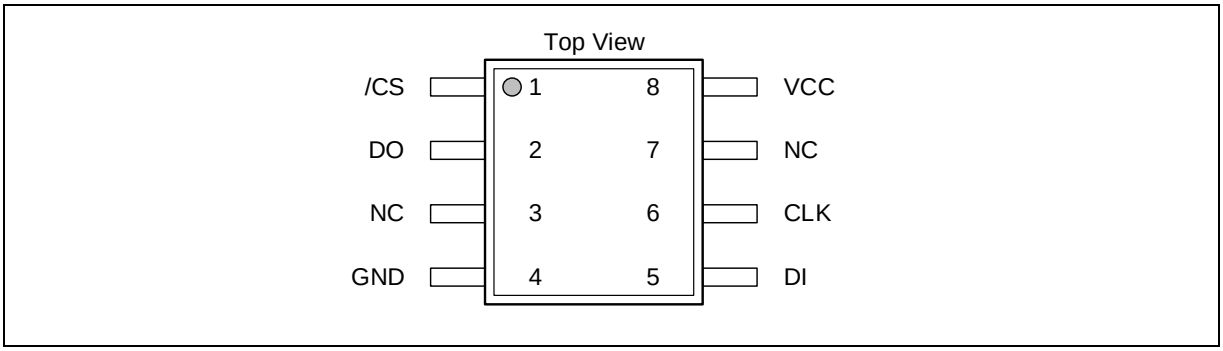


Figure 1. W74M00AV Pin Assignments, 8-pin SOIC 150-mil/208-mil (Package Code SN, SS)

3.2 Pin Description SOIC 150-mil/208-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO	O	Data Output
4	GND		Ground
5	DI	I	Data Input
6	CLK	I	Serial Clock Input
8	VCC		Power Supply
3,7	NC		No connect

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the device power consumption will be at standby level unless an internal write cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active level and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see Figure 11). If needed a pull-up resister on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output (DI, DO)

The W74M00AV supports standard SPI interface operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI interface also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

4.3 Serial Clock (CLK)

The Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

5. BLOCK DIAGRAM

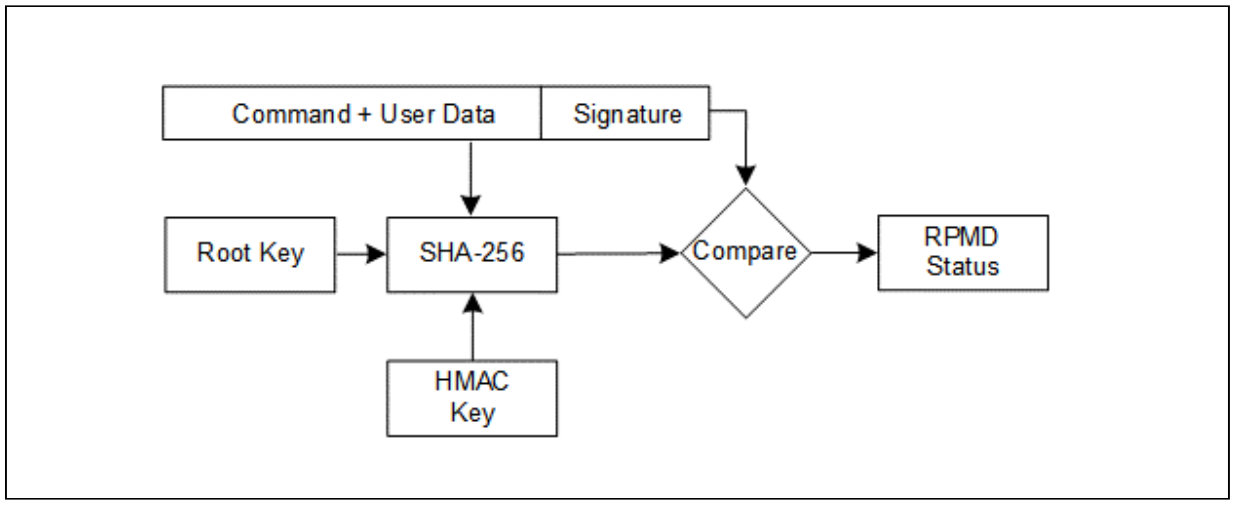


Figure 2. W74M00AV Block Diagram

6. FUNCTIONAL DESCRIPTIONS

6.1 Replay Protected Memory Device Operations

To prevent hardware vulnerability attack, Replay Protection provides a build-in block towards providing Confidentiality and Integrity of read/write data. The W74M00AV is equipped with four 32-bit Monotonic Counters and can be addressed individually by the 8-bit Counter_Address. These monotonic counters are used by the SPI Controllers to ensure the physical authenticity of the attached flash devices.

RPMD operation is based on the HMAC-SHA-256 cryptographic algorithm. HMAC-SHA-256 is a type of keyed hash algorithm that is constructed from the SHA-256 hash function and used as a Hash-based Message Authentication Code (HMAC). The HMAC process mixes a secret key with the message data, hashes the result with the hash function, mixes that hash value with the secret key again, and then applies the hash function a second time. The output hash is 256 bits in length.

An HMAC can be used to determine whether a meFCssage sent over an insecure channel has been tampered with, provided that the sender and receiver share a secret key. The sender computes the hash value for the original data and sends both the original data and hash value as a single message. The receiver recalculates the hash value on the received message and checks that the computed HMAC matches the transmitted HMAC.

6.1.1 RPMD Initialization

RPMD operation is initialized in an OEM manufacturing environment by issuing the “Write Root Key Register” command. When this command is successfully received and executed, a 256-bit Root Key will be written into the RPMD permanently, and the corresponding Monotonic Counter will also be initialized to 0. After the initialization procedure, the Root Key value can no longer be altered or accessed externally through the SPI interface. The initialized Monotonic Counter is ready to accept the authenticated RPMD commands.

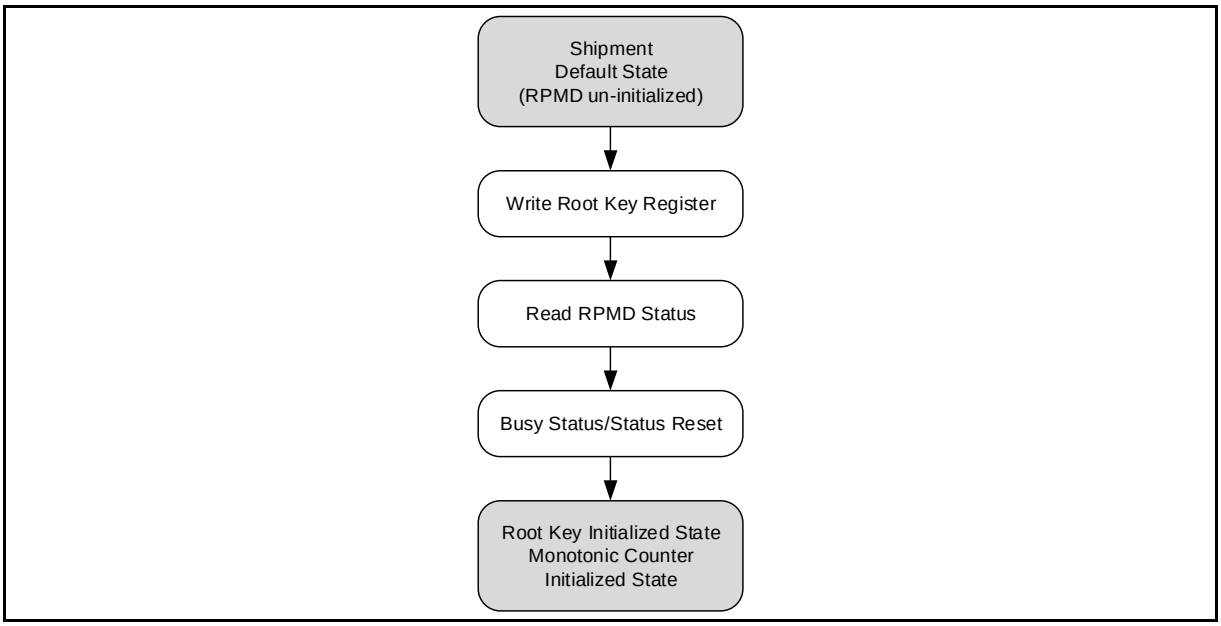


Figure 3a. W74M00AV RPMD Initialization Flow Diagram

6.1.2 RPMD Operation Flow

Once the root key and the Monotonic Counter have been initialized, every time after the device is powered on, prior to any RPMD operations, the external SPI controller must update the HMAC Key register in the RPMD.

After initializing the HMAC key register, there are two different RPMD operations can be performed. “Increment Monotonic Counter” is used to increase the Monotonic Counter value by 1. “Request Monotonic Counters” is used to read out the existing Monotonic Counter data.

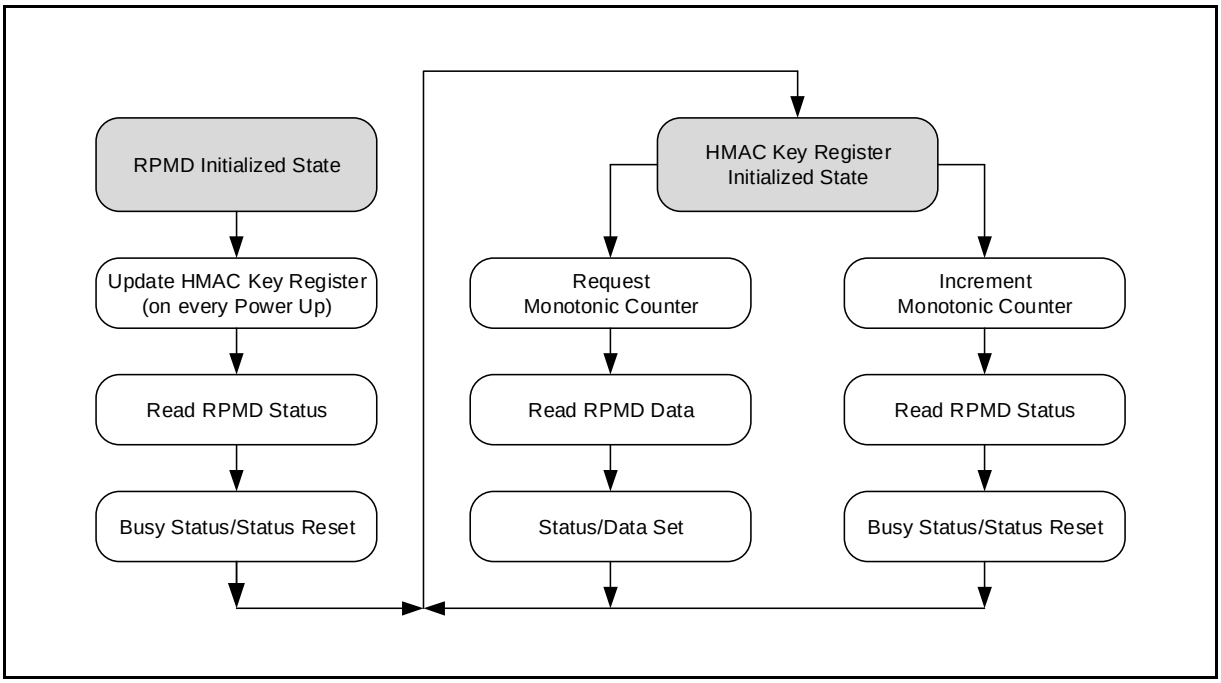


Figure 3b. W74M00AV RPMD Operation Flow Diagram

6.1.3 Operations Allowed / Disallowed During RPMD Operation

The RPMD operation is independent to the other SPI flash operations. The RPMD input command OP1 (9Bh) will initial internal operations after the authenticated command is accepted by the device. During the internal operation period, the BUSY bit in the RPMD Status Register (bit 0) will be set to 1. The RPMD internal operation cannot be suspended and can only be interrupted by the Device Reset command (66h+99h).

Operations	Device Behavior
RPMD OP1 command	The RPMD input command OP1 will be ignored while a RPMD operation is on-going.
Read RPMD Status/Data OP2 command	The RPMD Status Register can be read out while a RPMD operation is on-going and this is the way to check if the RPMD operation has finished or not. If the BUSY bit of RPMD Status Register is set as 1, the RPMD data output following the Status Register is not reliable.
Device Reset	The software reset sequence can be issued any time during RPMD internal operations. All volatile settings will be reset.

6.1.4 RPMD Status Register Definition

During the RPMD operations, an 8-bit Status Register is used to indicate various states of the command execution and device status. A “Read RPMD Status” command can be issued during any RPMD operation to check the Status Register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Successful Completion	Not Defined	Fatal Error (Pgm/Erase Fail or no valid counter found)	Monotonic_Counter_Data Mismatch	HMAC Key Reg Uninitialized	Signature Mismatch or Counter Address out of range or Write_Mode out of range	Root Keys Overwrite or Root Keys length mismatch or TruncatedSig Mismatch	BUSY

RPMD Status Register[7:0]	Applicable CmdType(s)	Description
00000000	--	Power On State (Read RPMD Status is issued directly after power-up).
10000000	00, 01, 02, 03	This status must be set on successful completion (no errors) of OP1 command (9Bh).
0xxxxxx1	00, 01, 02, 03, 04-FF	This bit must be set to 1, when device is busy executing OP1 command (9Bh). It is reset to 0 when the command execution is done.
0xxxxx1x	00, 01	This bit is set only when the correct payload size is received. For CmdType = 00, this bit must be set on Root Key Register Overwrite or Counter Address out of range or Truncated Signature mis-match error. For CmdType = 01, this bit is set when the corresponding Monotonic Counter is uninitialized.
0xxxx1xx	00, 01, 02, 03	This bit must be set on Signature Mismatch, Counter Address out of range when correct payload size is received; or CmdType is out of range; or incorrect payload size is received.
0xxx1xxx	02, 03	This bit must be set on HMAC Key Register (or Monotonic Counter) uninitialized on previous OP1 command when correct payload size is received.
0xx1xxxx	02	This bit must be set on Monotonic_Counter_Data Mismatch on previous increment when correct payload size is received.
0x1xxxxx	--	Fatal Error, e.g. program fail, no valid counter found after initialization.
Current value	--	Status register will naturally not be updated until first 8 bits of OP1 (9Bh) is received. However it is expected that the correct error type is reflected for any OP1 operation that exceeds a minimum of 16 clocks with active chip-select.

6.2 Instruction Set Tables

6.2.1 Instruction Set Table 2-1 (RPMD Input Instruction, OP1)(1)

INSTRUCTION NAME	BYTE 0	BYTE 1 (CmdType)	BYTE 2	BYTE 3(2)		
Write Root Key Register	**9Bh**	**00h**	CounterAddr[7:0]	Reserved[7:0]	Byte 4 - 35 RootKey[255:0]	Byte 36 - 63 TruncatedSign[223:0]
Update HMAC Key Register	**9Bh**	**01h**	CounterAddr[7:0]	Reserved[7:0]	Byte 4 - 7 KeyData[31:0]	Byte 8 - 39 Signature[255:0]
Increment Monotonic Counter	**9Bh**	**02h**	CounterAddr[7:0]	Reserved[7:0]	Byte 4 - 7 CounterData[31:0]	Byte 8 - 39 Signature[255:0]
Request Monotonic Counter	**9Bh**	**03h**	CounterAd dr[7:0]	Reserved[7:0]	Byte 4 - 15 Tag[95:0]	Byte 16 - 47 Signature[255:0]
Reserved Commands	**9Bh**	04h ~ FFh	Reserved			

6.2.2 Instruction Set Table 2-2 (RPMD Output Instruction, OP2)(1)

INSTRUCTION NAME	BYTE 0	BYTE 1	BYTE 2	BYTE 3 - 14	BYTE 15 - 18	BYTE 19 - 50
Read RPMD Status / Data(3)(4)	**96h**	Dummy	(RPMD Status[7:0])	(Tag[95:0])	(CounterData[31:0])	(Signature[255:0])

6.2.3 Instruction Set Table 2-3 (RPMD Reset Instruction)(1)

INSTRUCTION NAME	BYTE 0	
Enable Reset	**66h**	
Reset	**99h**	

Notes:

1. All RPMD instructions are in Standard SPI format. Each Input/Output Byte requires 8 clocks.
2. The Reserved[7:0] field for RPMD OP1 must be all 0s (00000000'b).
3. The controller may terminate the Read RPMD Status/Data instruction at any time without going through the entire data output sequence.
4. When BUSY=1, from Byte-3 and beyond, the device will output the RPMD_Status[7:0] value continuously until /CS terminates the instruction. The device will not output Tag, CounterData & Signature fields when BUSY=1. Once BUSY becomes 0, another OP2 command must be issued to read out the correct Tag, CounterData & Signature fields.

6.3 Instruction Descriptions

6.3.1 Write Root Key Register (9Bh + 00h)

This command is used by the SPI Controller to initialize the Root Key Register corresponding to the received Counter Address with the received Root Key. It is expected to be used in an OEM manufacturing environment when the SPI Controller is powered for the first time.

After the command is issued on the interface, the RPMD must ensure that the received transaction is error free. This includes checking following conditions:

- Payload size is correct. (including OP1 is 64 bytes)
- Counter Address falls within the range of supported counters.
- The Root Key Register corresponding to the requested Counter Address was previously uninitialized. [Root_Key_Reg_Init_State[Monotonic_Counter_Address] = 0xFFh]
- Truncated signature field is the same as least significant 224 bits of HMAC-SHA-256 based signature computed based on received input parameters.

If the received transaction is error free, RPMD successfully executes the command and posts “successful completion” in the RPMD Status Register. This command must be executed to ensure that power cycling in the middle of command execution is properly handled. This requires that the internal state tracking the root key register initialization is written as the last operation of the command execution. (Root_Key_Reg_Init_State[Monotonic_Counter_Address] = 0).

Root Key Register Write with root key is = 256’hFF…FF is used as a temporary key. When this request is received error-free Root_Key_Reg_Init_State[Monotonic_Counter_Address] is not affected. Instead only the corresponding Monotonic Counter is initialized to 0 if previously uninitialized. This state is tracked as separate state using MC_Init_State[Monotonic_Counter_Address]. This state is used to leave the Monotonic Counter at the current value when an error free Root Key Register Write operation is received. (Both 256’hFF..FF and non 256’hFF..FF)

Once this command is successfully executed with a non 256’hFF..FF Root Key, the device will not accept the “Write Root Key Register” command any more, and the Root Key value cannot be read out by any instructions.

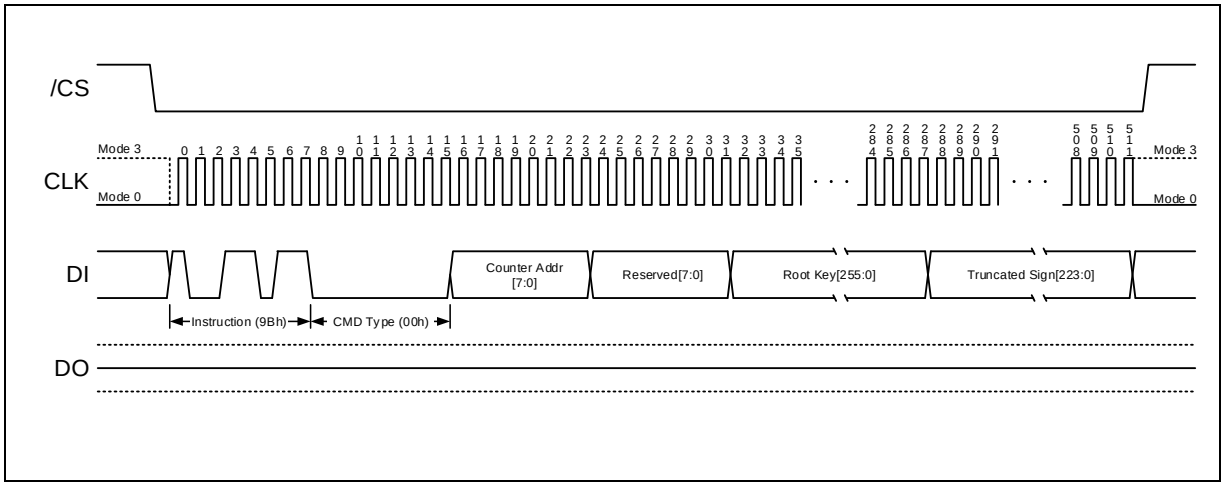


Figure 4. Write Root Key Register Instruction

6.3.2 Update HMAC Key Register(9Bh + 01h)

This command is used by the SPI Controller to update the HMAC-Key corresponding to the received Counter Address with a new HMAC key calculated based on received input. This command must be issued once only on every power cycle event on the interface. This allows the HMAC key storage to be implemented using volatile memory. Status register busy indication is expected to indicate busy for double the amount of Read_Counter_Polling_Delay specified in SFDP table since this command performs two distinct HMAC-SHA-256 computations.

After the command is issued on the interface, the RPMD must ensure that the received transaction is error free. This includes checking following conditions:

- Payload size is correct. (including OP1 = 40 bytes)
- Counter Address falls within the range of supported counters.
- The Monotonic Counter corresponding to the requested Counter Address was previously initialized.
- Signature matches the HMAC-SHA-256 based signature computed based on received input parameters. This command performs two HMAC-SHA-256 operations.

If the received transaction is error free, the RPMD successfully executes the command and posts “successful completion” in the RPMD Status Register.

If the received transaction has errors, the RPMD does not execute the transaction and posts the corresponding error in the RPMD Status Register.

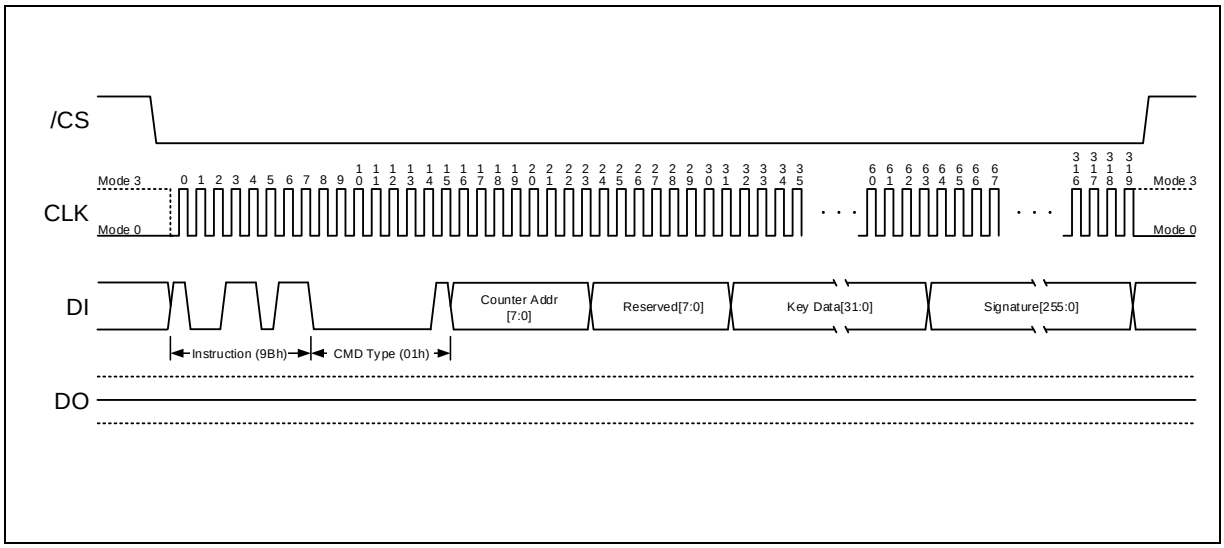


Figure 5. Update HMAC Key Register Instruction

6.3.3 Increment Monotonic Counter (9Bh + 02h)

This command is used by the SPI Controller to increment the Monotonic Counter by 1 inside the RPMD.

After the command is issued on the interface, the RPMD must ensure that the received transaction is error free. This includes checking following conditions:

- Payload size is correct. (including OP1 = 40 bytes)
- Counter Address falls within the range of supported counters.
- The Monotonic Counter corresponding to the requested Counter Address was previously initialized.
- The HMAC Key Register corresponding to the requested Counter Address was previously initialized.
- The requested Signature matches the HMAC-SHA-256 based signature computed based on received input parameters.
- The received Monotonic_Counter_Data matches the current value of the counter.

If the received transaction is error free, the RPMD successfully executes the command and posts "successful completion" in the RPMD Status Register. The increment counter implementation should make sure that the counter increment operation is performed in a power glitch aware manner.

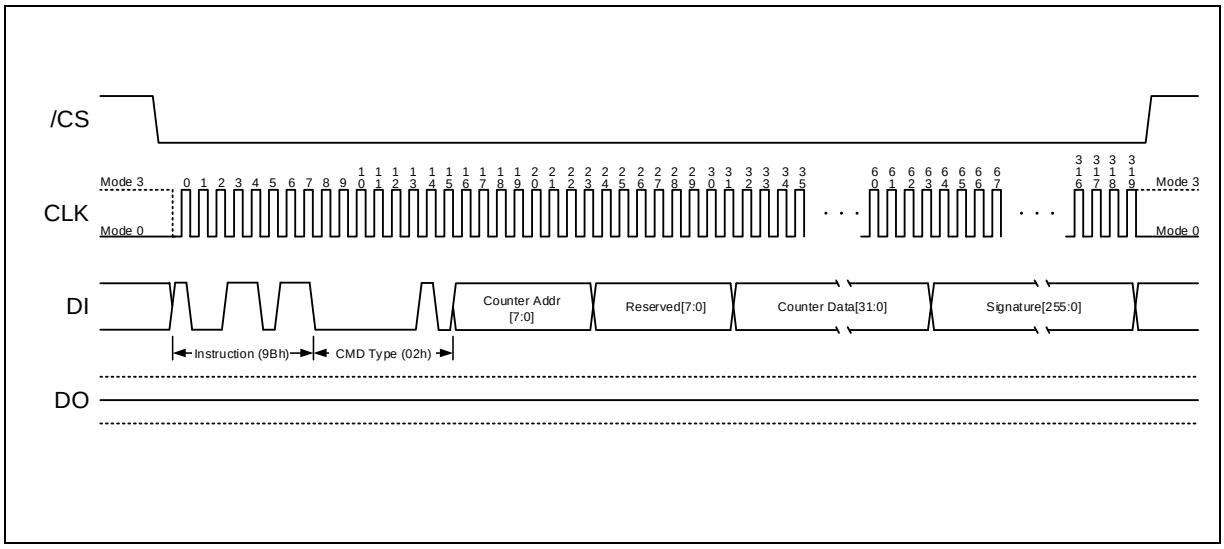


Figure 6. Increment Monotonic Counter Instruction

6.3.4 Request Monotonic Counter (9Bh + 03h)

This command is used by the SPI Controller to request the Monotonic Counter value inside the RPMD.

After the command is issued on the interface, the RPMD must ensure that the received transaction is error free. This includes checking following conditions:

- Payload size is correct. (including OP1 = 48 bytes)
- Counter Address falls within the range of supported counters.
- The Monotonic Counter corresponding to the requested Counter Address was previously initialized.
- The HMAC Key Register corresponding to the requested Counter Address was previously initialized.
- The requested Signature matches the HMAC-SHA-256 based signature computed based on received input parameters.

If the received transaction is error free, the RPMD successfully executes the command and posts "successful completion" in the RPMD Status Register. In response to this command, the SPI controller reads the Monotonic Counter addressed by counter address. It calculates HMAC-SHA-256 signatures the second time, based on following parameters.

- HMAC Message[127:0] = Tag [95:0], Counter_Data_Read[31:0]
- HMAC Key[255:0] = HMAC_Key_Register[Monotonic_Counter_Address][255:0]

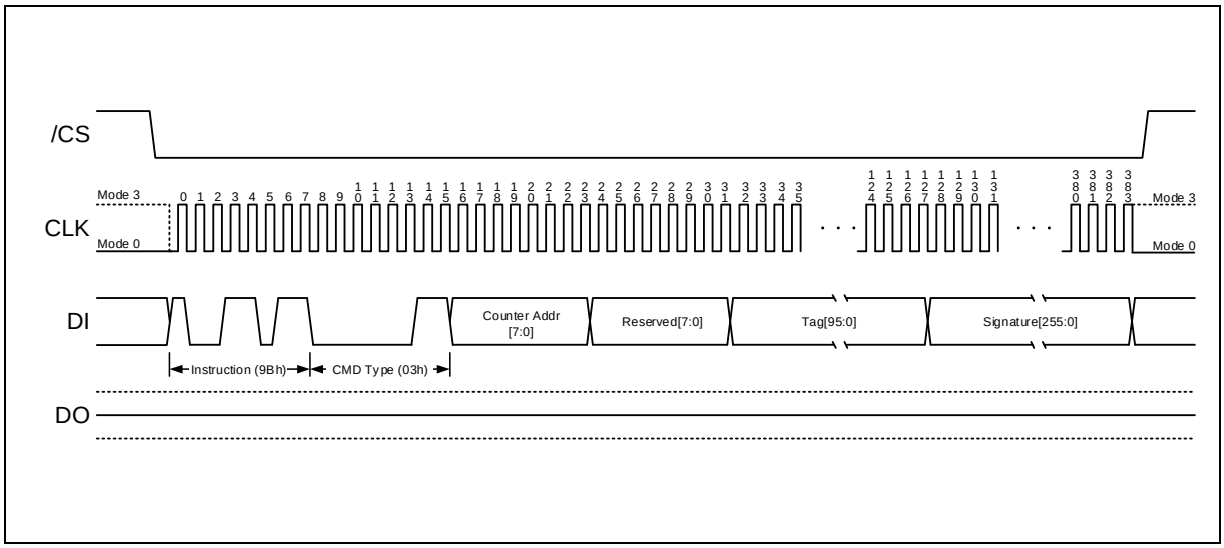


Figure 7. Request Monotonic Counter Instruction

6.3.5 Reserved Replay Protected Memory Device Commands (9Bh + 04h~FFh)

If the SPI Controller issues any of the reserved command-types, the RPMD must return Error status in the RPMD Status Register. It asserts bit 2 to indicate that a reserved command-type was issued.

6.3.6 Read Replay Protected Memory Device Status / Data (96h)

This command is used by the SPI Controller to read the RPMD status from any previously issued OP1 command. In addition, if previous OP1 command is Request Monotonic Counter and if SPI Flash returns successful completion (BUSY=0) in the RPMD Status Register, then it must also return valid values in the Tag, Monotonic_Counter_Data and Signature field. If there're other error flags, the values returned in Tag, Counter and Signature field are invalid. The controller may abort the read prematurely prior to completely reading the entire payload. This may occur when the controller wants to simply read the RPMD status or when it observes an error being returned in the RPMD status field. The controller may also continue reading past the defined payload size of 49 bytes. Since this is an error condition, the SPI Flash may return any data past the defined payload size. The controller must ignore the data.

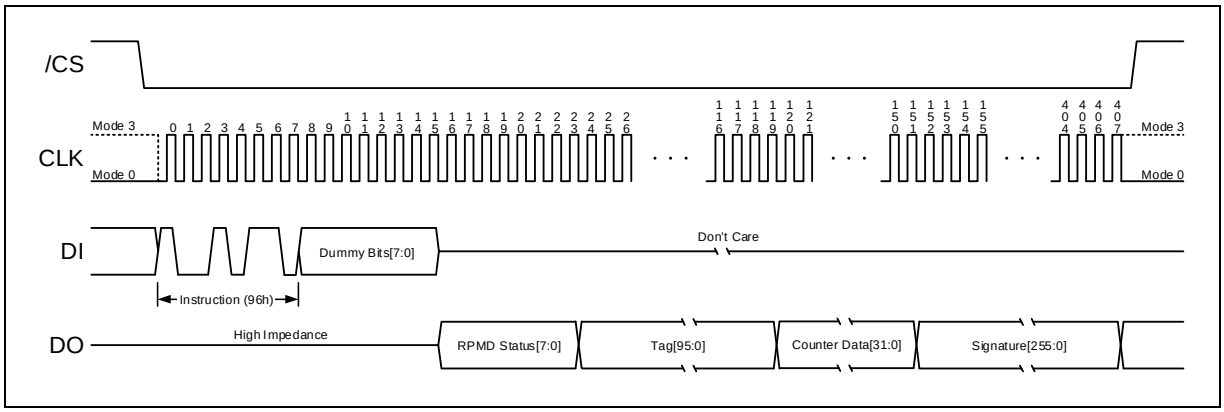


Figure 8a. Read RPMD Data Instruction (BUSY=0)

When BUSY=1, from Byte-3 and beyond, the device will output the RPMD Status[7:0] value continuously until /CS terminates the operation. The device will not output Tag, CounterData & Signature fields when BUSY=1. Once BUSY becomes 0, another OP2 command must be issued to read out the correct Tag, CounterData & Signature fields.

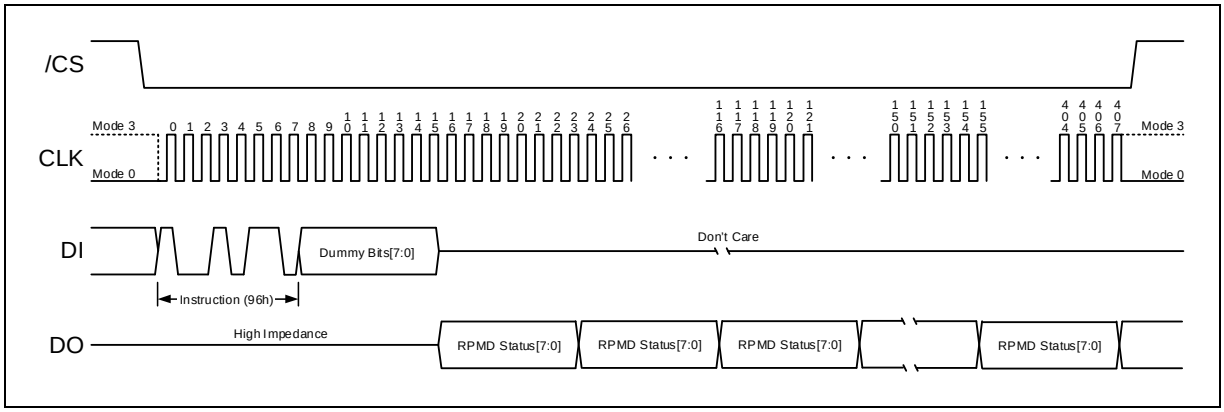


Figure 8b. Read RPMD Data Instruction (BUSY=1)

6.3.7 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the RPMD provide a software Reset instruction. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits.

To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit RPMD Register before issuing the Reset command sequence.

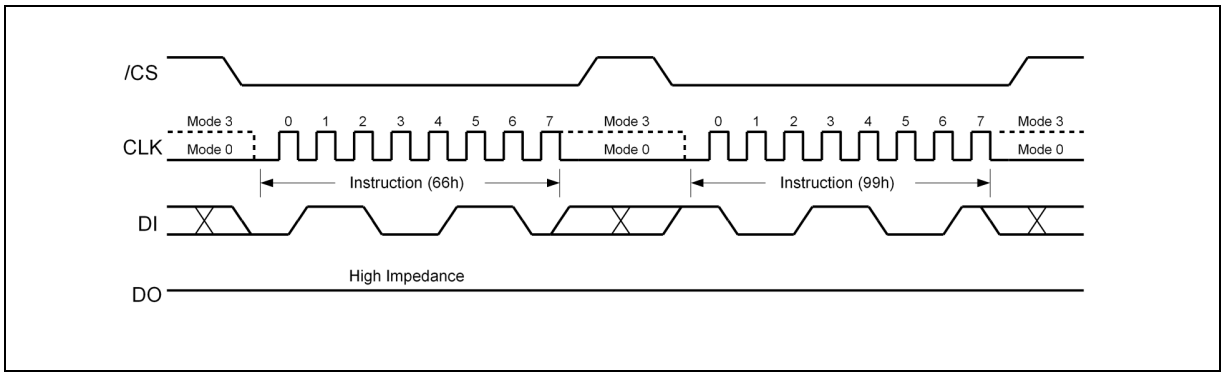


Figure 9. Enable Reset and Reset Instruction Sequence

7. ELECTRICAL CHARACTERISTICS[1]

7.1 Absolute Maximum Ratings [2]

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to VCC+0.4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note [3]	°C
Electrostatic Discharge Voltage	VESD	Human Body Model[4]	–2000 to +2000	V

Notes:

1. Specification for W74M00AV is preliminary. See preliminary designation at the end of this document.
2. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
3. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
4. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

7.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC	F_R = 80MHz	2.7	3.6	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	℃

7.3 Power-Up Power-Down Timing and Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}[1]	20		µs
Time Delay Before Write Instruction	t_{PUW}[1]	5		ms
Write Inhibit Threshold Voltage	V_{WI}[1]	1.0	2.0	V

Note:

1. These parameters are characterized only.

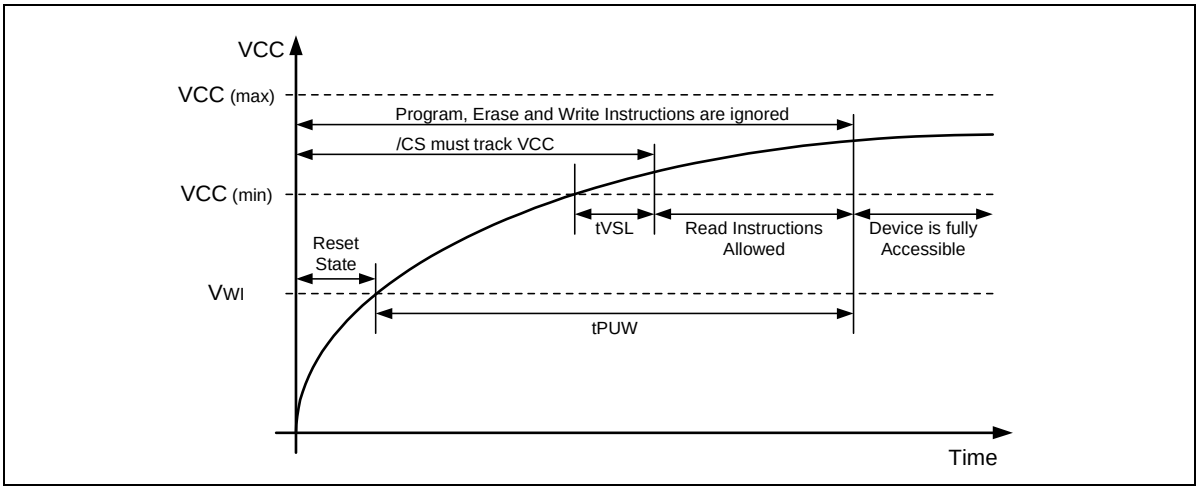


Figure 10a. Power-up Timing and Voltage Levels

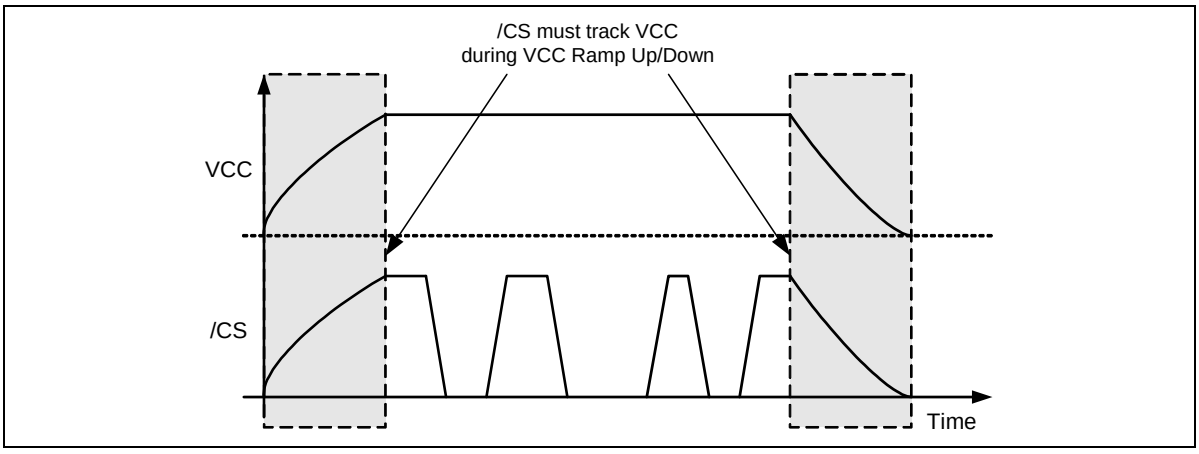


Figure 10b. Power-up, Power-Down Requirement

7.4 DC Electrical Characteristics(1)

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	CIN	VIN = 0V			6	pF
Output Capacitance	Cout	VOUT = 0V			8	pF
Input Leakage	ILI				±2	µA
I/O Leakage	ILO				±2	µA
Standby Current	ICC1	/CS = VCC, VIN = GND or VCC		25	50	µA
RPMD OP1 Write Only	ICC2	/CS = VCC		15	20	mA
RPMD OP2 Read Only	ICC3	C = 0.1 VCC / 0.9 VCC			30	mA
Input Low Voltage	VIL				VCC x 0.3	V
Input High Voltage	VIH		VCC x 0.7			V
Output Low Voltage	VOL	IOL = 100 µA			0.2	V
Output High Voltage	VOH	IOH = –100 µA	VCC – 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25°C, VCC = 3. 0V.

7.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

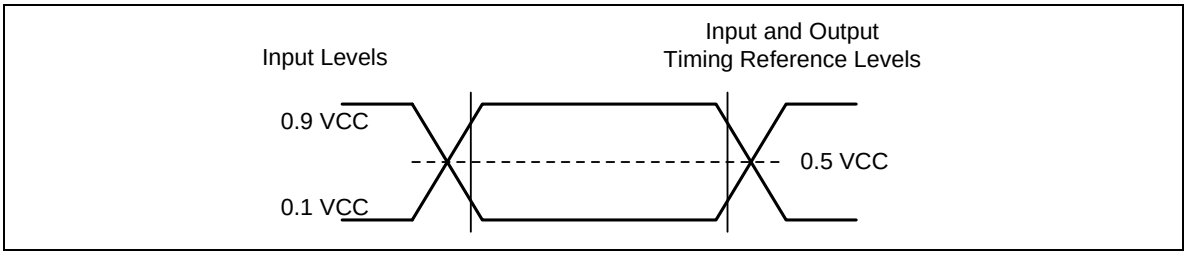


Figure 11. AC Measurement I/O Waveform

7.6 AC Electrical Characteristics(3)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency	FR	fC	D.C.		80	MHz
Clock High, Low Time	tCLH, tCLL(1)		5			ns
Clock Rise Time peak to peak	tCLCH(2)		0.1			V/ns
Clock Fall Time peak to peak	tCHCL(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	tSLCH	tCSS	5			ns
/CS Not Active Hold Time relative to CLK	tCHSL		5			ns
Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	5			ns
/CS Active Hold Time relative to CLK	tCHSH		3			ns
/CS Not Active Setup Time relative to CLK	tSHCH		3			ns
/CS Deselect Time	tSHSL	tCSH	50			ns
Output Disable Time / Output Disable Time	tSHQZ	tDIS			7 / 8.5	ns
Clock Low to Output Valid 2.7V-3.0V / 3.0V-3.6V	tCLQV1	tV1			7 / 6	ns
Clock Low to Output Valid for RPMD OP2 command 2.7V-3.0V / 3.0V-3.6V	tCLQV2	tV2			8.5 / 7.5	ns
Output Hold Time	tCLQX	tHO	2			ns

Continued – next page

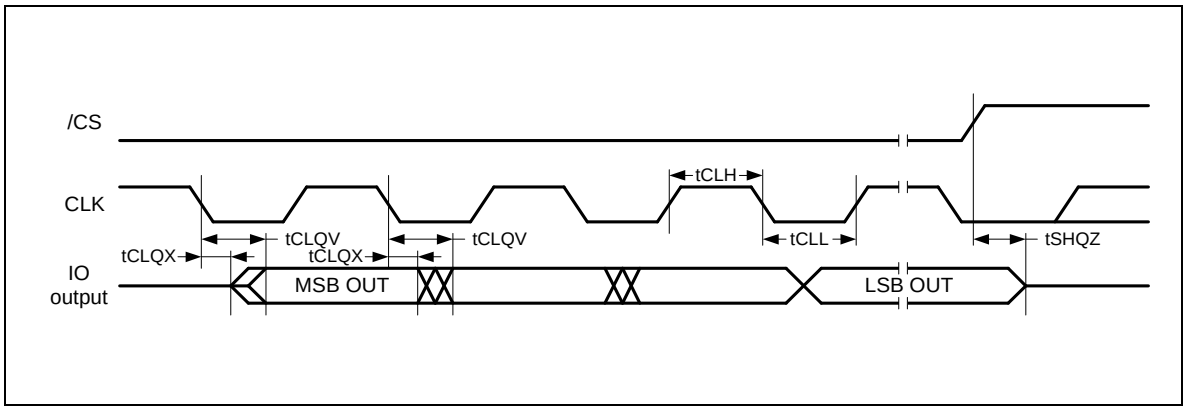
AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/CS High to Standby Mode	t_{RES1}(2)				3	µs
/CS High to next Instruction after Reset	t_{RST}(2)				30	µs
Write Root Key Register	t_{KEY}			170	250	µs
Update HMAC Key Register	t_{HMAC}			50	75	µs
Increment Monotonic Counter	t_{INC1}			80	200	µs
Increment Monotonic Counter (Counter Switching)	t_{INC2}			75	250	ms
RPMD Request Monotonic Counter	t_{REQ}			80	120	µs

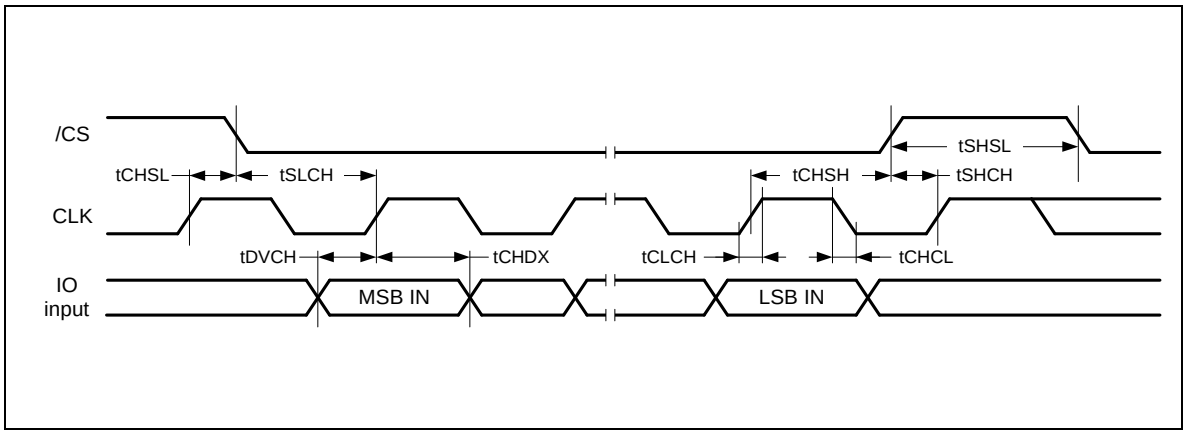
Notes:

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Tested on sample basis and specified through design and characterization data. TA = 25°C, VCC = 3. 0V.

7.7 Serial Output Timing Diagram

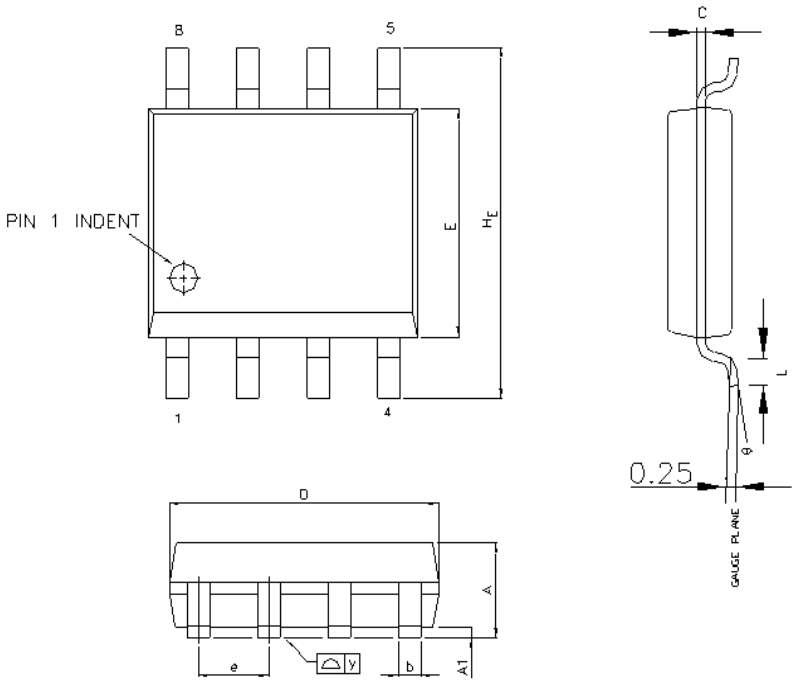


7.8 Serial Input Timing Diagram



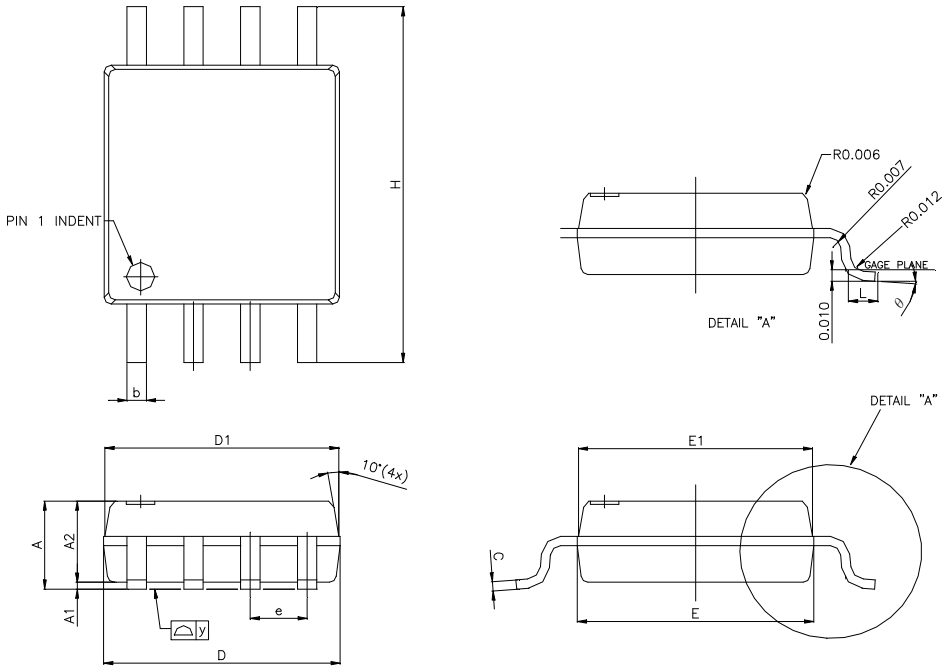
8. PACKAGE SPECIFICATIONS

8.1 8-Pin SOIC 150-mil (Package Code SN)



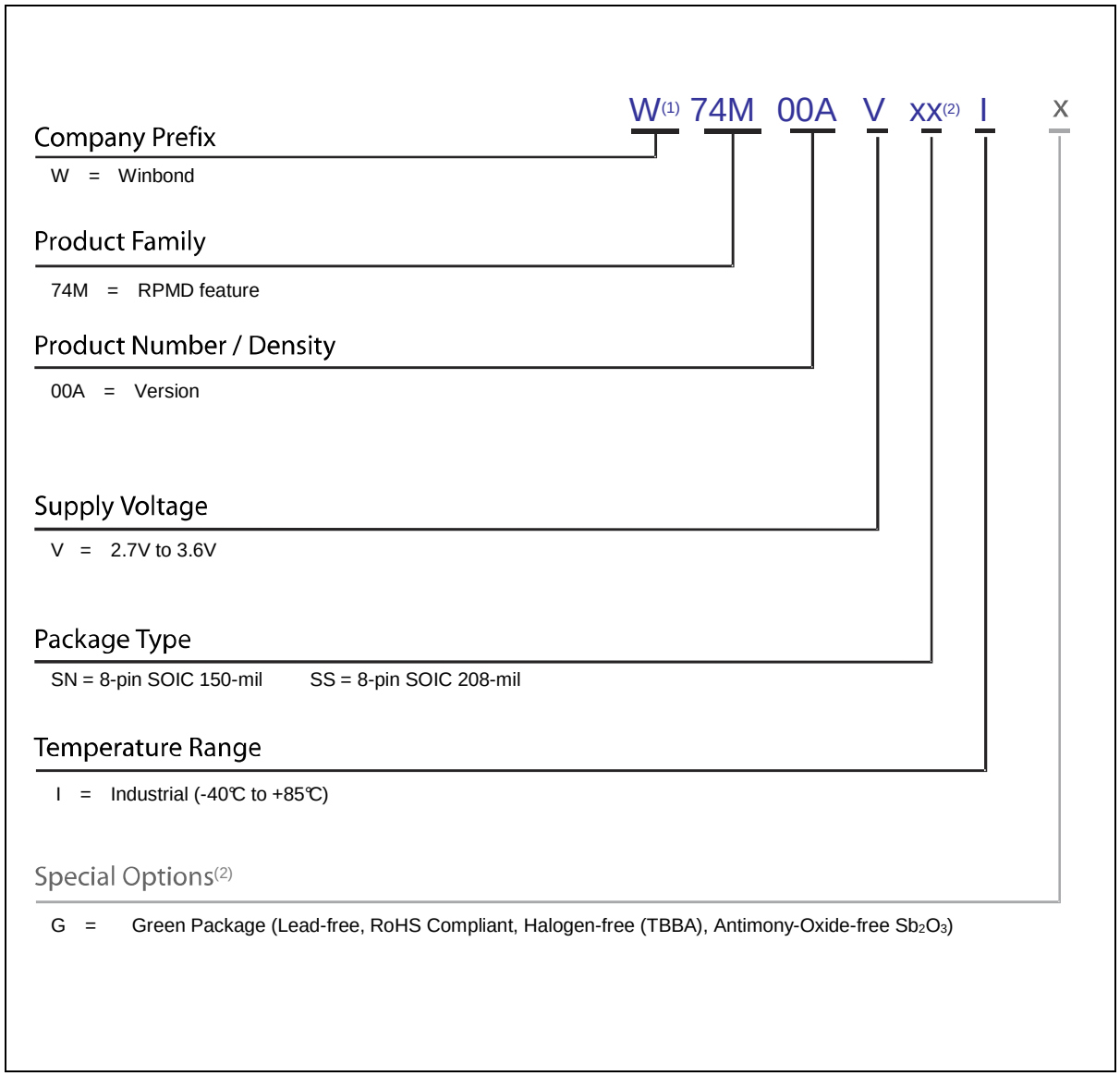
Symbol	Millimeters			Inches		
	Min	Mon	Max	Min	Mon	Max
A	1.35	1.60	1.75	0.053	0.062	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.0078	0.0098
D	4.80	4.85	5.00	0.188	0.190	0.197
E	3.80	3.90	4.00	0.150	0.153	0.157
H_E	5.80	6.00	6.20	0.228	0.236	0.244
e		1.27 BSC			0.050 BSC	
L	0.40	0.71	1.27	0.016		0.050
Y	---	---	0.10	---	---	0.004
θ	0°	---	10°	0°	---	10°

8.2 8-Pin SOIC 208-mil (Package Code SS)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.35	0.42	0.48	0.014	0.017	0.019
C	0.19	0.20	0.25	0.007	0.008	0.010
D	5.18	5.28	5.38	0.204	0.208	0.212
D1	5.13	5.23	5.33	0.202	0.206	0.210
E	5.18	5.28	5.38	0.204	0.208	0.212
E1	5.13	5.23	5.33	0.202	0.206	0.210
e	1.27 BSC			0.050 BSC		
H	7.70	7.90	8.10	0.303	0.311	0.319
L	0.50	0.65	0.80	0.020	0.026	0.031
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°

9. ORDERING INFORMATION



Notes:

1. The "W" prefix is not included on the part marking.
2. Standard bulk shipments are in Tube (shape E). Please specify alternate packing method, such as Tape and Reel (shape T) or Tray (shape S), when placing orders.

9.1 Valid Part Numbers and Top Side Markings

The following table provides the valid part numbers for the W74M00AV. Please contact Winbond for specific availability of different package types. Winbond RPMD use a 12-digit Product Number for ordering. However, due to limited space, the Top Side Marking on all packages uses an abbreviated 10-digit number.

PACKAGE TYPE	PRODUCT NUMBER	TOP SIDE MARKING
SN SOIC-8 150-mil	W74M00AVSNIG	74M00AVNIG
SS SOIC-8 208-mil	W74M00AVSSIG	74M00AVSIG

Note:

Contact Winbond for other package options.

10. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	08/31/2016		New Create Preliminary

Preliminary Designation

The “Preliminary” designation on a *Winbond* datasheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *Winbond* or an authorized sales representative should be consulted for current information before using this product.

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All other marks are the property of their respective owner.

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