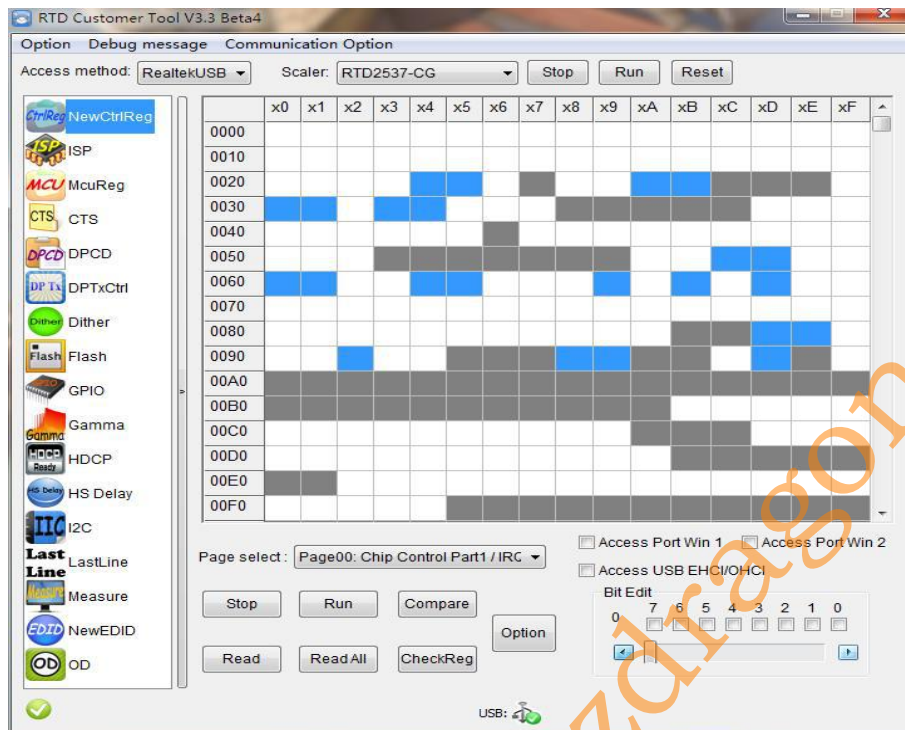


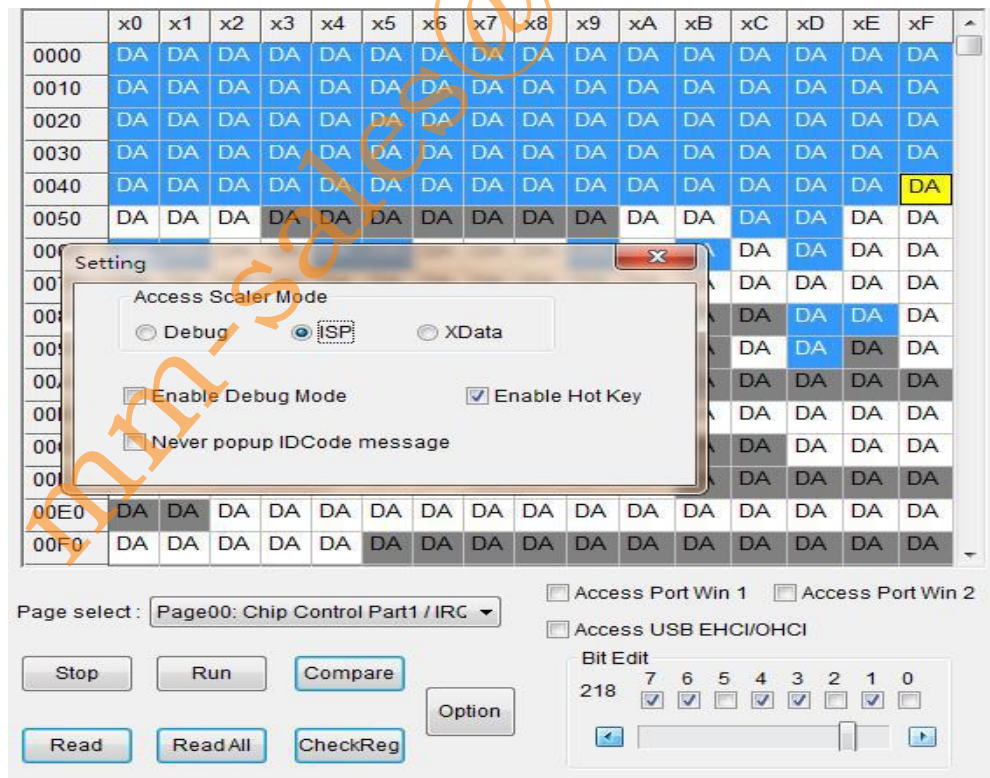


RTDTool-NewCtrlReg 使用

1. 打开 RTDTool.exe 软件，选择 NewCtrlReg 功能

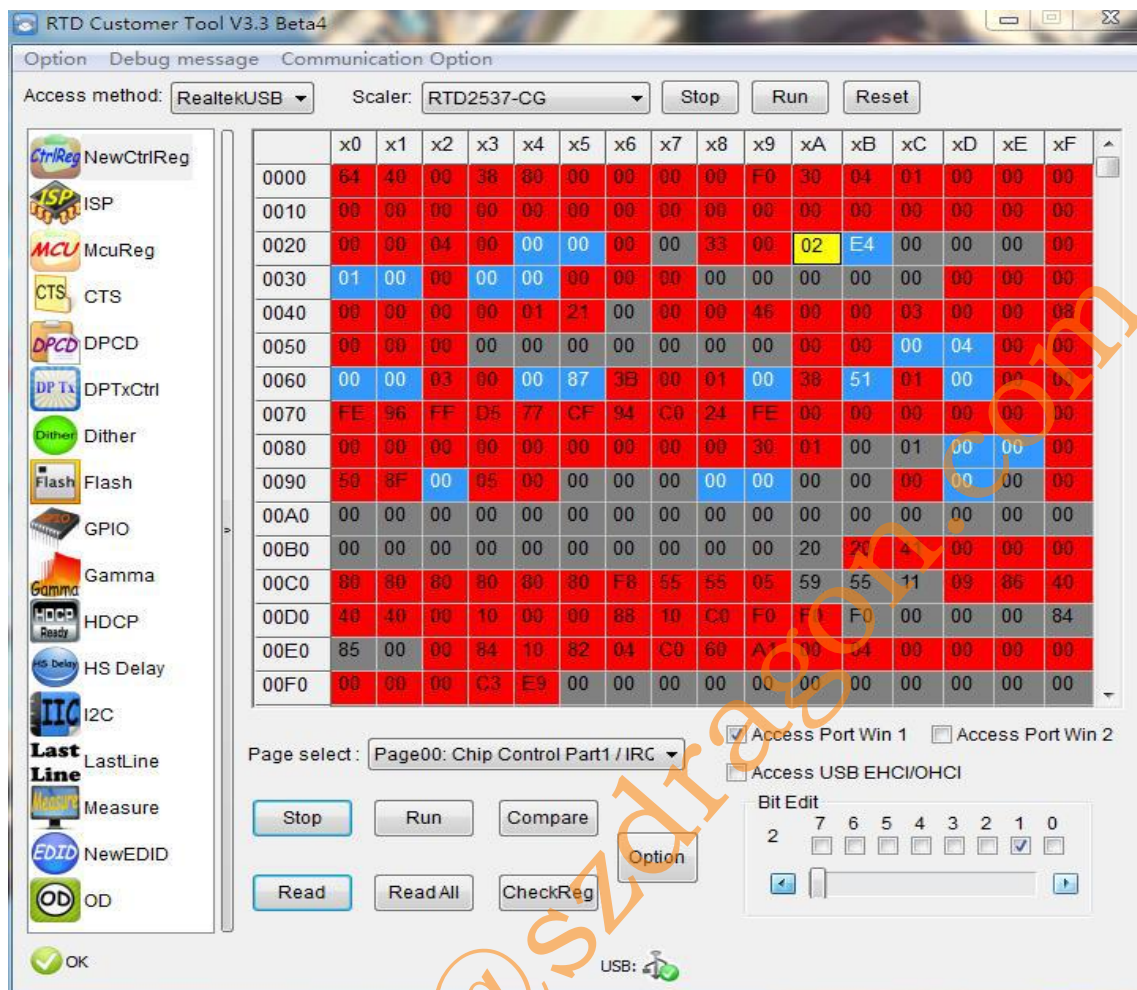


2. 点击左上角 “Option->Setting” 选择 ISP

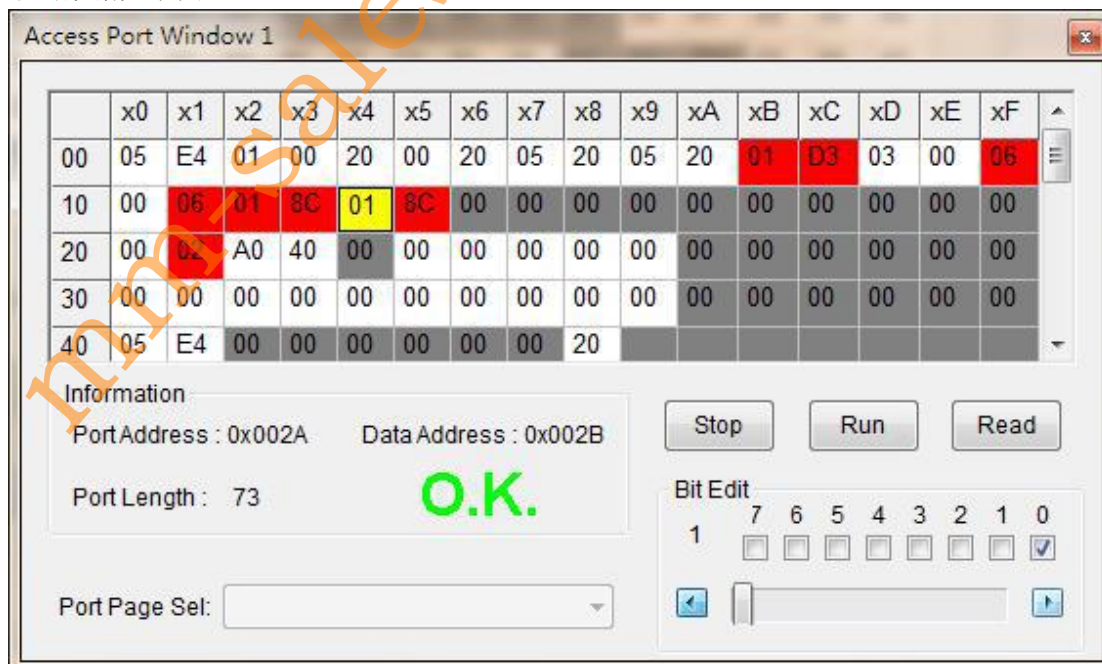




3.VGA 连接板子和电脑，待到测试屏出现图像时，点击“Read”读取数据



4.选择寄存器 A（上图黄色 02 处），点击右下角的“Access Port Win1”接着点击 Read 后读取的数据如下图：





Dragon Source

龍源電子

5.单击第一个数据（05，呈黄色），按下 F1，出现寄存器位的值，如下图所示：

Name	Bits	R/W	Default	Comments
series_linebufe	7	R/W	0	Merge four line buffers to two line buffers
Dummy	6:4	R/W	b000	Dummy Register
dh_total[11:8]	3:0	R/W/D	0x00	Display Horizontal Total Pixel Clocks: High Byte[11:8] Read value effective immediately after 0x002B_01 is written. When 0x002B_01 is written, then hardware will auto load these value into RTD as the trigger event happens. Double buffer triggered: If IMD_DB_EN (0x31C0[7]) is disable, and disp_dbl_en (0x002F[7]=1) is enable, when disp_dbl_rdy (0x002F[6]=1) is set, function effective as the DVS happens. If IMD_DB_EN (0x31C0[7]) is enable, function effective

6.通过一一读取各个寄存器位，最后汇成的数据如下图：

可以得到：

DH_TOAL:0X05E4-1508

DV_TOAL:0X01D3-467

dh_hs_width:0x0001-1

dv_vs_width:0x0003-3

分辨率：

width:1312-32=1280;

height:396-6=390

.....具体见下图



Dragon Source

龍源電子

DH_TOTAL: 0574 - 1508 ~~DATE~~

VT_TOTAL: 01D3 - 467

ah-hs-width: 0X0001 - 1

main-bh-sta: 0X0020 - 32

main-ah-sta: 0X0020 - 32

main-ah-end: 0X0520 - 1312

main-bh-end: 0X0520 - 1312

dlv-hs-width: 0X0003 - 3

main-bv-sta: 0X0006 - 6

main-cv-sta: 0X0006 - 6

main-cv-end: 0X018C - 396

main-bv-end: 0X018C - 396

px1032 = 1508 X 467 X 60 ~~1000~~
= 4225460 = 62M10

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7.修改程序的参数为:

```
//-----  
//1280x800  
code PanelType Panel3 =  
{  
    // Panel Style  
    ....  
  
    32,          // Display Horizontal Start Position  
    1280,        // Display Horizontal Width  
    3016, //1508, // Display Horizontal Total Clock Number in One Display  
Line  
    3016, //1508, // Display Horizontal Total Clock Number in One Display  
Line for CVBS PAL  
    3016, //1508, // Display Horizontal Total Clock Number in One Display  
Line for CVBS NTSC  
  
    6,  // Display Vertical Start Position  
    390, // Display Vertical Height  
    467, // Display Vertical Total Line Number in One Frame  
  
    8, //1,  // Display H Sync Width  
    3,  // Display V Sync Height  
  
    94, //52,  // Typical Pixel Clock in MHz  
  
    1100, // H Sync Max Freq Unit in 0.1 kHz  
    100,  // H Sync Min Freq Unit in 0.1 kHz  
    760,  // V Sync Max Freq Unit in 0.1 HZ  
    490,  // V Sync Min Freq Unit in 0.1 HZ  
  
    // TTL setting  
    //(2 << 4) | // Delay  
    //(1 << 1) | // DCLK output enable  
    0x00,      // DCLK Polarity  
};
```

蓝色部分的参数是根据读到的寄存器参数填写进入，后来编译发现没图像，最后将 DH_TOAL, DV_TOAL 翻一倍即红色部分才出图像。