LibreSilicon process HKUST (NFF)

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January 18, 2019

Abstract

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

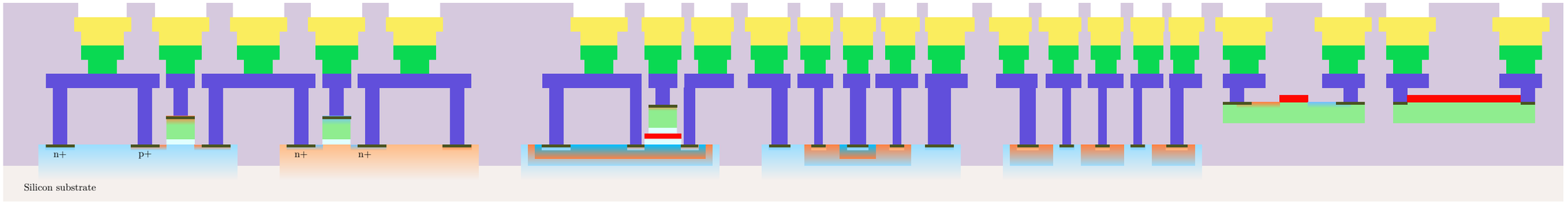
Please see the document with the generic steps[2] in order to get a detailed description of the different steps.

[1] https://github.com/chipforge/StdCellLib

[2] https://github.com/libresilicon/process/raw/master/process_steps/process_hightech/process_hightech_steps.pdf

Process Flow of Lanceville Technologies LibreSilicon $1\mu m$

- Project: LibreSilicon $1\mu m$
- Name: Lanceville Technologies Group
- Substrate: P-Substrate silicon wafer <100>
- Date: January 18, 2019



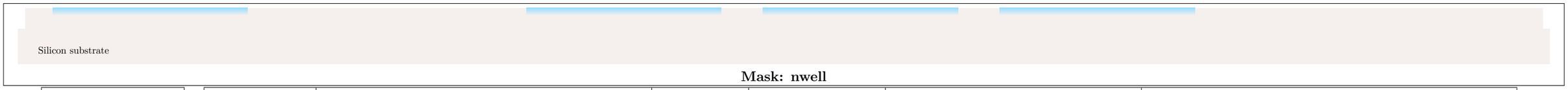
1 Initial alignment mask

Silicon substrate

Mask: basic

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	1.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	1.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	1.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5 \mu m$), soft bake: 110°C 1min
Clean	1.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Clean	1.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	1.6	Lam 490 etcher (DRY-490)	P2-01000	Clean	Etching the alignment crosses from HKUST	2 minutes (120nm)
Clean	1.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	1.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	1.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

2 N-well



Mask: nwell

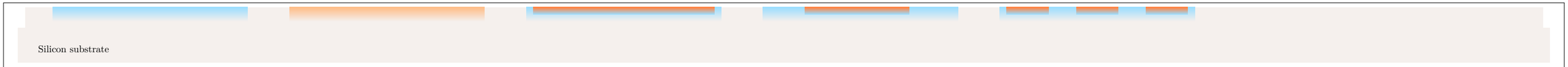
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	2.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	2.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	2.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Clean	2.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340 mJ cm^2$
Clean	2.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	2.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.33 \times 10^{12} cm^{-2}$@70keV
Clean	2.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	2.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	2.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

3 P-well

Mask: pwell

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	3.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	3.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	3.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Clean	3.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340 mJcm^2$
Clean	3.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	3.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$1.93 \times 10^{12} cm^{-2}$@40keV
Clean	3.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	3.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	3.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Clean	3.10	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	3.11	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	3.12	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Drive in	2 hours @ 1050°C in inert (N_2) environment

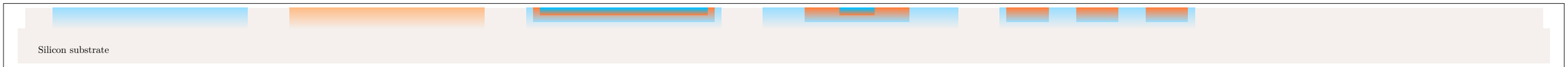
4 P-Base



Mask: pbase

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	4.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	4.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	4.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ($\approx 1.5 \mu m$), soft bake: 110°C 1min
Clean	4.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340 mJcm^2$
Clean	4.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	4.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$1.93 \times 10^{12} cm^{-2}$@40keV
Clean	4.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	4.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	4.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Clean	4.10	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	4.11	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	4.12	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Drive in	1 hour @ 1050°C in inert (N_2) environment

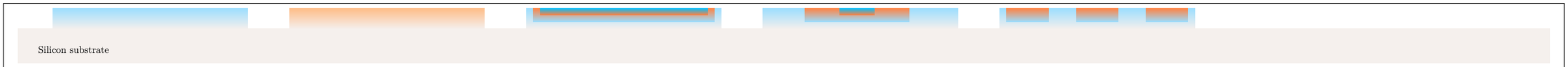
5 N-Base



Mask: nbase

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	5.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	5.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	5.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Clean	5.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340 mJcm^2$
Clean	5.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	5.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.33 \times 10^{12} cm^{-2}$@70keV
Clean	5.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	5.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	5.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Clean	5.10	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	5.11	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	5.12	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Drive in	1 hour @ 1050°C in inert (N_2) environment

6 Shallow trench isolation



Mask: sti

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	6.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	6.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	6.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Clean	6.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Clean	6.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	6.6	DRIE Etcher #1 (DRY-Si-1)	P2-01000	Clean	Etching the trenches	Thin line recipe, $1\mu m$: 7 cycles -> 14 cycles
Clean	6.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	6.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	6.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

7 Field oxide

Mask: fox

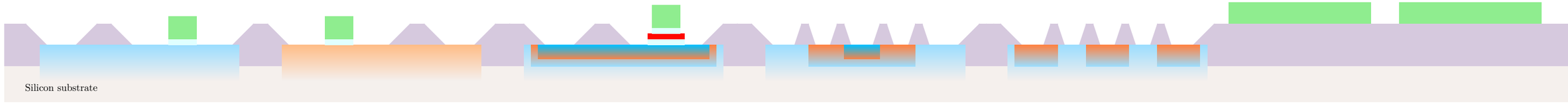
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	7.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	7.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	7.3	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Oxide deposition	$3\mu m$ LTO
Clean	7.4	Strasbaugh CMP (CMP-1)	P2-10000	Clean	Planarize oxide down to silicon	Use oxide planarization slurry
Clean	7.5	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	7.6	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	7.7	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Oxide deposition	100 nm LTO
Clean	7.8	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Clean	7.9	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Clean	7.10	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	7.11	AOE Etcher (DRY-AOE)	P2-01000	Clean	Etch oxide FOX openings	Etch through 100nm
Clean	7.12	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	7.13	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	7.14	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

8 SONOS

Mask: sonos

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	8.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	8.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	8.3	Diff. Furnace-D1 Dry Oxidation (Only for gate oxide) (DIF-D1)	P2-01000	Clean	Lower gate oxide growth	5nm
Clean	8.4	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	8.5	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	8.6	LPCVD-B2 Nitride/Low-Stress Nitride (CVD-B2)	P2-01000	Clean	Charge carrying nitride growth	10nm
Clean	8.7	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Clean	8.8	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Clean	8.9	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	8.10	Lam 490 etcher (DRY-490)	P2-01000	Clean	Nitride etch	6 seconds (10nm, 100nm/min)
Clean	8.11	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	8.12	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	8.13	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

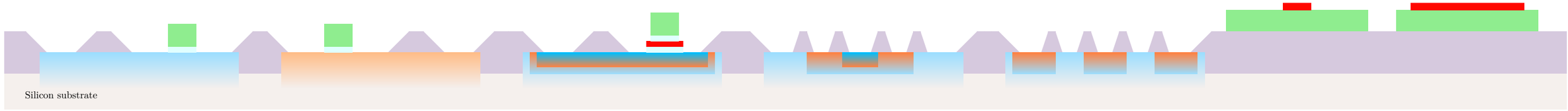
9 Gate



Mask: poly

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	9.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	9.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	9.3	Diff. Furnace-D1 Dry Oxidation (Only for gate oxide) (DIF-D1)	P2-01000	Clean	Gate oxide growth	40nm, 33 minutes 14 seconds @ 1050°C in dry environment
Clean	9.4	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	9.5	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	9.6	LPCVD-A3: Amor-Si/Poly (CVD-A3)	P2-01000	Clean	Gate electrode growth	100nm of poly silicon
Clean	9.7	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Clean	9.8	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Clean	9.9	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	9.10	Poly etcher (DRY-Poly)	P2-01000	Clean Semi clean	Poly silicon etch	HBr only, 2 minutes
Clean	9.11	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	9.12	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	9.13	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

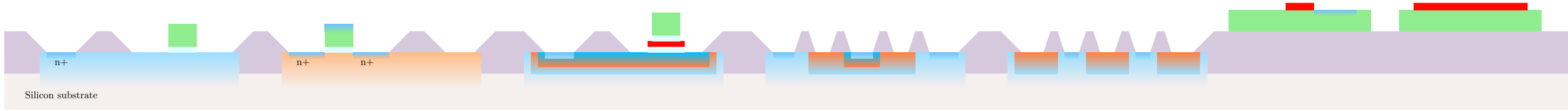
10 Implant stop



Mask: implantstop

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	10.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	10.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	10.3	LPCVD-B2 Nitride/Low-Stress Nitride (CVD-B2)	P2-01000	Clean	Implant stop Nitride hard mask	100nm
Clean	10.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Clean	10.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Clean	10.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	10.7	Lam 490 etcher (DRY-490)	P2-01000	Clean	Nitride etch	roughly 1 minute (100nm, 100nm/min)
Clean	10.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
Clean	10.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

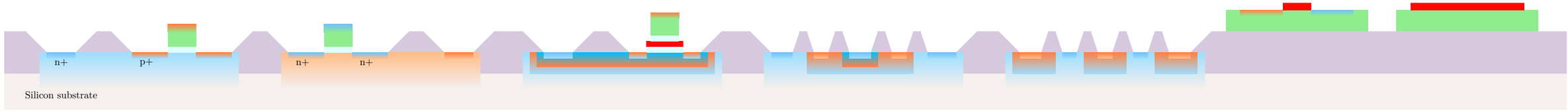
11 N+ implant



Mask: nimplant

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	11.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	11.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	11.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ($\approx 1.5 \mu m$), soft bake: 110°C 1min
Clean	11.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340 mJ cm^2$
Clean	11.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	11.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$ @ 90keV
Clean	11.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	11.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	11.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

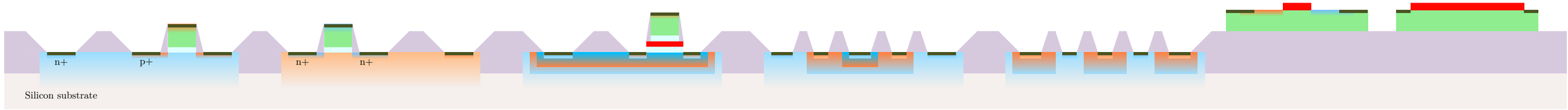
12 P+ implant



Mask: pimplant

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	12.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	12.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	12.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ($\approx 1.5 \mu m$), soft bake: 110°C 1min
Clean	12.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340 mJ cm^2$
Clean	12.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	12.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$ @ 35keV
Clean	12.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	12.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	12.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Clean	12.10	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	12.11	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	12.12	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Drive in	10 minutes @ 1050°C in inert (N_2) environment

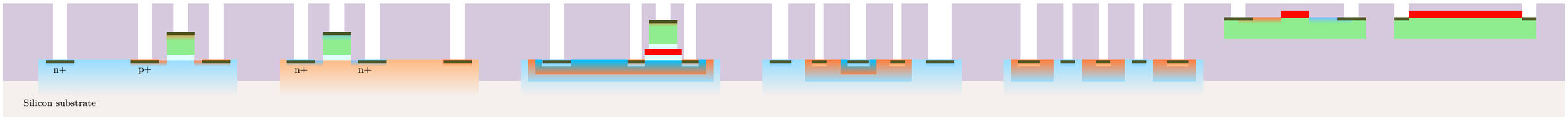
13 Silicification



Mask: silicideblock

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	13.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	13.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	13.3	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Spacer oxide	50 nm
Clean	13.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Clean	13.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Clean	13.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	13.7	AOE Etcher (DRY-AOE)	P2-01000	Clean	Anisotropic oxide etch	12 seconds
Clean	13.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
Clean	13.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	13.10	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Titanium	15 seconds (roughly 60nm)
Semi clean	13.11	AG610 RTP (DIF-R2)	P2-01000	Semi clean	First reaction phase	240 seconds @ 700°C
Semi clean	13.12	E2: General purpose (WET-E2)	P2-01000	Semi clean	Remove unreacted Titanium	HF:DI (1:10) solution, a few seconds
Semi clean	13.13	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	13.14	AG610 RTP (DIF-R2)	P2-01000	Semi clean	Second reaction phase	240 seconds @ 800°C

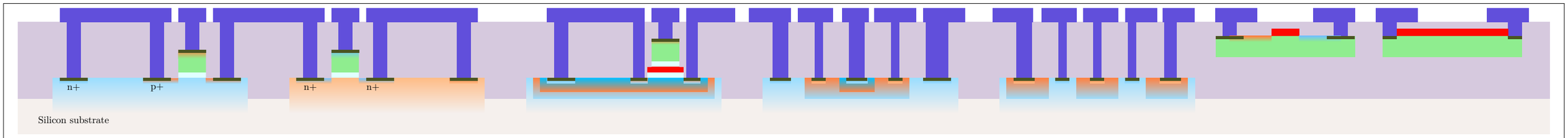
14 Contact



Mask: contact

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	14.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	14.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	14.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	$1\mu m$ LTO
Semi clean	14.4	Buehler Polisher #1 (CMP-4)	Rm. 2227	Semi clean	Planarize oxide	
Semi clean	14.5	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Semi clean	14.6	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJ cm^2$
Semi clean	14.7	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	14.8	Trion RIE Etcher (DRY-Trion)	P2-01000	Semi clean	$1\mu m$ LTO etch	TODO
Semi clean	14.9	IPC 3000 Asher #1 (DRY-PR-2)	P2-01000	Semi clean	Resist strip	pr 25 minutes

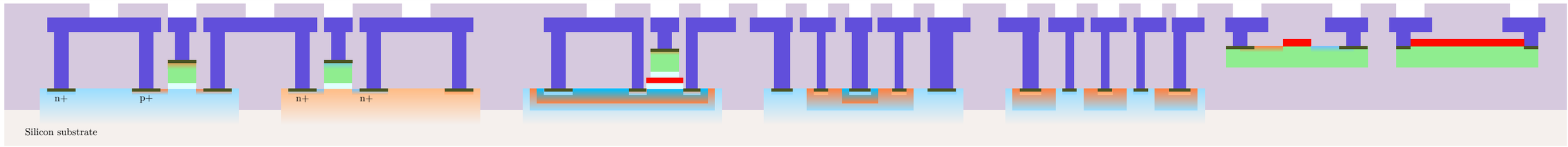
15 Metal 1



Mask: metal1

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	15.1	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Aluminum + Titanium finish	Aluminum (roughly 200nm) + Titanium (roughly 30nm)
Semi clean	15.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Semi clean	15.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Semi clean	15.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	15.5	AST Metal Etcher (DRY-Metal-1)	P2-01000	Semi clean	Wire formation	200 nm
Semi clean	15.6	IPC 3000 Asher #1 (DRY-PR-2)	P2-01000	Semi clean	Resist strip	pr 25 minutes

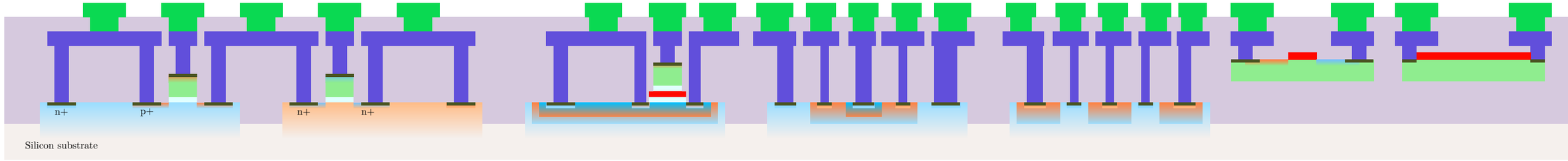
16 Via 1



Mask: via1

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	16.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	16.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	16.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	$1\mu m$
Semi clean	16.4	Buehler Polisher #1 (CMP-4)	Rm. 2227	Semi clean	Planarize oxide	
Semi clean	16.5	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Semi clean	16.6	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Semi clean	16.7	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	16.8	Trion RIE Etcher (DRY-Trion)	P2-01000	Semi clean	$1\mu m$ LTO etch	TODO
Semi clean	16.9	IPC 3000 Asher #1 (DRY-PR-2)	P2-01000	Semi clean	Resist strip	pr 25 minutes

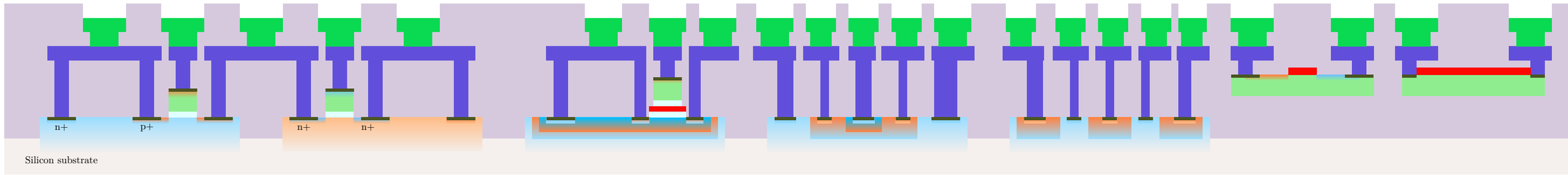
17 Metal 2



Mask: metal2

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	17.1	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Aluminum + Titanium finish	Aluminum (roughly 200nm) + Titanium (roughly 30nm)
Semi clean	17.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Semi clean	17.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Semi clean	17.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	17.5	AST Metal Etcher (DRY-Metal-1)	P2-01000	Semi clean	Wire formation	200 nm
Semi clean	17.6	IPC 3000 Asher #1 (DRY-PR-2)	P2-01000	Semi clean	Resist strip	pr 25 minutes

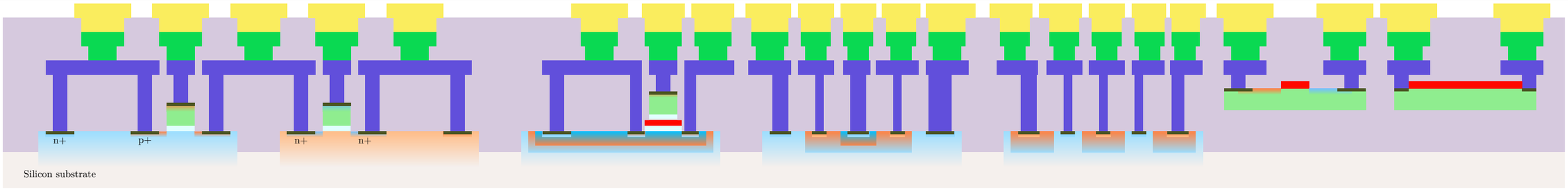
18 Via 2



Mask: via2

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	18.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	18.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	18.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	$1\mu m$
Semi clean	18.4	Buehler Polisher #1 (CMP-4)	Rm. 2227	Semi clean	Planarize oxide	
Semi clean	18.5	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Semi clean	18.6	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Semi clean	18.7	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	18.8	Trion RIE Etcher (DRY-Trion)	P2-01000	Semi clean	$1\mu m$ LTO etch	TODO
Semi clean	18.9	IPC 3000 Asher #1 (DRY-PR-2)	P2-01000	Semi clean	Resist strip	pr 25 minutes

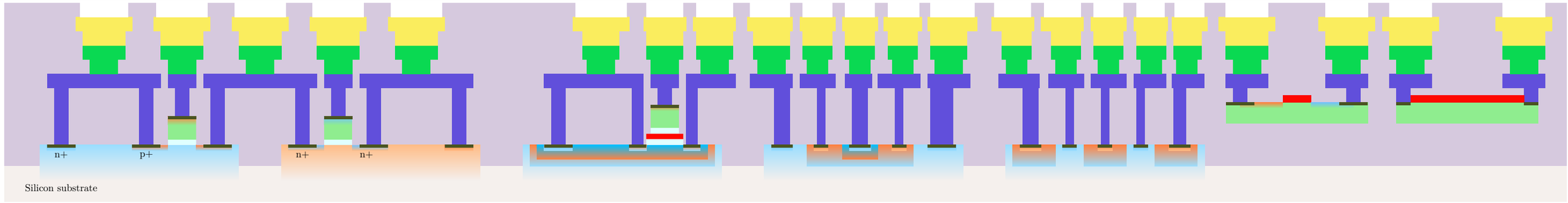
19 Metal 3



Mask: metal3

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	19.1	Varian 3180 Sputter (SPT-3180)	P2-01000	Semi clean	Deposit Aluminum + Titanium finish	Aluminum (roughly 200nm) + Titanium (roughly 30nm)
Semi clean	19.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Semi clean	19.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Semi clean	19.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	19.5	AST Metal Etcher (DRY-Metal-1)	P2-01000	Semi clean	Wire formation	200 nm
Semi clean	19.6	IPC 3000 Asher #1 (DRY-PR-2)	P2-01000	Semi clean	Resist strip	pr 25 minutes

20 Glass



Mask: glass

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	20.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	20.2	Spin Dryer-D (SRD-D)	P2-01000	Semi clean	Dry the wafer automatically	
Semi clean	20.3	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	$1\mu m$
Semi clean	20.4	Buehler Polisher #1 (CMP-4)	Rm. 2227	Semi clean	Planarize oxide	
Semi clean	20.5	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ($\approx 1.5\mu m$), soft bake: 110°C 1min
Semi clean	20.6	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280 mJcm^2$
Semi clean	20.7	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	20.8	Trion RIE Etcher (DRY-Trion)	P2-01000	Semi clean	$1\mu m$ LTO etch	TODO
Semi clean	20.9	IPC 3000 Asher #1 (DRY-PR-2)	P2-01000	Semi clean	Resist strip	pr 25 minutes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