Abstract

This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells[1] and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent $1\mu m$ to smaller structure sizes. **This process is for manufacturing $1\mu m$ only!** But further releases which will have been tested with smaller structure sizes can be expected.

[1] `https://github.com/chipforge/StdCellLib`

Contents

Libre Silicon process steps

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July 14, 2019

The general flow chart of the overall process flow can be seen in Figure 1. These process steps will be discussed within the following sections.

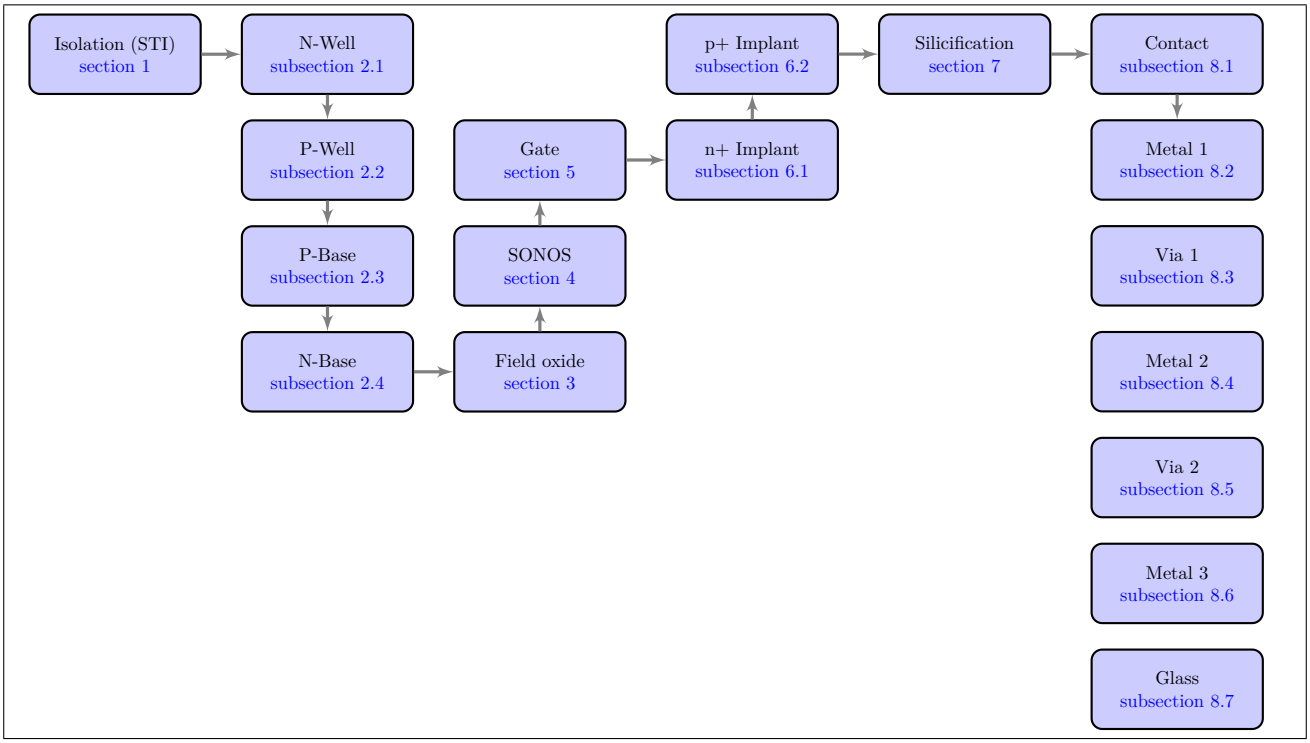

Figure 1: Frontend and backend process flow

The six overall process steps are part of an active part of the technology, while the final metal (respectively contact) layers will be used for making a contact between the logic gates and macro cells and making them available to the exterior world.
For this process p-substrate is the required basic substrate, but forks and modifications will be very well possible based on a Graphene substrate or alike, still under the LSPL. The starting material is a p-type, <100> oriented silicon with a doping concentration of $\approx 9 \times 10^{14} cm^{-3}$.

Machines required:

- Ion implanter
- Plasma etcher
- Sputter engine (Metal deposition)
- Diffusion furnace
- Exposure unit

1 Shallow trench isolation

The geometry of a substrate with STI implemented can be seen in Figure 2.

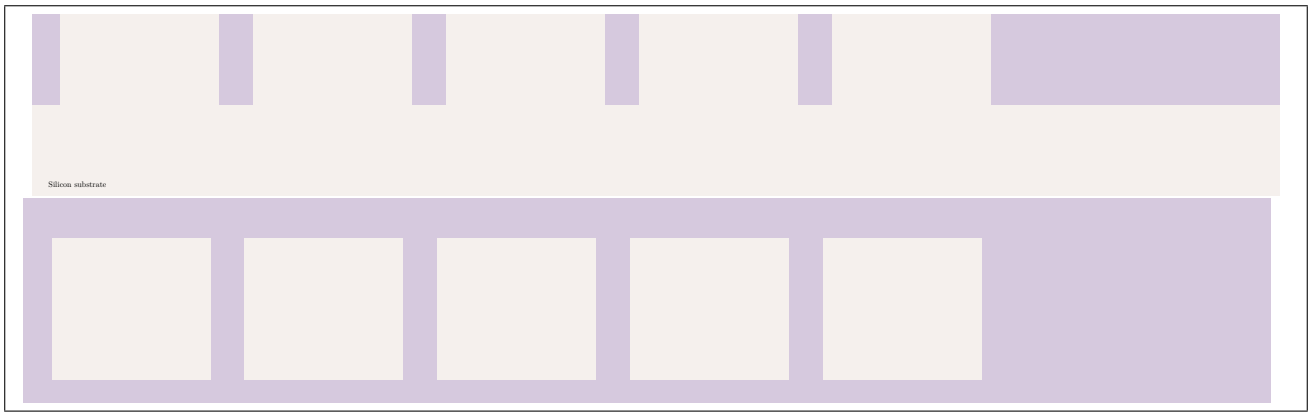

Figure 2: Shallow trench isolation target geometry

As can be seen in Figure 5, the N-well and the STI trench are supposed to have approximately the same depth but the N-well and P-well go down a little bit further.
Because the N-well will be $\approx 4\mu m$ in depth we have to match this with our trench depth.
I order to allow a sufficiently low resistance of the ESD diode but at the same time a sufficient isolation of between the standard cells a trade-off has been done.
The targeted depth of the box isolation is $\approx 4\mu m$.
The STI area will be everywhere, where no well areas are.
We use a dry etching method for cutting into the silicon substrate and making the active area become islands with trenches in between.
After that we fill the trenches with LTO or PSG and polish the wafer until the LTO/PSG surface and the silicon island surface are sufficiently on the same level.
Our minimum width and height as well as the space between the active areas comes from the line space constrain of the silicon etcher and of course the optical limitations of the stepper which are as well $0.5\mu m$.

1.1 Silicon etching

The trench depth has to be at least 4.5 microns deep, in order to compensate for sacrificial silicon polishing during the later CMP steps.

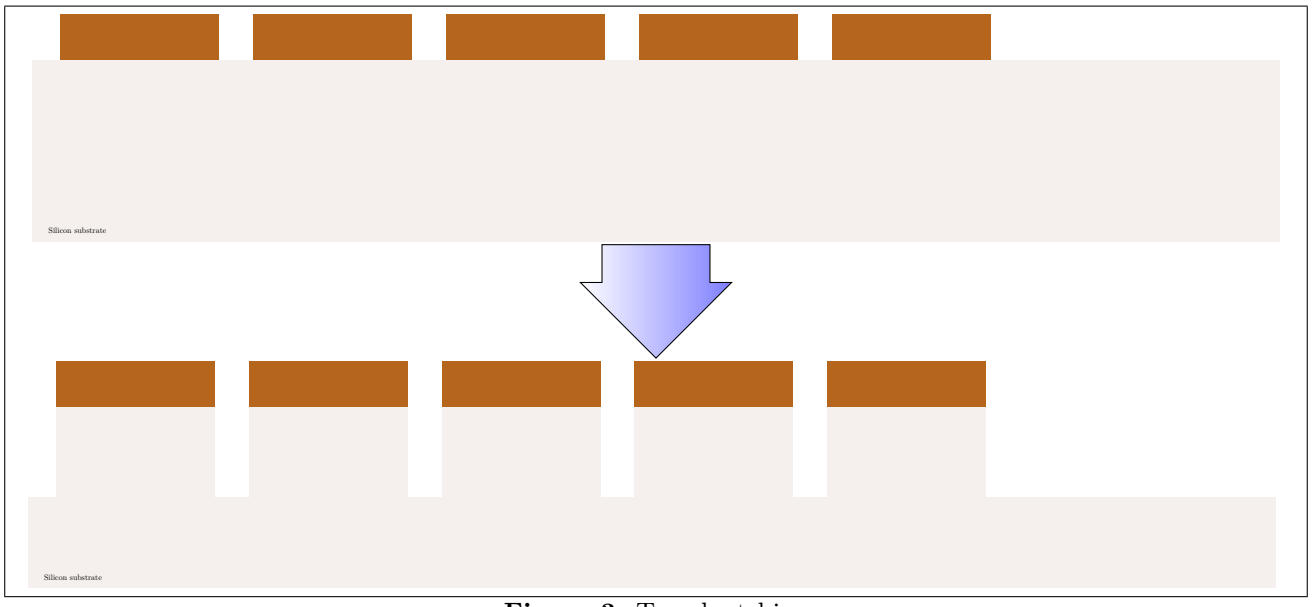

Figure 3: Trench etching

Typically it's a good approach to set the parameters of the DRIE recipe to an amount of cycles which will result in a depth of roughly 5 microns.

1.2 LTO/PSG+CMP

Now we trenches need to be filled up with LTO/PSG and planarized until we meet a sufficiently low height differential between the oxide surface and the silicon surface.

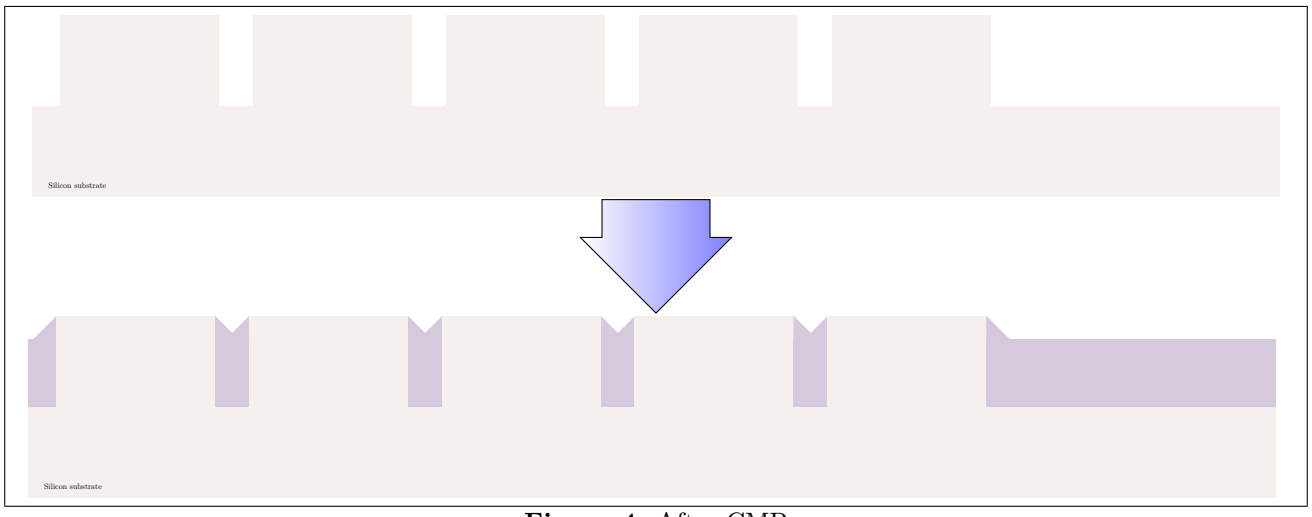

Figure 4: After CMP

This process loop until a height differential below 200nm is being reached turned out to be a good approach. We start counting LTO+CMP steps at 1:

- Deposit $\frac{5\mu}{2^{step-1}}$ LTO/PSG
- CMP around $\frac{5\mu}{2^{step-1}}$ LTO/PSG
- Clean in hot ammonia
- Put into DI:HF (50:1) for one or two minutes, until silicon surface on the islands is free of LTO/PSG
- Repeat until height differential lower than 200nm

2 Tripple Well

In order to build BiCMOS we need nested wells for getting the vertical diode structures which form the bi junction transistors.
A vertical isolation, which allows us to have some bulk areas on a higher potential than others, and isolated FETs come along from this tripple well architecture for free.
The cross section of the targeted geometry are shown in Figure 5

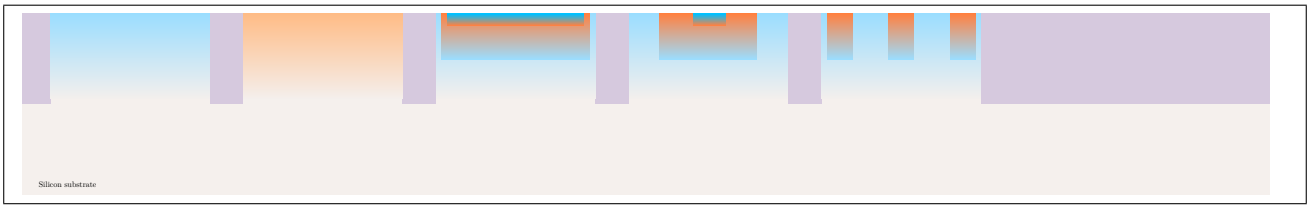

Figure 5: Tripple well target geometry

Since the diffusion constant variates with the concentration of background dopants, we have to make sure that the thermal budget has enough slack during every single tripple well formation step, in order to avoid the consumption of one of the wells during further processing.

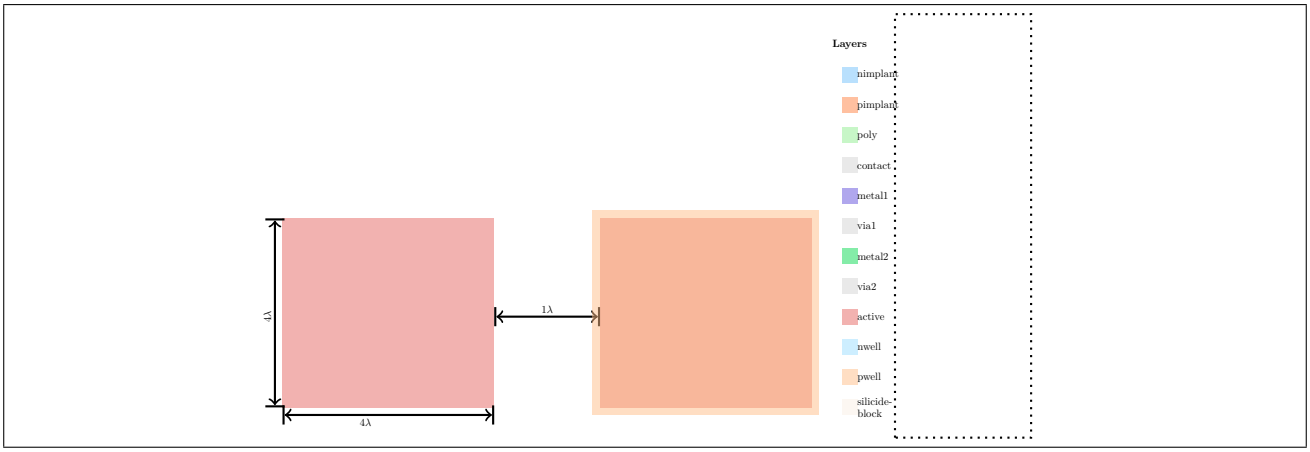

Figure 6: P-Well layout

In Figure 6 the layout of the well and base regions on top of the active area region can be seen.
The implant values are as calculated in the documentation of the process design leading to these steps[1].

[1] https://github.com/leviathanch/libresiliconprocess/raw/master/process_design/process_design.pdf

2.1 N-well

In order to build CMOS on the same substrate, an N-well is required for building the complementary P-channel transistor for a NFET+PFET logic circuitry.
The cross section as well as the top view of the targeted geometry are shown in Figure 7

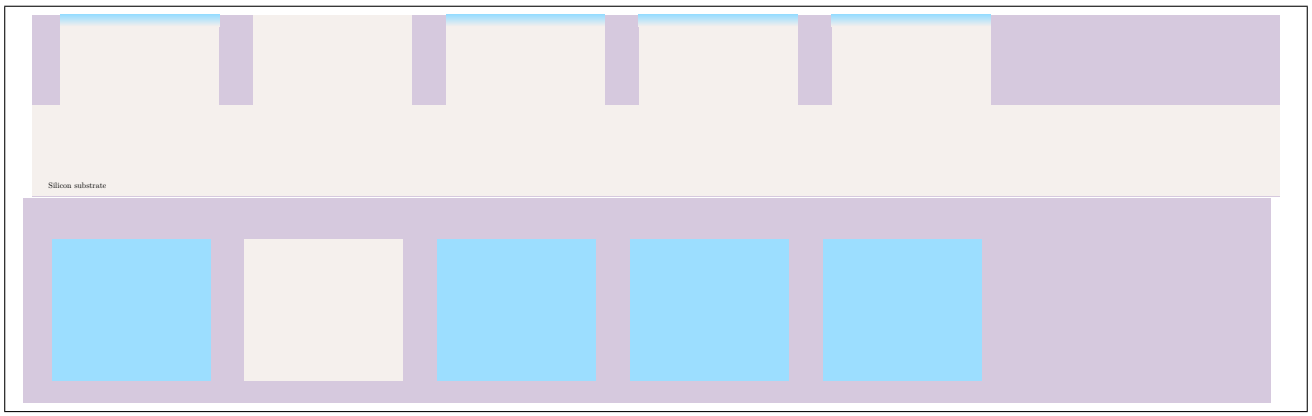

Figure 7: N-well target geometry

The N-well will serve us as an island of N-doped substrate within the P-doped basis substrate.
The P-dopant concentration of our prime grade, p-type, single side polished, four inch wafers is between $8.76 \cdot 10^{14} \frac{1}{cm^3}$ and $5.23 \cdot 10^{14} \frac{1}{cm^3}$
This means we need a dose of $2.33 \times 10^{12} cm^{-2}$ Phosphorus at 70 keV.
The concentration will need adjustment when the used substrate has different properties!

2.2 P-well

In order to build CMOS on the same substrate, a P-well is required for building the complementary N-channel transistor for a NFET+PFET logic circuitry.
The cross section as well as the top view of the targeted geometry are shown in Figure 7

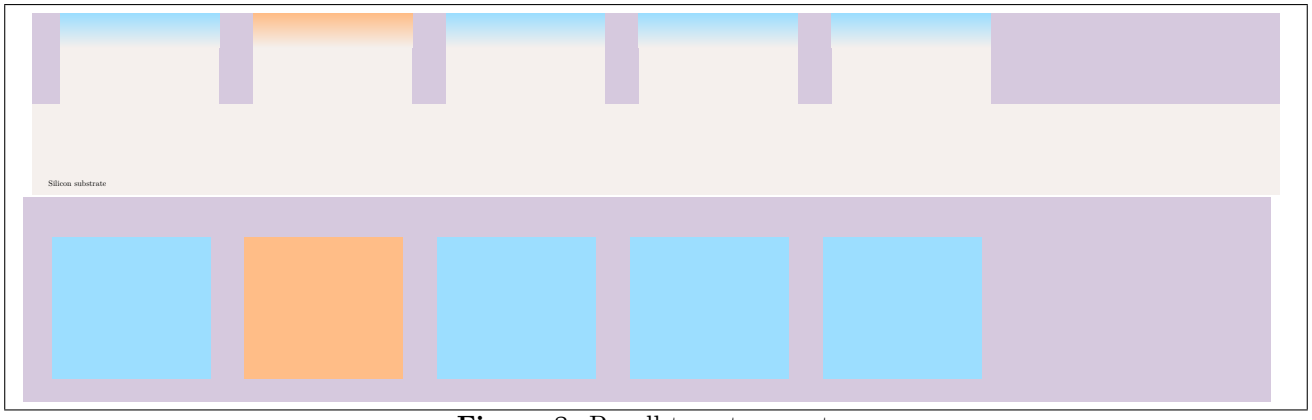

Figure 8: P-well target geometry

The "P-well" will serve us as an island of higher p-doped substrate within the slightly p-doped basis substrate and gives us more flexibility with suppliers, because we can just adjust the doping in case the concentration might be different with another supplier.
The P-dopant concentration of our prime grade, p-type, single side polished, four inch wafers is between $8.76 \cdot 10^{14} \frac{1}{cm^3}$ and $5.23 \cdot 10^{14} \frac{1}{cm^3}$
This means we need a dose of $1.93 \times 10^{12} cm^{-2}$ Boron atoms at 40 keV.
The concentration will need adjustment when the used substrate has different properties!
After the implantation we perform a drive-in in inert atmosphere at 1050°C for two hours and don't have to worry about the substrate anymore.

2.3 P-base

In order to build BiCMOS on the same substrate, a nested P-well within the N-well (now it's twin well) is required for building the bijunction transistors.
The cross section as well as the top view of the targeted geometry are shown in Figure 9

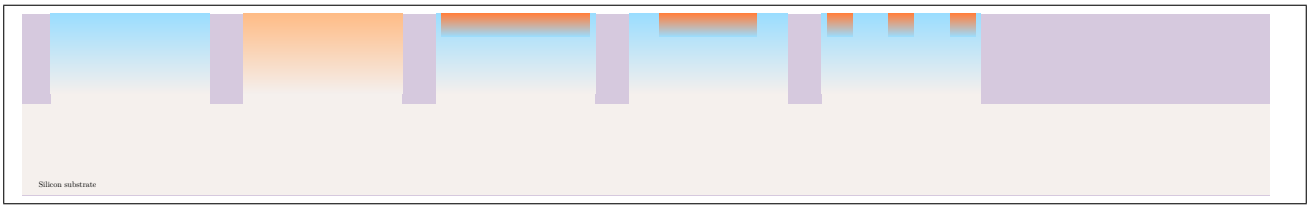

Figure 9: P-base cross section

The P-base will serve us as an island of higher P-doped substrate within the slightly N-well basis substrate, which will result in a isolated area by forming PN junction versus PN junction.
The dopant dose will be $1.93 \times 10^{12} cm^{-2}$ at 40 keV.
The P-base can very well cover the N-well area since the expansion mostly is vertical, but it should be kept in mind, that there is also a lateral diffusion when placing contacts also on N-well around the P-base.
After the implantation we perform a drive-in in inert atmosphere at 1050°C for one hour.

2.4 N-base

In order to build BiCMOS on the same substrate, another N-well within the P-Base (tripple well!) is required for building the complementary isolated P-channel transistor for a n-p-channel logic circuitry as shown above in the example section.
The cross section as well as the top view of the targeted geometry are shown in Figure 10

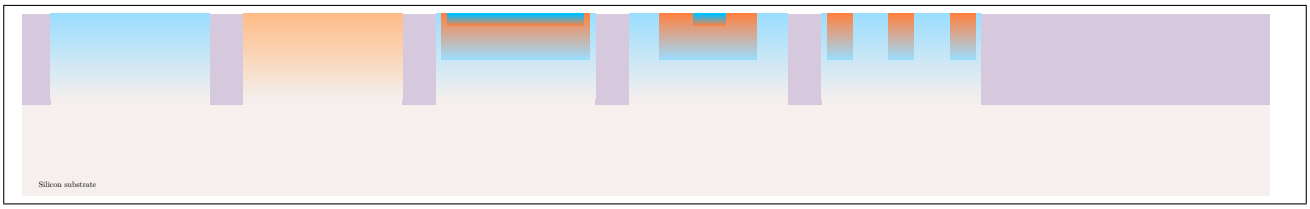

Figure 10: N-base target geometry

The N-well will serve us as an island of N-doped substrate within the P-doped basis substrate.
The dopant dose will be $2.33 \times 10^{12} cm^{-2}$ at 70 keV.

3 Field oxide

The geometry of a substrate with the field oxide filling the shallow trenched from section 1 now needs to be made.

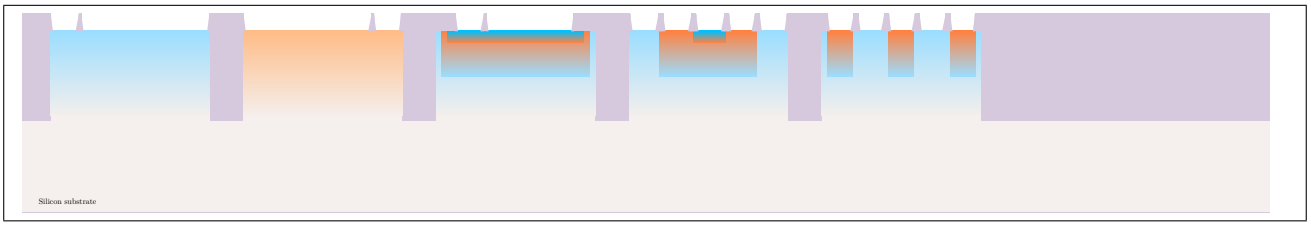

Figure 11: Shallow trench isolation target geometry

As can be seen in Figure 11, the islands need to be covered with silicon oxide and windows need to be etched into the oxide so that the gate can be constructed later on.
The covering oxide and windows are needed so that the poly silicon is far enough away from the non-active areas so that the threshold voltage of the parasitic FETs is so high that they will never switch.
Only within the active areas we want to allow the poly layer to touch down closer to the silicon.
The mask is called ”fox” on the mask set.
LTO is used here, but can also be replaced by PSG if LTO deposition isn't available for higher thicknesses.
The LTO thickness has been chosen to be 200nm which is thin enough for the polysilicon gates to overcome the height difference without damage and still being enough for eliminating parasitic effects.

3.1 Oxide deposition

Now we need to deposit the silicon dioxide which will provide a spacer between the non active area and the polysilicon gate layer. within the non-active areas.

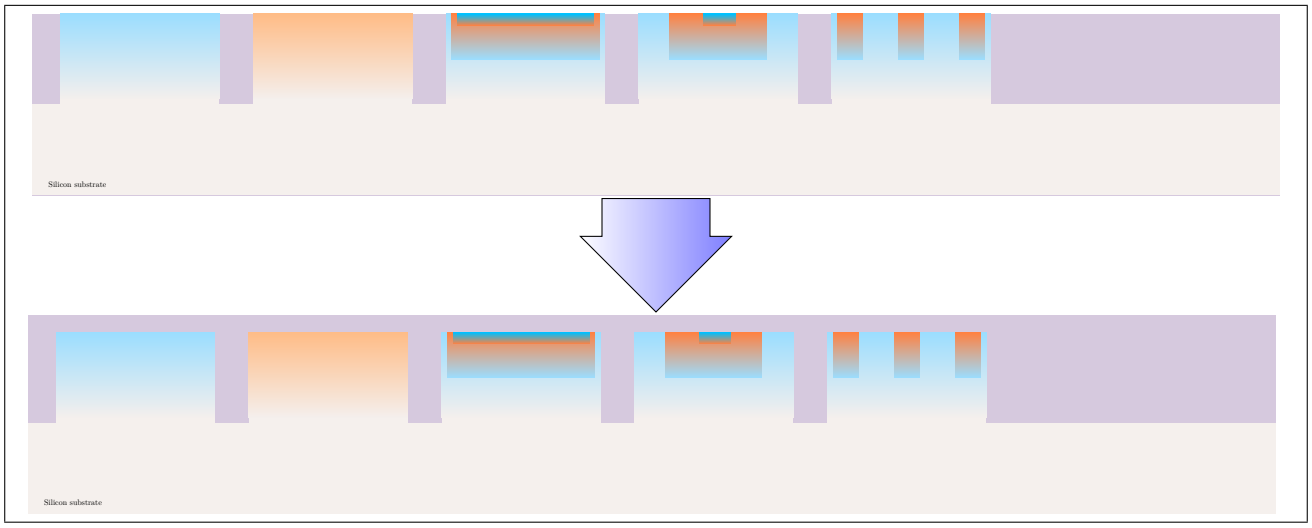

Figure 12: LTO deposition

We deposit a roughly 200nm thick layer of silicon dioxide by putting the wafer into the LPCVD furnace.

3.2 Etching

We open the access to the silicon inside of the active areas in order to touch down with the polysilicon further on.

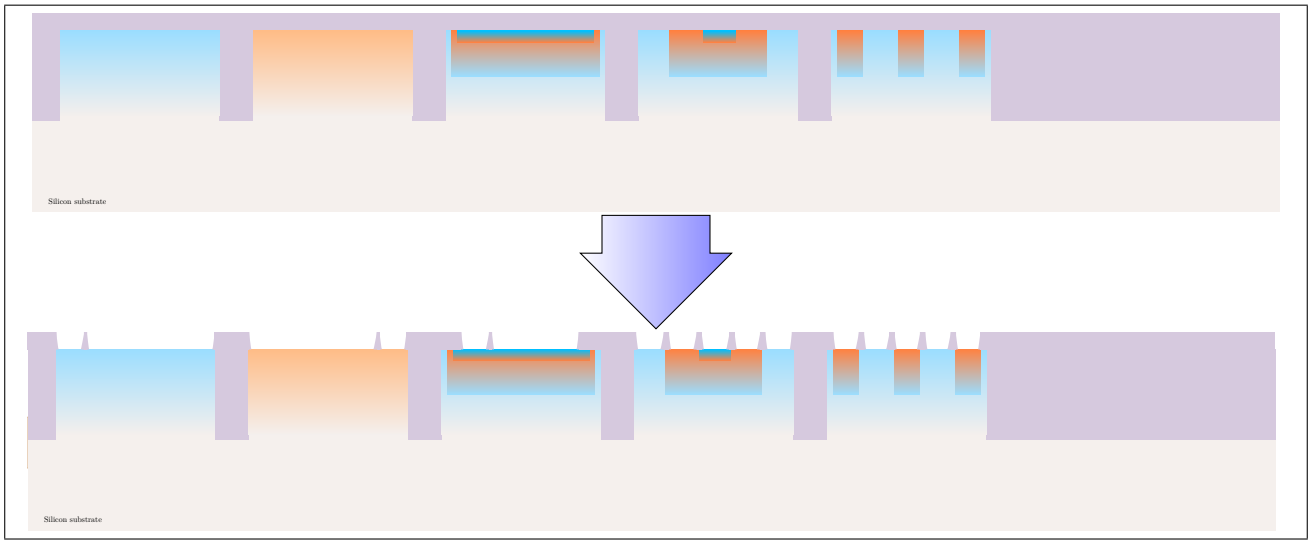

Figure 13: LTO etching

The etching time variates from machine to machine and recipe to recipe. Do the math.

4 SONOS

Before we can construct the gate, we have to put some pads of oxide-nitride-oxide sandwich roughly in the area where the SONOS (silicon oxide nitride oxide silicon) gates will be located.
Later on, during etching of the polysilicon gates, the SONOS gate oxide sandwich will be automatically aligned with the gate because excess SONOS sandwich material will be etched away with the normal gate oxide.

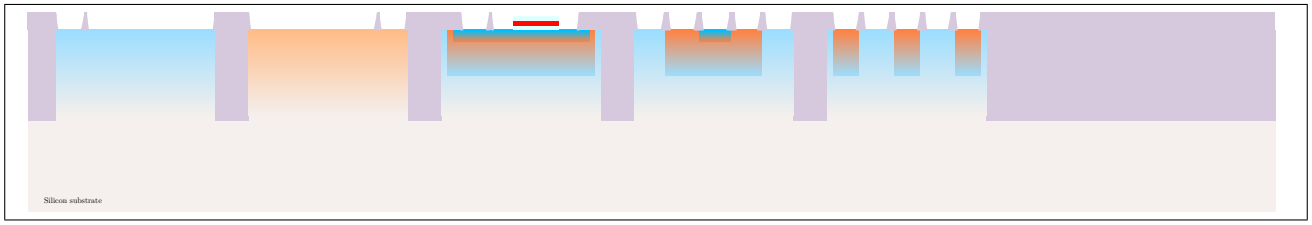

Figure 14: SONOS sandwich pad

The line spacing of the SONOS shape has to be at least $0.5\mu m$ because of the resolution of the stepper and also because of the etching process which has $0.5\mu m$ as the minimum line spacing.
Also there has to be at least one lambda on each site to compensate for offsets, so the SONOS mask is bloated by $0.5\mu m$.

4.1 Lower oxide deposition

Now we have to deposit the lower part of the SONOS sandwich by depositing LTO.
As designed in the process design document, the layer will be around 7nm thick.

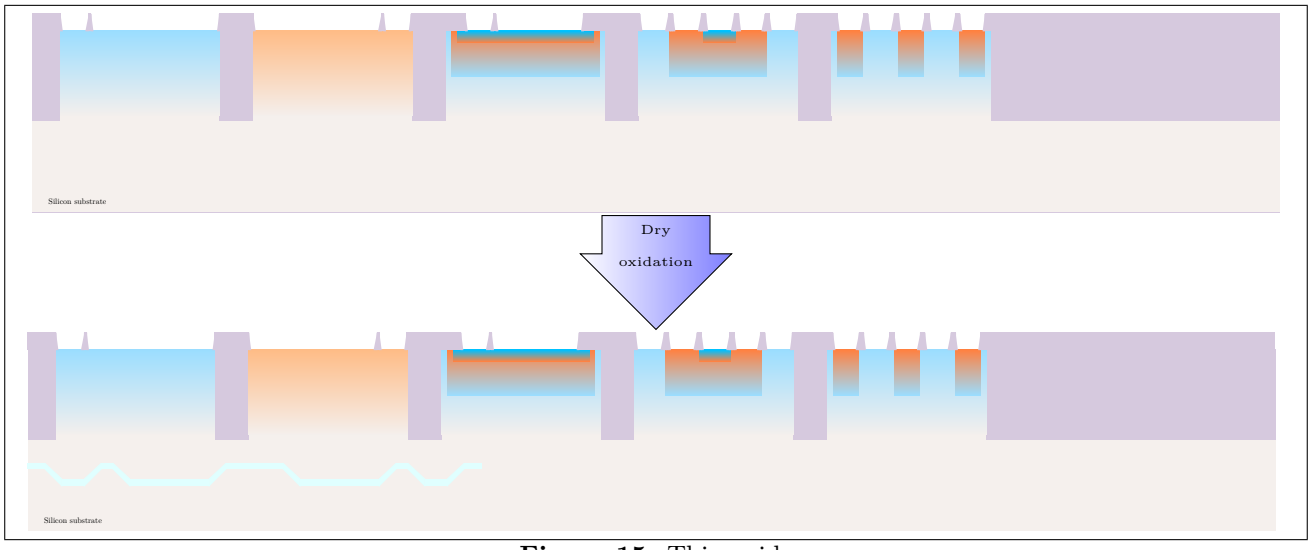

Figure 15: Thin oxide

This might be difficult depending on the CVD machine used. Typically a reduced pressure can reduce the deposition rate, do not reduce the temperature however, since this can cause the formation of grains.

4.2 Silicon nitride deposition

Now we need to add the nitride layer for forming the SONOS sandwich.

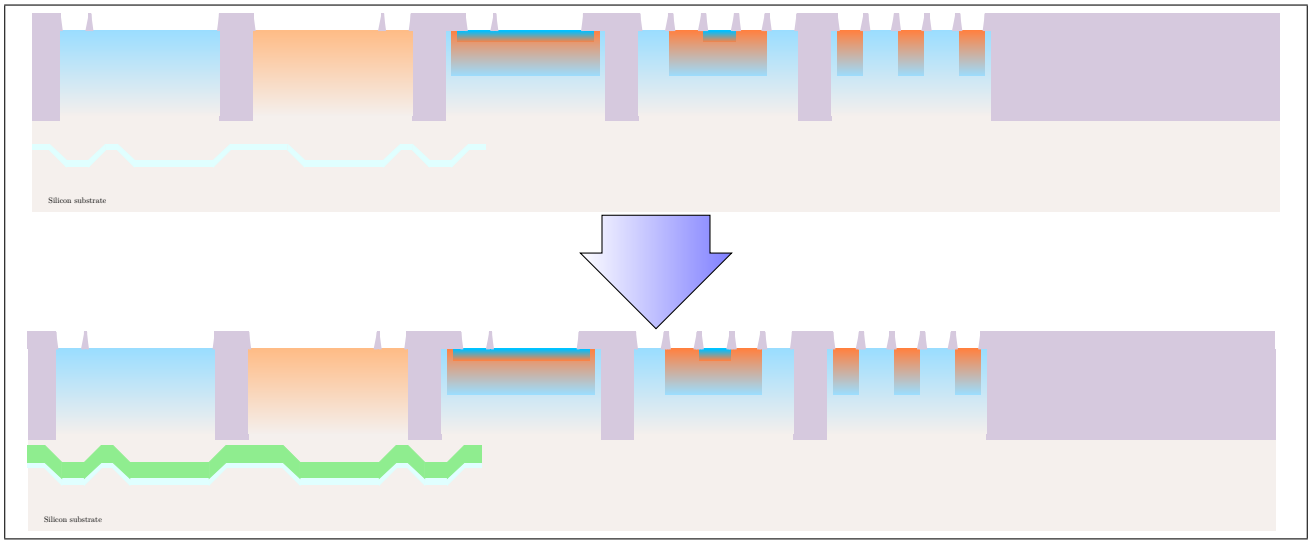

Figure 16: Polysilicon

We use the LPCVD machine and deposit a layer of around 7nm nitride.
Since the deposition rate of nitride in a CVD furnace is by nature quite slow (usually 2nm per minute) we have a much better control over this thickness.

4.3 Upper oxide deposition

Now we have to deposit the upper part of the SONOS sandwich by depositing LTO.
As designed in the process design document, the layer will be around 7nm thick.

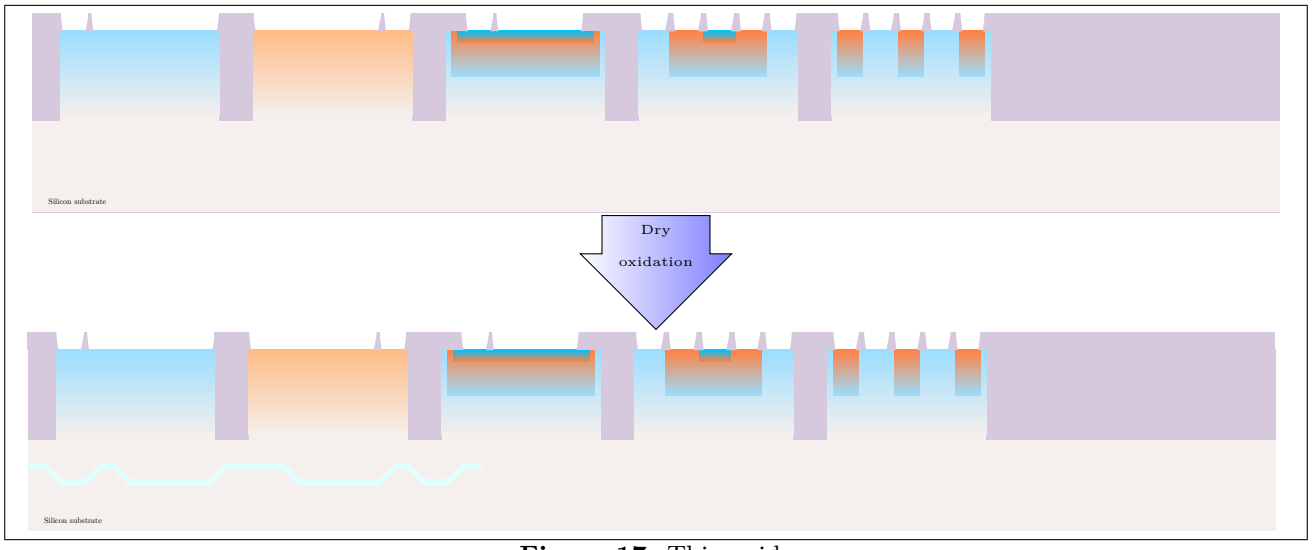

Figure 17: Thin oxide

It's exactly the same recipe as for the first oxide deposition step.

4.4 Etching

Now we've got to etch the SONOS structures.

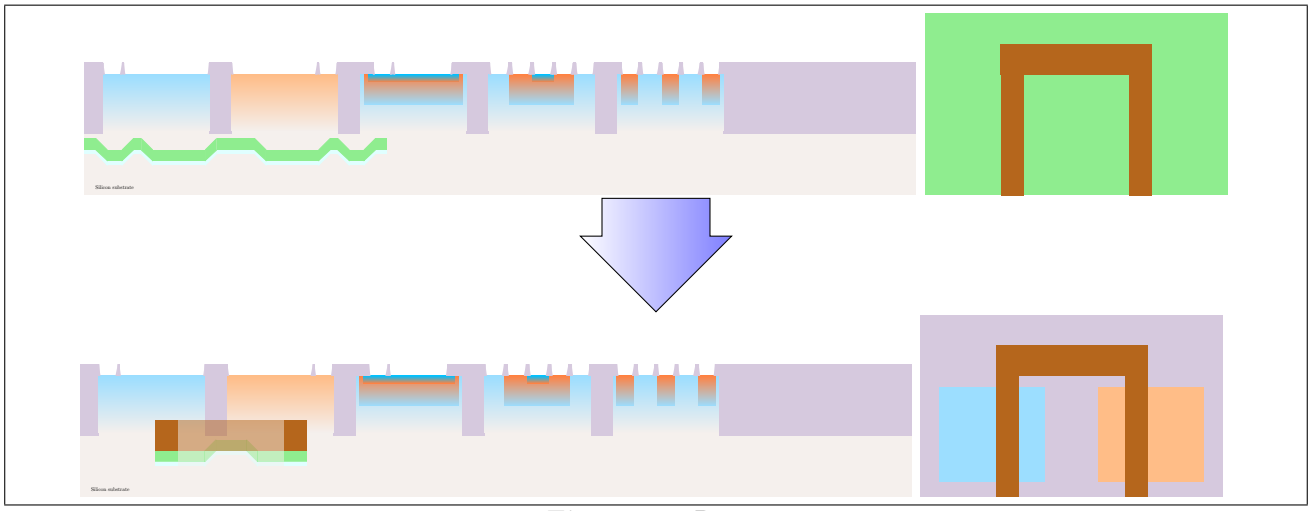

Figure 18: Resist

The etching time depends on the dry etcher and recipe used.

5 Gate

Now we have to build the initial gate structure which contains of the 40nm thick dielectric (in our case just silicon dioxide) and the polysilicon electrode.

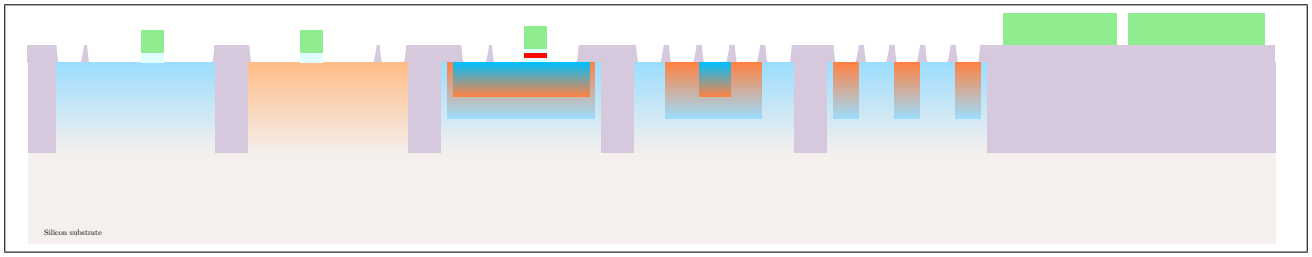

Figure 19: Poly silicon gate contacts with gate oxide

The line spacing of the polysilicon electrode shape has to be at least $0.5\mu m$ because of the resolution of the stepper and also because of the etching process which has $0.5\mu m$ as the minimum line spacing.

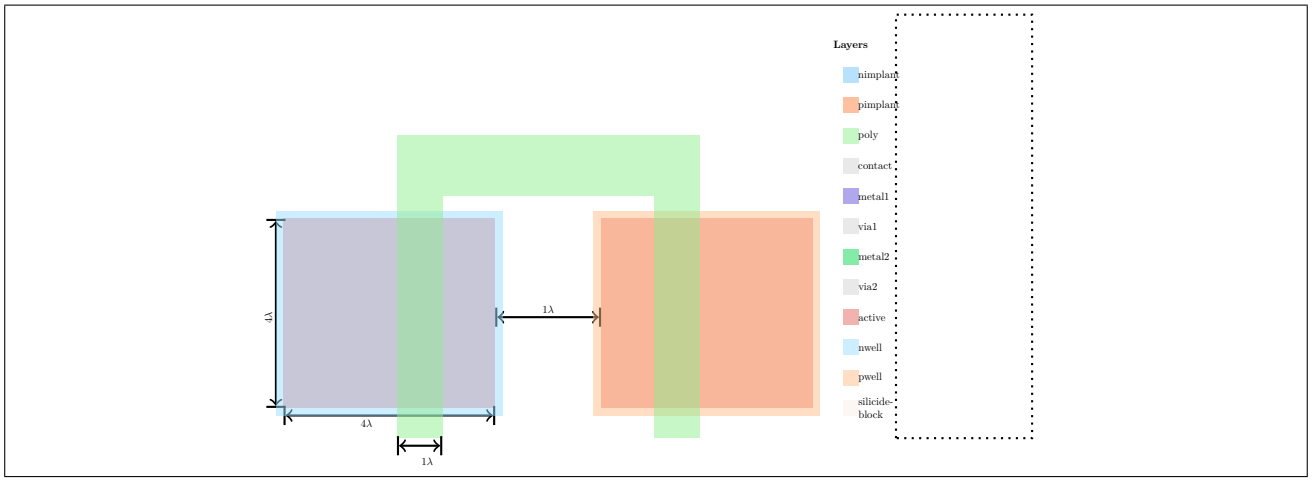

Figure 20: Gate layout

In Figure 20 we can see the layout honoring the $0.5\mu m$ spacing design rule for the gate structure shape and poly-layer interconnect between NMOS and PMOS.

5.1 Gate oxide deposition

Now we have to deposit the dielectric isolator between the gate electrode and the channel. As designed in the process design document, the layer will be 40nm thick.

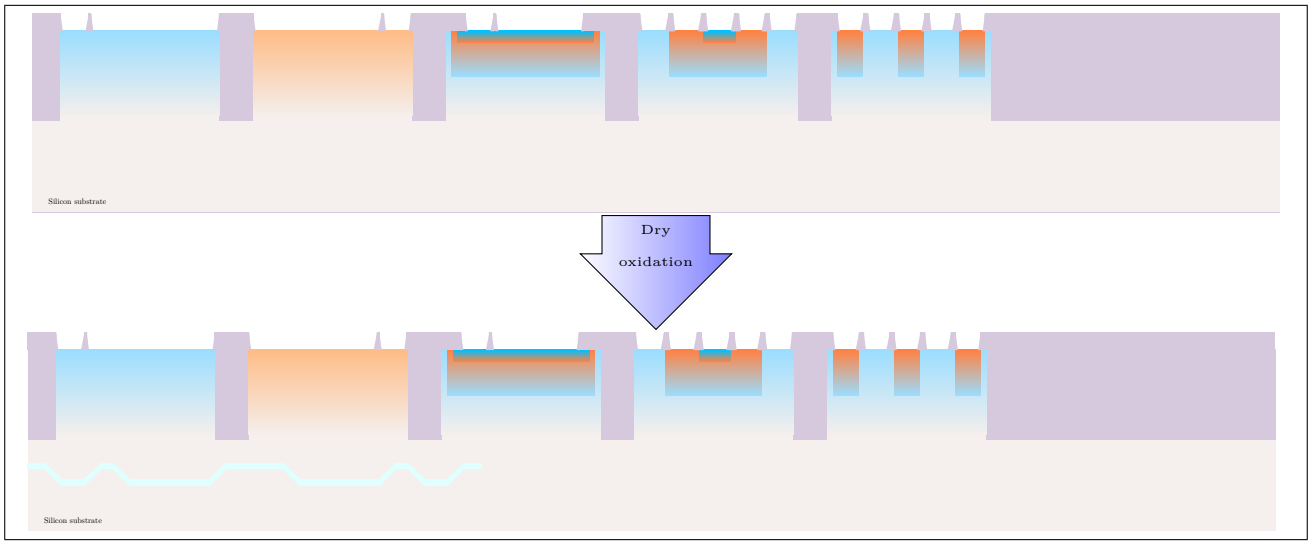

Figure 21: Thin oxide

The thickness of this layer decides over many critical key properties of the transistor, hence there should be little to no variation in the thickness of the gate oxide layer. For that reason we put the wafer into the diffusion furnace and perform dry oxidation at $1050°C$ for 33 minutes and 14 seconds.[2]

5.2 Polysilicon deposition

Now we need to add the polysilicon layer for forming the gate structure after etching.

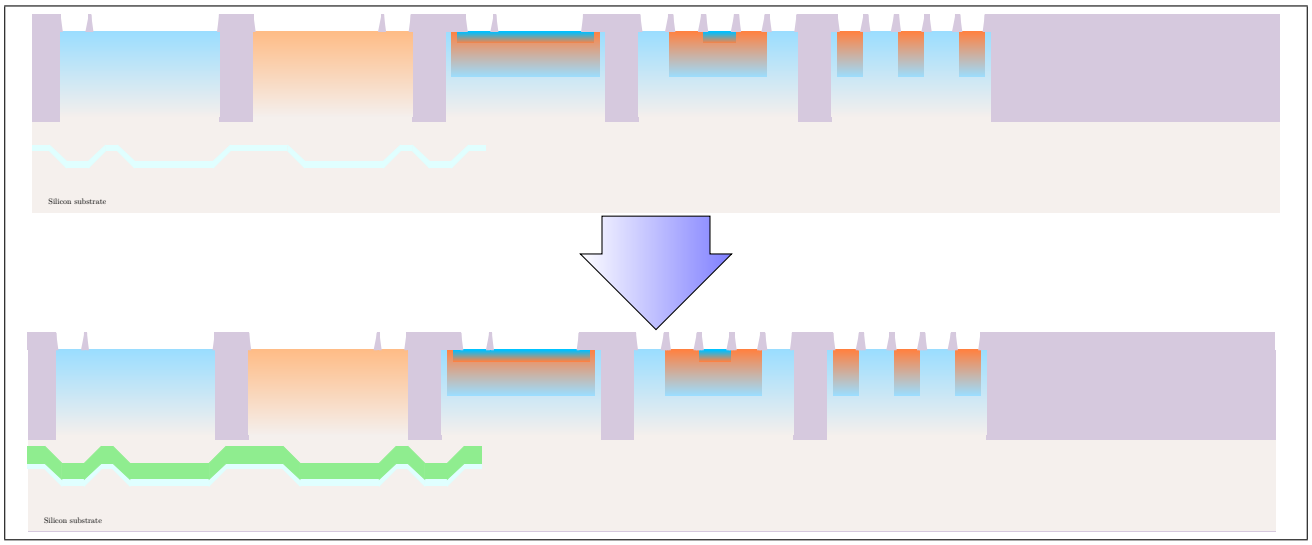

Figure 22: Polysilicon

We use the LPCVD machine and deposit a layer of around 600nm polysilicon[3].
We set the temperatue to $650°C$, the gas will be Silane (SiH_4 ($Si + 2H_2$)), the pressure will be set to 300 mTorr with a flow of 90sccm.
This will give us a growth rate of roughly 23.5 nm per minute, so for 600nm we let it grow half an hour.

[2] `http://cleanroom.byu.edu/OxideTimeCalc`
[3] `https://people.rit.edu/lffeee/LPCVD_Recipes.pdf`

5.3 Etching

Now we've got to etch the gate structures.

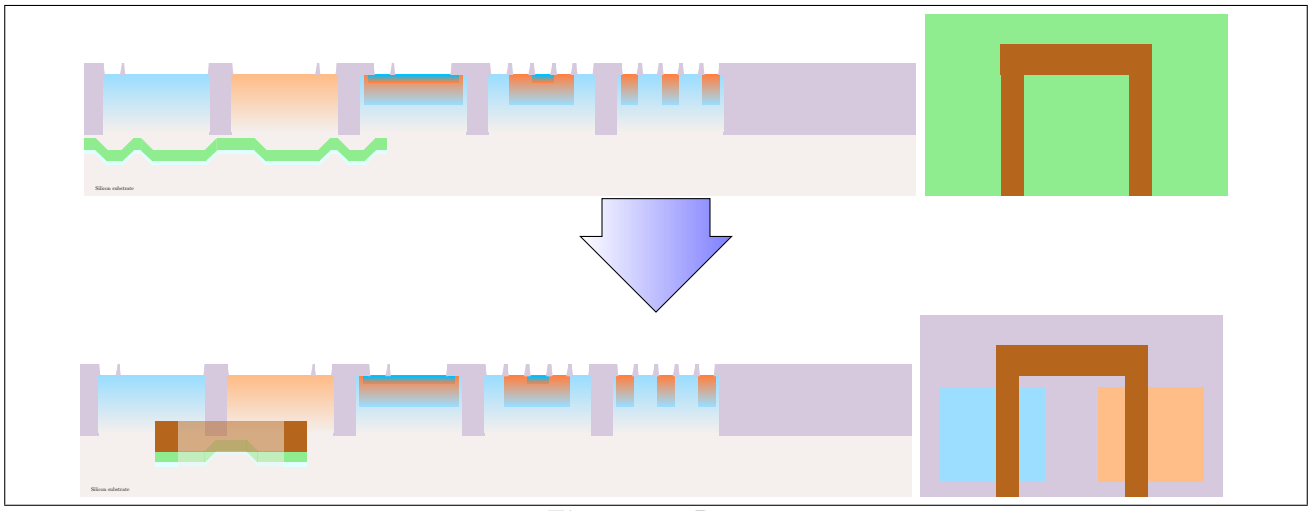

Figure 23: Resist

For now we only have the plasma etcher variant being verified because chemically etching polysilicon isn't allowed at the HKUST labs for contamination control reasons. In case you can verify this in your lab with a chemical etching method, please update this chapter and make a pull request!

Possible approaches:

- **"Poly Etcher (DRY-Poly)" from HKUST**
  An anisotropic plasma etcher, in order to etch the polysilicon and gate oxide layer. In subsection 5.2 we've grown 600nm of polysilicon which takes 200 seconds (= 3 minutes 20 seconds) (at 180nm/min) to etch. The selectivity to oxide is 13:1 which leads to an oxide etching speed of around 14nm/min, in subsection 5.1 we've grown a 40nm thick oxide layer which leads to the oxide adding another 2 minutes 51 seconds to the etching time. All together, we will have to etch for around **6 minutes and 10 seconds**.
- **Chemical method**
  Please add a verified method here!

6 Junction implants

After we've etches the gate structures and have implemented the implant stop structures we perform the junction implants in subsection 6.2 and subsection 6.1.
Thanks to the implant stop mask we have a nice control over channel lenghts because the implant stop structure compensates for alignment issues, which is crucial for Polysilicon diodes for instance.

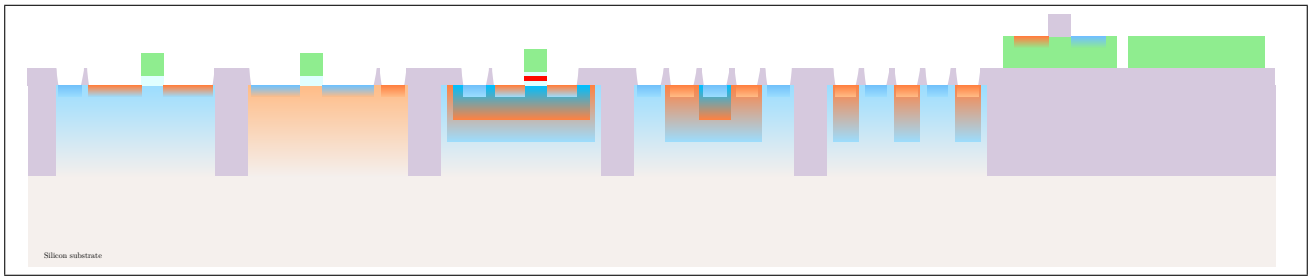

Figure 24: P+ and N+ junctions

After implantation we have to drive in the shallow junction implants in order to form the pn-junctions in the polysilicon gates and to increase the depth of the junctions to a degree so that it won't be fully consumed during the silicide formation(section 7) step later on.
After we've implanted the Boron and Phosphorus, we will drive the whole thing in for 30 minutes at $900°C$ and at the same time oxidize it with O_2 (dry oxidation) so that we can form the pad oxide needed to deposit the nitride for the side wall spacers later on in subsection 7.1.

6.1 n+ Implant

For the bulk of the PMOS transistors and for the source and drain of the NMOS transistors highly doped n+ areas are required.
In this step we're going to build these.

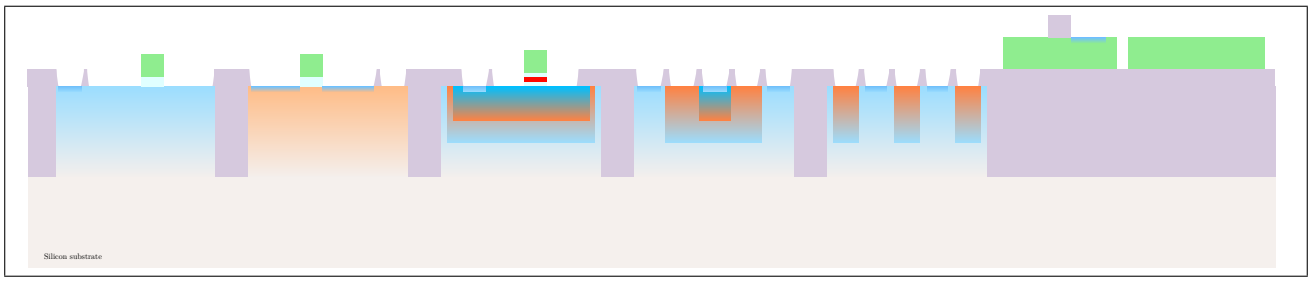

Figure 25: N+ implant geometry target

The tricky thing here is to have a reasonable implant depth but not too deep because the deeper the junction, the higher the junction capacity which in turn limits the switching performance of the CMOS circuitry.
Also important to notice is that the implantation energy must not be too high, otherwise the dopants may leak through the polysilicon gate.
The nselect is implanted with a Phosphorus (P^{31}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 30 keV (43nm±18nm deep)

6.2 p+ Implant

For the bulk of the NMOS transistors and for the source and drain of the PMOS transistors highly doped p+ areas are required.
In this step we're going to build these.

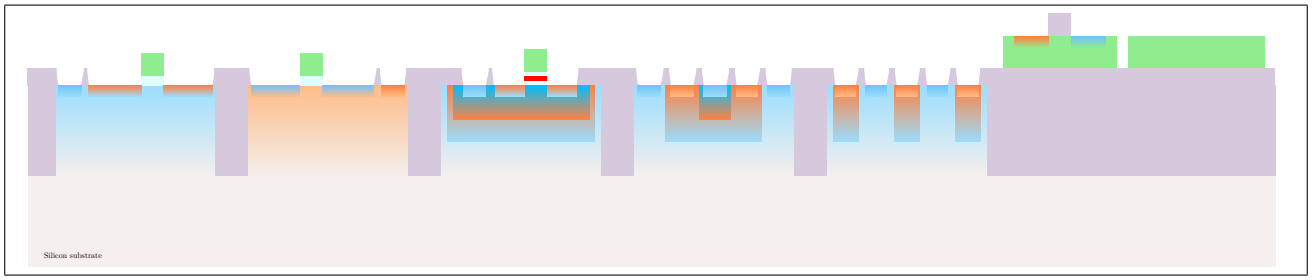

Figure 26: P+ implant geometry target

The tricky thing here is to have a reasonable implant depth but not too deep because the deeper the junction, the higher the junction capacity which in turn limits the switching performance of the CMOS circuitry.
Also important to notice is that the implantation energy must not be too high, otherwise the dopants may leak through the polysilicon gate.
The pselect is implanted with a Boron (B^{11}) dose of $2.5 \times 10^{12} cm^{-2}$ at an energy of 20 keV (43nm±18nm deep)

7 Silicification

Titanium silicide is one of the first SALICIDE material introduced in ULSI devices owing to its low resistivity, high thermal stability, ease in deposition and compatibility with silicon processes. Titanium has been one of the familiar materials in ULSI productions, which is also an important advantage in practical use of titanium SALICIDE.[4]

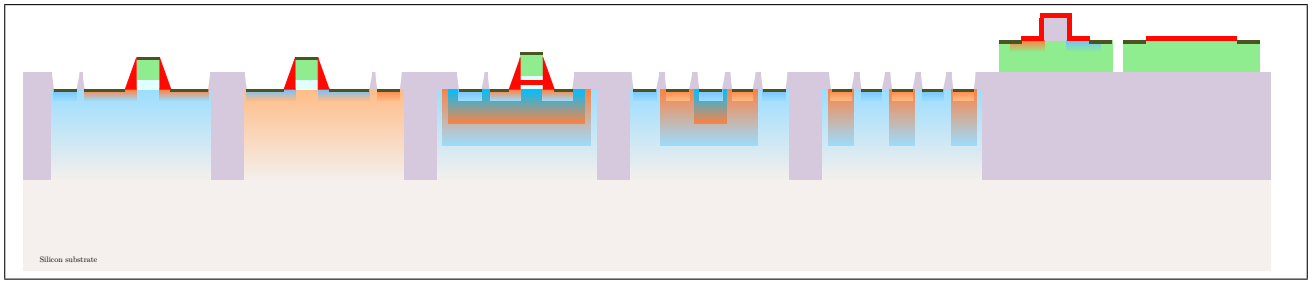

Figure 27: Silicide geometry target

In order to reduce the gate contact resistance as well as the source and drain resistance and in order to provide a more effective etch stop when plasma etching the contact windows to drain, source and gate, silicide/polycide is being added to the wafer as shown in Figure 27.
The side walls[5] are required in order avoid short circuits between the junction and the gate.
When titanium and silicon are brought into contact and heated at temperatures above 800 °C (in the presence of excess silicon) $TiSi_2$ forms.
The $TiSi_2$ has a resistivity of $12 - 20\mu\Omega - cm$.
The basic formation process of titanium SALICIDE is as follows:
A thin titanium film of roughly 30 nm thickness is deposited on an entire wafer with MOSFETs structure.
The deposited Ti film reacts with the exposed silicon areas such as the source/drain area and polysilicon gate electrodes during the annealing at 800°C in Argon atmosphere.
Then, the unreacted titanium film on the dielectric layer such as SiO_2 or SiN is selectively etched by APM (Ammonia and Hydrogen Peroxide Mixture) solution for around 2-3 minutes.

[4] A Study on Formation of High Resistivity Phases of Nickel Silicide at Small Area and its Solution for Scaled CMOS Devices, 07D53437, Ryuji Tomita
[5] `http://www.fujitsu.com/jp/group/mifs/en/resources/news/library/tech-intro/process/side-wall.html`

7.1 Nitride deposition

The thickness of this CVD deposited nitride layer will be the width of the spacer after having used highly anisotropic etching in the next few steps, for this reason the thickness of the nitride decides over the distance between the silicide and the gate oxide.
Considering, due to the edge effects during dry etching, the thickness of the nitride has to be less than 25% of the polysilicon thickness, we choose 50nm for the nitride thickness.

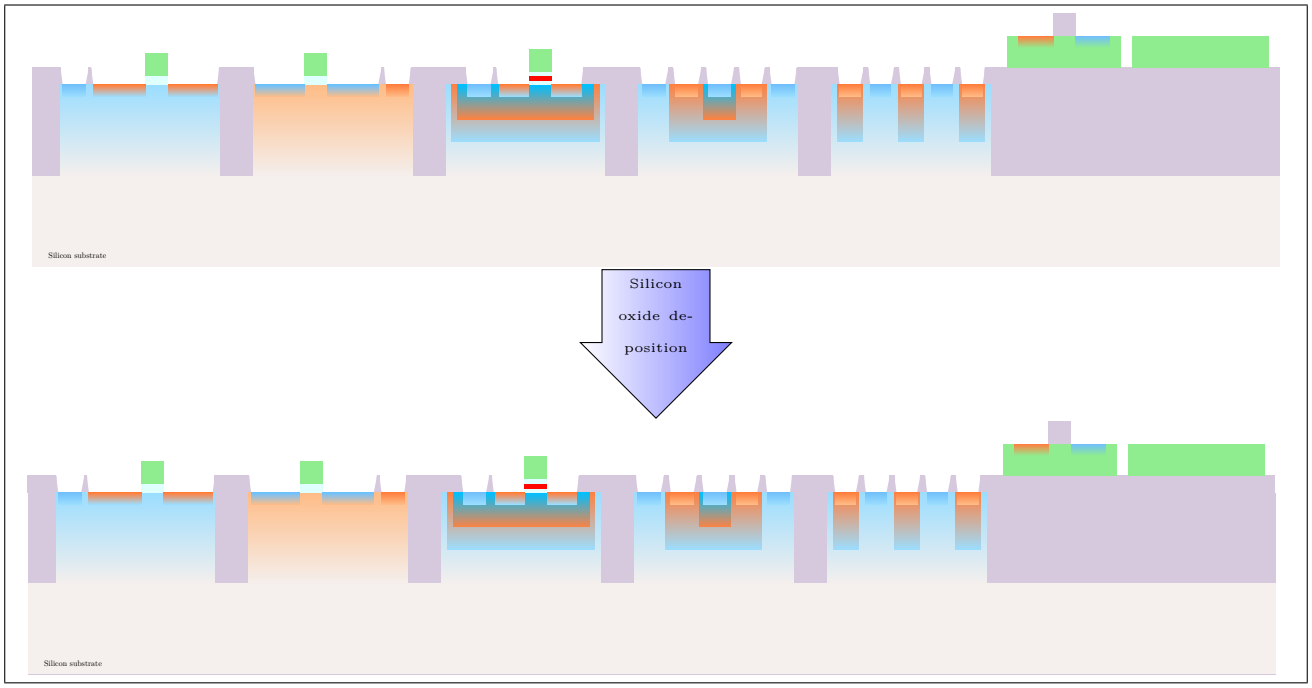

Figure 28: Oxide layer

The deposition rates might variate between LPCVDs and recipes. It's at the discretion of the operation engineer to achieve those 50nm.

7.2 Spacer etching

Now we have to etch our nitride as anisotropic as possible.
This means that the etching mostly only comes ”from above” with a few to nearly none horizontal etching.
Thit means the etching process only ”sees” the sidewall as a ”thicker layer” and starts etching downward.

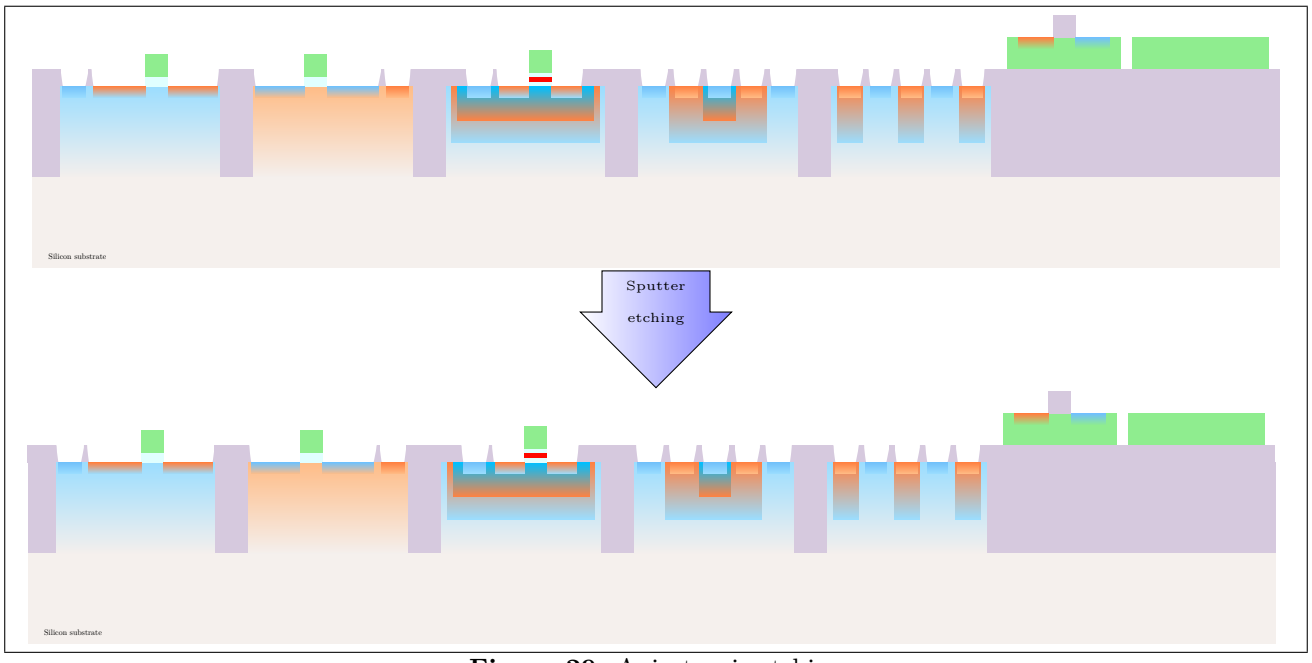

Figure 29: Anisotropic etching

After that we will have our desired spacer geometry forming as well as any potentially resist covered area (if silicide block is being used) with sharp etches.

7.3 Titanium deposition

We deposit a layer of titanium with a thickness of around 30nm which will then be reacted into titanium-silicide and titanium-polycide respectively in the further steps.

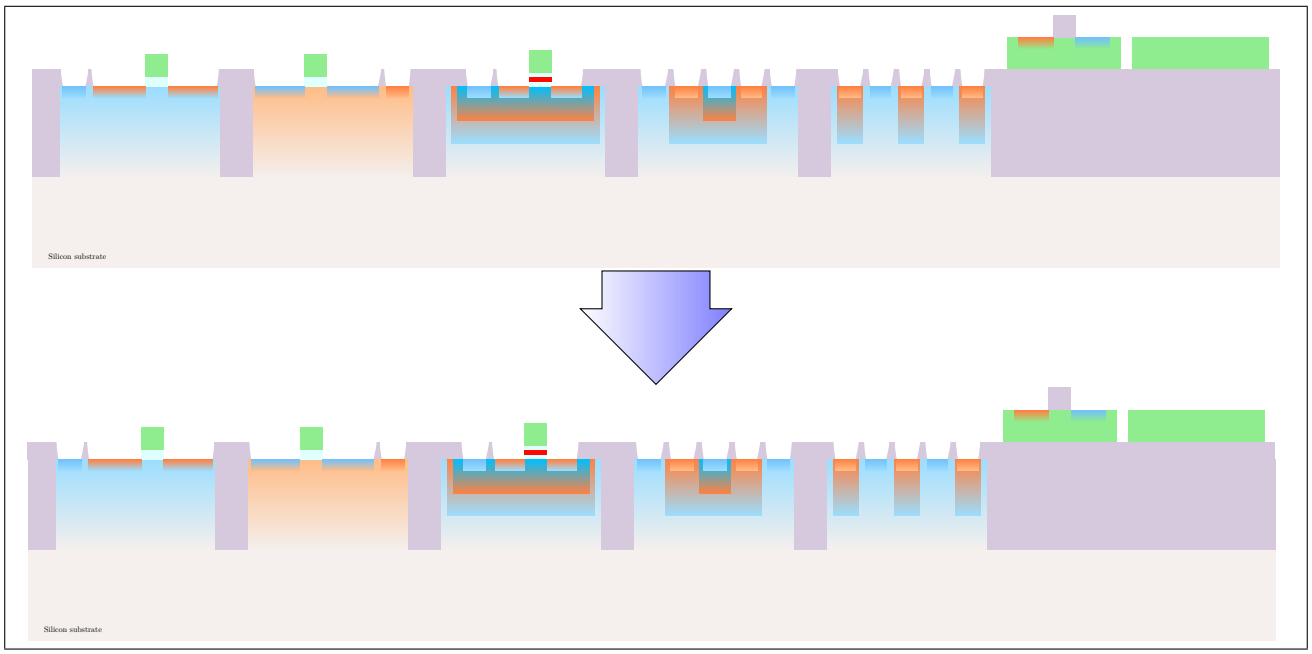

Figure 30: Titanium deposition

The titanium can either be applied by sputtering or by chemical deposition.

7.4 Silicide formation

The deposited Ti film reacts with the exposed silicon areas such as the source/drain area and polysilicon gate electrodes during RTP (Rapid Thermal Processing) at $800°C$ in Argon ambient for 30 seconds.
In this annealing step the $TiSi_2$ is formed.

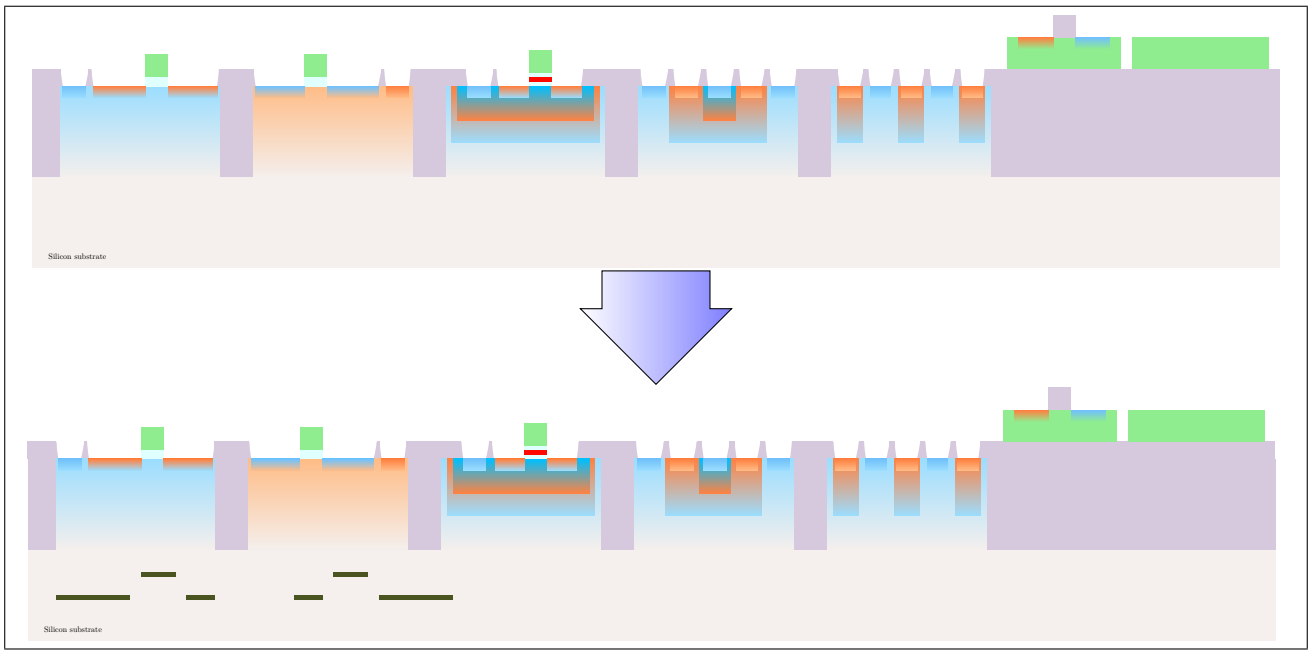

Figure 31: Reaction 1

The resulting $TiSi_2$ film will be around 77nm in tickness with around 20nm unreacted titanium left on top. A color change can be observed of the titanium on top of the oxide.

7.5 Metal removal

The unreacted titanium film on the dielectric layer such as SiO_2 or SiN is selectively etched by APM (Ammonia and Hydrogen Peroxide Mixture) solution.

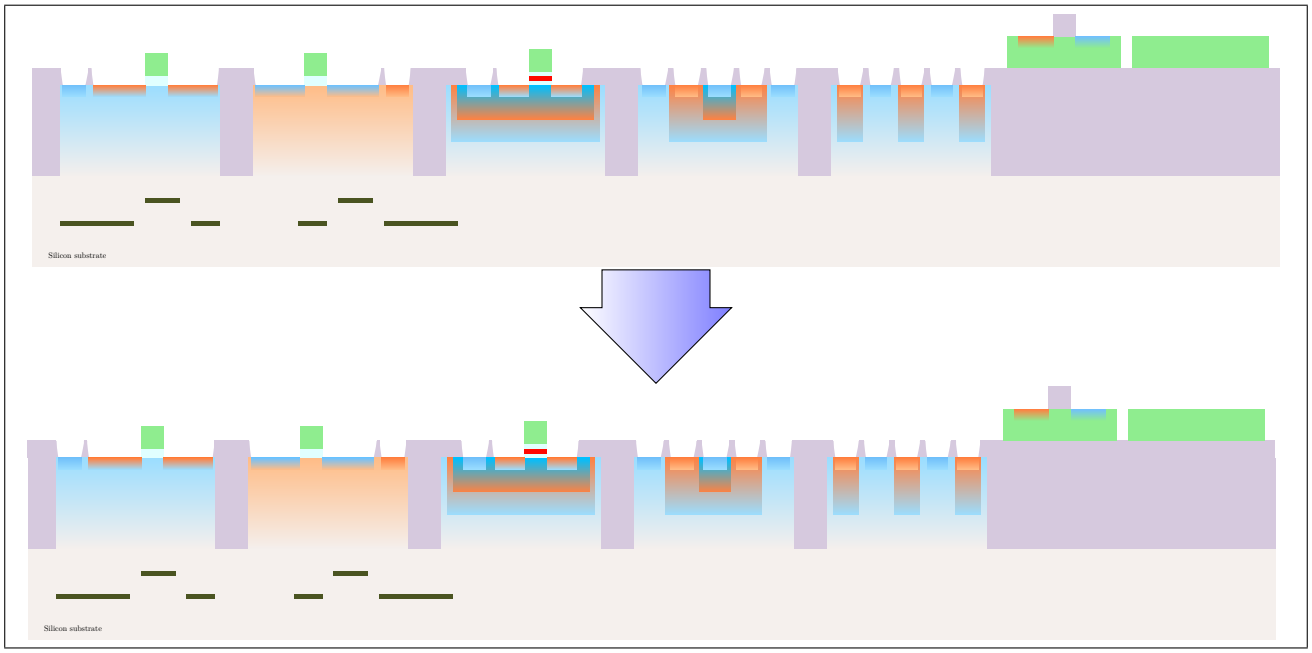

Figure 32: Titanium etch

After 2-3 minutes in APM, with a bit mechanical help, all the unreacted Titanium should be gone and the oxide should become visible again.

8 Interconnect

Now that we've built all the devices, we've got to put wires on them in order to make them do something useful.

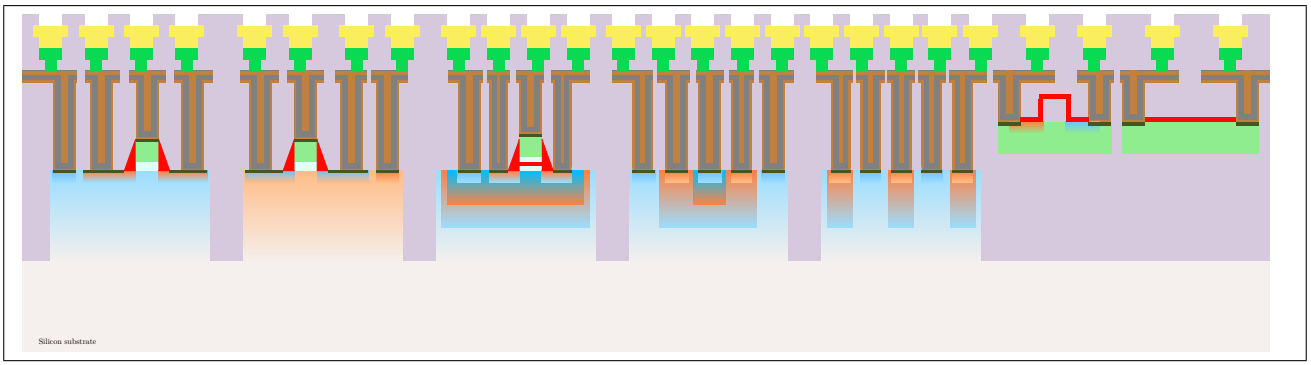

Figure 33: Interconnect geometry target

From here on it's basically just always the same game:

1. Deposit roughly 150nm LTO/PSG
2. Etch vias
3. Sputter metal
4. Etch wires
5. Go to 1

As can be seen in Figure 33
We have the holes where we sputter the metal into. All the oxide holes which are subsection 8.1, subsection 8.3, subsection 8.5 and subsection 8.7, are basically the same. We deposit 150nm LTO/PSG and etch holes into it, in order to contact through to the lower layer. For the first layer, the etch stop is silicide, for the other layers it's the Nickel passivation.

8.1 Contacts

Now we have to build the first set of vias connecting the first metal layer to the active area. These vias are in the fringe between front-end and back-end process.

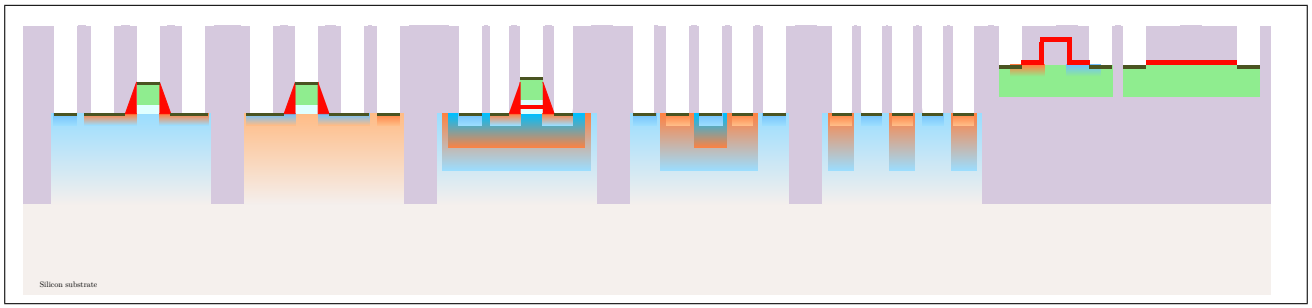

Figure 34: Contact geometry target

As can be seen in Figure 34, the goal of this step is purely to deposit a layer of isolation oxide, get the holes into it, down to the silicide and polyside in order to form wires later on. We do not wanna etch down anywhere else than the silicide/polycide areas because these function as etch stoppers, while everywhere else we might etch further than desired with small variations in etching time which might result in a drastic variation in sheet resistance of the junctions and gate. In later iterations of this process we might be switching to Tungsten as the metal material for this step.

8.2 Metal 1

Now we've got to build the first interconnect wires, connecting the contact vias to the "metal1" wires, which will provide a way to contact to them with the via1 contact layout.

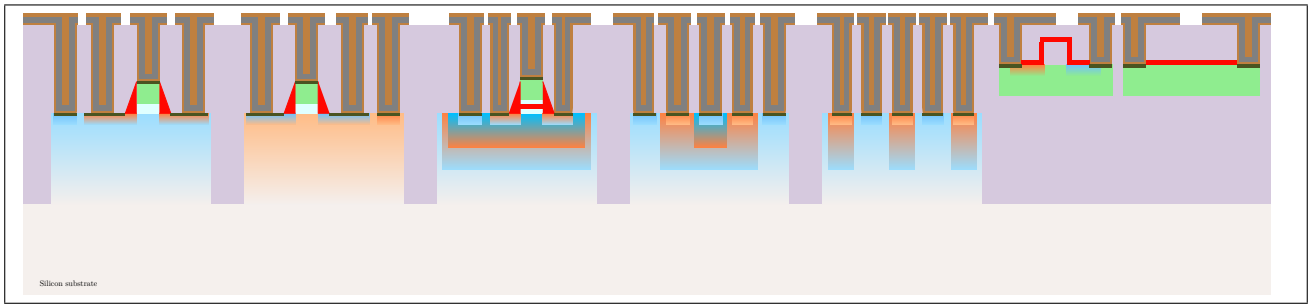

Figure 35: Metal geometry target

In later iterations of this process we might be switching to Tungsten as the metal material for this step so the etching method might change in further releases.

8.3 Via 1

Now we have to build an additional set of via1. connecting the first metal layer to the next metal layer. These via1. are already part of the front-end process.

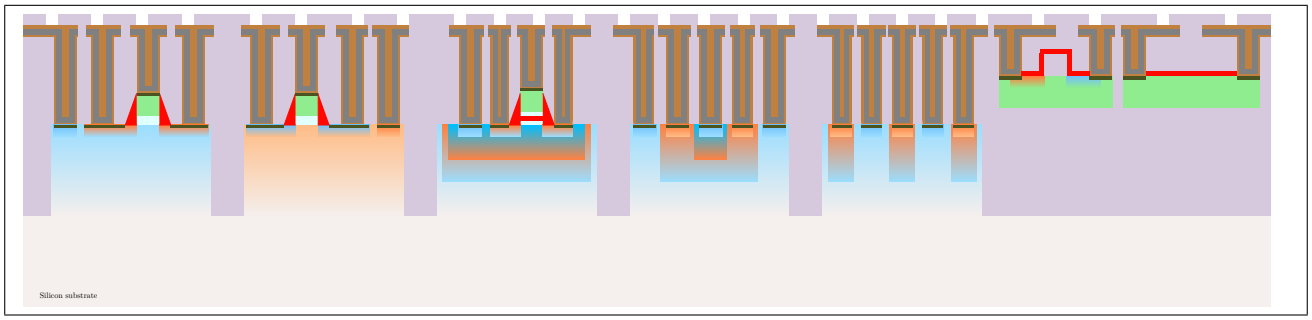

Figure 36: Contact geometry target

As can be seen in Figure 36, the goal of this step is purely to deposit a layer of isolation oxide, get the holes into it, down to the metal layer below in order to form wires later on.
In a later iterations of this process we might be switching to Copper as the metal material for this step which will result in a variation of this step because the usage of damascene method.

8.4 Metal 2

Now we've got to build the more interconnect wires, connecting the contact vias to the "metal2" wires, which will provide a way to contact to them with the via2 contact layout.

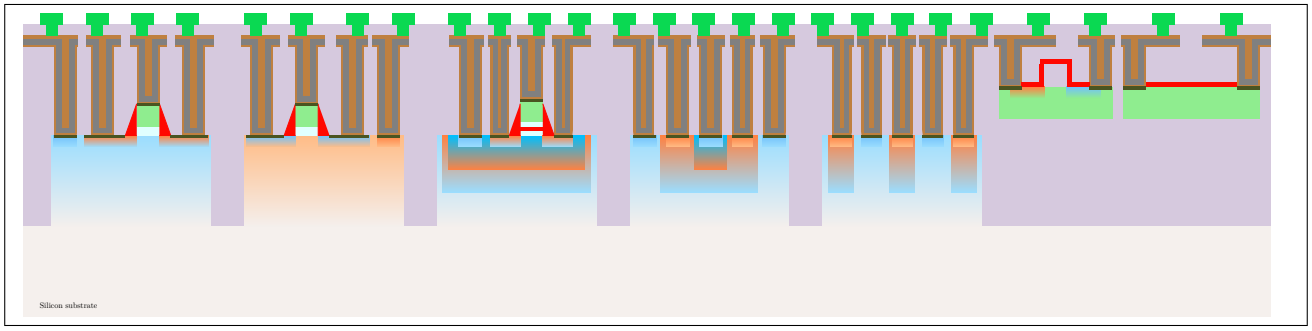

Figure 37: Metal geometry target

As can be seen in Figure 37, the goal of this step is purely to etch the wire structure for the additional metal layer into the in **??** deposited metal layer, and form wires by doing so.
In later iterations of this process we might be switching to Tungsten as the metal material for this step so the etching method might change in further releases.

8.5 Via 2

Now we have to build an additional set of via1. connecting the first metal layer to the next metal layer. These via1. are already part of the front-end process.

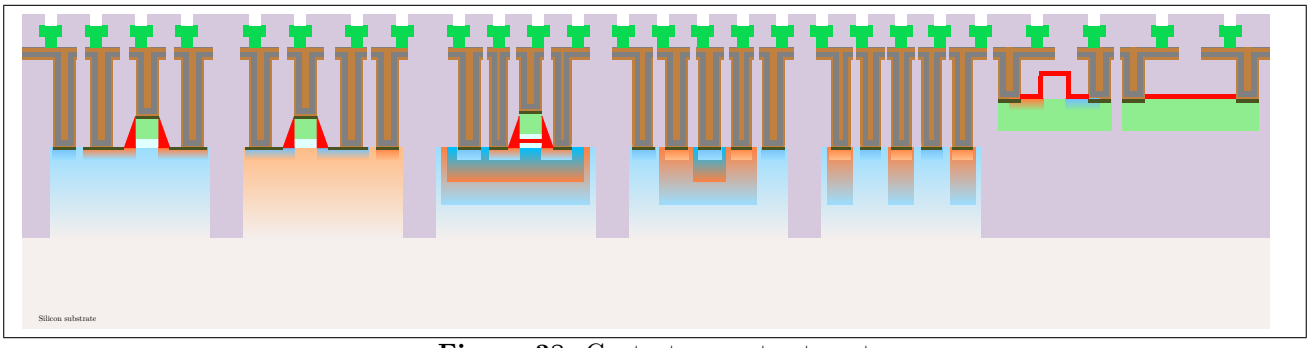

Figure 38: Contact geometry target

As can be seen in Figure 38, the goal of this step is purely to deposit a layer of isolation oxide, get the holes into it, down to the metal layer below in order to form wires later on.
In a later iterations of this process we might be switching to Copper as the metal material for this step which will result in a variation of this step because the usage of damascene method.

8.6 Metal 3

Now we've got to build the more interconnect wires, connecting the contact vias to the "metal2" wires, which will provide a way to contact to them with the via2 contact layout.

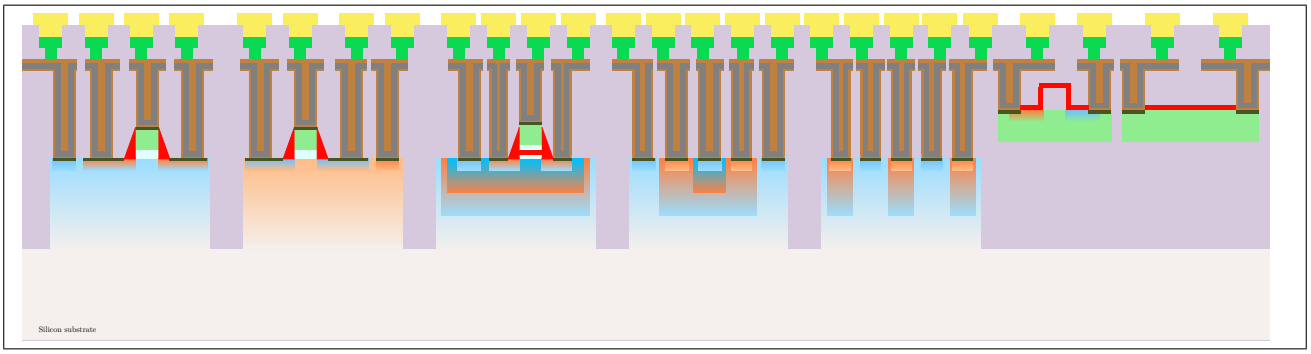

Figure 39: Metal geometry target

As can be seen in Figure 39, the goal of this step is purely to etch the wire structure for the additional metal layer into the in **??** deposited metal layer, and form wires by doing so.
In later iterations of this process we might be switching to Tungsten as the metal material for this step so the etching method might change in further releases.

8.7 Glass

Now we have to build an additional set of via1. connecting the first metal layer to the next metal layer. These via1. are already part of the front-end process.

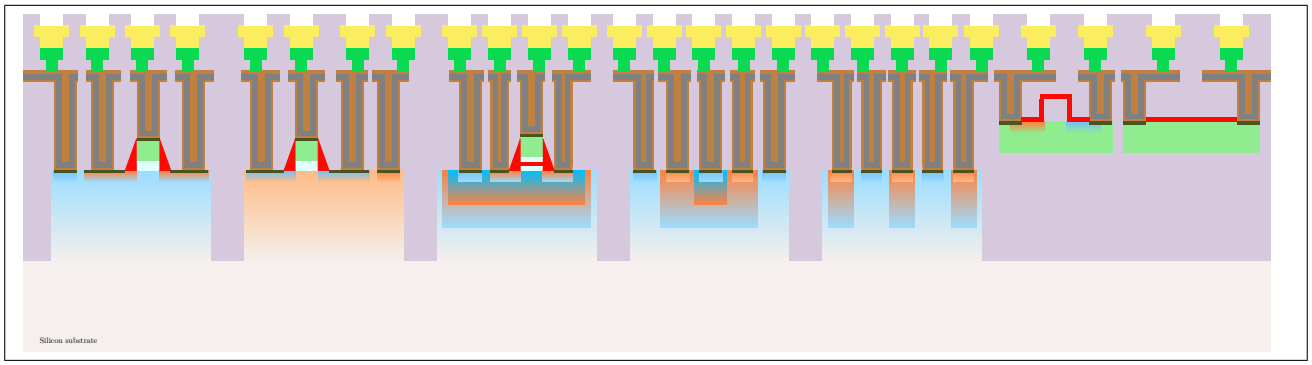

Figure 40: Glass geometry target

As can be seen in Figure 36, the goal of this step is purely to deposit a layer of isolation oxide, get the holes into it, down to the metal layer below in order to form wires later on.
In a later iterations of this process we might be switching to Copper as the metal material for this step which will result in a variation of this step because the usage of damascene method.