## LibreSilicon process HKUST (NFF)

David Lanzendörfer July 10, 2019

#### Abstract

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This document is part of the specification of the free silicon manufacturing standard for manufacturing the LibreSilicon standard logic cells<sup>1</sup> and related free technology nodes from the LibreSilicon project.

For this initial revision 0.1 a gate-first approach has been chosen which led to the choice of polysilicon as the gate electrode material because of the simplicity of the gate alignment. For better isolation properties of the transistors and gates in overall a box-isolation approach has been chosen. All of these choices have been made with the future scale down from the recent  $1\mu m$  to smaller structure sizes. This process is for manufacturing  $1\mu m$  only! But further releases which will have been tested with smaller structure sizes can be expected.

Please see the document with the generic steps<sup>2</sup> in order to get a detailed description of the different steps.

<sup>1</sup>https://github.com/chipforge/StdCellLib

<sup>&</sup>lt;sup>2</sup>https://github.com/libresilicon/process/raw/master/process\_steps/process\_hightech/process\_hightech\_steps.pdf

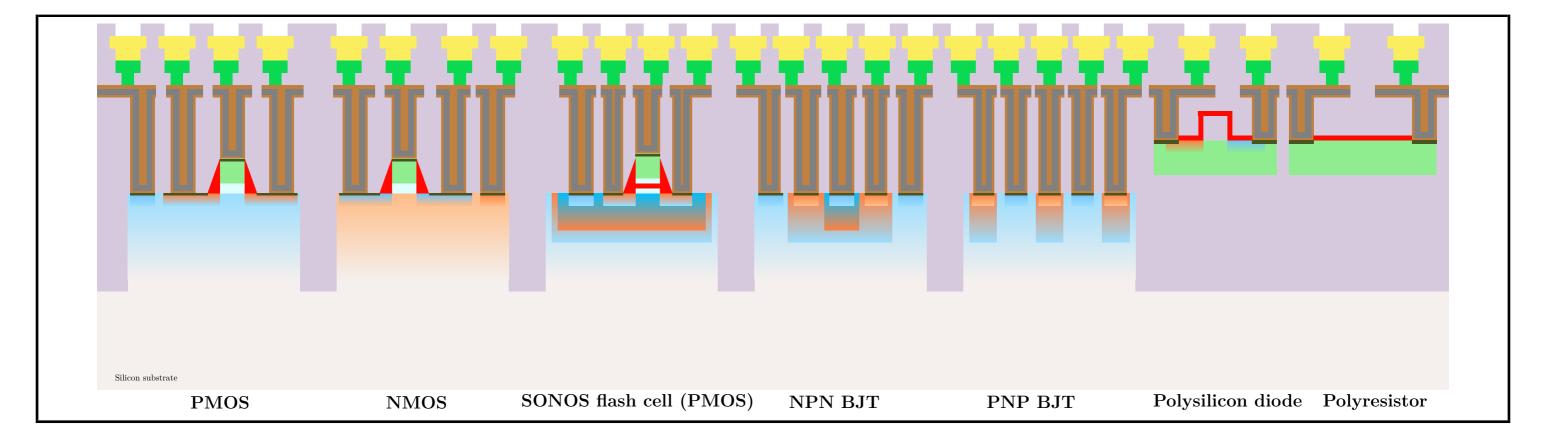
Process Flow of Lanceville Technologies Libre Silicon<br/>  $1\mu m$ 

• Project: LibreSilicon  $1\mu m$ 

• Name: Lanceville Technologies Group

- Substrate: P-Substrate silicon wafer  $<\!100\!>$ 

• Date: July 10, 2019



# 1 Initial alignment mask

Silicon substrate

Mask:	hasic

Wafer Cleanliness	Step Number	Equipment	Location	Location Cleanliness Process		Requirements
Clean	1.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	1.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	1.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min
Clean	1.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Clean	1.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	1.6	NFF RIE Etcher (DRY-RIE-2)	P2-01000	Clean Semi clean	CF4 Etch	140 seconds
Clean	1.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	1.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	1.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

## 2 Shallow trench isolation

Silicon substrate

Mask: sti

Wafer Cleanliness	Step Number	Equipment	Equipment Location Cleanliness Process		Requirements	
Clean	2.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	2.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	2.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5\mu m$ ), soft bake: 110°C 1min
Clean	2.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Clean	2.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	2.6	DRIE Etcher #1 (DRY-Si-1)	P2-01000	Clean	Etching the trenches	Thin line recipe, $1\mu m$ : 7 cycles -> 35 cycles
Clean	2.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	2.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	2.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Clean	2.10	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	

Silicon substrate

Mask: sti

Wafer Cleanliness	Step Number	Equipment	Location Cleanliness Process		Process	Requirements
Clean	2.11	Spin Dryer-A (SRD-A)	P2-01000 Clean I		Dry the wafer automatically	
Clean	2.12	LPCVD-B3 LTO (CVD-B3)	P2-01000	P2-01000 Clean Oxide deposition		$4\mu m~{ m LTO}$
Clean	2.13	Strasbaugh CMP (CMP-1)	P2-10000	P2-10000 Clean Planarize oxide down to sil		Use oxide planarization slurry, 15 minutes
Clean	2.14	G1:TMAH (WET-G1)	P2-01000	Clean	Ammonium cleaning	$70^{\circ}\mathrm{C}$ , $10\mathrm{mins}$
Clean	2.15	C3:BOE (WET-C3)	P2-01000	.01000 Clean HF dip		1 minute
Clean	2.16	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	2.17	Spin Dryer-A (SRD-A)	P2-01000	2-01000 Clean Dry the wafer autom		
Clean	2.18	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Oxide deposition	$2\mu m$ LTO
Clean	2.19	Strasbaugh CMP (CMP-1)	P2-10000	Clean	Planarize oxide down to silicon	Use oxide planarization slurry, 10 minutes
Clean	2.20	G1:TMAH (WET-G1)	P2-01000	Clean	Ammonium cleaning	70°C , 10mins

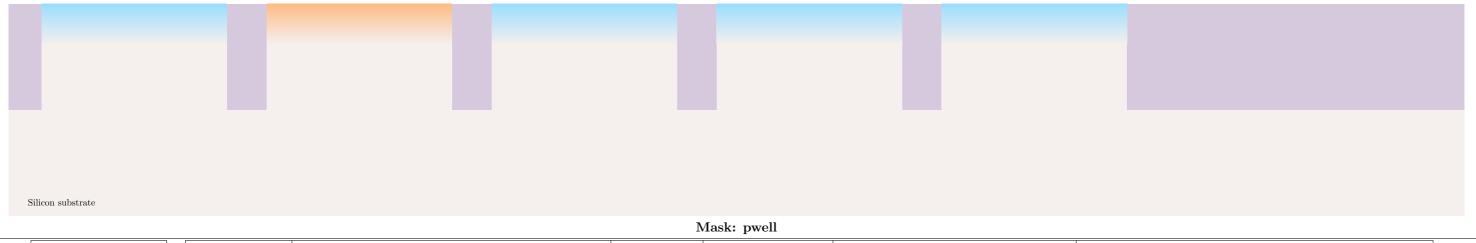
## 3 N-well

Silicon substrate

Mask:	nwell
wask.	nwen

Wafer Cleanliness	Step Number	Equipment	Location Cleanliness Process		Requirements		
Clean	3.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	01000 Clean Default cleaning			
Clean	3.2	Spin Dryer-B (SRD-B)	P2-01000	P2-01000 Clean Dry the wafer automatically			
Clean	3.3	SVG Coater Track (PHT-T1)	P2-00100	2-00100 Clean Semi clean HMDS, PR coating, soft bake		FH 6400L: 3krpm ( ${\approx}1.5\mu m$ ), soft bake: 110°C 1min	
Clean	3.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean Exposure of the layer		$340mJcm^2$	
Clean	3.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean  Develop, Hard bake		FHD-5, 1min; hard bake: $120^{\circ}\mathrm{C}$ , $30\mathrm{min}$	
Clean	3.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.33 \times 10^{12} cm^{-2}$ @70keV	
Clean	3.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip		
Clean	3.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip		
Clean	3.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically		

## 4 P-well

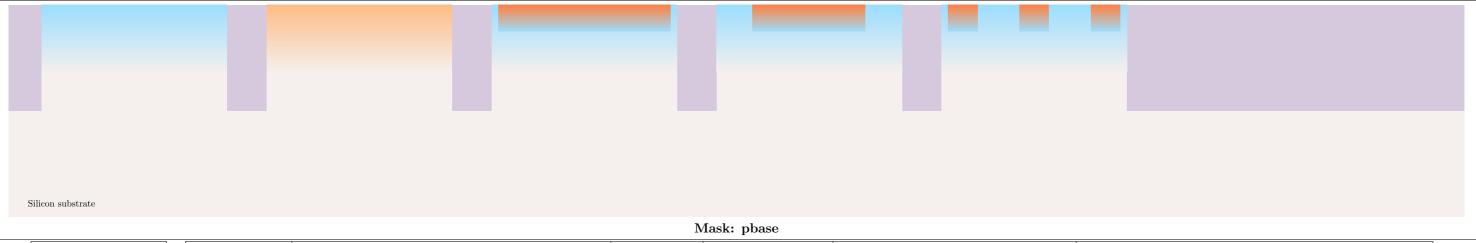


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	4.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	4.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	4.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean  HMDS, PR coating, soft bake		FH 6400L: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min
Clean	4.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340mJcm^2$
Clean	4.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 30min
Clean	4.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$1.93 \times 10^{12} cm^{-2} @40 \text{keV}$
Clean	4.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	4.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	4.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Clean	4.10	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	

Silicon substrate						
Sincon Substitute			7	Mask: pwell		
			N	viask; pwell		
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements

Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	4.11	Spin Dryer-A (SRD-A)	P2-01000 Clean		Dry the wafer automatically	
Clean	4.12	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Drive in	2 hours @ 1050°C in inert $(N_2)$ environment

## 5 P-Base

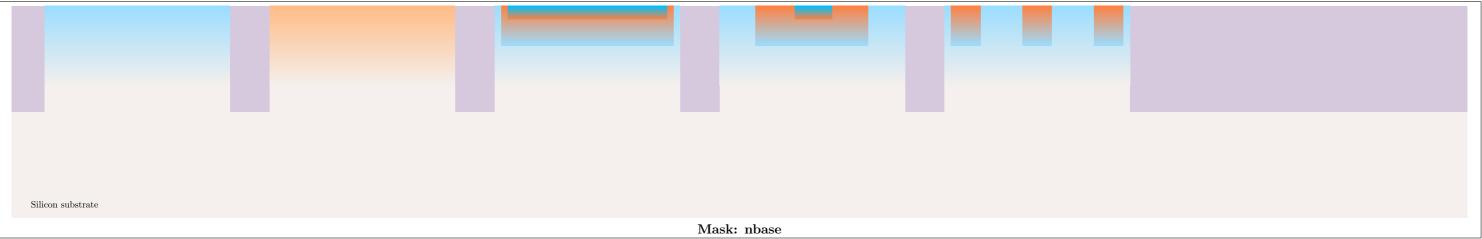


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	5.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	5.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	5.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ( $\approx\!1.5\mu m$ ), soft bake: 110°C 1min
Clean	5.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340mJcm^2$
Clean	5.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 30min
Clean	5.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$1.93 \times 10^{12} cm^{-2}$ @40keV
Clean	5.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	5.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	5.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Clean	5.10	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	

Silicon substrate						
		Mas	k: pbase			

Wafer Cleanliness	Cleanliness         Step Number         Equipment         Location         Cleanliness           Clean         5.11         Spin Dryer-A (SRD-A)         P2-01000         Clean		Cleanliness	Process	Requirements	
Clean			P2-01000 Clean		Dry the wafer automatically	
Clean	5.12	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Drive in	1 hour @ 1050°C in inert $(N_2)$ environment

## 6 N-Base

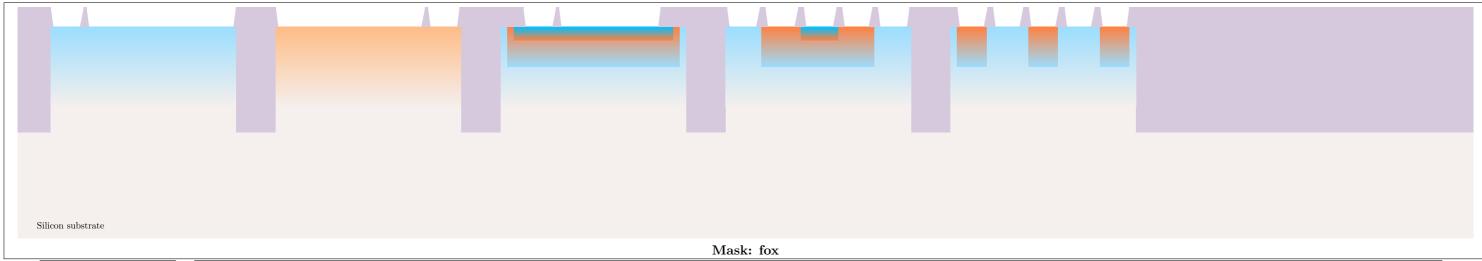


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	6.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	6.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	6.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min
Clean	6.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340mJcm^2$
Clean	6.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 30min
Clean	6.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.33 \times 10^{12} cm^{-2}$ @70keV
Clean	6.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	6.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	6.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Clean	6.10	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	

Silicon substrate				
		Mask: nbase		

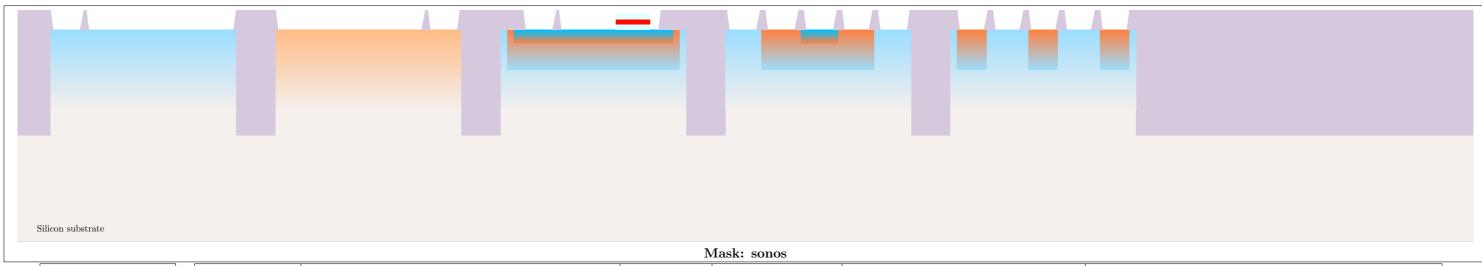
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	6.11	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	6.12	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Drive in	30 minutes @ 1050°C in inert $(N_2)$ environment

## 7 Field oxide

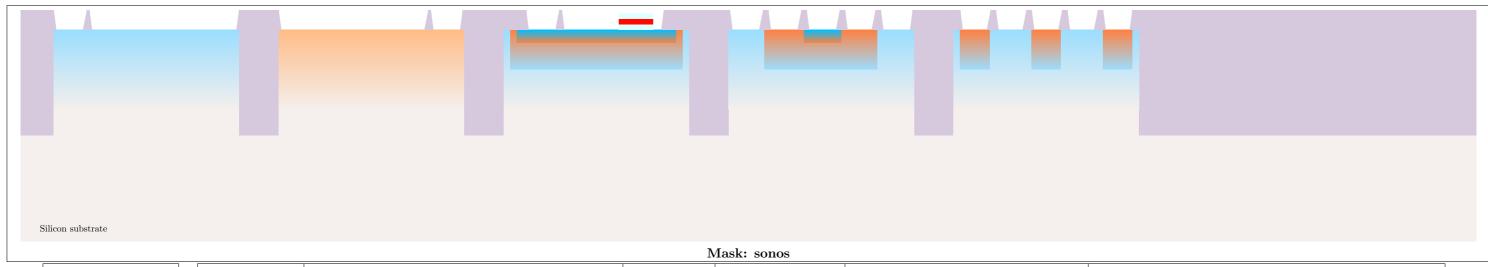


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	7.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	7.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	7.3	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Oxide deposition	200nm LTO
Clean	7.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5\mu m$ ), soft bake: 110°C 1min
Clean	7.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Clean	7.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	7.7	AOE Etcher (DRY-AOE)	P2-01000	Clean	Etch oxide FOX openings	Etch through 200nm
Clean	7.8	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	7.9	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	7.10	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

## 8 SONOS

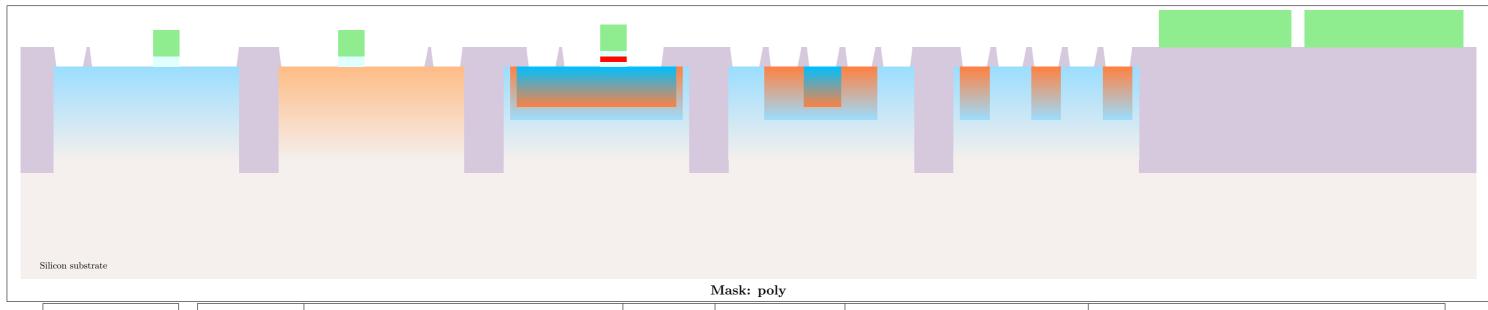


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	8.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	8.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	8.3	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Lower gate oxide growth	5nm
Clean	8.4	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	8.5	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	8.6	LPCVD-B2 Nitride/Low-Stress Nitride (CVD-B2)	P2-01000	Clean	Charge carrying nitride growth	10nm
Clean	8.7	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	8.8	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	8.9	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Lower gate oxide growth	5nm
Clean	8.10	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min

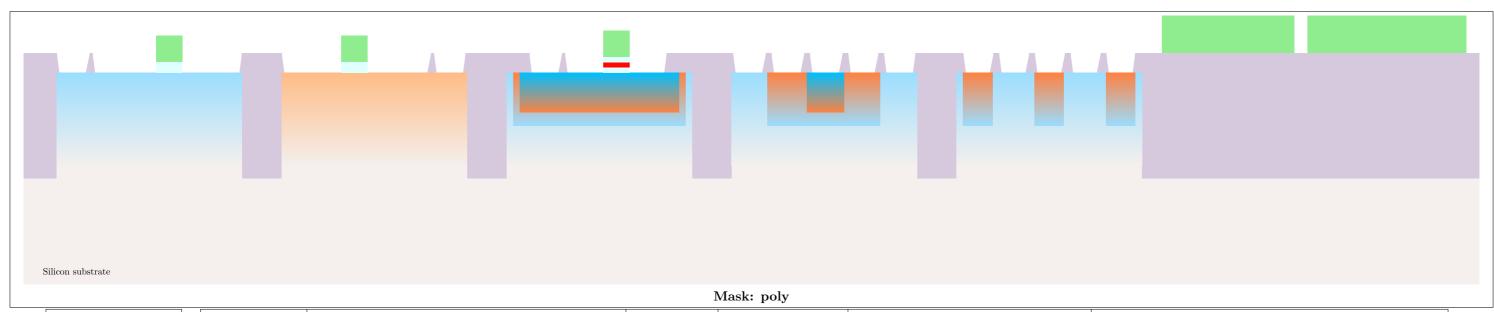


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	8.11	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Clean	8.12	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	8.13	NFF RIE Etcher (DRY-RIE-2)	P2-01000	Clean Semi clean	Nitride etch	6 seconds (10nm, 100nm/min)
Clean	8.14	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	8.15	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	8.16	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

## 9 Gate

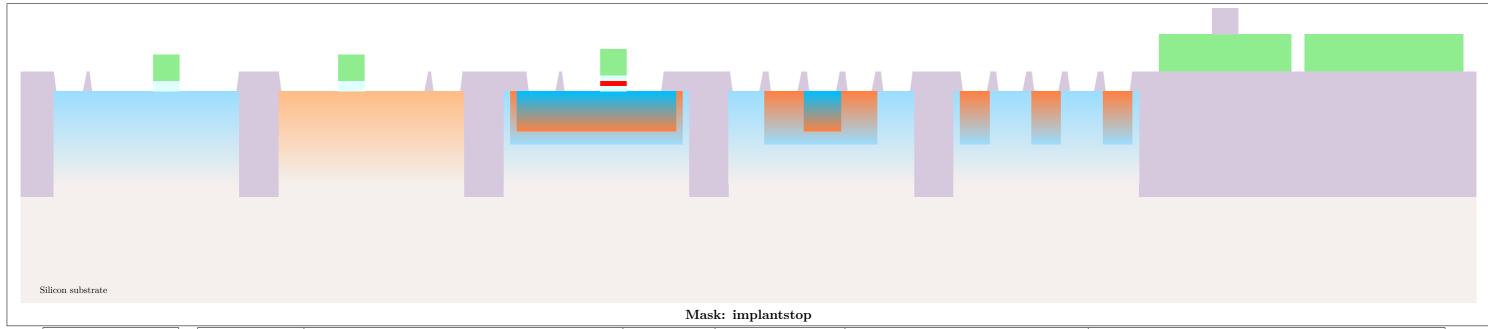


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	9.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	9.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	9.3	Diff. Furnace-D1 Dry Oxidation (Only for gate oxide) (DIF-D1)	P2-01000	Clean	Gate oxide growth	40nm, 33 minutes 14 seconds @ 1050°C in dry environment
Clean	9.4	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	9.5	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	9.6	LPCVD-A3: Amor-Si/Poly (CVD-A3)	P2-01000	Clean	Gate electrode growth	250nm of poly silicon
Clean	9.7	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min
Clean	9.8	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Clean	9.9	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	9.10	Poly etcher (DRY-Poly)	P2-01000	Clean Semi clean	Poly silicon etch	HBr only, 2 minutes



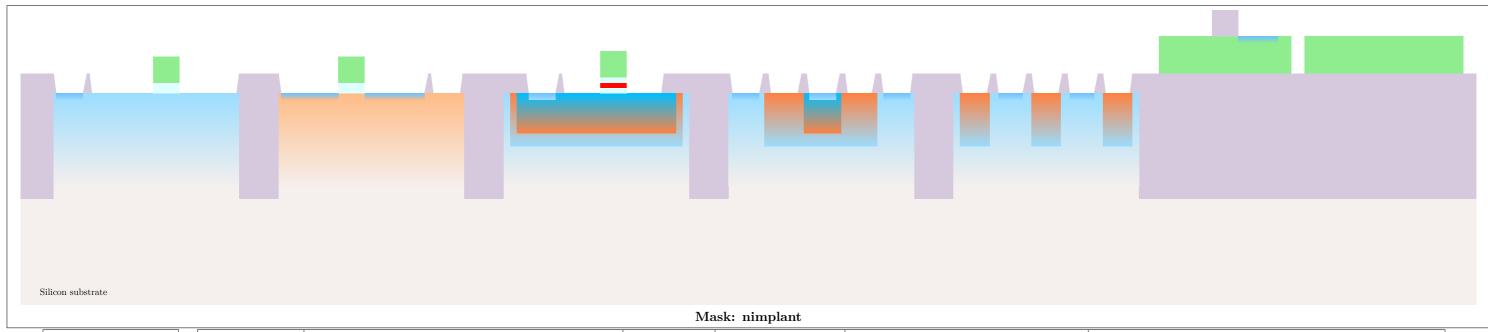
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	9.11	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	9.12	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	9.13	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

## 10 Implant stop



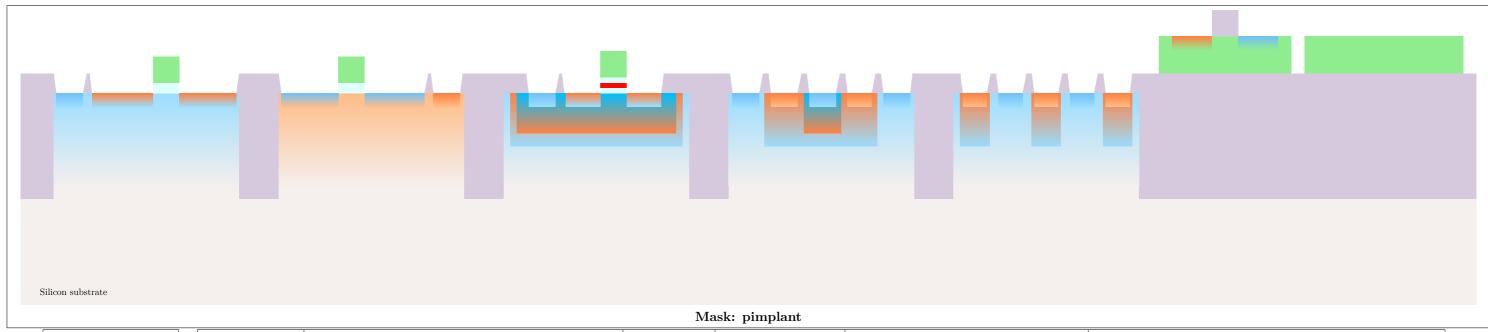
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	10.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	10.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	10.3	LPCVD-B3 LTO (CVD-B3)	P2-01000	Clean	Oxide deposition	200nm LTO
Clean	10.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5\mu m$ ), soft bake: 110°C 1min
Clean	10.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Clean	10.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	10.7	NFF RIE Etcher (DRY-RIE-2)	P2-01000	Clean Semi clean	CHF3 etch	300 seconds
Clean	10.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
Clean	10.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

# 11 N+ implant

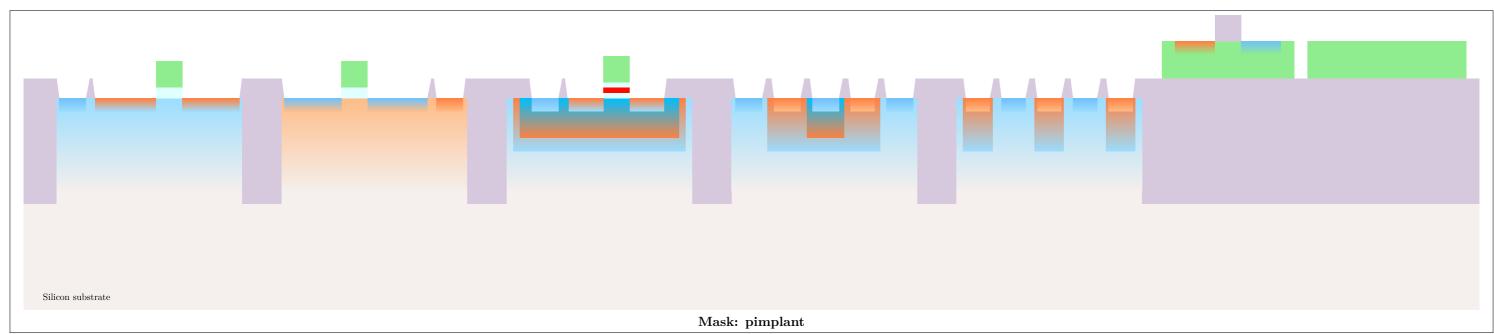


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	11.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	11.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	11.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min
Clean	11.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340mJcm^2$
Clean	11.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 30min
Clean	11.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Phorphorus implant	$2.5 \times 10^{12} cm^{-2}$ @ $30 \text{keV}$
Clean	11.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	11.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	11.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

## 12 P+ implant

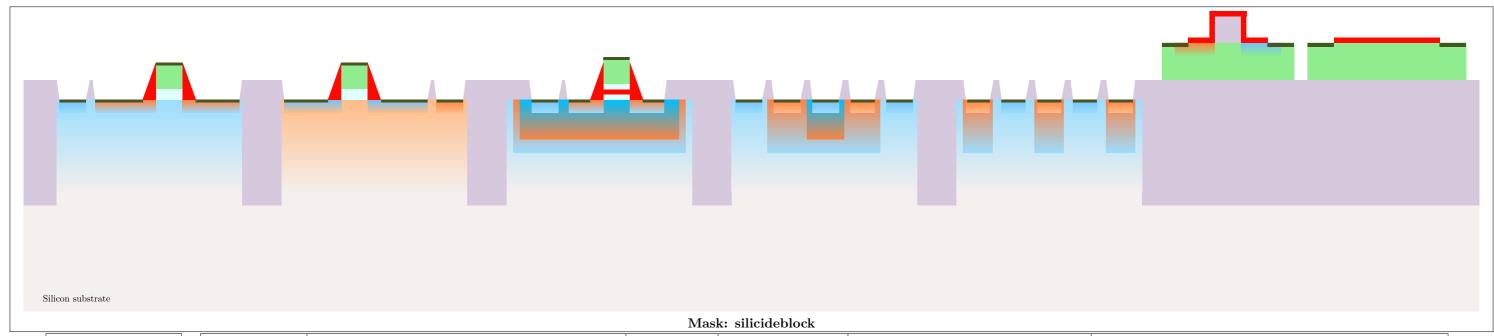


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Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	12.1	B1: Sulfuric cleaning (WET-B1)	P2-01000	Clean	Default cleaning	
Clean	12.2	Spin Dryer-B (SRD-B)	P2-01000	Clean	Dry the wafer automatically	
Clean	12.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	FH 6400L: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min
Clean	12.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$340mJcm^2$
Clean	12.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 30min
Clean	12.6	CF-3000 Implanter (IMP-3000)	P2-01000	Clean Semi clean	Boron implant	$2.5 \times 10^{12} cm^{-2}$ @ 20keV
Clean	12.7	PS210 Asher (DRY-PR-1)	P2-01000	Clean	Resist strip	
Clean	12.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Resist strip	
Clean	12.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Clean	12.10	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	

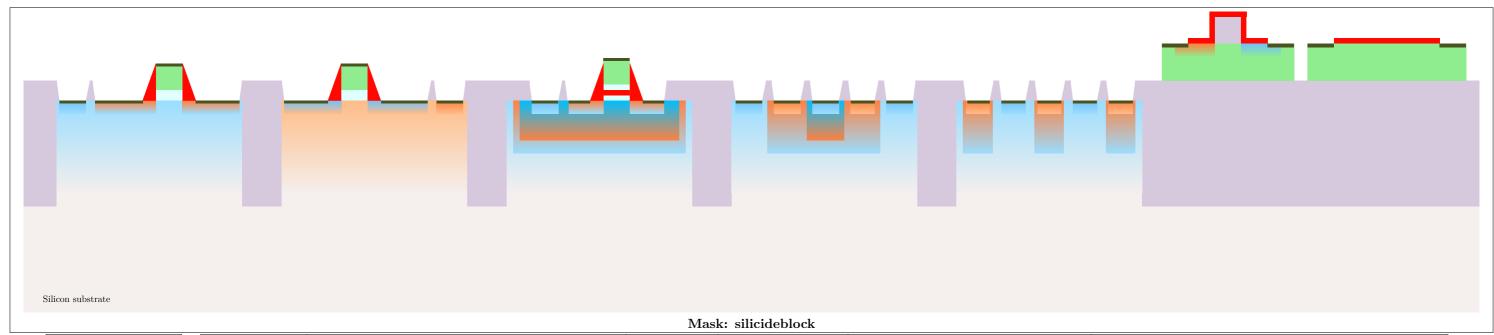


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	12.11	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	12.12	Diffusion Furnace-A1, anneal/oxidation (DIF-A1)	P2-01000	Clean	Drive in	30 minutes @ 900°C , drive in + dry oxidation

## 13 Silicification

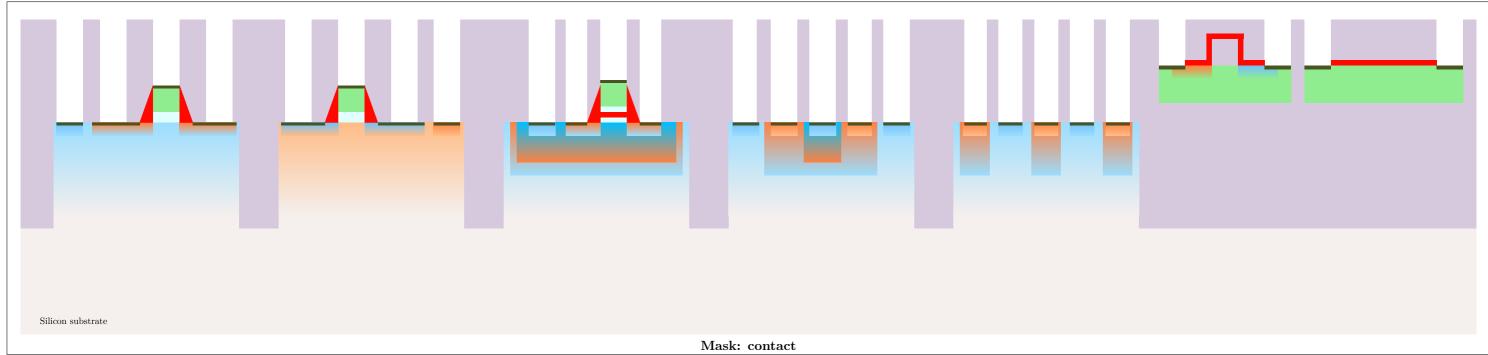


Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Clean	13.1	A3:Sulfuric cleaning (WET-A3)	P2-01000	Clean	Default cleaning	
Clean	13.2	Spin Dryer-A (SRD-A)	P2-01000	Clean	Dry the wafer automatically	
Clean	13.3	LPCVD-B2 Nitride/Low-Stress Nitride (CVD-B2)	P2-01000	Clean	Spacer nitride	50 nm
Clean	13.4	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5\mu m$ ), soft bake: 110°C 1min
Clean	13.5	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Clean	13.6	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Clean	13.7	NFF RIE Etcher (DRY-RIE-2)	P2-01000	Clean Semi clean	Anisotropic nitride etch	120 seconds
Clean	13.8	E4:Resist strip (WET-E4)	P2-01000	Clean Semi clean	Sulfuric resist strip	H2SO4+H2O2, 120°C , 10mins
Clean	13.9	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	
Semi clean	13.10	NSC3000 Sputter (SPT-NSC3000)	P2-01000	Semi clean	Deposit Titanium	50nm



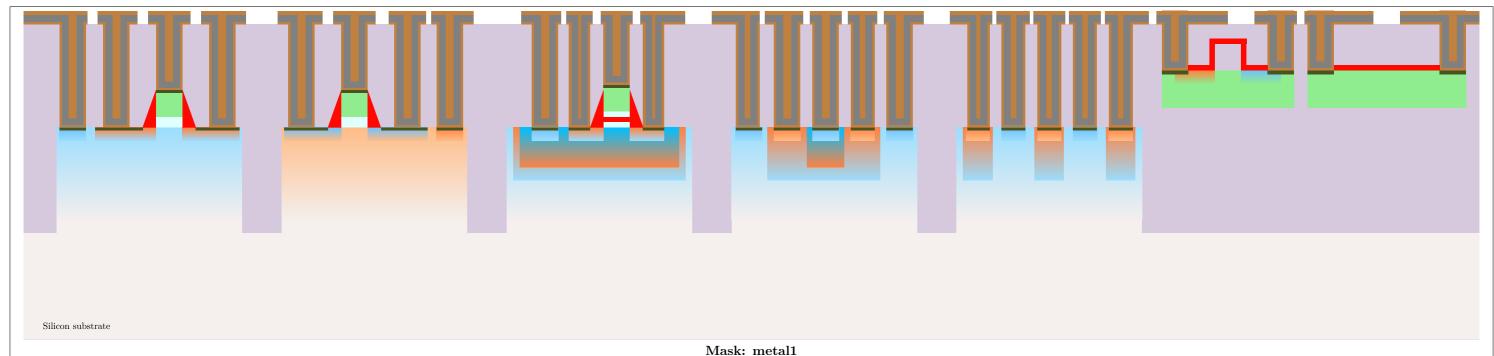
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	13.11	AG610 RTP (DIF-R2)	P2-01000	Semi clean	Reaction phase	30 seconds @ 800°C , Argon atmosphere
Semi clean	13.12	E2: General purpose (WET-E2)	P2-01000	Semi clean	Remove unreacted Titanium	RCA @ room temperature, 2 minutes
Semi clean	13.13	Spin Dryer-E (SRD-E)	P2-01000	Clean Semi clean	Dry the wafer automatically	

## 14 Contact



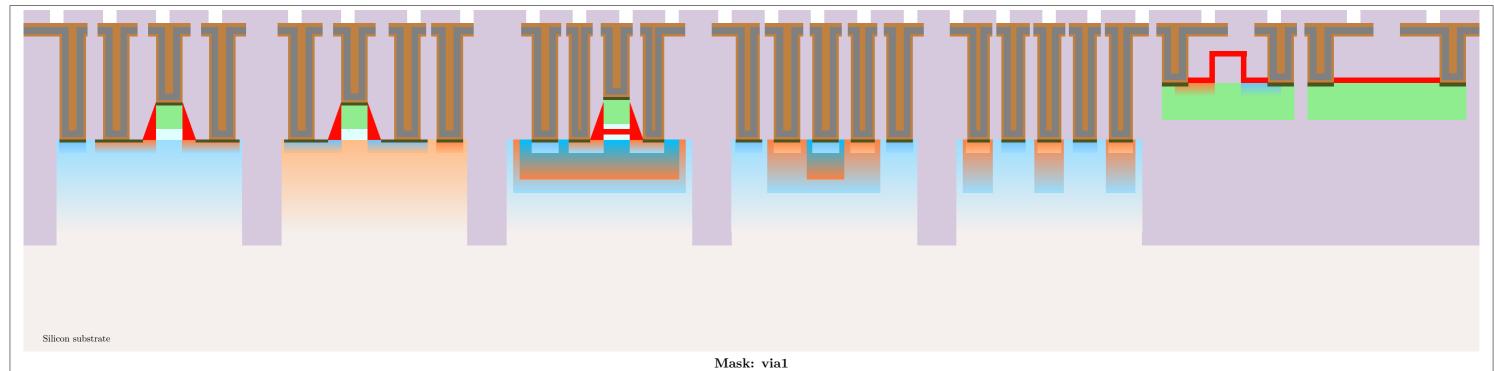
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	14.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	14.2	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	150 nm
Semi clean	14.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min
Semi clean	14.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Semi clean	14.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C, 1min
Semi clean	14.6	NFF RIE Etcher (DRY-RIE-2)	P2-01000	Clean Semi clean	150nm LTO etch	3 minutes
Semi clean	14.7	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist strip	10mins
Semi clean	14.8	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

#### 15 Metal 1



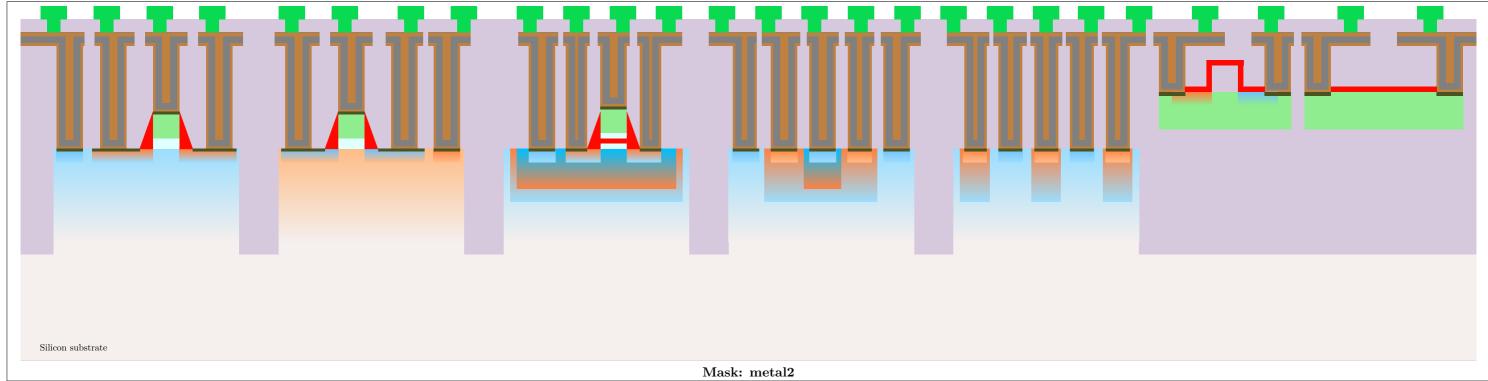
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	15.1	NSC3000 Sputter (SPT-NSC3000)	P2-01000	Semi clean	Nickel diffusion barrier + Deposit $Aluminum + Nickel finish$	Nickel (roughly 50nm) + Aluminum (roughly 100nm) + Nickel (roughly 50nm)
Semi clean	15.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5\mu m$ ), soft bake: 110°C 1min
Semi clean	15.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Semi clean	15.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	15.5	AST Metal Etcher (DRY-Metal-1)	P2-01000	Semi clean	Wire formation	200 nm
Semi clean	15.6	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist strip	10mins
Semi clean	15.7	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

#### 16 Via 1



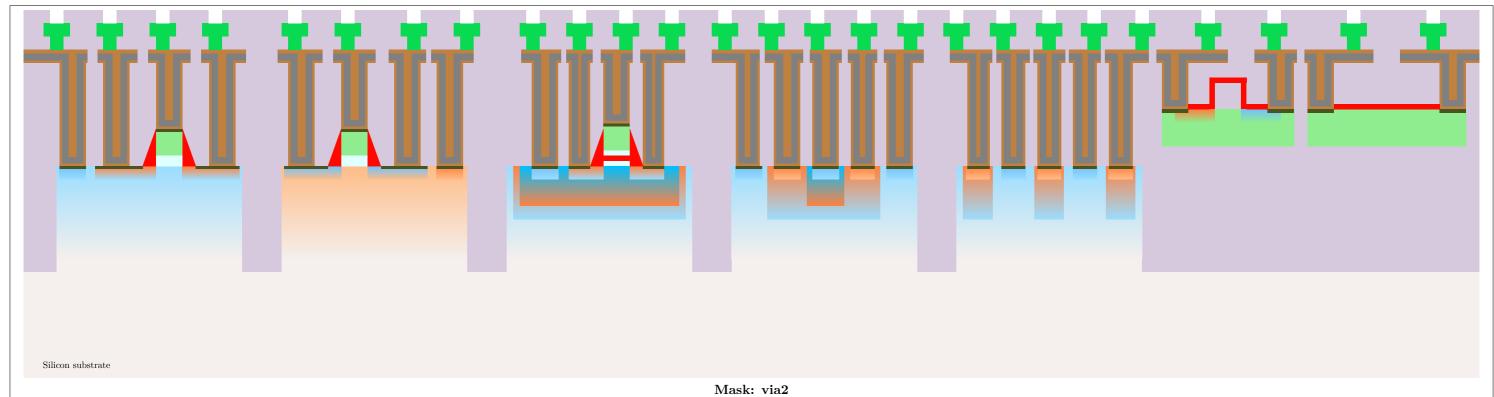
Wafer Cleanliness	Step Number	${\bf Equipment}$	Location	Cleanliness	Process	Requirements
Semi clean	16.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	16.2	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	150 nm
Semi clean	16.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min
Semi clean	16.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Semi clean	16.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	16.6	NFF RIE Etcher (DRY-RIE-2)	P2-01000	Clean Semi clean	150nm LTO etch	3 minutes
Semi clean	16.7	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist strip	10mins
Semi clean	16.8	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

## 17 Metal 2



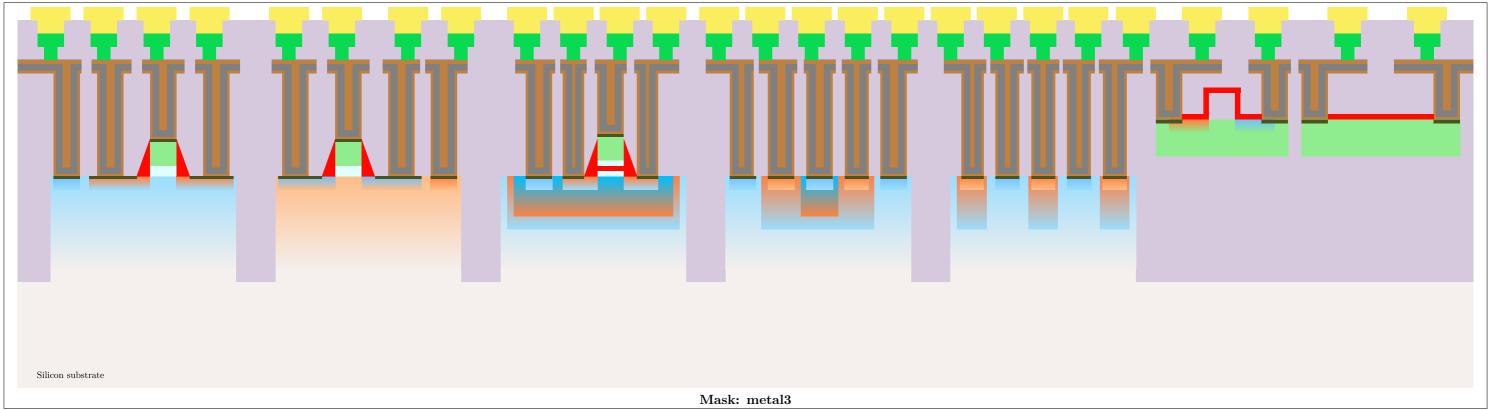
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	17.1	NSC3000 Sputter (SPT-NSC3000)	P2-01000	Semi clean	Deposit Aluminum + Nickel finish	Aluminum (roughly 100nm) + Nickel (roughly 50nm)
Semi clean	17.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5\mu m$ ), soft bake: 110°C 1min
Semi clean	17.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Semi clean	17.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	17.5	AST Metal Etcher (DRY-Metal-1)	P2-01000	Semi clean	Wire formation	150 nm
Semi clean	17.6	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist strip	10mins
Semi clean	17.7	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

#### 18 Via 2



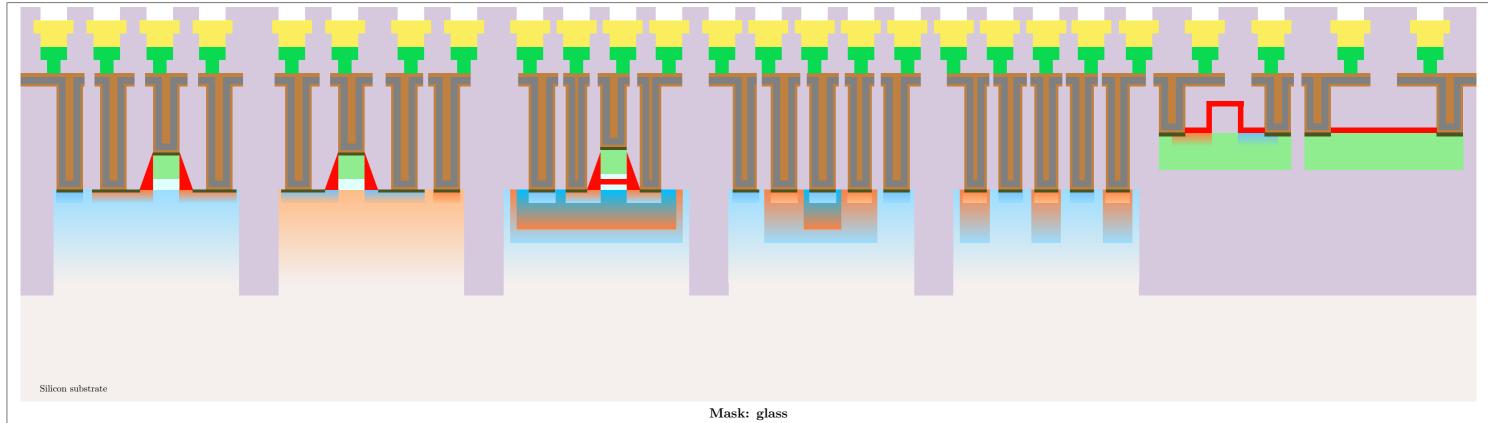
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	18.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning	
Semi clean	18.2	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	150nm
Semi clean	18.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5 \mu m$ ), soft bake: 110°C 1min
Semi clean	18.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Semi clean	18.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	18.6	NFF RIE Etcher (DRY-RIE-2)	P2-01000	Clean Semi clean	150nm LTO etch	3 minutes
Semi clean	18.7	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist strip	10mins
Semi clean	18.8	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

## 19 Metal 3



Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements
Semi clean	19.1	NSC3000 Sputter (SPT-NSC3000)	P2-01000	Semi clean	Deposit Aluminum + Nickel finish	Aluminum (roughly 100nm) + Nickel (roughly 50nm)
Semi clean	19.2	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5\mu m$ ), soft bake: 110°C 1min
Semi clean	19.3	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$
Semi clean	19.4	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min
Semi clean	19.5	AST Metal Etcher (DRY-Metal-1)	P2-01000	Semi clean	Wire formation	150 nm
Semi clean	19.6	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist strip	10mins
Semi clean	19.7	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry	

## 20 Glass



wask, glass								
Wafer Cleanliness	Step Number	Equipment	Location	Cleanliness	Process	Requirements		
Semi clean	20.1	D1: Dump rinse (WET-D-DR)	P2-01000	Semi clean	Wafer cleaning			
Semi clean	20.2	LPCVD-F4 LTO/PSG (CVD-F4)	P2-01000	Semi clean	Oxide deposition	150nm		
Semi clean	20.3	SVG Coater Track (PHT-T1)	P2-00100	Clean Semi clean	HMDS, PR coating, soft bake	HPR 504: 3krpm ( ${\approx}1.5\mu m$ ), soft bake: 110°C 1min		
Semi clean	20.4	ASML Stepper (PHT-S1)	P2-00100	Clean Semi clean	Exposure of the layer	$280mJcm^2$		
Semi clean	20.5	SVG Developer Track (PHT-T2)	P2-00100	Clean Semi clean	Develop, Hard bake	FHD-5, 1min; hard bake: 120°C , 1min		
Semi clean	20.6	NFF RIE Etcher (DRY-RIE-2)	P2-01000	Clean Semi clean	150nm LTO etch	3 minutes		
Semi clean	20.7	Y1:MS2001 Resist strip (WET-Y1)	P2-00100	Semi clean	Resist strip	10mins		
Semi clean	20.8	Spin Dryer-Y (SRD-Y)	P2-00100	Semi clean	Spin dry			

