

LAB을 위한 파일 설명

Auto PnR

파일확인

```
$> vi cmsdk_mcu.mmmmc.view
```

- 아래의 경로에서 cmsdk_mcu.mmmmc.view 파일확인

/home/ex_poly1/SoC2/SoC/smkcowl_make_S28/TOP/PNR

add_pad

cmsdk_mcu.mmmmc.view

cmsdk_mcu_syn_final.v
init.io

cmsdk_mcu_syn_final.sdc

Auto PnR

파일확인

```
$> vi cmsdk_mcu.mmmmc.view
```

- **cmsdk_mcu.mmmmc.view**는 constraints를 적용한 best condition과 worst condition을 setting해주는 파일임

```
1 ##### Create RC_Corner #####
2 ##### Create RC_Corner #####
3 #####
4
5 create_rc_corner -name BEST \
6   -T 0 \
7   -qx_tech_file ../../../../../../GPKD045/digital/gsclib045_all_v4.4/gsclib045/qrc/px/gpkd045.tch
8
9 create_rc_corner -name WORST \
10  -T 125 \
11  -qx_tech_file ../../../../../../GPKD045/digital/gsclib045_all_v4.4/gsclib045/qrc/px/gpkd045.tch
12
```

-T: 온도

1행 ~ 11행은 RC_Corner를 설정하기 위해 techfile의 경로를 입력해줌

Auto PnR

파일확인

```
$> vi cmsdk_mcu.mmmc.view
```

- 14행부터 31행은 라이브러리를 set하기위한 설정임

```
14 #####  
15 ##### Create Library_Set #####  
16 #####  
17  
18 create_library_set -name FF_Min_1p10v_0c \  
19     -timing \  
20     [list \  
21         ../../../../GPDK045/digital/giolib045_v3.5/timing/pads_FF_s1vg.lib \  
22         ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/timing/fast_vdd1v0_basicCells.lib \  
23         ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/timing/fast_vdd1v0_multibitsDFF.lib \  
24     ]  
25  
26 create_library_set -name SS_Max_0p90v_125c \  
27     -timing \  
28     [list \  
29         ../../../../GPDK045/digital/giolib045_v3.5/timi  
30         ../../../../GPDK045/digital/gsclib045_all_v4.4/  
31         ../../../../GPDK045/digital/gsclib045_all_v4.4/  
32     ]
```

18행은 이름을 FF_Min_1p10v_0c으로 설정하고
best condition에서 사용함 0도에 1.1V를 주면
가장 빠른 Cell_delay임

26행은 이름을 SS_Max_0p90v_125c으로 설정하고
worst condition에서 사용함
125도에 0.9V를 주면 가장 느린 Cell_delay임

Auto PnR

파일확인

```
$> vi cmsdk_mcu.mmmc.view
```

- 35행부터 45행은 앞서 설정한 내용을 사용하여 Delay_Corner을 만듦

```
34
35 #####
36 ##### Create Delay_Corner #####
37 #####
38
39 create_delay_corner -name FF_BEST \
40     -library_set FF_Min_1p10v_0c \
41     -rc corner BEST
42
43 create_delay_corner -name SS_WORST \
44     -library_set SS_Max_0p90v_125c \
45     -rc corner WORST
```

39행은 FF_BEST로 Best condition에 필요한 cell_delay와 net_delay 묶어 놓음

43행은 SS_WORST로 Worst condition에 필요한 cell_delay와 net_delay 묶어 놓음

Auto PnR

파일확인

```
$> vi cmsdk_mcu.mmmmc.view
```

- 48행부터 54행은 우리가 사용할 .sdc파일을 설정해주는 행임

```
48 #####
49 ##### Create Constraint_Mode #####
50 #####
51
52
53 create_constraint_mode -name FUNC \
54     -sdc files [list ./cmsdk mcu syn final.sdc]
```

Auto PnR

파일확인

```
$> vi cmsdk_mcu.mmmc.view
```

- 57행부터 68행은 설정한 .sdc 파일과 delay코너를 묶어 베스트와 워스트 각각의 Analysis_view를 만듦

```
--  
57 #####  
58 ##### Create Analysis_view #####  
59 #####  
60  
61  
62 create_analysis_view -name FUNC_FF_BEST \  
63     -constraint_mode FUNC \  
64     -delay_corner FF_BEST  
65  
66 create_analysis_view -name FUNC_SS_WORST \  
67     -constraint_mode FUNC \  
68     -delay_corner SS_WORST
```

Auto PnR

파일확인

```
$> vi cmsdk_mcu.mmmmc.view
```

- 70행부터 76행은 설정한 Analysis_view를 어떤 상황일 때 사용할지 정함

```
70 #####
71 ##### Set Analysis_view #####
72 #####
73
74
75 set analysis view -setup [list FUNC SS WORST] \
76     -hold [list FUNC_FF_BEST]
```

SS_WORST는 setup time violation을 확인
FF_BEST는 hold time violation을 확인함

Auto PnR

파일확인

```
$> vi init.io
```

- 아래의 경로에서 init.io 파일확인

/home/ex_poly1/SoC2/SoC/smkcow_make_S28/TOP/PNR

add_pad	cmsdk_mcu_syn_final.v
cmsdk_mcu.mmmmc.view	init.io
cmsdk_mcu_syn_final.sdc	

Auto PnR

파일확인

\$> vi init.io

- io cell의 위치와 pad번호 및 사용되는 cell목록을 설정해주는 파일임
- 코어영역 바깥으로 io셀이 생성됨

```
1 (globals
2     version = 3
3     io_order = default
4 )
5 (iopad
6     (left
7         (inst name="pad50"
8             (inst name="pad49"
9                 (inst name="pad48"
10                (inst name="pad47"
11                (inst name="pad46"
12                (inst name="pad45"
13                (inst name="pad44"
14                (inst name="pad43"
15                (inst name="pad42"
16                (inst name="pad41"
17                (inst name="pad40"
18                    (inst name="pad39"
```

1. 사용할 패드 번호 지정
2. 패드에 연결할 io셀 지정
3. offset으로 좌표 지정

```
cell="PADVSSIOR" offset=300 )
cell="PADVSSIOR" offset=370 )
cell="PADVDDIOR" offset=440 )
cell="PADVSS" offset=510 )
cell="PADVDD" offset=580 )
cell="PADDB" offset=650 )
cell="PADDB" offset=720 )
cell="PADDB" offset=790 )
cell="PADDB" offset=860 )
cell="PADDB" offset=930 )
cell="PADDB" offset=1000)
cell="PADDB" offset=1070)
```

```
58 (topleft
59     (inst name="CORNER_TL" cell="padIORINGCORNER")
60 )
```

58행은 코너 셀의 위치를 지정함

Auto PnR

파일확인

\$> vi init.io

- Pad의 위치, 용도, 거리 등의 정보는 모두 엔지니어가 직접 설계해야 함
- 다음 페이지에 pad와 셀의 정보를 보면 **실습 진행**

```
1 (globals
2     version = 3
3     io_order = default
4 )
5 (iopad
6     (left
7         (inst name="pad50"      cell="PADVSSIOR" offset=300 )
8         (inst name="pad49"      cell="PADVSSIOR" offset=370 )
9         (inst name="pad48"      cell="PADVDDIOR" offset=440 )
10        (inst name="pad47"      cell="PADVSS"      offset=510 )
11        (inst name="pad46"      cell="PADVDD"      offset=580 )
12        (inst name="pad45"      cell="PADDB"       offset=650 )
13        (inst name="pad44"      cell="PADDB"       offset=720 )
14        (inst name="pad43"      cell="PADDB"       offset=790 )
15        (inst name="pad42"      cell="PADDB"       offset=860 )
16        (inst name="pad41"      cell="PADDB"       offset=930 )
17        (inst name="pad40"      cell="PADDB"       offset=1000)
18        (inst name="pad39"      cell="PADDB"       offset=1070)

58    (topleft
59        (inst name="CORNER_TL" cell="padIORINGCORNER")
60    )
```

Auto PnR

Init.io 작성

```
$> vi cmsdk_mcu_syn_final.v
```

- 아래의 경로에서 cmsdk_mcu_syn_final.v 파일 확인

/home/ex_poly1/SoC2/SoC/smkcowl_make_S28/TOP/PNR

add_pad
cmsdk_mcu.mmmc.view

cmsdk_mcu_syn_final.v
init.io

cmsdk_mcu_syn_final.sdc

Auto PnR

Init.io 작성

```
$> vi cmsdk_mcu_syn_final.v
```

- 우리가 사용하는 **cmsdk_mcu**에 대한 모든 cell 정보가 들어있는 파일임

```
1 // Generated by Cadence Genus(TM) Synthesis Solution 22.16-s078_1
2 // Generated on: Jan 22 2025 15:09:17 KST (Jan 22 2025 06:09:17 UTC)
3
4
5 // Verification Directory fv/cmsdk_mcu
6
7 module cmsdk_mcu_clkctrl_CLKGATE_PRESENT0(XTAL1, NRST, APBACTIVE,
8     SLEEPING, SLEEPDEEP, SYSRESETREQ, DBGRESETREQ, LOCKUP,
9     LOCKUPRESET, CGBYPASS, RSTBYPASS, XTAL2, FCLK, PCLK, PCLKG,
10    PCLKEN, PORESETn, HRESETn, PRESETn);
11   input XTAL1, NRST, APBACTIVE, SLEEPING, SLEEPDEEP, SYSRESETREQ,
12     DBGRESETREQ, LOCKUP, LOCKUPRESET, CGBYPASS, RSTBYPASS;
13   output XTAL2, FCLK, PCLK, PCLKG, PCLKEN, PORESETn, HRESETn, PRESETn;
14   wire XTAL1, NRST, APBACTIVE, SLEEPING, SLEEPDEEP, SYSRESETREQ,
15     DBGRESETREQ, LOCKUP, LOCKUPRESET, CGBYPASS, RSTBYPASS;
16   wire XTAL2, FCLK, PCLK, PCLKG, PCLKEN, PORESETn, HRESETn, PRESETn;
17   wire [2:0] reset_sync_reg;
18   wire n_2;
19   DFFRHQX1 hrst_reg_reg(.RN (PORESETn), .CK (XTAL1), .D (n_2), .Q
20     (HRESETn));
21   DFFRHQX1 prst_reg_reg(.RN (PORESETn), .CK (XTAL1), .D (n_2), .Q
22     (PRESETn));
23   DFFRHQX1 reset_sync_reg_reg_2(.RN (NRST), .CK (XTAL1), .D
24     (reset_sync_reg[1]), .Q (PORESETn));
25   DFFRHQX1 reset_sync_reg_reg_1(.RN (NRST), .CK (XTAL1), .D
26     (reset_sync_reg[0]), .Q (reset_sync_reg[1]));
27   AOI21X1 g69_2398(.A0 (LOCKUPRESET), .A1 (LOCKUP), .B0 (SYSRESETREQ),
28     .Y (n_2));
29   DFFRHQX1 reset_sync_reg_reg_0(.RN (NRST), .CK (XTAL1), .D (1'b1), .Q
30     (reset_sync_reg[0]));
31 endmodule
```

Auto PnR

Init.io 작성

```
$> vi cmsdk_mcu_syn_final.v
```

- `/pad1(` 을 입력해 pad에 대한 정보 검색

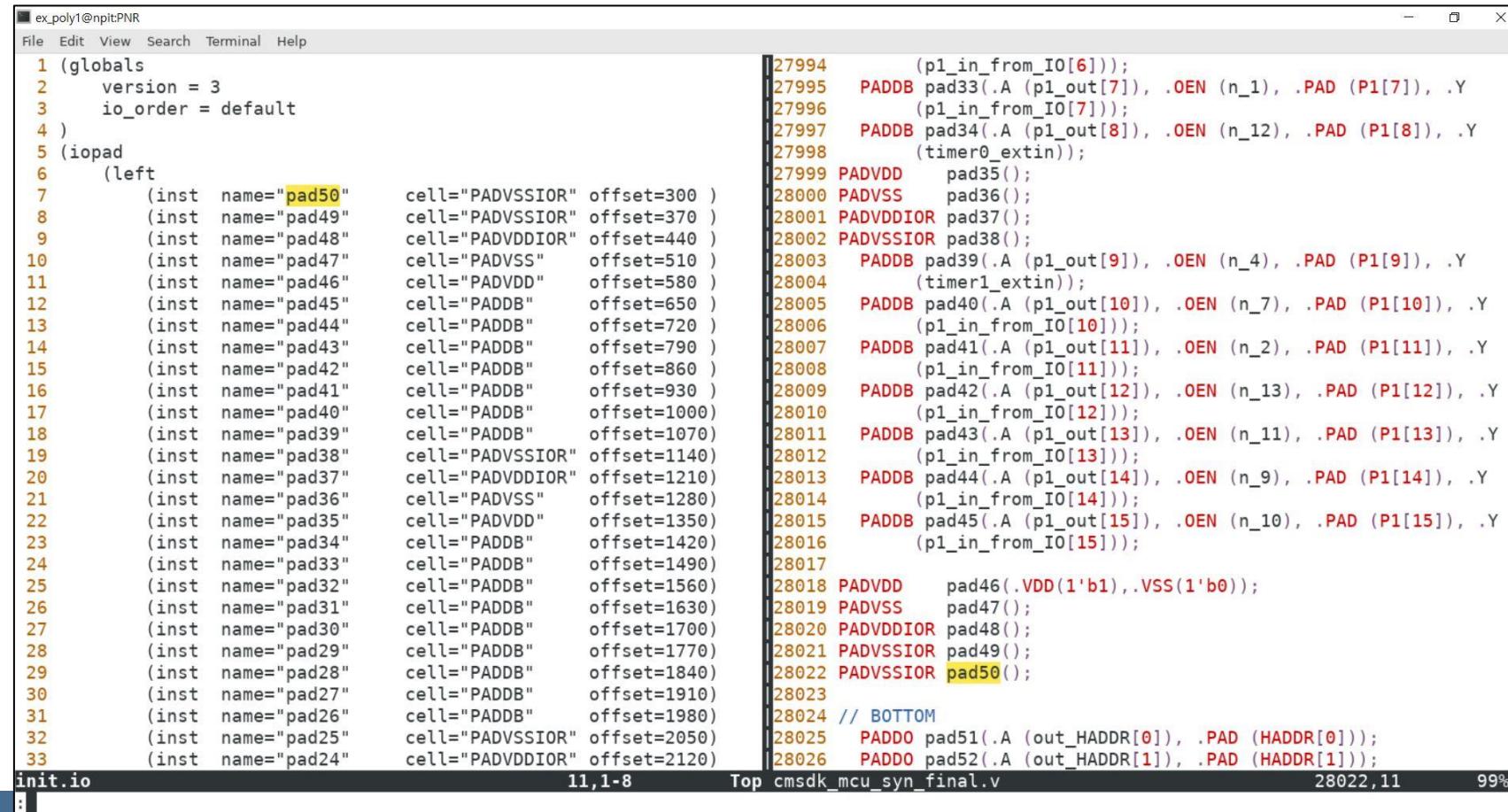
```
27955 //LEFT
27956 PADVDDIOR pad1();
27957 PADVSSIOR pad2();
27958 PADVDDIOR pad3();
27959 PADVDDIOR pad4();
27960    PADDO pad5(.A (1'b1), .PAD (TDO));
27961    PADDI pad6(.PAD (XTAL1), .Y (FCLK));
27962 PADVSS      pad7();
27963 PADVSSIOR pad8();
27964    PADDO pad9(.A (n_6), .PAD (XTAL2));
27965 PADVSSIOR pad10();
27966
27967
27968 PADVDD      pad11();
27969 PADVSS      pad12();
27970 PADVDDIOR pad13();
27971 PADVSSIOR pad14();
27972 PADDI pad15(.PAD (NRST), .Y (in_NRST));
27973 PADDO pad16(.A (out_HRESETn), .PAD (HRESETn));
```

Auto PnR

Init.io 작성

\$> vi cmsdk_mcu_syn_final.v

- 화면을 분할한 후 검색 기능을 통해 직접 입력함



```
File Edit View Search Terminal Help
1 (globals
2     version = 3
3     io_order = default
4 )
5 (iopad
6     (left
7         (inst name="pad50"      cell="PADVSSIOR" offset=300 )
8         (inst name="pad49"      cell="PADVSSIOR" offset=370 )
9         (inst name="pad48"      cell="PADVDDIOR" offset=440 )
10        (inst name="pad47"      cell="PADVSS"      offset=510 )
11        (inst name="pad46"      cell="PADVDD"      offset=580 )
12        (inst name="pad45"      cell="PADDB"       offset=650 )
13        (inst name="pad44"      cell="PADDB"       offset=720 )
14        (inst name="pad43"      cell="PADDB"       offset=790 )
15        (inst name="pad42"      cell="PADDB"       offset=860 )
16        (inst name="pad41"      cell="PADDB"       offset=930 )
17        (inst name="pad40"      cell="PADDB"       offset=1000)
18        (inst name="pad39"      cell="PADDB"       offset=1070)
19        (inst name="pad38"      cell="PADVSSIOR" offset=1140)
20        (inst name="pad37"      cell="PADVDDIOR" offset=1210)
21        (inst name="pad36"      cell="PADVSS"      offset=1280)
22        (inst name="pad35"      cell="PADVDD"      offset=1350)
23        (inst name="pad34"      cell="PADDB"       offset=1420)
24        (inst name="pad33"      cell="PADDB"       offset=1490)
25        (inst name="pad32"      cell="PADDB"       offset=1560)
26        (inst name="pad31"      cell="PADDB"       offset=1630)
27        (inst name="pad30"      cell="PADDB"       offset=1700)
28        (inst name="pad29"      cell="PADDB"       offset=1770)
29        (inst name="pad28"      cell="PADDB"       offset=1840)
30        (inst name="pad27"      cell="PADDB"       offset=1910)
31        (inst name="pad26"      cell="PADDB"       offset=1980)
32        (inst name="pad25"      cell="PADVSSIOR" offset=2050)
33        (inst name="pad24"      cell="PADVDDIOR" offset=2120)
27994    (p1_in_from_I0[6]));
27995    PADDB pad33(.A (p1_out[7]), .OEN (n_1), .PAD (P1[7]), .Y
27996    (p1_in_from_I0[7]));
27997    PADDB pad34(.A (p1_out[8]), .OEN (n_12), .PAD (P1[8]), .Y
27998    (timer0_extin));
27999    PADVDD   pad35();
28000    PADVSS   pad36();
28001    PADVDDIOR pad37();
28002    PADVSSIOR pad38();
28003    PADDB pad39(.A (p1_out[9]), .OEN (n_4), .PAD (P1[9]), .Y
28004    (timer1_extin));
28005    PADDB pad40(.A (p1_out[10]), .OEN (n_7), .PAD (P1[10]), .Y
28006    (p1_in_from_I0[10]));
28007    PADDB pad41(.A (p1_out[11]), .OEN (n_2), .PAD (P1[11]), .Y
28008    (p1_in_from_I0[11]));
28009    PADDB pad42(.A (p1_out[12]), .OEN (n_13), .PAD (P1[12]), .Y
28010    (p1_in_from_I0[12]));
28011    PADDB pad43(.A (p1_out[13]), .OEN (n_11), .PAD (P1[13]), .Y
28012    (p1_in_from_I0[13]));
28013    PADDB pad44(.A (p1_out[14]), .OEN (n_9), .PAD (P1[14]), .Y
28014    (p1_in_from_I0[14]));
28015    PADDB pad45(.A (p1_out[15]), .OEN (n_10), .PAD (P1[15]), .Y
28016    (p1_in_from_I0[15]));
28017
28018    PADVDD   pad46(.VDD(1'b1),.VSS(1'b0));
28019    PADVSS   pad47();
28020    PADVDDIOR pad48();
28021    PADVSSIOR pad49();
28022    PADVSSIOR pad50();
28023
28024 // BOTTOM
28025    PADDO pad51(.A (out_HADDR[0]), .PAD (HADDR[0]));
28026    PADDO pad52(.A (out_HADDR[1]), .PAD (HADDR[1]));
init.io          11,1-8      Top cmsdk_mcu_syn_final.v      28022,11      99%
```

:vs → :e .
init.io Enter

Auto PnR

Init.io 작성

\$> vi cmsdk_mcu_syn_final.v

후에 복사, 레코딩 기능 추가예정

:vs → :e .
init.io Enter

- 화면을 분할한 후 검색 기능을 통해 직접 입력함

```
File Edit View Search Terminal Help
1 (globals
2     version = 3
3     io_order = default
4 )
5 (iopad
6     (left
7         (inst name="pad50"      cell="PADVSSIOR" offset=300 )
8         (inst name="pad49"      cell="PADVSSIOR" offset=370 )
9         (inst name="pad48"      cell="PADVDDIOR" offset=440 )
10        (inst name="pad47"     cell="PADVSS"      offset=510 )
11        (inst name="pad46"     cell="PADVDD"      offset=580 )
12        (inst name="pad45"     cell="PADDB"       offset=650 )
13        (inst name="pad44"     cell="PADDB"       offset=720 )
14        (inst name="pad43"     cell="PADDB"       offset=790 )
15        (inst name="pad42"     cell="PADDB"       offset=860 )
16        (inst name="pad41"     cell="PADDB"       offset=930 )
17        (inst name="pad40"     cell="PADDB"       offset=1000)
18        (inst name="pad39"     cell="PADDB"       offset=1070)
19        (inst name="pad38"     cell="PADVSSIOR" offset=1140)
20        (inst name="pad37"     cell="PADVDDIOR" offset=1210)
21        (inst name="pad36"     cell="PADVSS"      offset=1280)
22        (inst name="pad35"     cell="PADVDD"      offset=1350)
23        (inst name="pad34"     cell="PADDB"       offset=1420)
24        (inst name="pad33"     cell="PADDB"       offset=1490)
25        (inst name="pad32"     cell="PADDB"       offset=1560)
26        (inst name="pad31"     cell="PADDB"       offset=1630)
27        (inst name="pad30"     cell="PADDB"       offset=1700)
28        (inst name="pad29"     cell="PADDB"       offset=1770)
29        (inst name="pad28"     cell="PADDB"       offset=1840)
30        (inst name="pad27"     cell="PADDB"       offset=1910)
31        (inst name="pad26"     cell="PADDB"       offset=1980)
32        (inst name="pad25"     cell="PADVSSIOR" offset=2050)
33        (inst name="pad24"     cell="PADVDDIOR" offset=2120)
27994    (p1_in_from_I0[6]));
27995    PADDB pad33(.A (p1_out[7]), .OEN (n_1), .PAD (P1[7]), .Y
27996    (p1_in_from_I0[7]));
27997    PADDB pad34(.A (p1_out[8]), .OEN (n_12), .PAD (P1[8]), .Y
27998    (timer0_extin));
27999    PADVDD   pad35();
28000    PADVSS   pad36();
28001    PADVDDIOR pad37();
28002    PADVSSIOR pad38();
28003    PADDB pad39(.A (p1_out[9]), .OEN (n_4), .PAD (P1[9]), .Y
28004    (timer1_extin));
28005    PADDB pad40(.A (p1_out[10]), .OEN (n_7), .PAD (P1[10]), .Y
28006    (p1_in_from_I0[10]));
28007    PADDB pad41(.A (p1_out[11]), .OEN (n_2), .PAD (P1[11]), .Y
28008    (p1_in_from_I0[11]));
28009    PADDB pad42(.A (p1_out[12]), .OEN (n_13), .PAD (P1[12]), .Y
28010    (p1_in_from_I0[12]));
28011    PADDB pad43(.A (p1_out[13]), .OEN (n_11), .PAD (P1[13]), .Y
28012    (p1_in_from_I0[13]));
28013    PADDB pad44(.A (p1_out[14]), .OEN (n_9), .PAD (P1[14]), .Y
28014    (p1_in_from_I0[14]));
28015    PADDB pad45(.A (p1_out[15]), .OEN (n_10), .PAD (P1[15]), .Y
28016    (p1_in_from_I0[15]));
28017
28018    PADVDD   pad46(.VDD(1'b1),.VSS(1'b0));
28019    PADVSS   pad47();
28020    PADVDDIOR pad48();
28021    PADVSSIOR pad49();
28022    PADVSSIOR pad50();
28023
28024 // BOTTOM
28025    PADDO pad51(.A (out_HADDR[0]), .PAD (HADDR[0]));
28026    PADDO pad52(.A (out_HADDR[1]), .PAD (HADDR[1]));
init.io          11,1-8      Top cmsdk_mcu_syn_final.v      28022,11      99%
```

LAB 준비

Auto PnR

Innovus 툴 사용 준비

- 두개의 터미널 사용 (아래의 경로에서 진행)
- 하나는 innovus 툴 실행, 나머지는 파일 확인을 위해 대기

```
ex.poly1@npitphysical_design ~
File Edit View Search Terminal Help
Cadence Innovus(TM) Implementation System.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved worldwide.

Version: v22.16-s082_1, built Fri Jun 7 09:42:52 PDT 2024
Options: -stylus
Date: Wed Feb 19 13:48:11 2025
Host: npit.ic.rnd1 (x86_64 w/Linux 3.10.0-1160.119.1.el7.x86_64) (20cores*80cpus*Intel(R) Xeon(R) Silver 4316 CPU @ 2.30 GHz 30720KB)
OS: Red Hat Enterprise Linux Server 7.9 (Maipo)

License:
[13:48:11.440209] Configured Lic search path (22.01-s003): 35266@npit-service1.iptime.org

      invs  Innovus Implementation System 22.1      ch
eckout succeeded
      8 CPU jobs allowed with the current license(s). U
se set_multi_cpu_usage to set your required CPU count.

Create and set the environment variable TMPDIR to /home/ex_poly1/
SoC2/RAK/RTLtoGDSII/counter_design_database_45nm/physical_design/
innovus_temp_71034_5f85f843-0c94-4c00-af10-9ddbeaaba754_npit.ic.r
nd1_ex_poly1_4tsHgP.

Change the soft stacksize limit to 0.2%RAM (771 mbytes). Set glob
al soft_stack_size_limit to change the value.

**INFO: MMC transition support version v31-84

@innovus 1> 
```

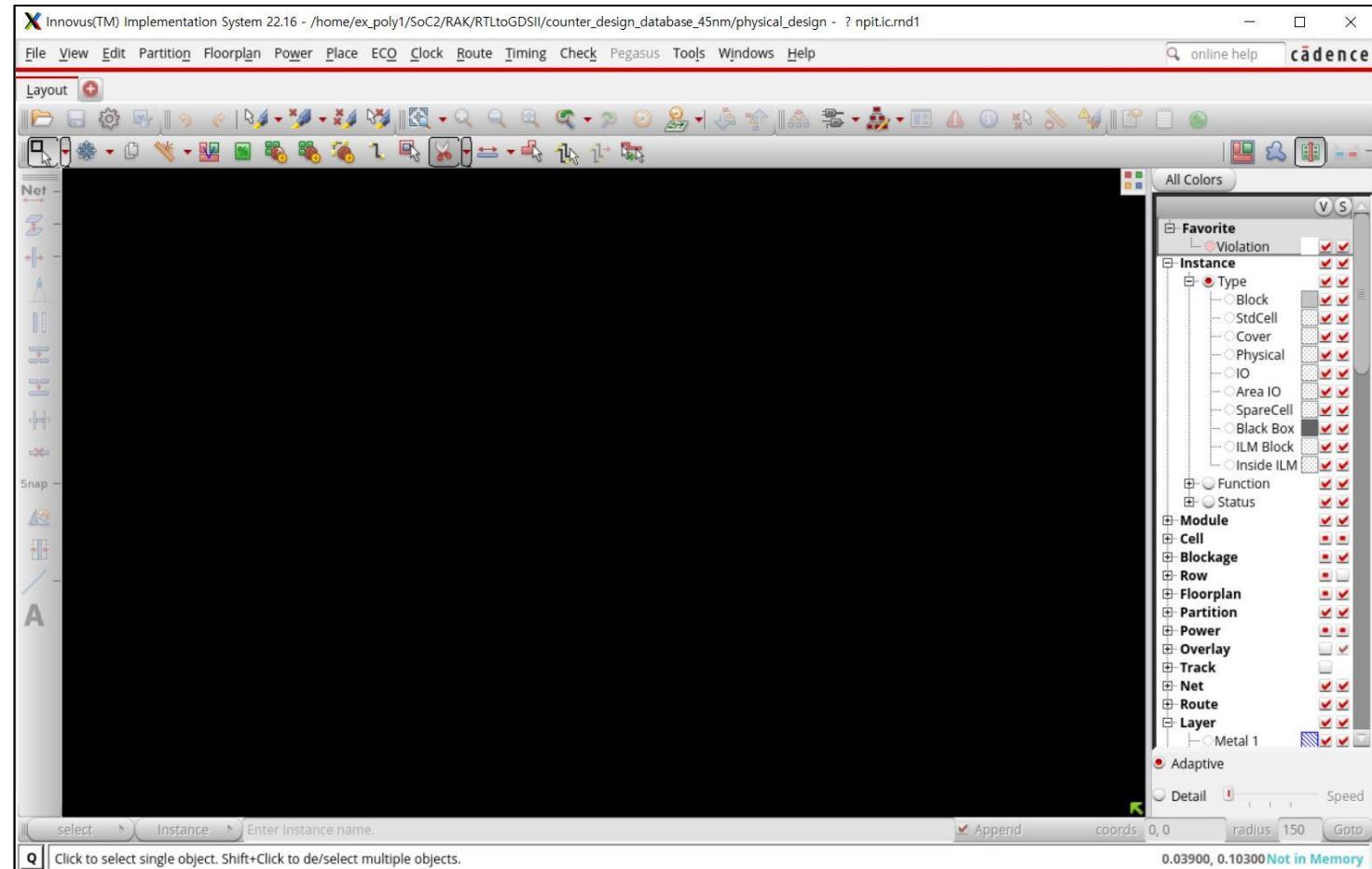
```
ex_poly1@npit physical_design ~
File Edit View Search Terminal Help
[ex_poly1@npit physical_design]$ pwd
/home/ex_poly1/SoC2/RAK/RTLtoGDSII/counter_design_database_45nm/physical_design
[ex_poly1@npit physical_design]$ 
```

Auto PnR

Innovus 툴 사용 준비

\$> innovus

- Innovus의 gui가 자동으로 실행됨
- 이번 LAB은 실제 우리가 합성한 디자인으로 Place and Route 하는 과정임
- 각 옵션과 자세한 툴 사용법은 전의 LAB(예시)에서 진행했으므로 자세한 설명 생략함

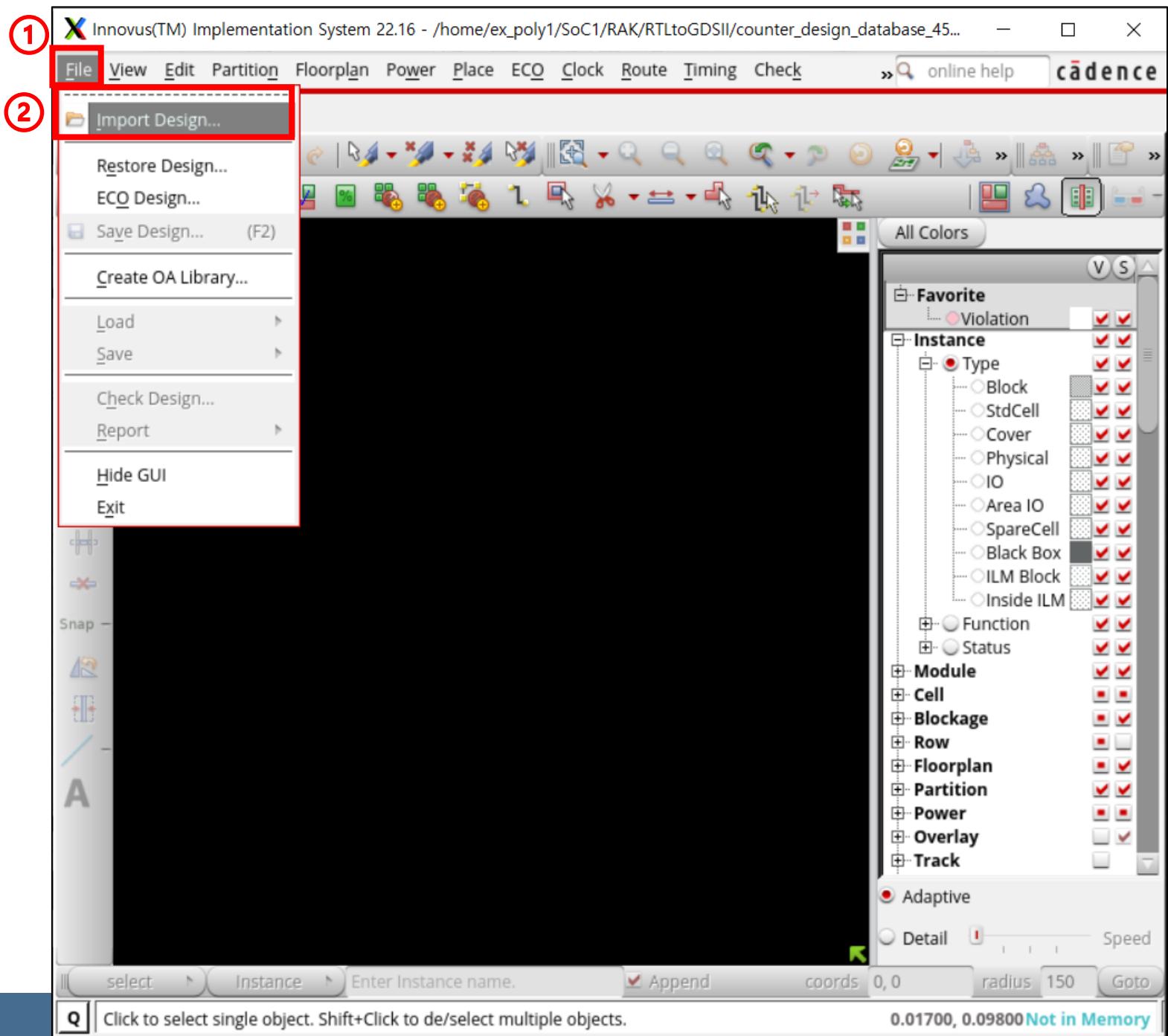


LAB

Auto PnR

Innovus

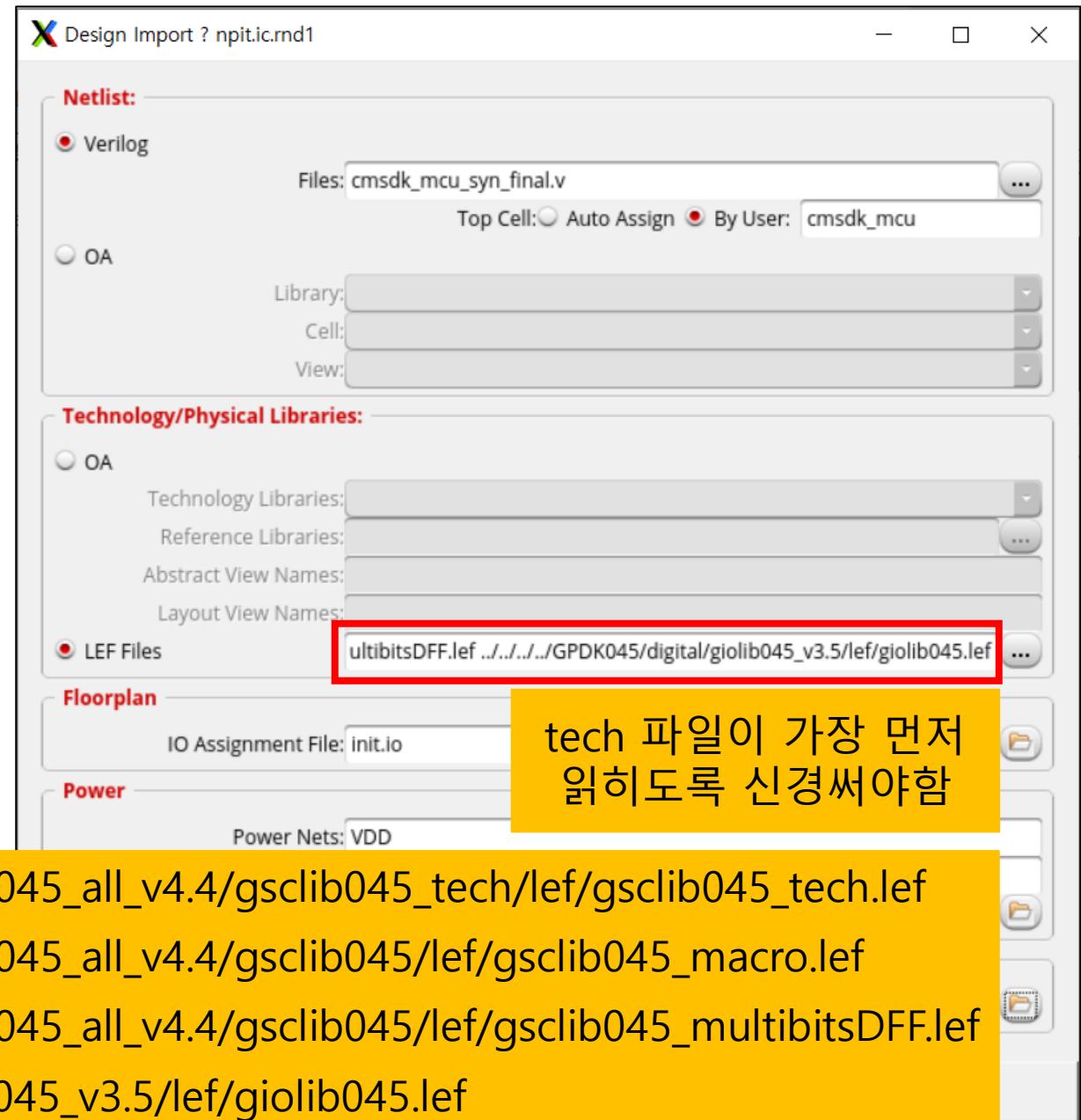
- **Import Design:** 준비된 디자인을 불러와서 진행함



Auto PnR

Innovus

- **Import Design:** 준비된 디자인을 불러와서 진행함
- 오른쪽과 같이 설정 후 OK 클릭

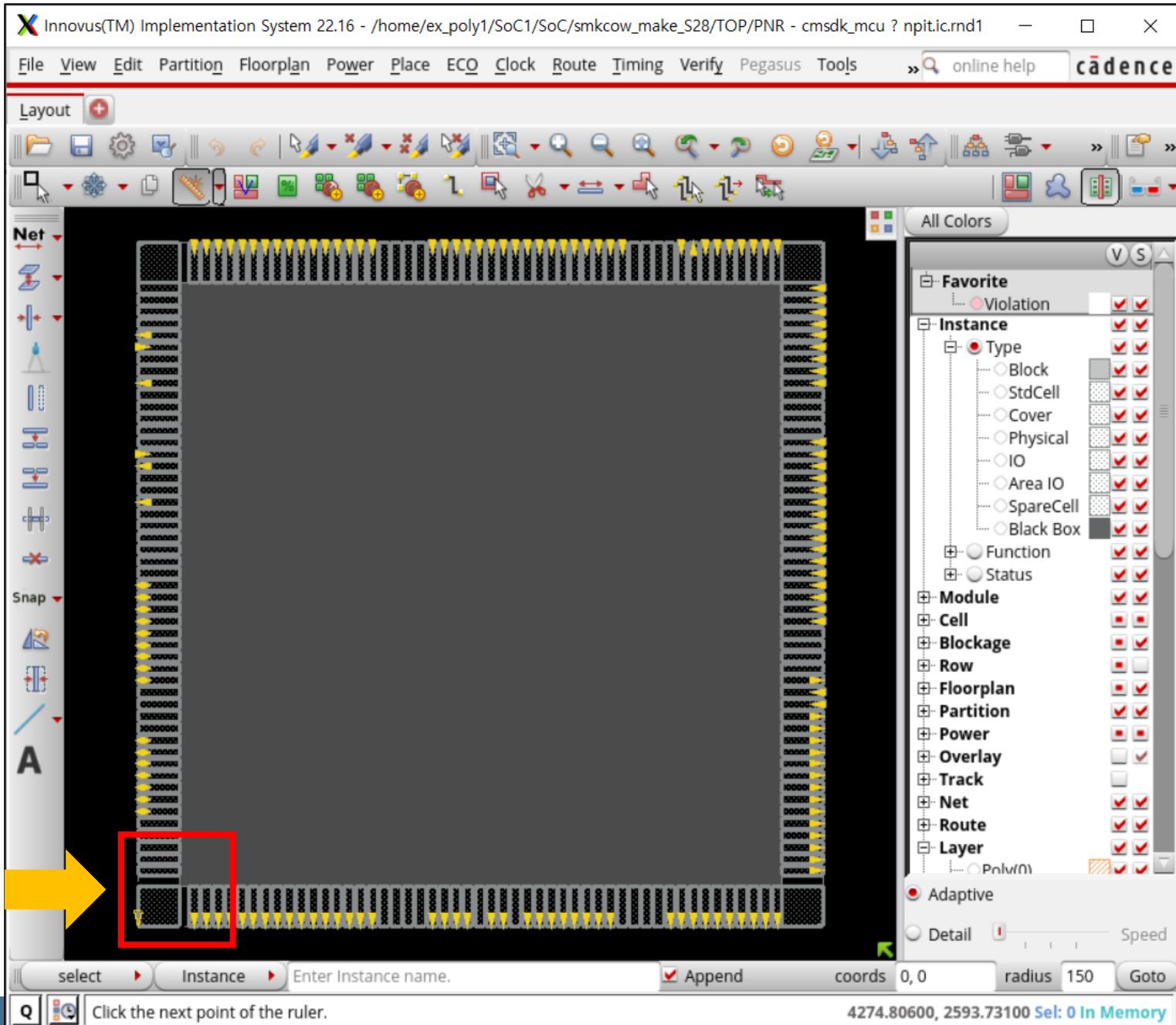


Auto PnR

Innovus

- 디자인이 잘 불러와졌는지 확인

마우스 우클릭
드래그 확대



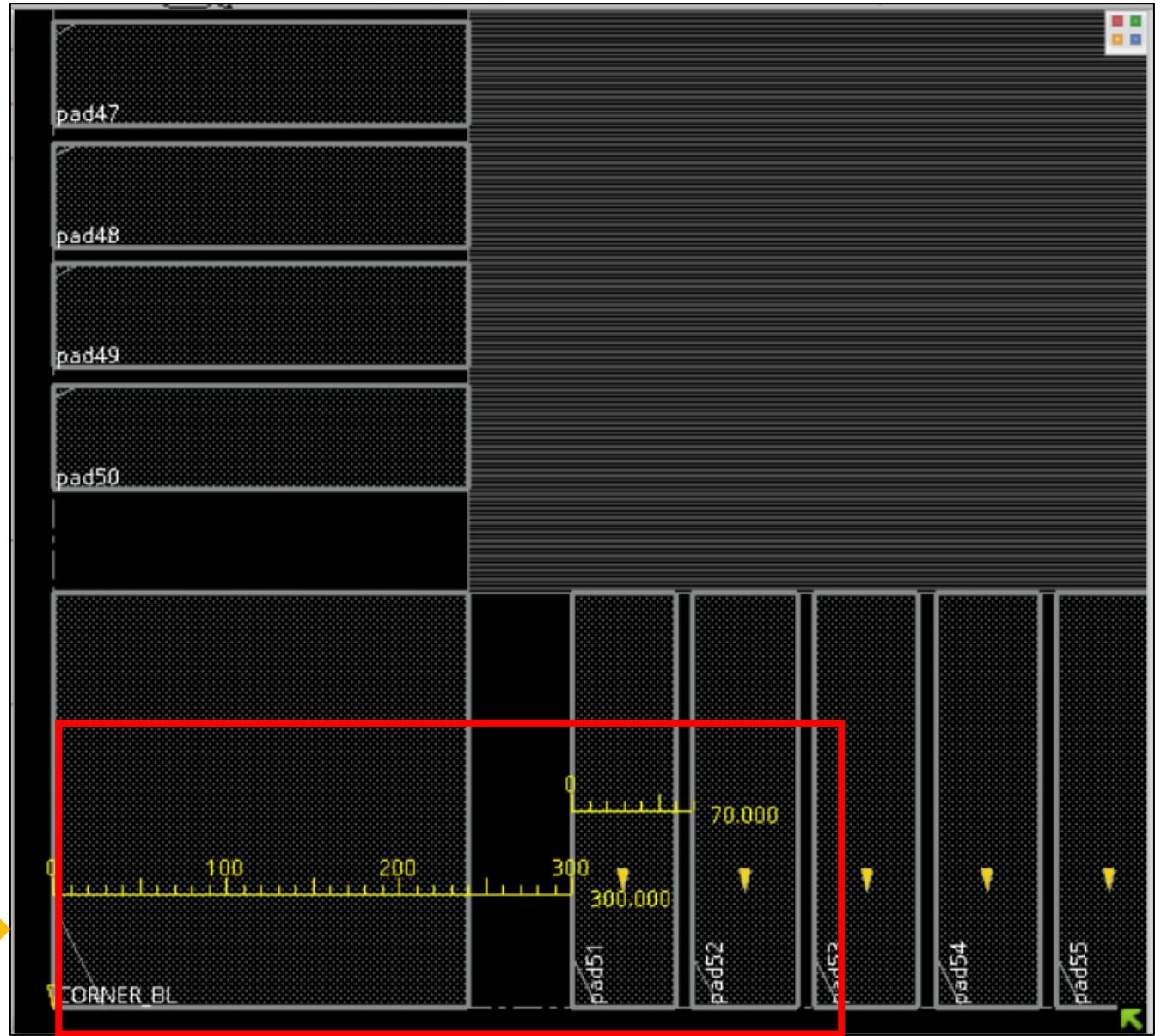
Auto PnR

Innovus

- 코너셀과 io셀의 크기, 간격 확인

```
offset=300 )  
offset=370 )  
offset=440 )  
offset=510 )  
offset=580 )  
offset=650 )  
offset=720 )  
offset=790 )  
offset=860 )  
offset=930 )  
offset=1000)  
offset=1070)
```

init.io에서 확인 했던
offset 값과 같음을 확인



Auto PnR

Innovus

\$>vi ../../..../GPDK045/digital/giolib045_v3.5/lef/giolib045.lef

- io셀의 세부 사항을 확인하기 위해 나머지 터미널에서
giolib045.lef 파일 확인

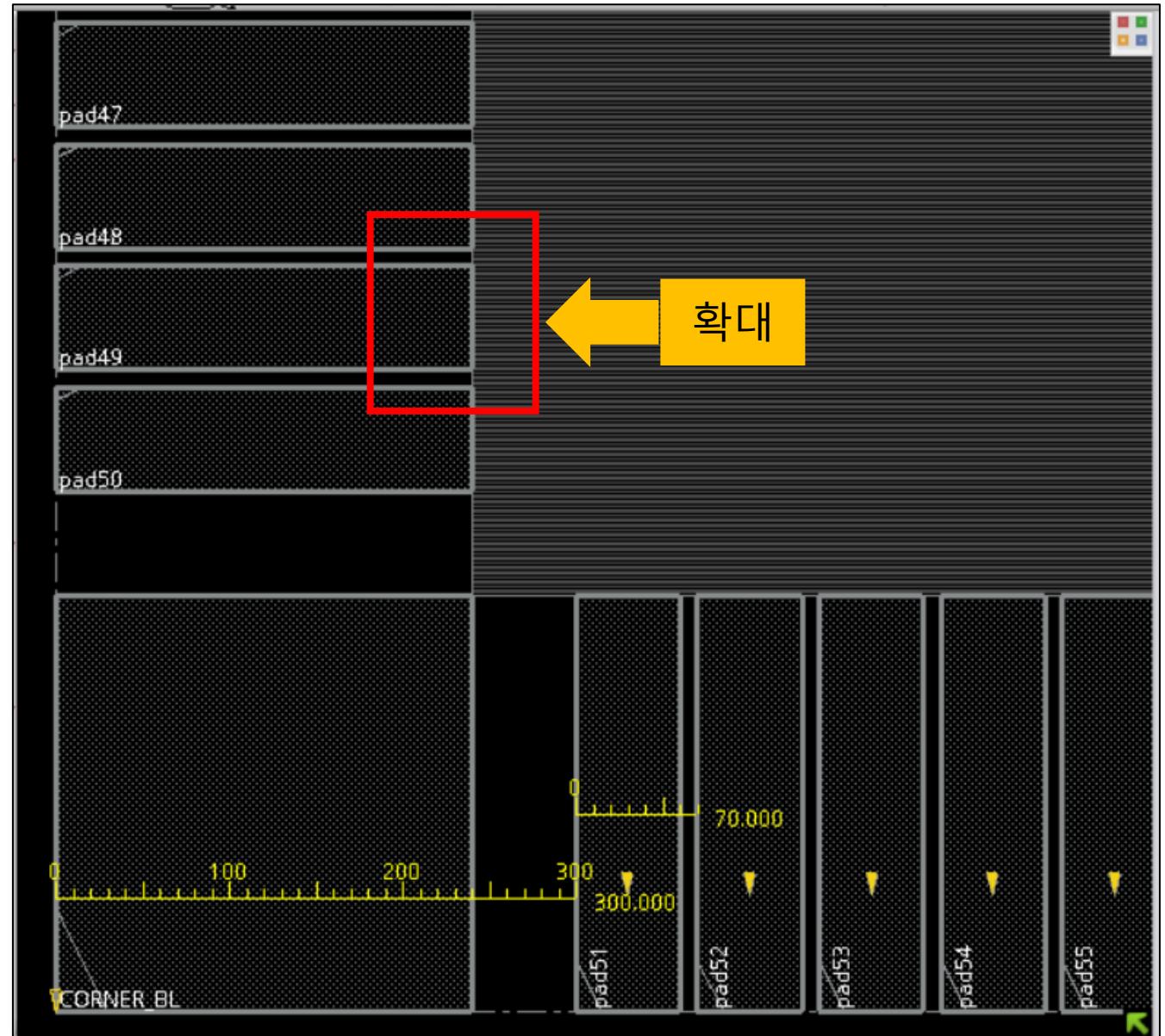
```
562 MACRO PADVDD
563 CLASS PAD ;
564 ORIGIN 0 80 ;
565 FOREIGN PADVDD 0 -80 ;
566 SIZE 60 BY 240 ; SIZE 60 BY 240 ;
567 SYMMETRY X Y R90 ;
568 SITE IOSite ;
569 PIN VDD
570 DIRECTION INOUT ;
571 USE POWER ;
572 NETEXPR "VDD VDD!" ;
573 PORT
574 LAYER Metal3 ;
575 RECT 53.815 156.64 57.165 160 ;
576 LAYER Metal2 ;
577 RECT 53.815 156.64 57.165 160 ;
578 LAYER Metal3 ;
579 RECT 2.855 156.64 6.205 160 ;
580 LAYER Metal2 ;
581 RECT 2.855 156.64 6.205 160 ;
582 END
```

io셀의 사이즈가 가로60,
세로240임을 알 수 있음

Auto PnR

Innovus

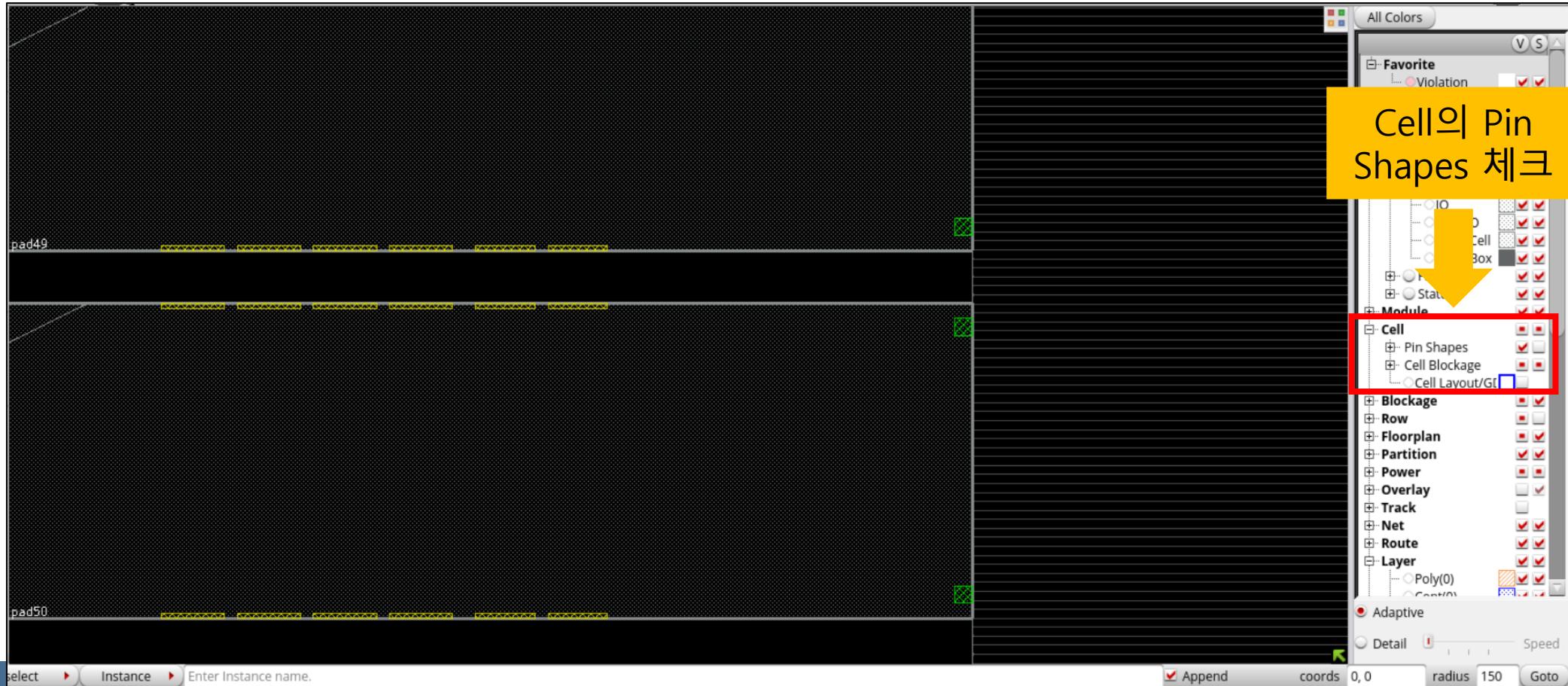
- io셀의 핀 확인



Auto PnR

Innovus

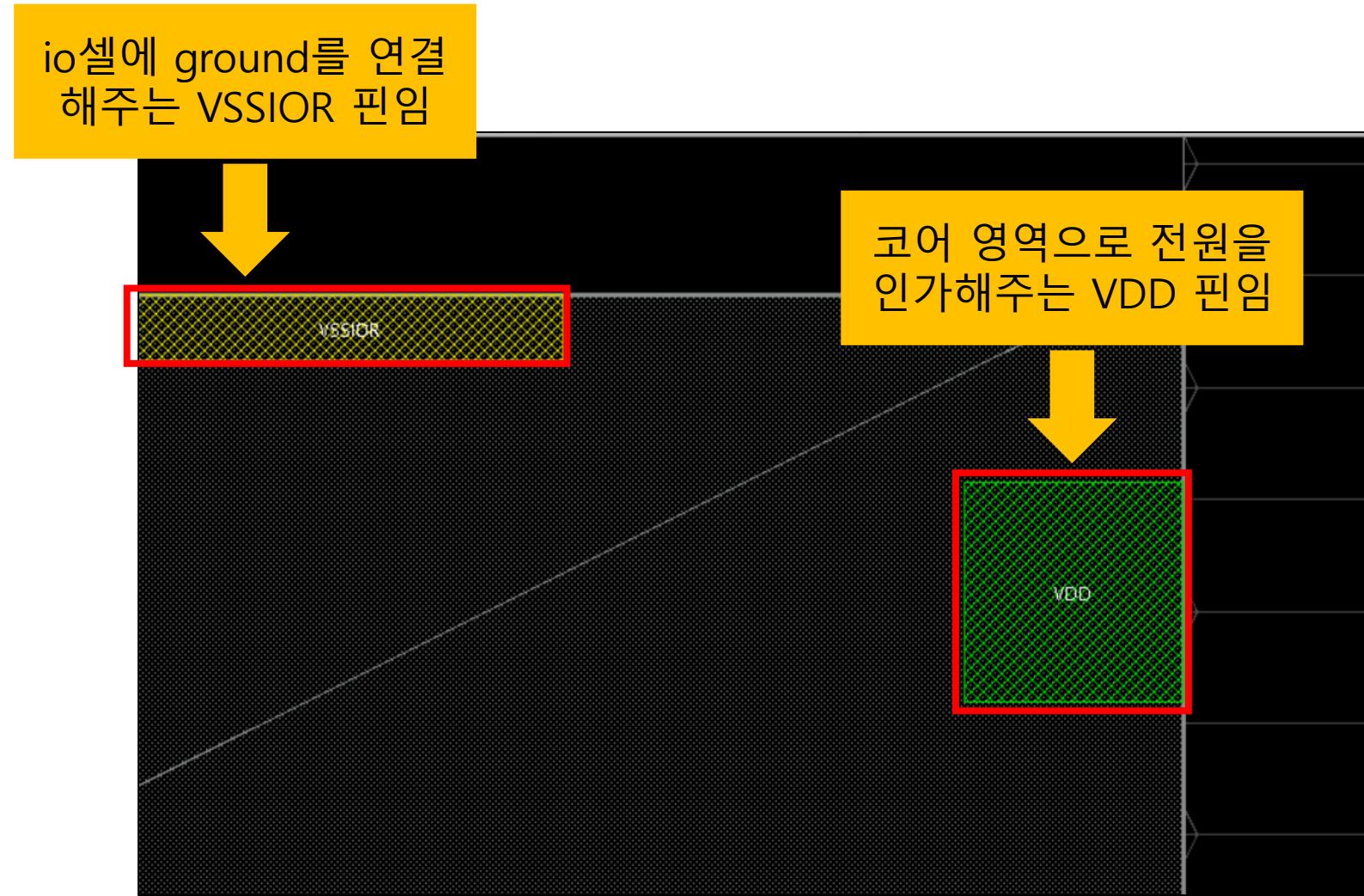
- io셀의 핀 확인



Auto PnR

Innovus

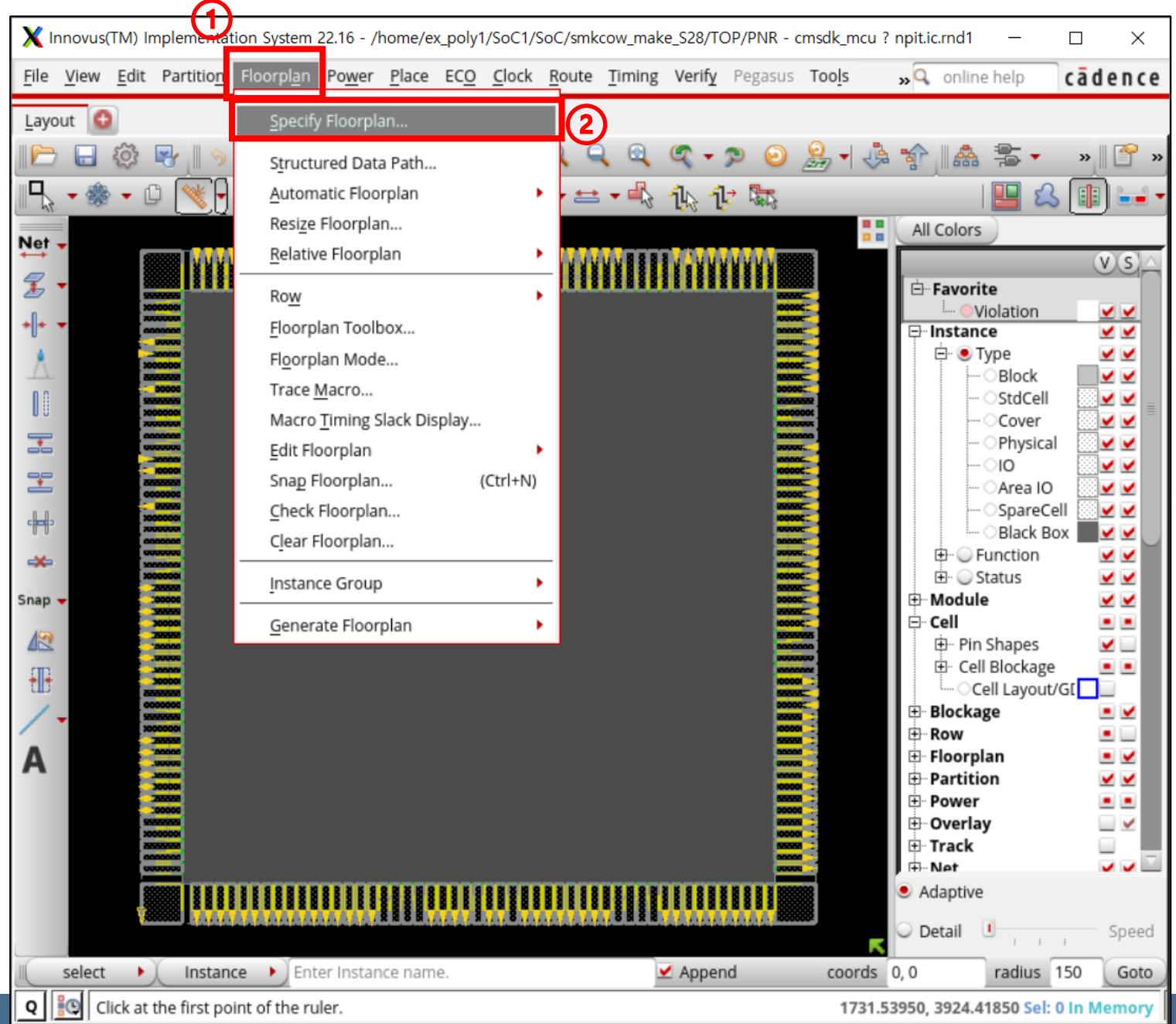
- io셀의 핀 확인



Auto PnR

Innovus

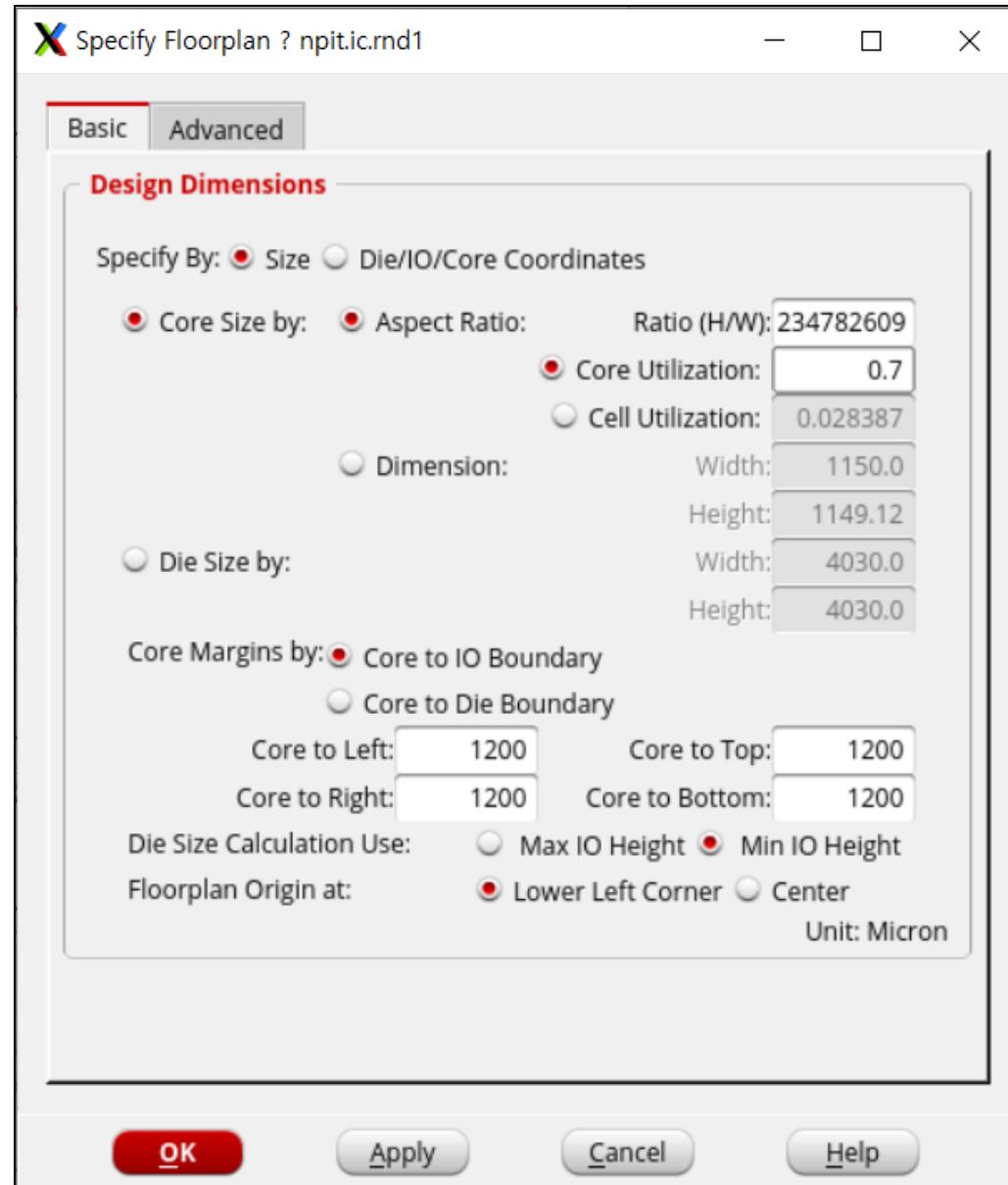
- **FloorPlan**



Auto PnR

Innovus

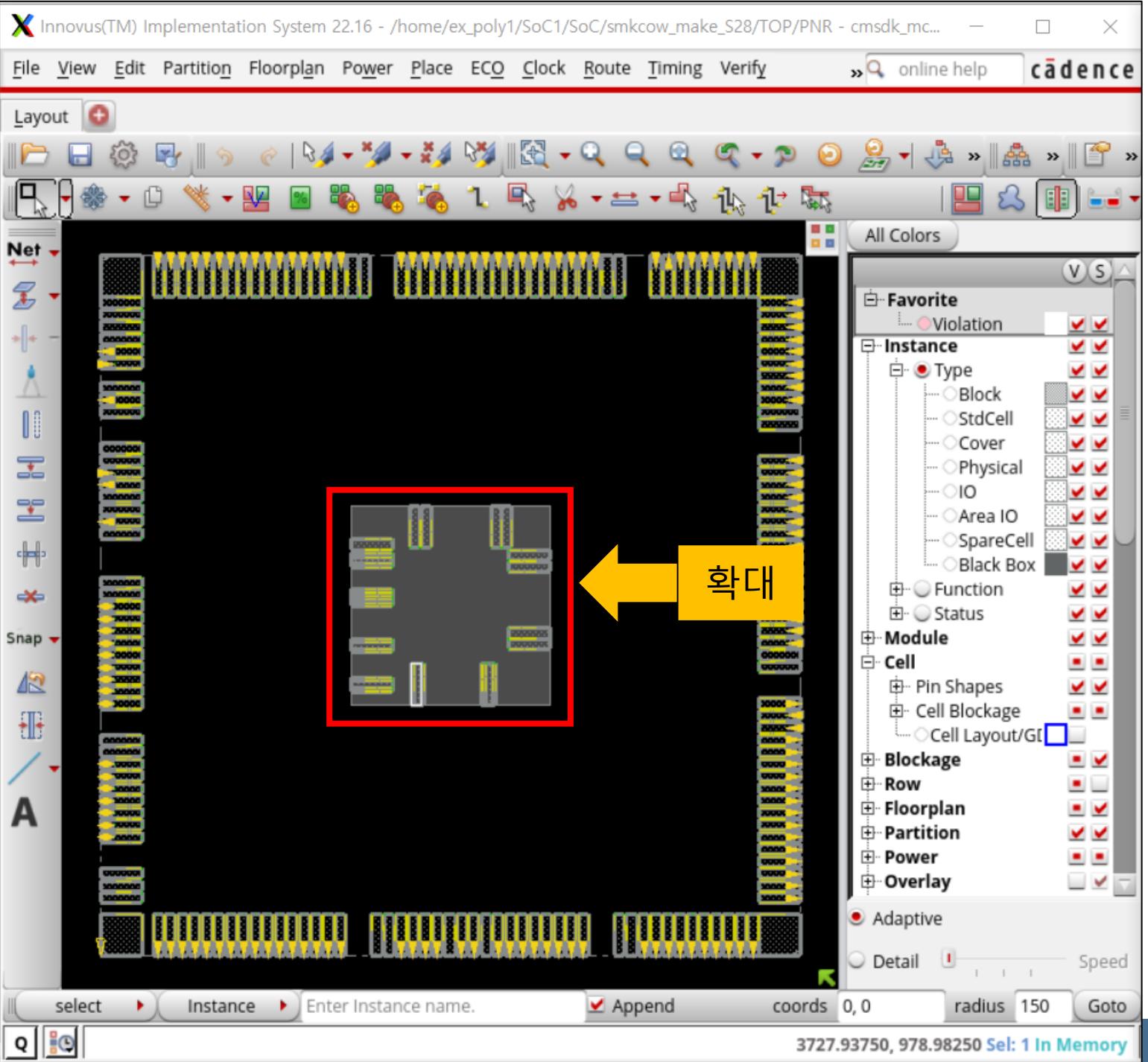
- **FloorPlan**
- 오른쪽과 같이 설정 후 Apply 클릭



Auto PnR

Innovus

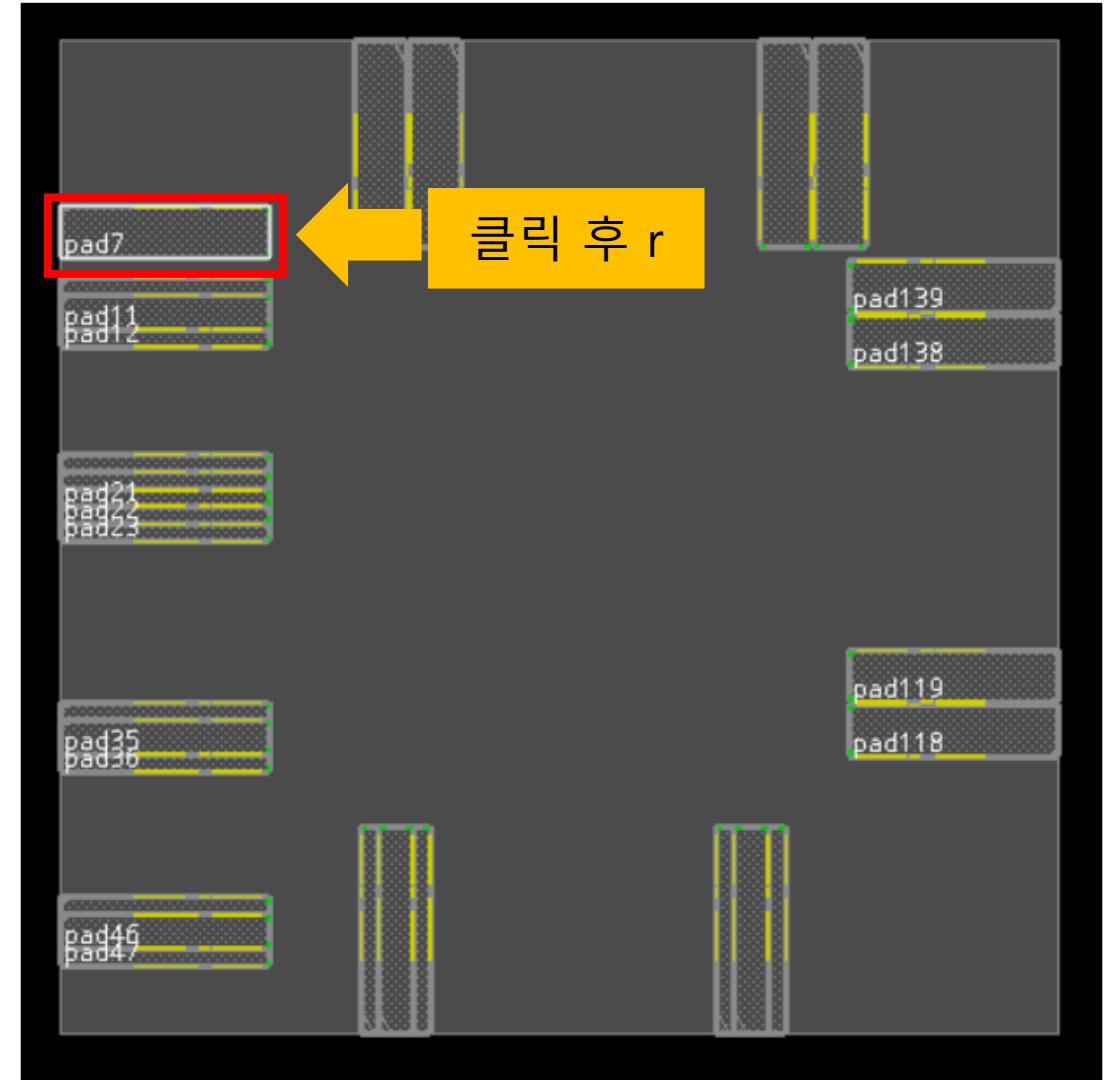
- FloorPlan
- 코어영역이 설정에 맞게 배치된 것을 확인



Auto PnR

Innovus

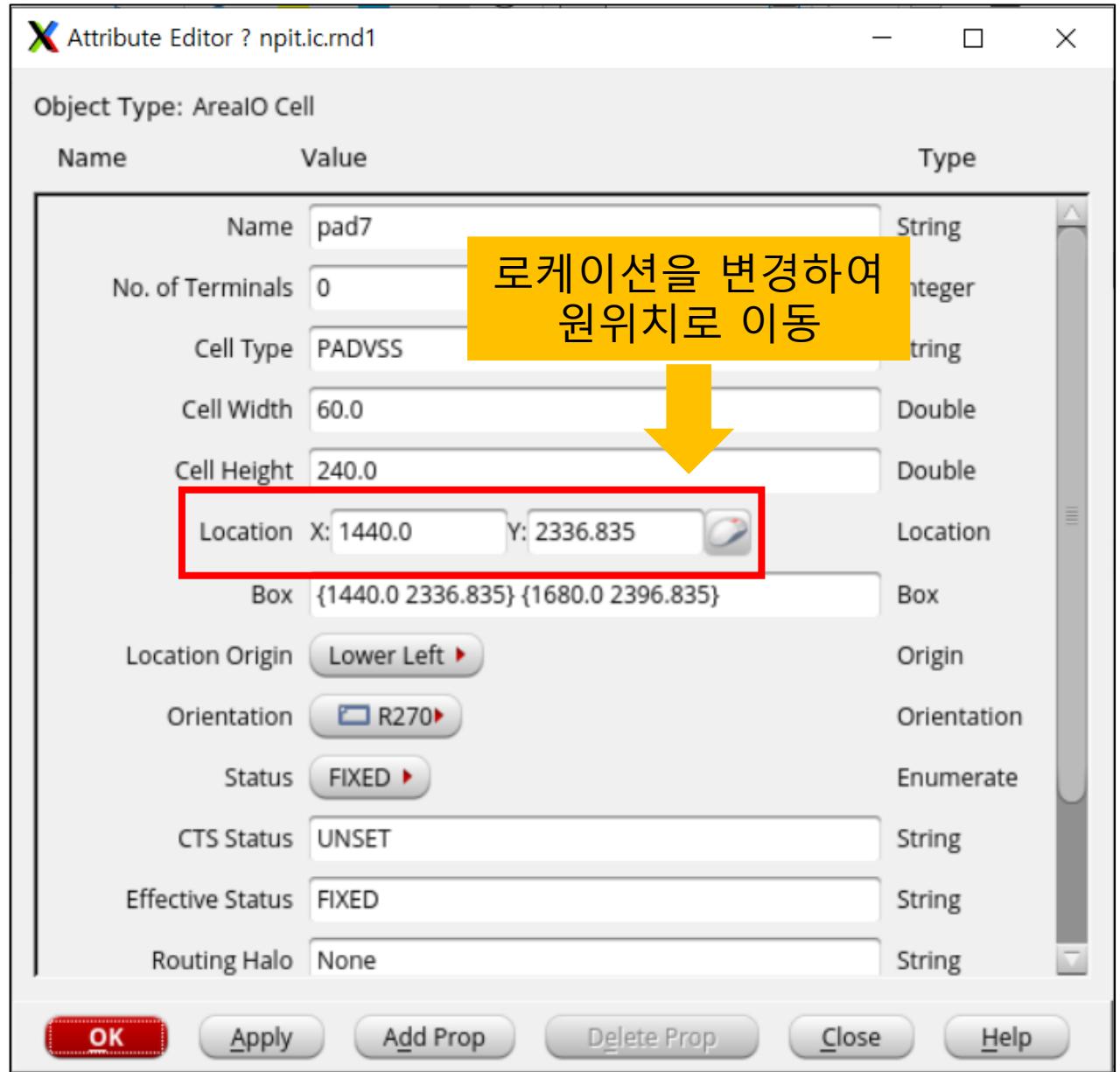
- **FloorPlan**
- floorplan 과정에서 pad들이 코어 영역으로 들어온 것을 볼 수 있음



Auto PnR

Innovus

- **FloorPlan**
- 나머지 터미널에서 init.io 파일을 vi하여 offset값 확인



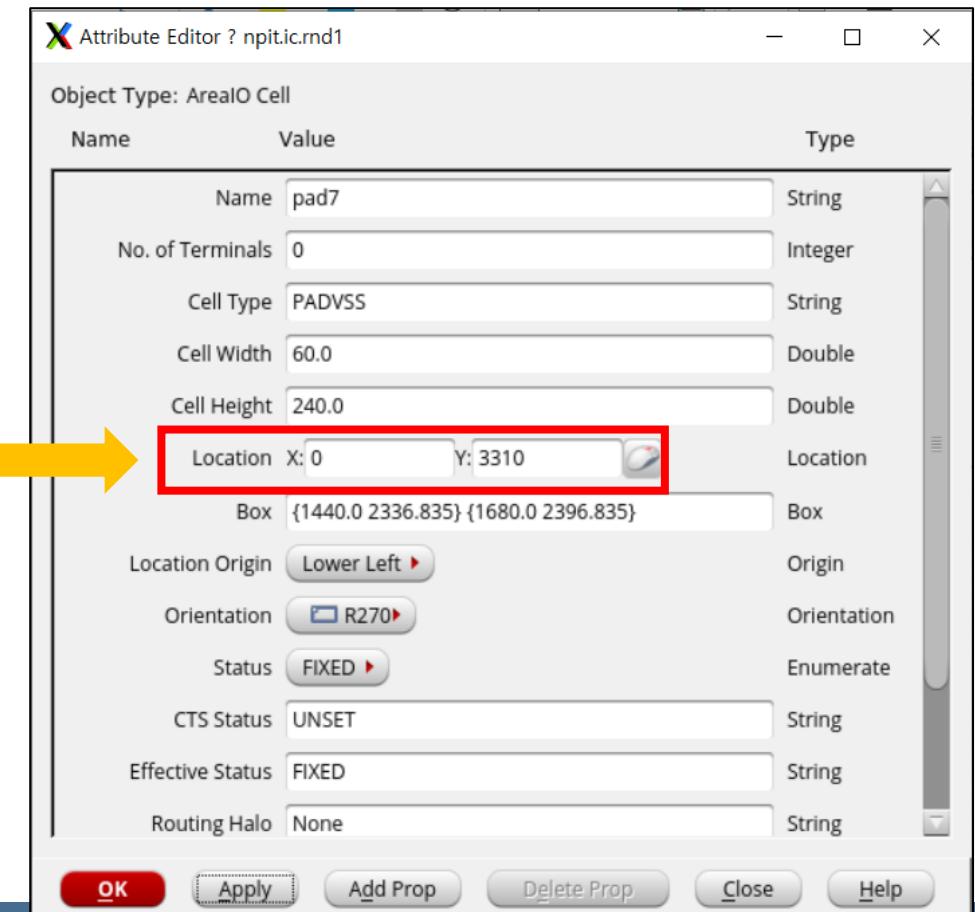
Auto PnR

Innovus

- FloorPlan
- 나머지 터미널에서 init.io 파일을 vi하여 offset값 확인

```
ex_poly1@npit:PNR
File Edit View Search Terminal Help
35      (inst name="pad22"      cell="PADVDD"      offset=2260)
36      (inst name="pad21"      cell="PADVDD"      offset=2330)
37      (inst name="pad20"      cell="PADVSSIOR"   offset=2400)
38      (inst name="pad19"      cell="PADD0"       offset=2470)
39      (inst name="pad18"      cell="PADVSSIOR"   offset=2540)
40      (inst name="pad17"      cell="PADVSSIOR"   offset=2610)
41      (inst name="pad16"      cell="PADD0"       offset=2680)
42      (inst name="pad15"      cell="PADDI"        offset=2750)
43      (inst name="pad14"      cell="PADVSSIOR"   offset=2820)
44      (inst name="pad13"      cell="PADVDDIOR"   offset=2890)
45      (inst name="pad12"      cell="PADVSS"       offset=2960)
46      (inst name="pad11"      cell="PADVDD"       offset=3030)
47      (inst name="pad10"      cell="PADVSSIOR"   offset=3100)
48      (inst name="pad9"       cell="PADD0"       offset=3170)
49      (inst name="pad8"       cell="PADVSSTOR"   offset=3240)
50      (inst name="pad7"       cell="PADVSS"       offset=3310)
51      (inst name="pad6"       cell="PADD1"       offset=3380)
52      (inst name="pad5"       cell="PADD0"       offset=3450)
53      (inst name="pad4"       cell="PADVDDIOR"   offset=3520)
54      (inst name="pad3"       cell="PADVDDIOR"   offset=3590)
55      (inst name="pad2"       cell="PADVSSIOR"   offset=3660)
56      (inst name="pad1"       cell="PADVDDIOR"   offset=3730)
57 )
58 (topleft
:set nu
58,1          16%
```

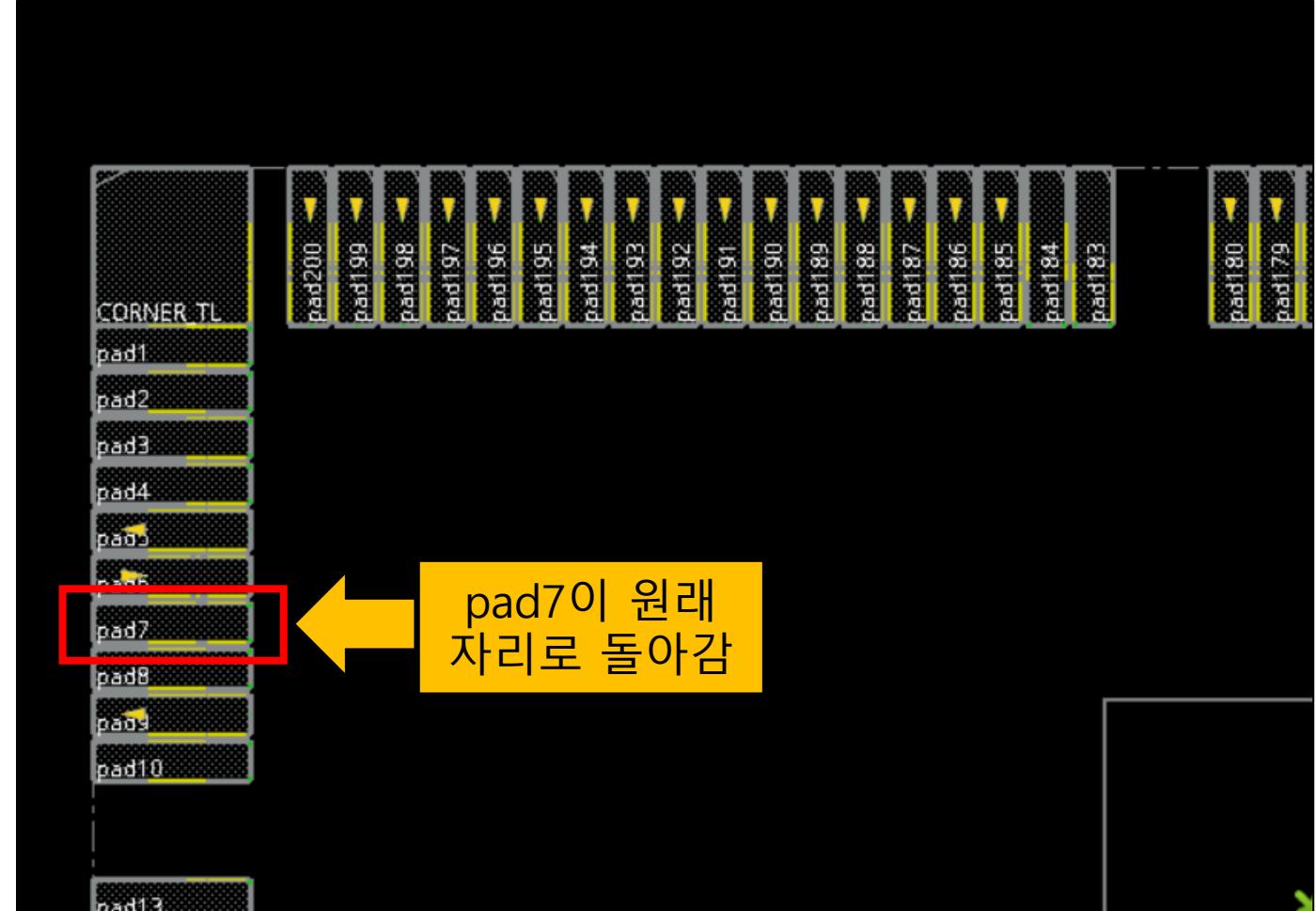
pad7의 offset값
3310 확인 후 입력



Auto PnR

Innovus

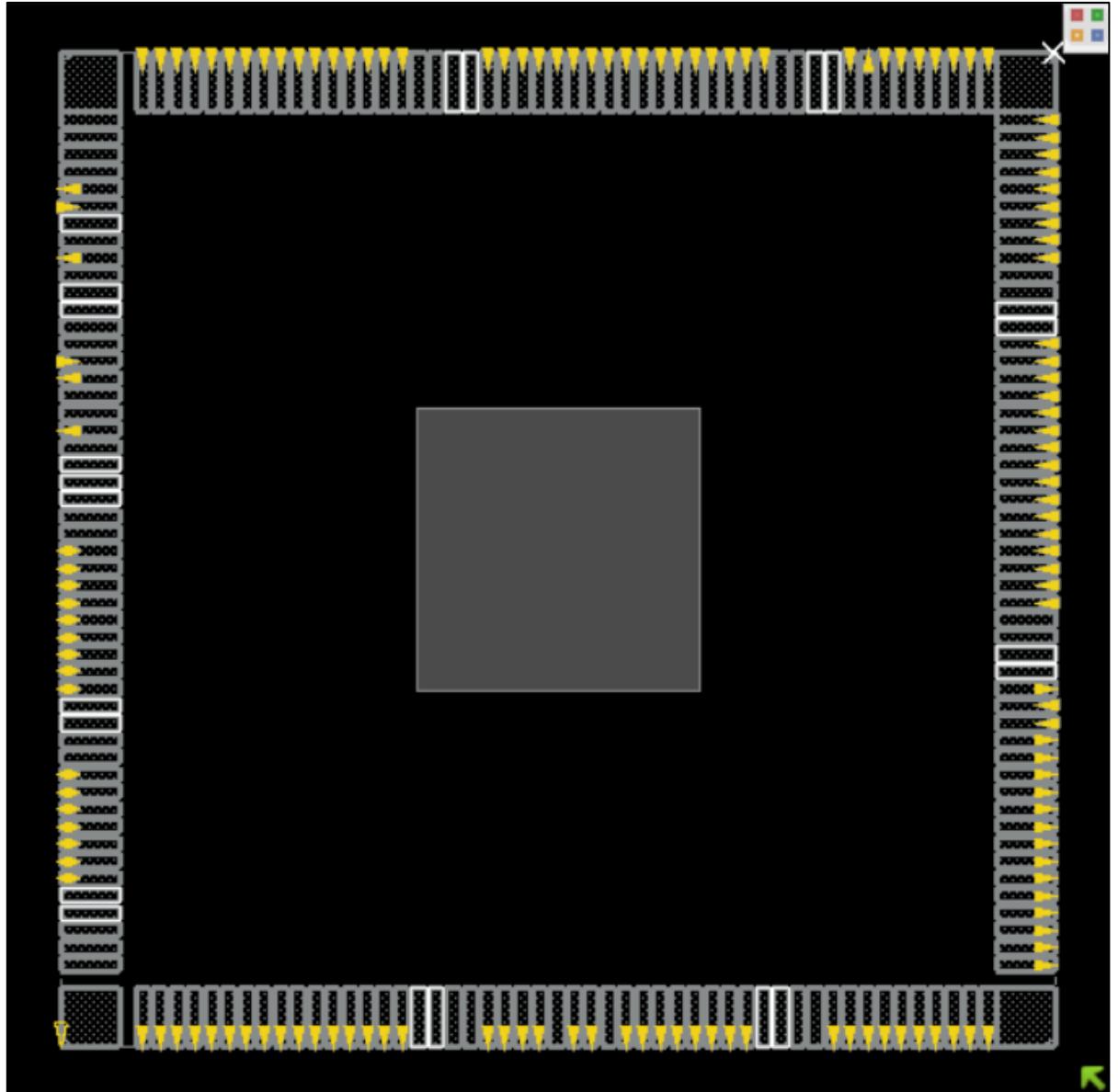
- FloorPlan
- 같은 방식으로 나머지 pad도 진행



Auto PnR

Innovus

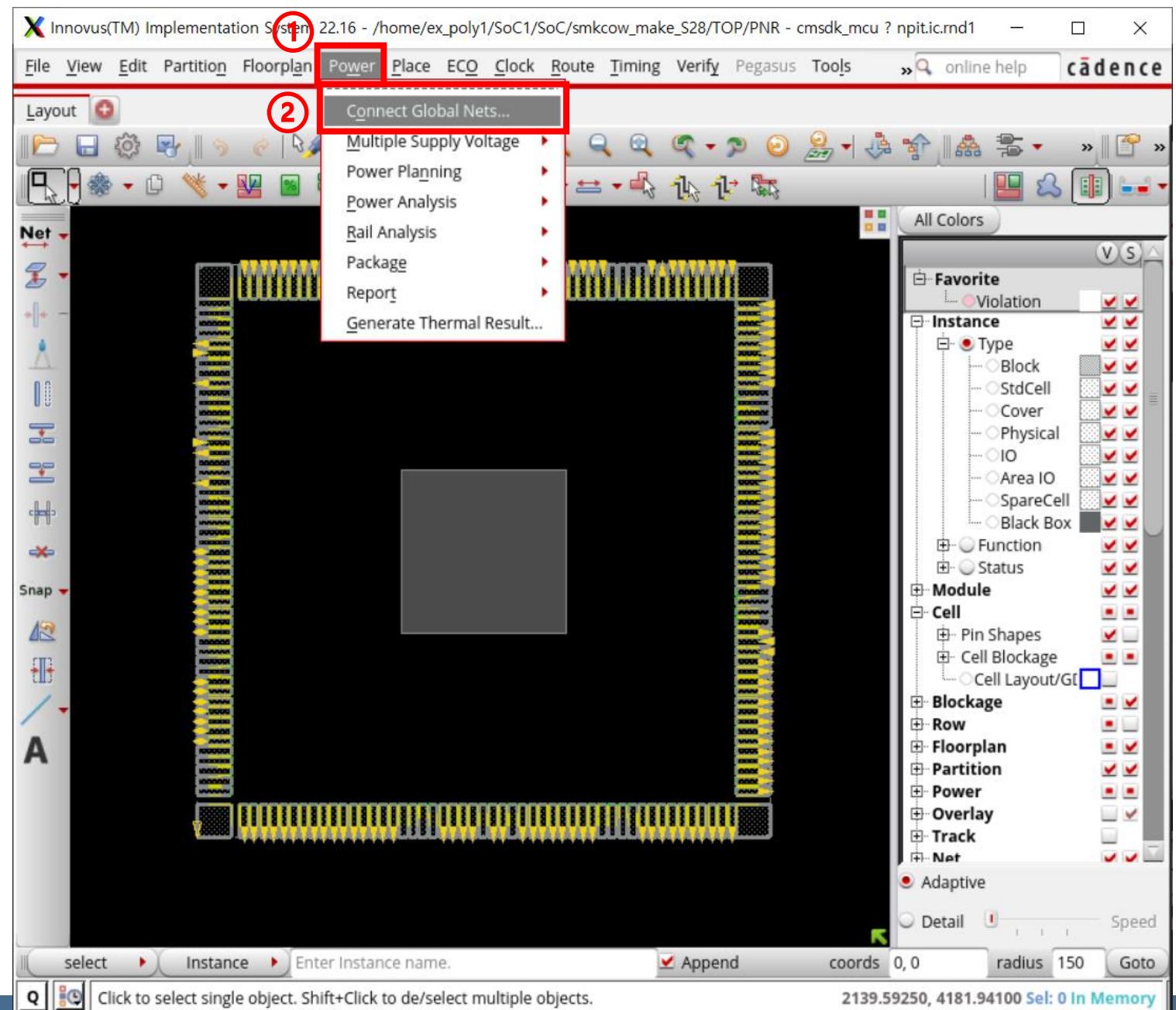
- **FloorPlan**
- 전부 제자리로 옮긴 것을 확인함



Auto PnR

Innovus

- **Connect Global Nets:** powerplan을 진행하기 전 Pin과 Net을 연결해주는 과정임

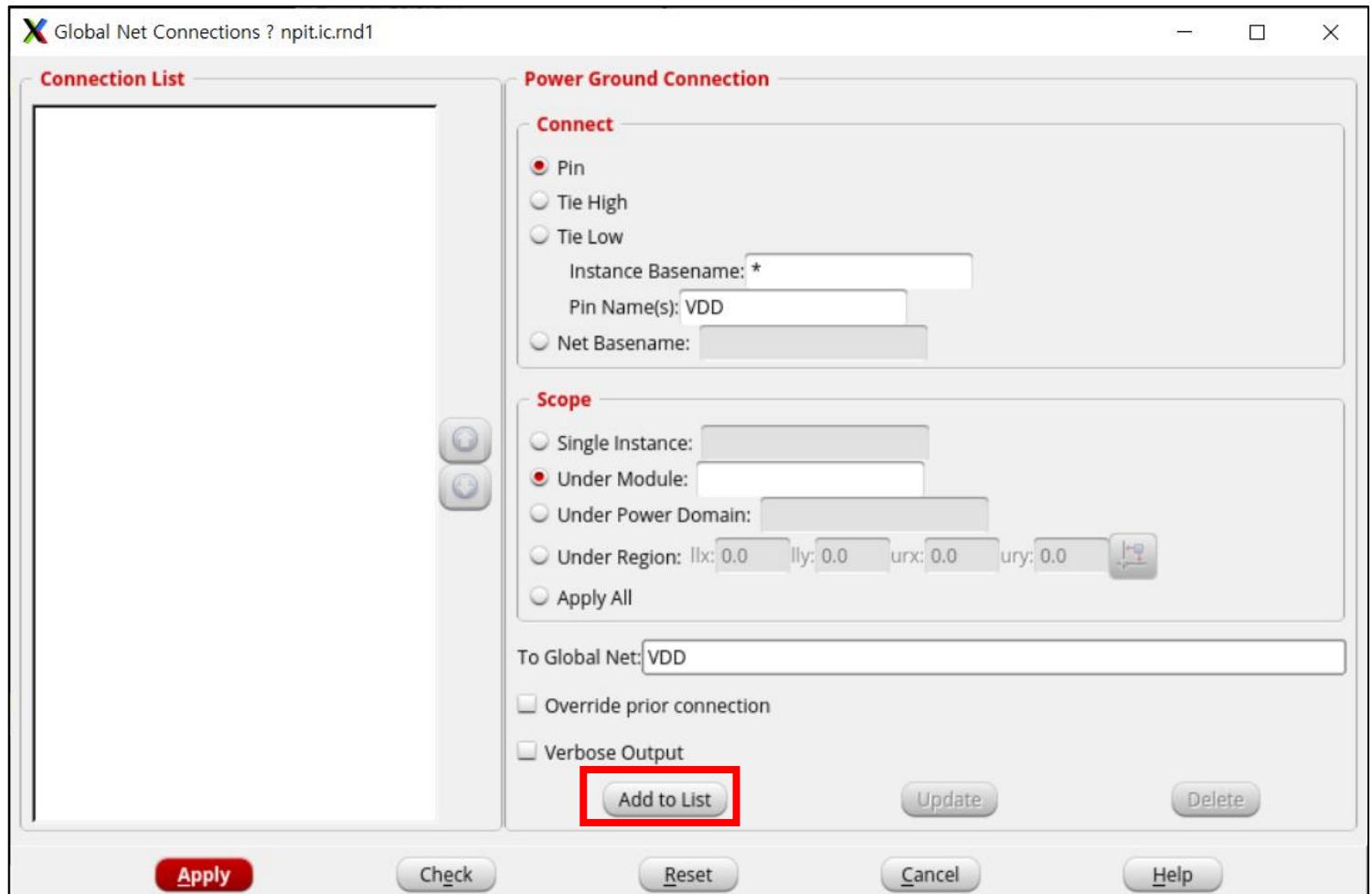


Auto PnR

Innovus

VDD pin과 VDD net을 연결함

- **Connect Global Nets:** powerplan을 진행하기 전 Pin과 Net을 연결해주는 과정임
- 오른쪽과 같이 설정 후 Add to List 클릭

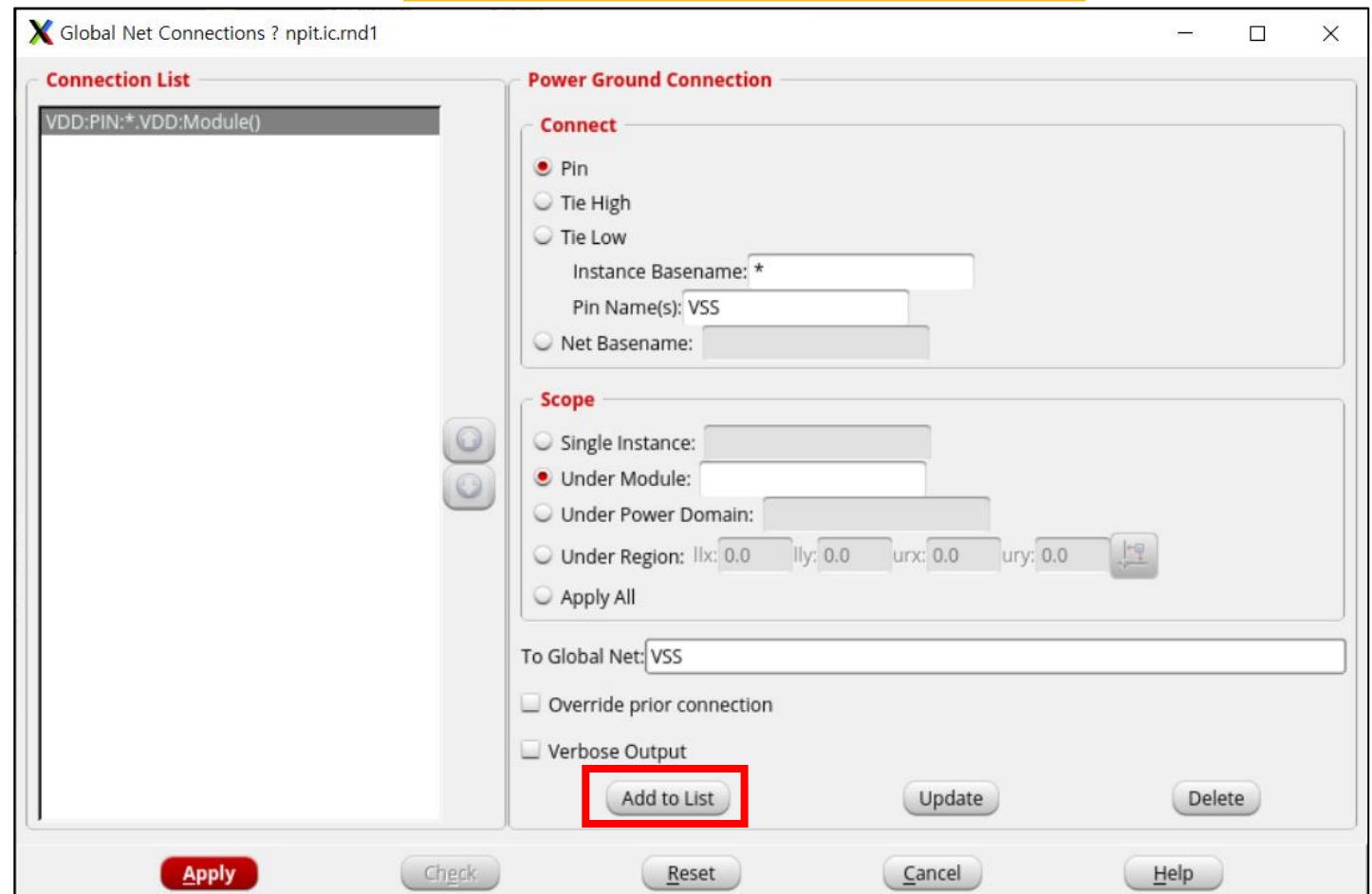


Auto PnR

Innovus

VSS pin과 VSS net을 연결함

- **Connect Global Nets:** powerplan을 진행하기 전 Pin과 Net을 연결해주는 과정임
- 오른쪽과 같이 설정 후 Add to List 클릭

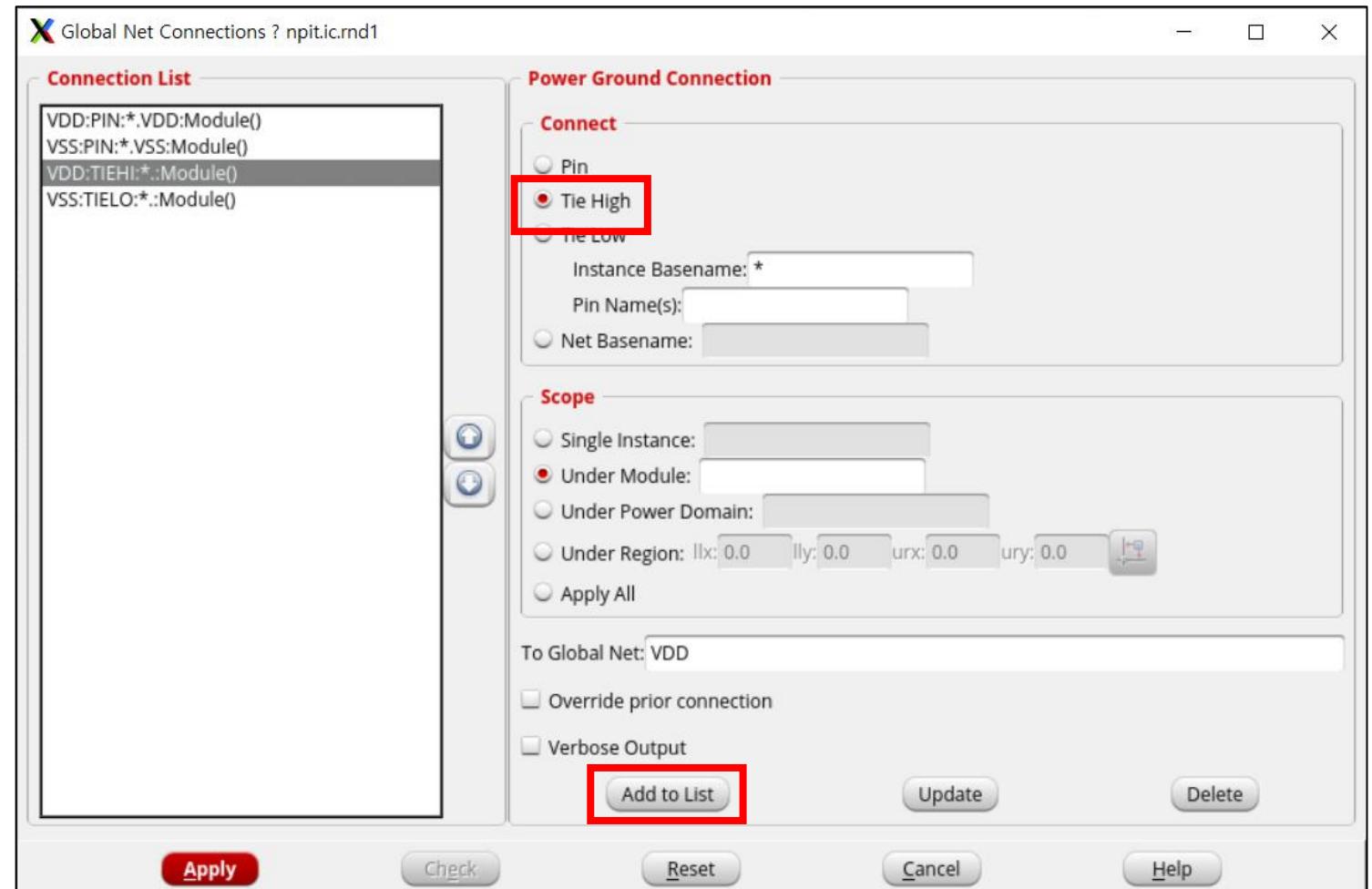


Auto PnR

Innovus

VDD net과 high의 값을 필요로 하는 곳을 연결함

- **Connect Global Nets:** powerplan을 진행하기 전 Pin과 Net을 연결해주는 과정임
- 오른쪽과 같이 설정 후 Add to List 클릭

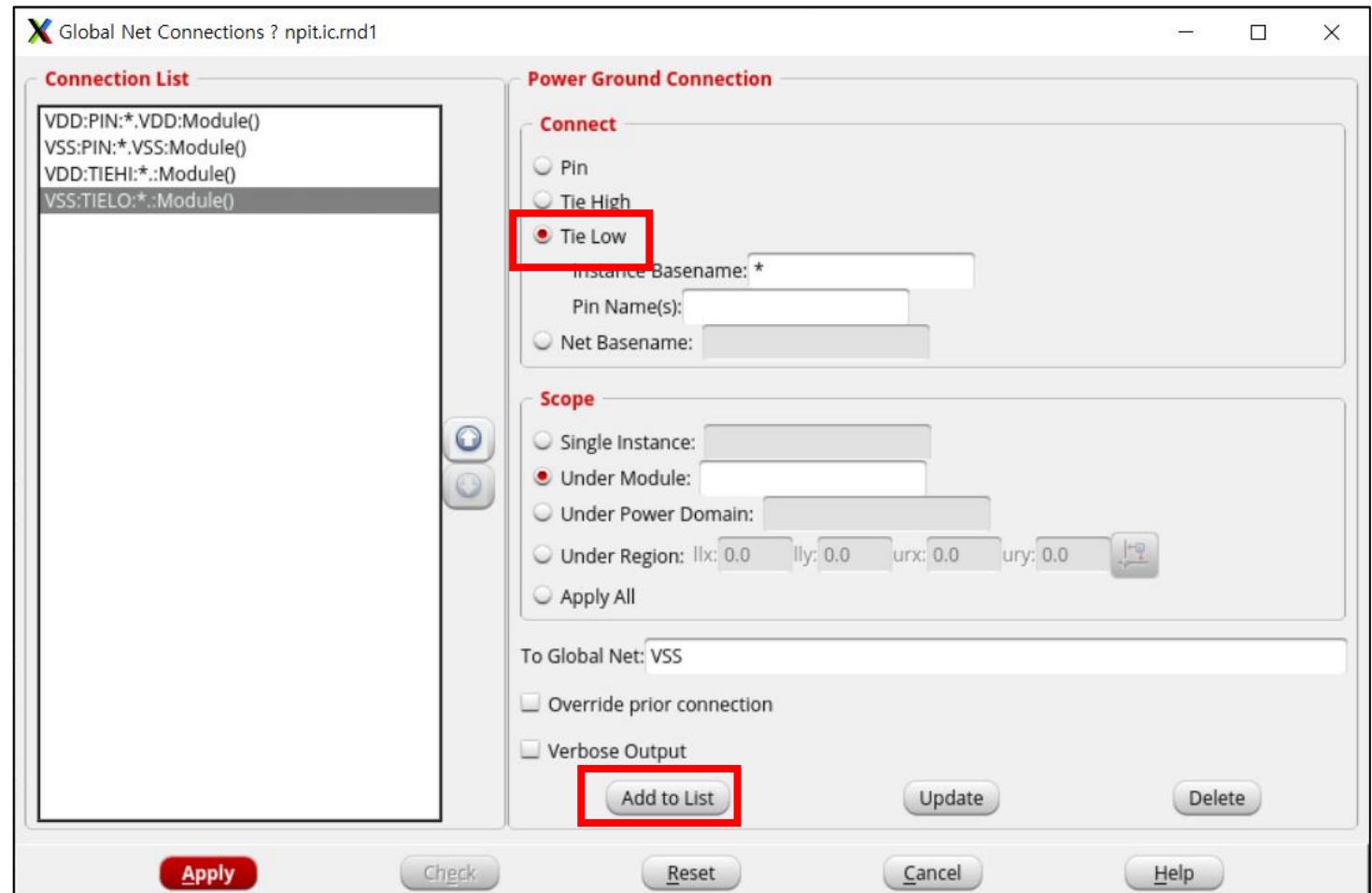


Auto PnR

Innovus

VSS net과 low의 값을 필요로 하는 곳을 연결함

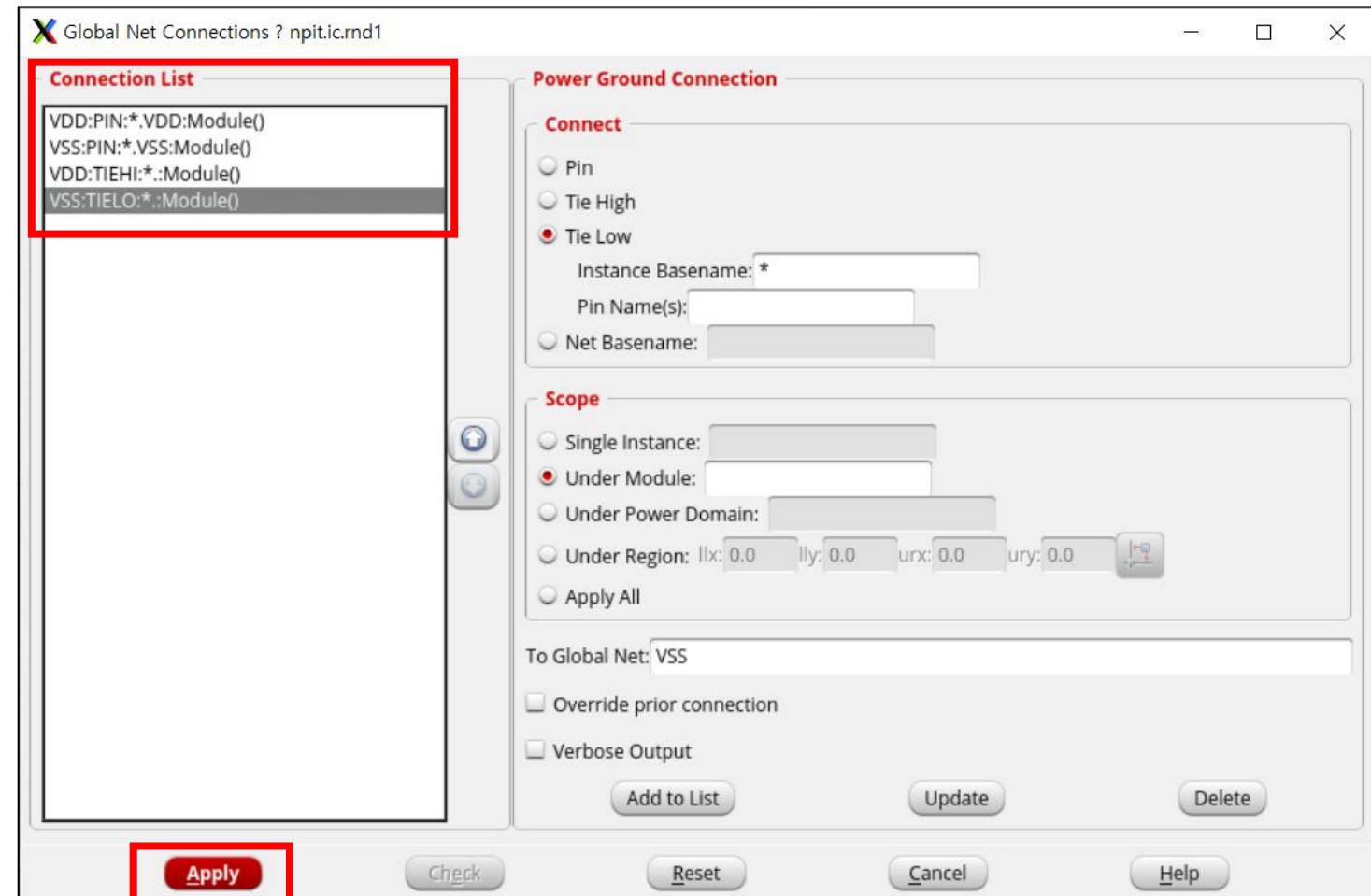
- **Connect Global Nets:** powerplan을 진행하기 전 Pin과 Net을 연결해주는 과정임
- 오른쪽과 같이 설정 후 Add to List 클릭



Auto PnR

Innovus

- **Connect Global Nets:** powerplan을 진행하기 전 Pin과 Net을 연결해주는 과정임
- 리스트확인 후 Apply 클릭



Auto PnR

Innovus

- **Connect Global Nets:** powerplan을 진행하기 전 Pin과 Net을 연결해주는 과정임
- 터미널에 Warning이 발생함
- IO cell의 VSSIOR과 VDDIOR은 나중에 IO Filler로 연결되므로 무시해도 상관없음

```
Warning: pg term VSSIOR of inst CORNER_TL is not connect to global special net.  
Warning: pg term VDDIOR of inst CORNER_TL is not connect to global special net.  
Warning: pg term VSSIOR of inst CORNER_TR is not connect to global special net.  
Warning: pg term VDDIOR of inst CORNER_TR is not connect to global special net.  
Warning: pg term VSSIOR of inst CORNER_BR is not connect to global special net.  
Warning: pg term VDDIOR of inst CORNER_BR is not connect to global special net.  
Warning: pg term VSSIOR of inst CORNER_BL is not connect to global special net.  
Warning: pg term VDDIOR of inst CORNER_BL is not connect to global special net.
```

Auto PnR

Innovus

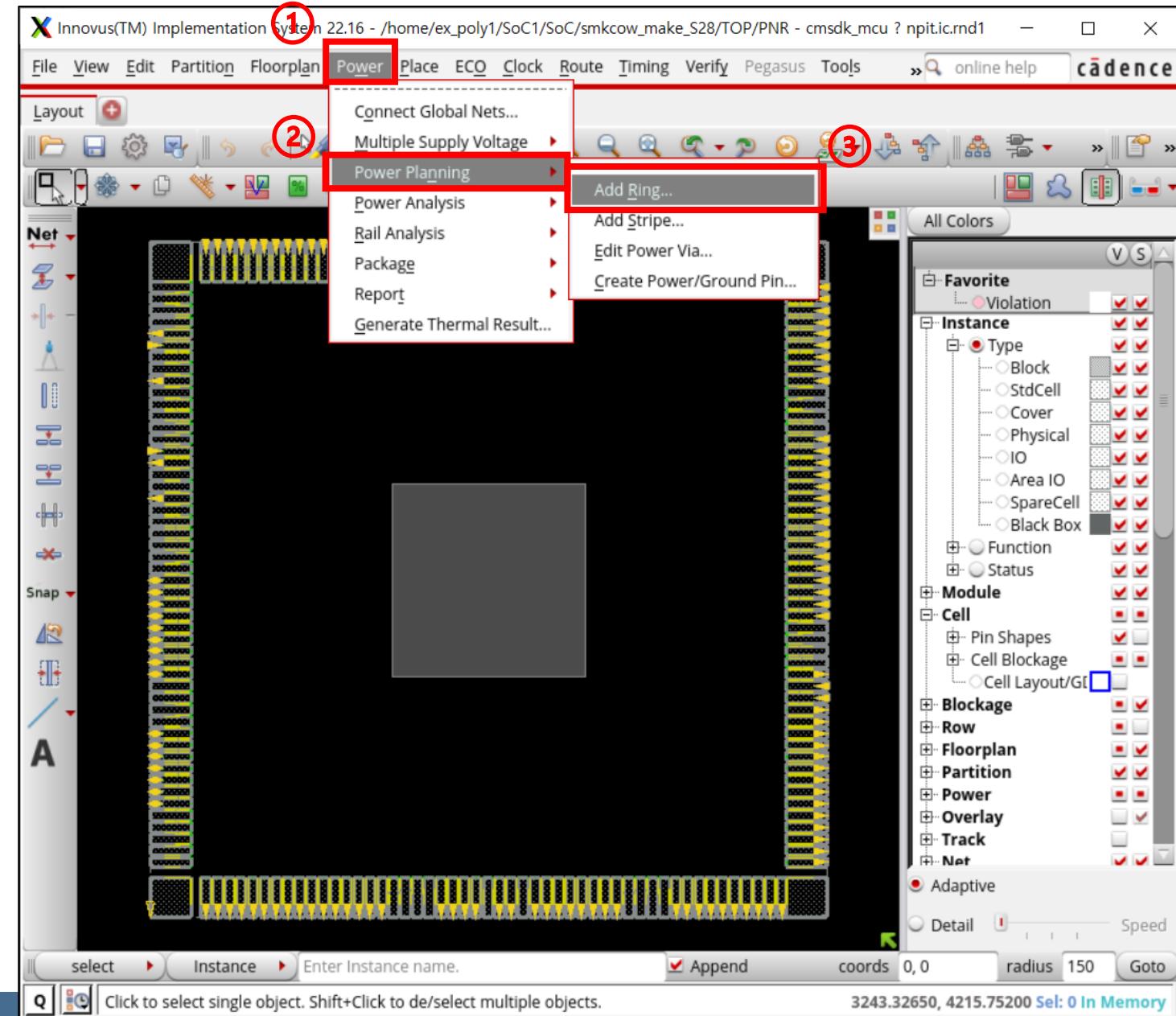
- **PowerPlan**
- powerplan은 배치해야할 라인이 많으므로 via가 원활하게 연결될 수 있도록 순서를 정해줌

core 주변 power ring 생성 → core영역 rail, stripe 연결 → IO주변 power ring 생성 → Core power ring, IO power ring
연결 순으로 진행함

Auto PnR

Innovus

- PowerPlan
- core 주변 power ring 생성

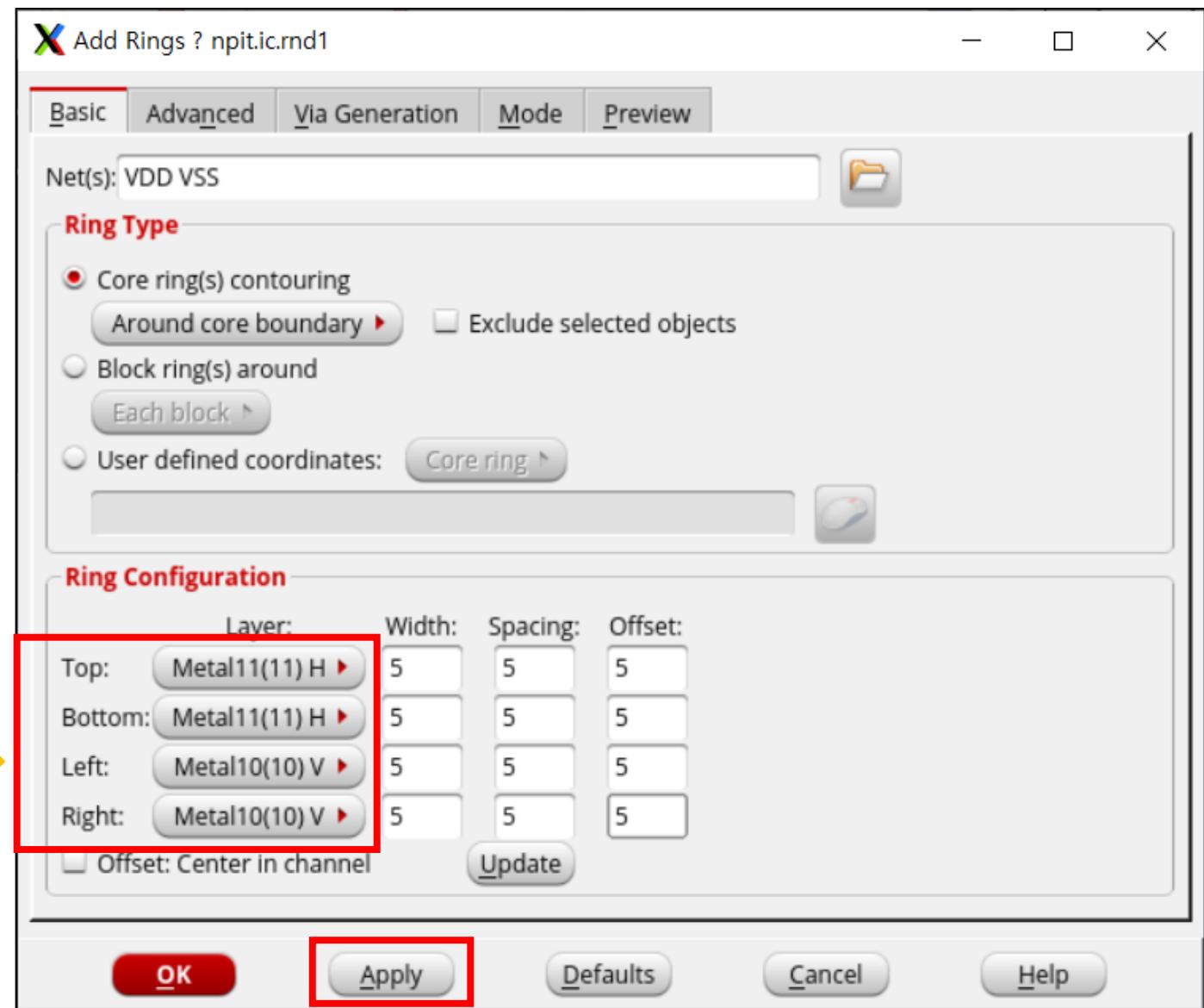


Auto PnR

Innovus

- **PowerPlan**
- core 주변 power ring 생성
- 오른쪽과 똑같이 설정 후 Apply

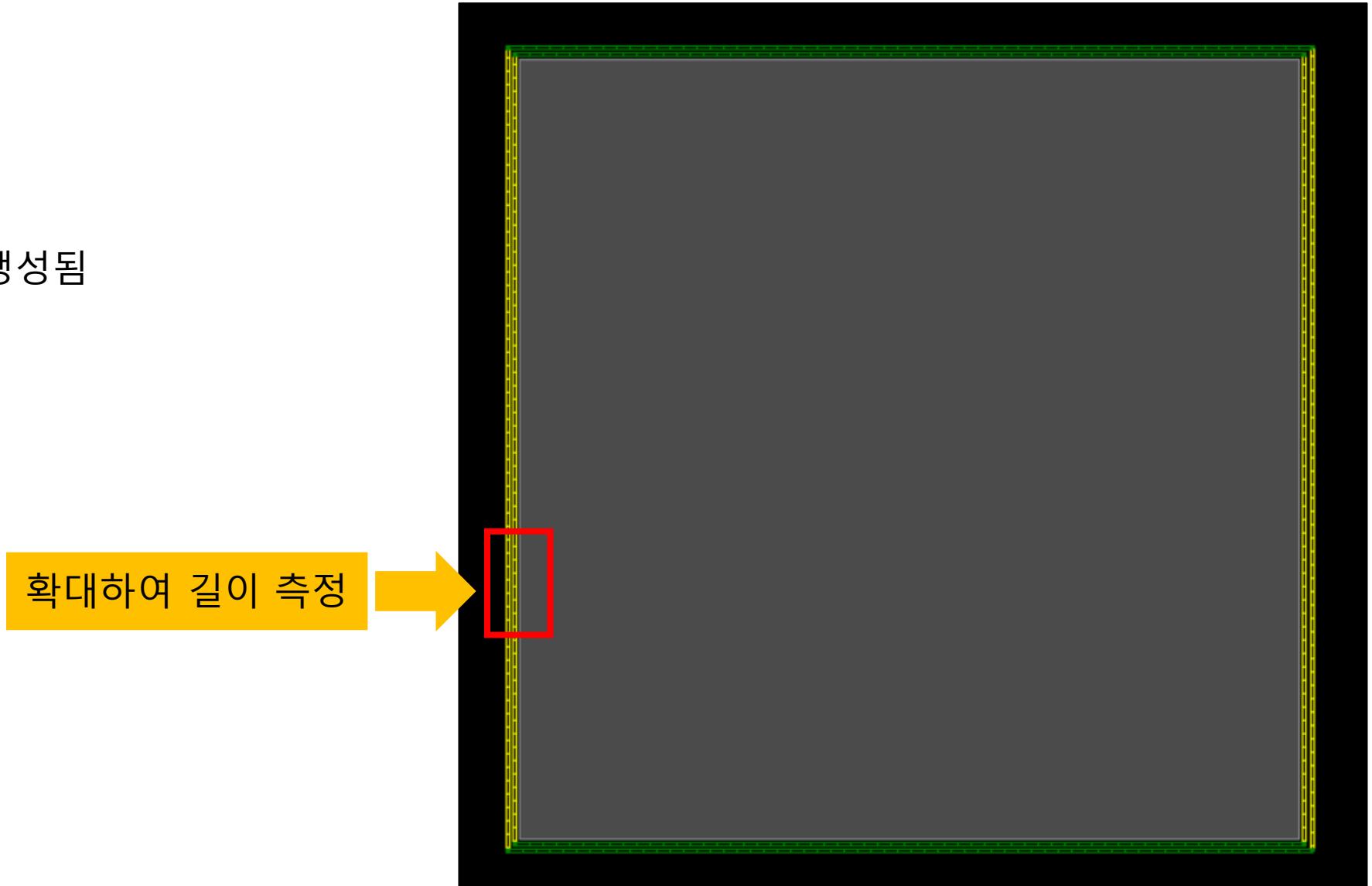
layer 설정에 주의



Auto PnR

Innovus

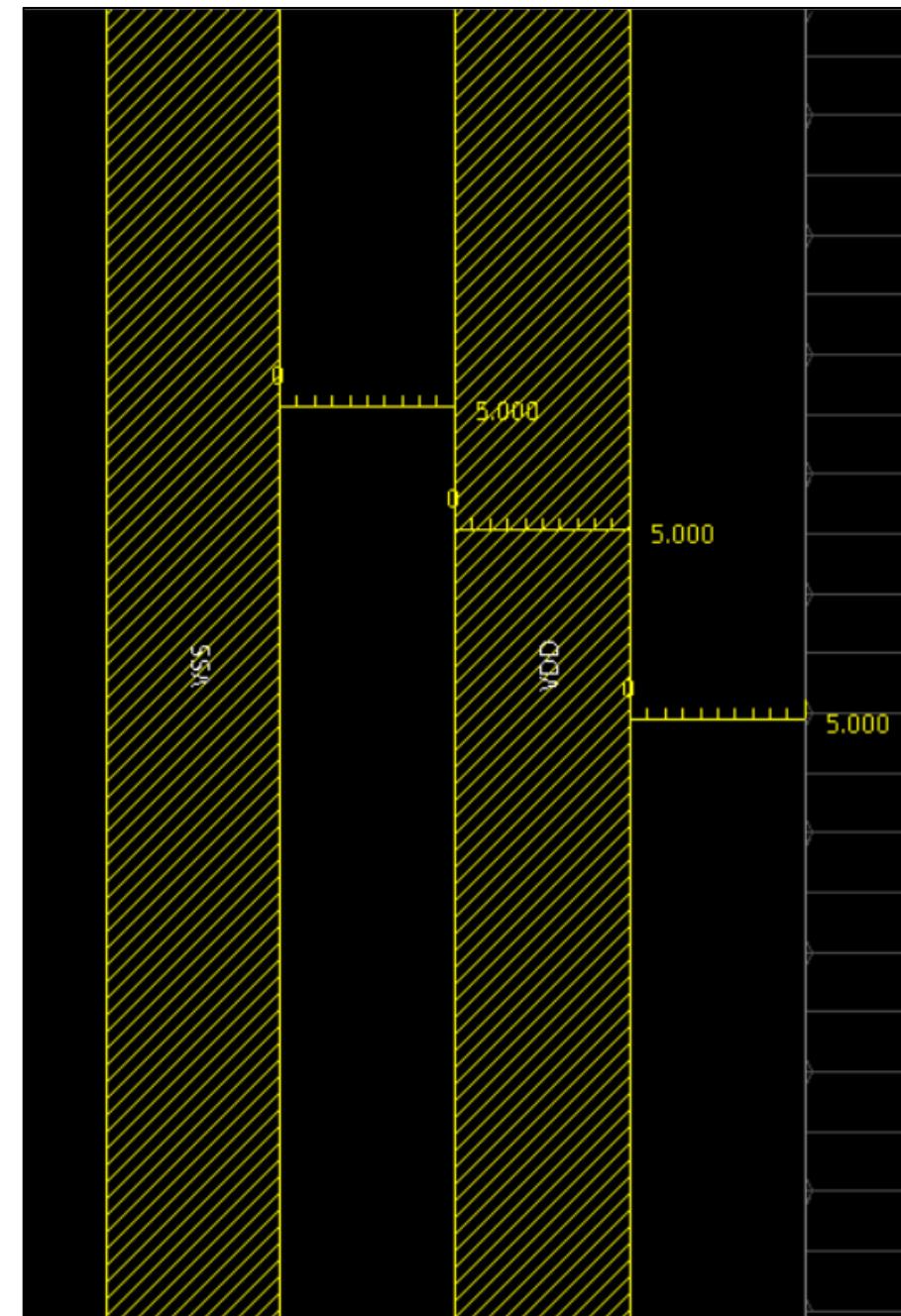
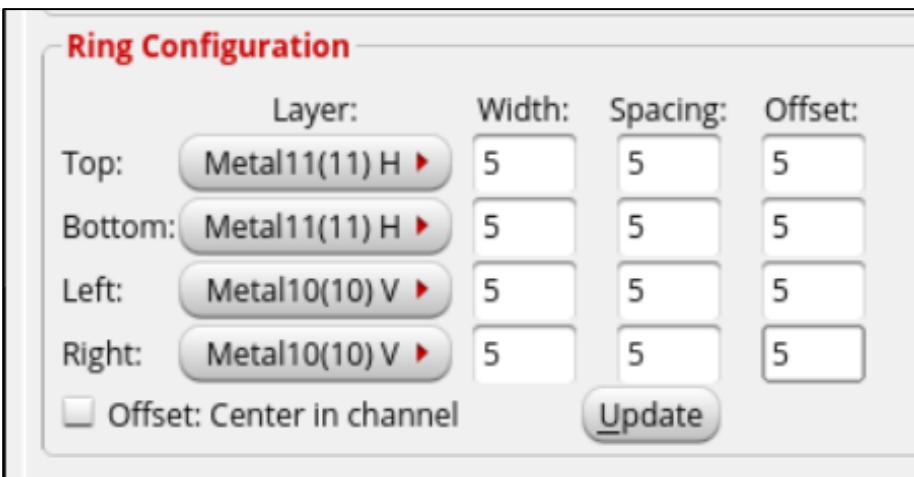
- **PowerPlan**
- core 주변 power ring 생성됨



Auto PnR

Innovus

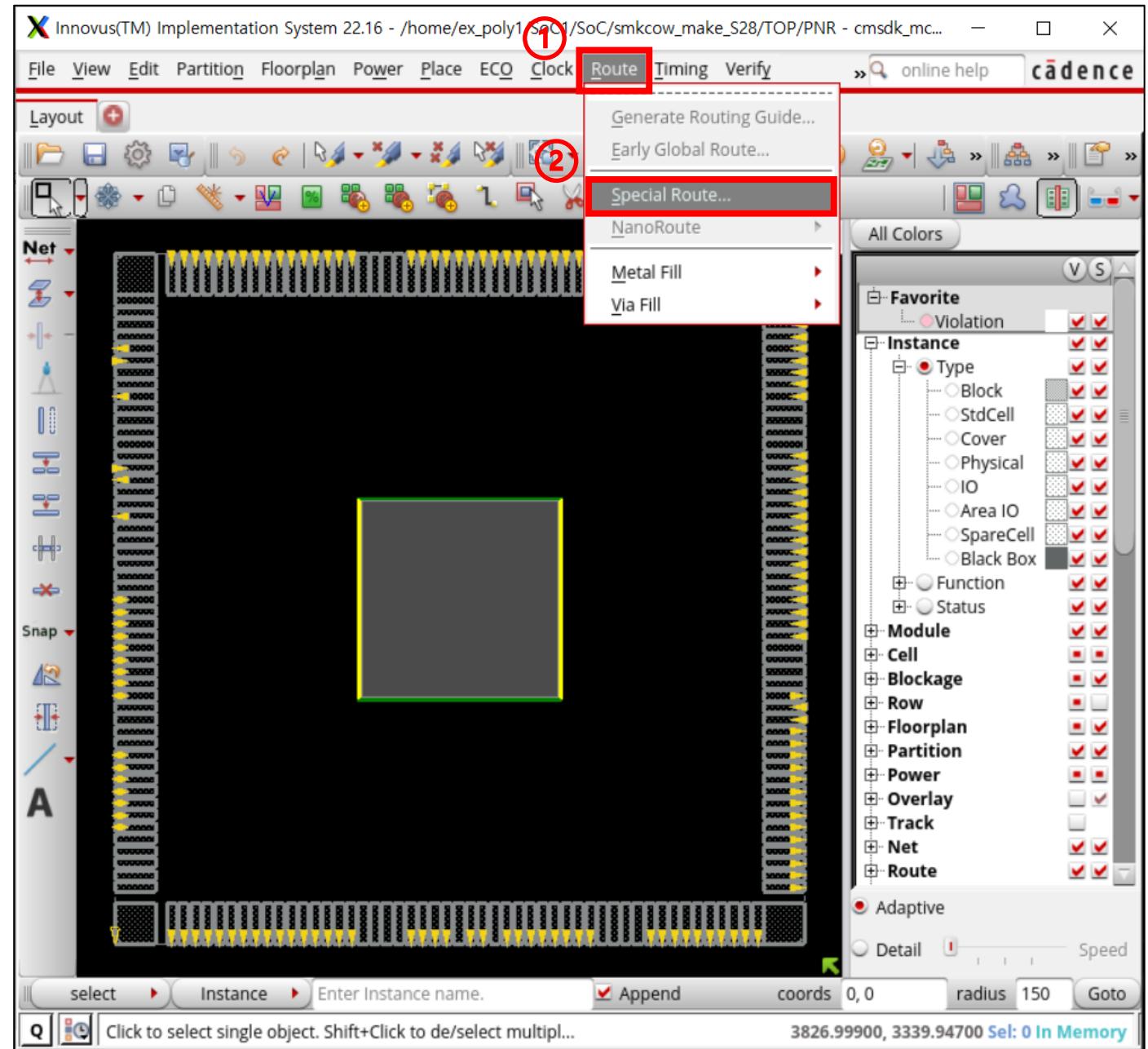
- **PowerPlan**
- core 주변 power ring 생성됨
- Width, Spacing, Offset 모두 설정과 일치하는 것을 확인함



Auto PnR

Innovus

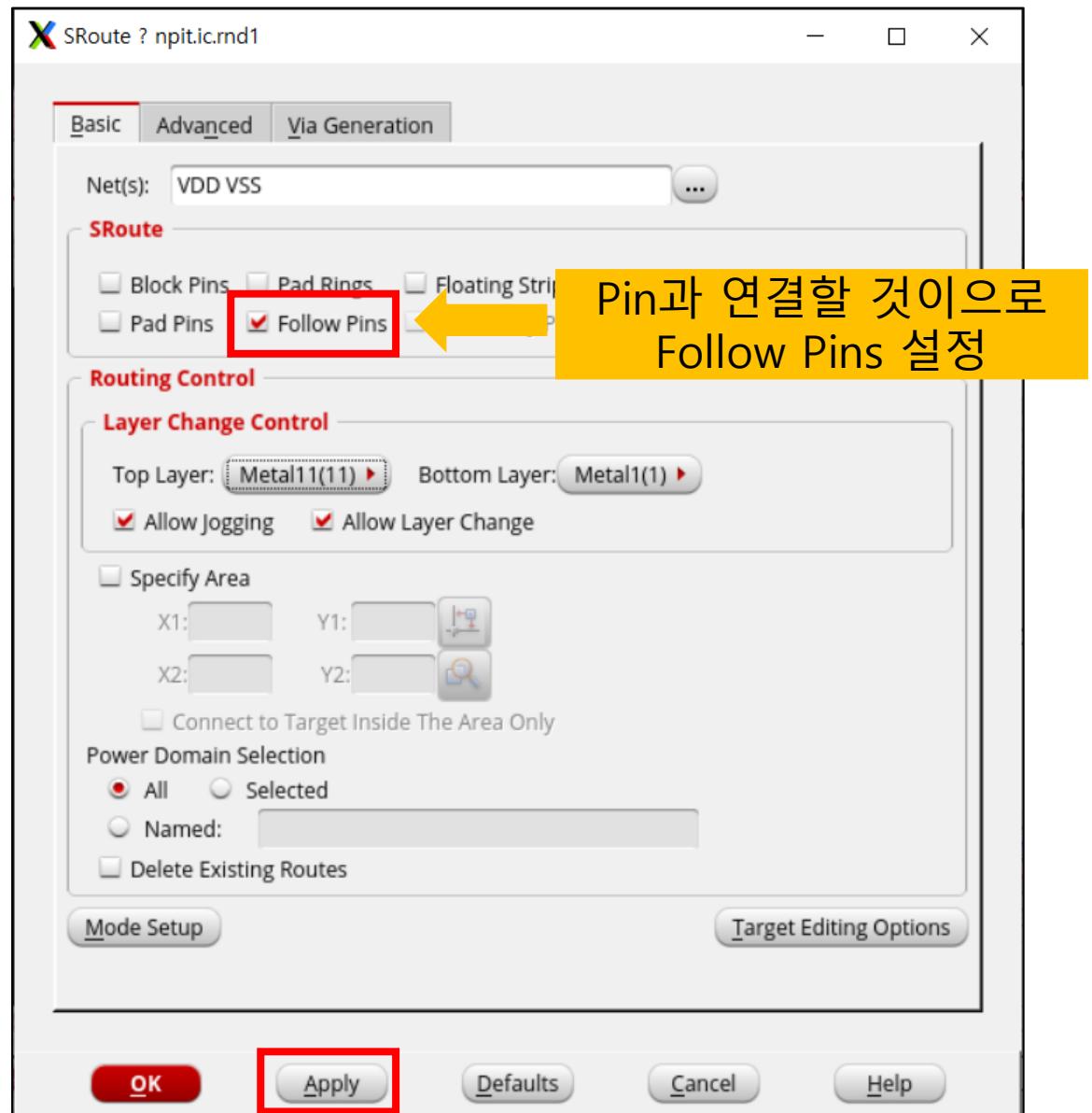
- PowerPlan
- core영역에 rail 형성



Auto PnR

Innovus

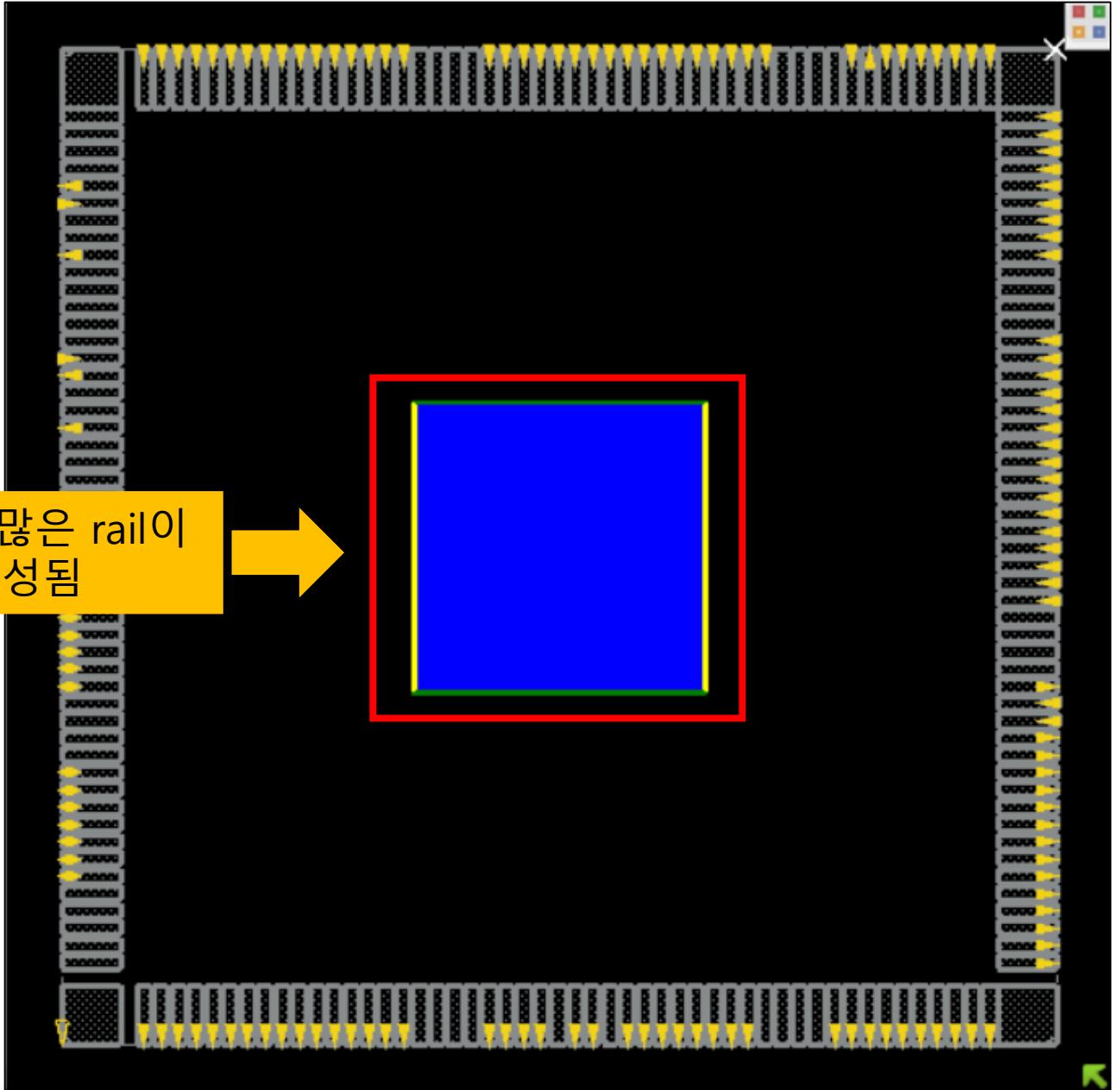
- PowerPlan
- core영역에 rail 형성
- 오른쪽과 똑같이 설정 후 Apply



Auto PnR

Innovus

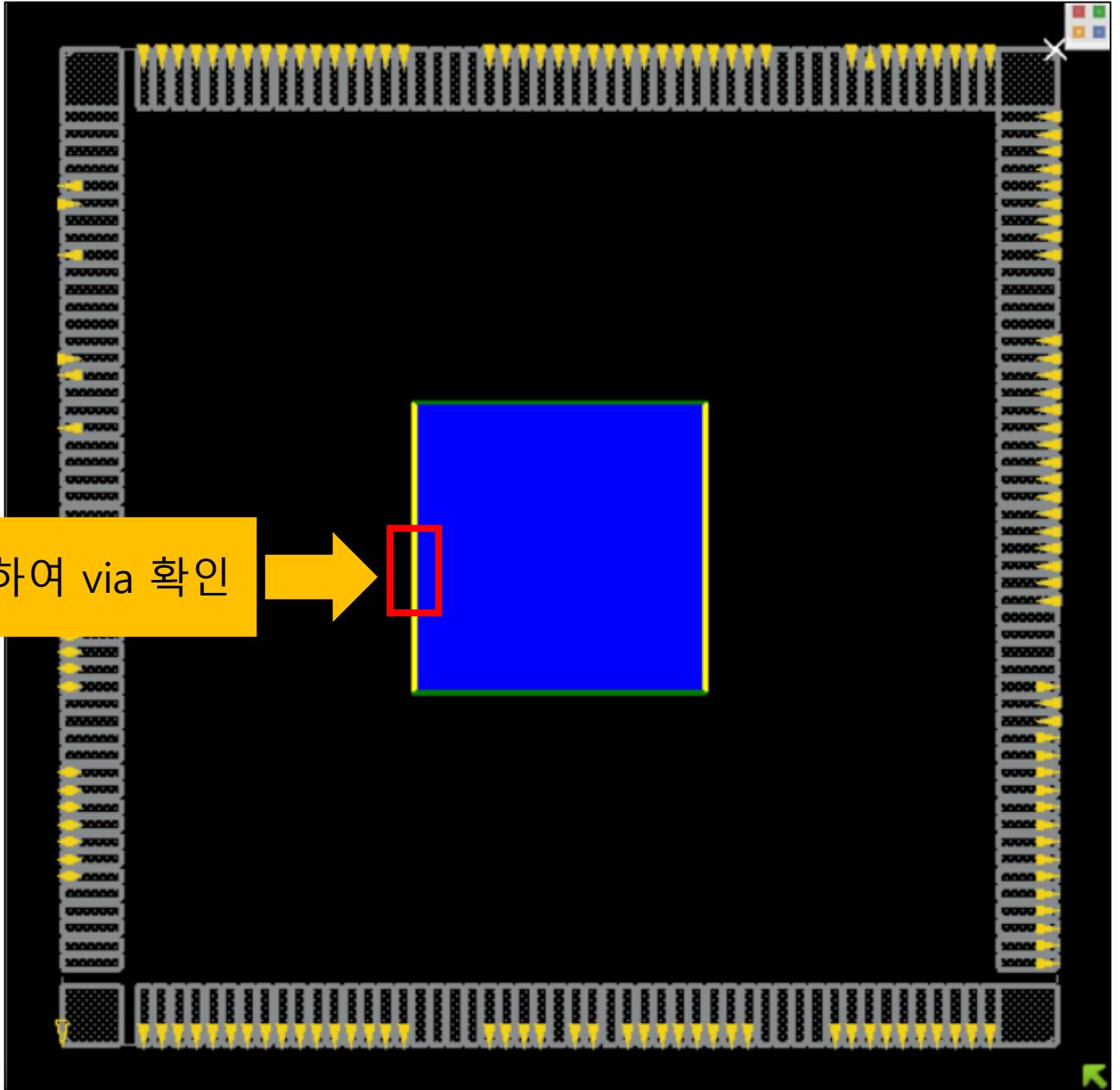
- PowerPlan
- core영역에 rail 형성



Auto PnR

Innovus

- PowerPlan
- core영역에 rail 형성

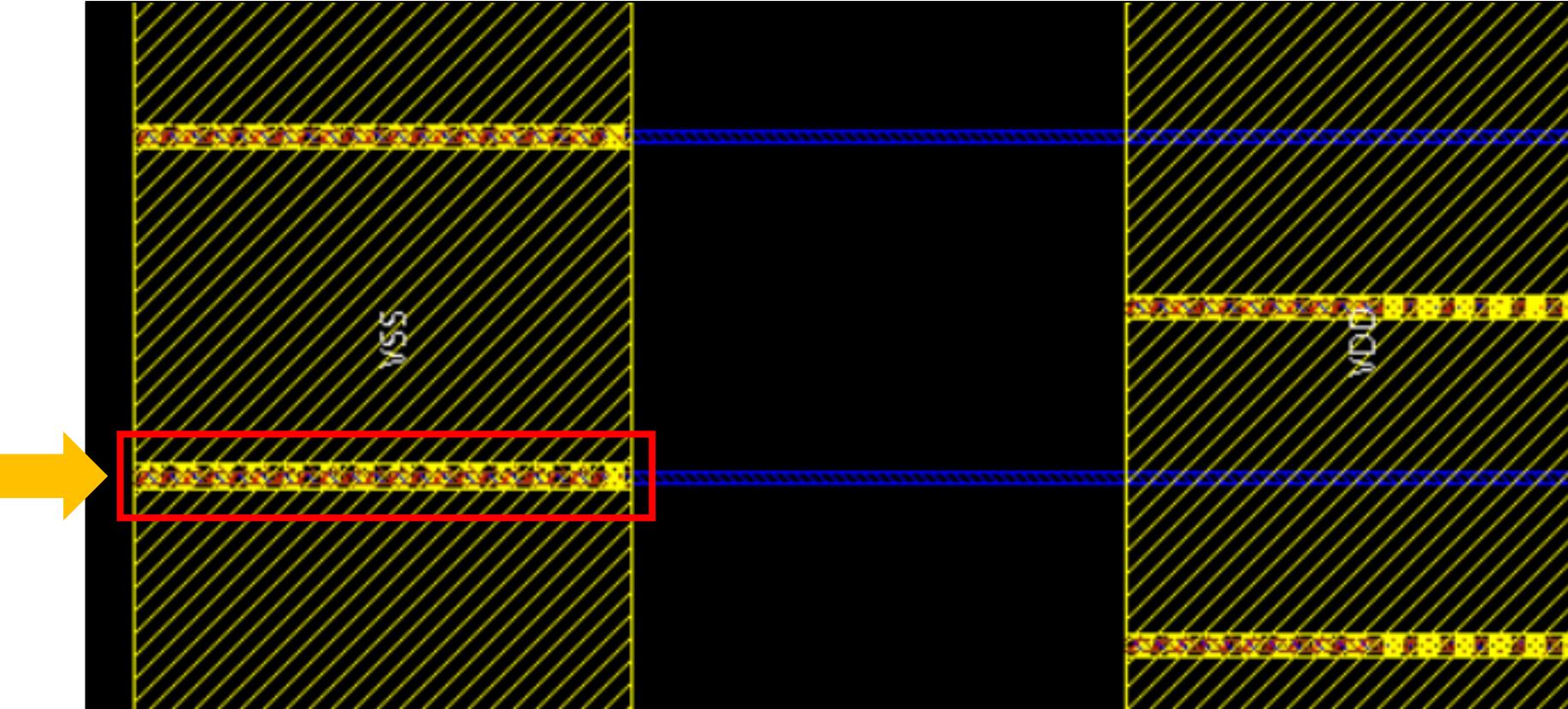


Auto PnR

Innovus

- PowerPlan
- core영역에 rail 형성

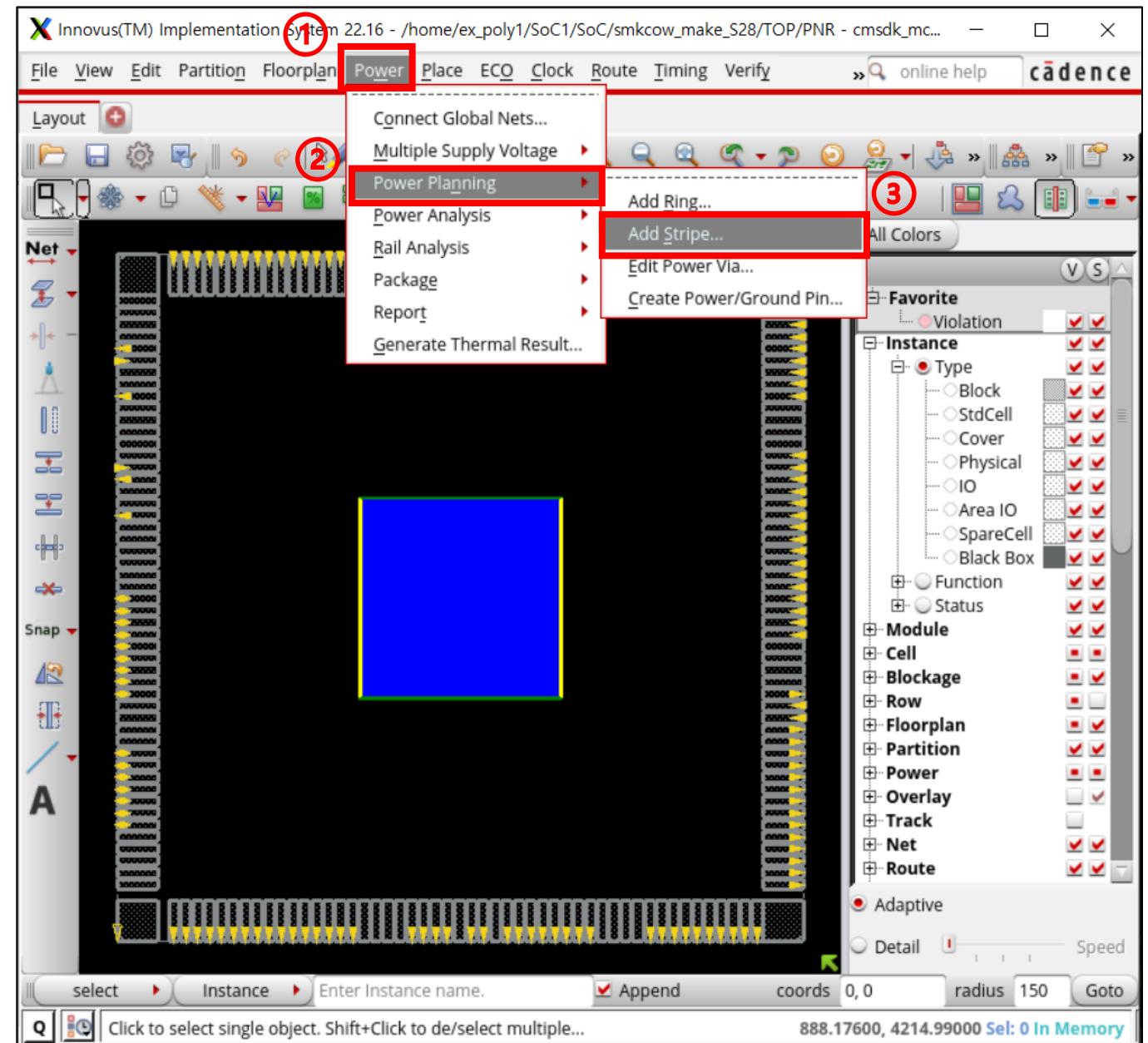
via가 잘 형성된 것을
확인함



Auto PnR

Innovus

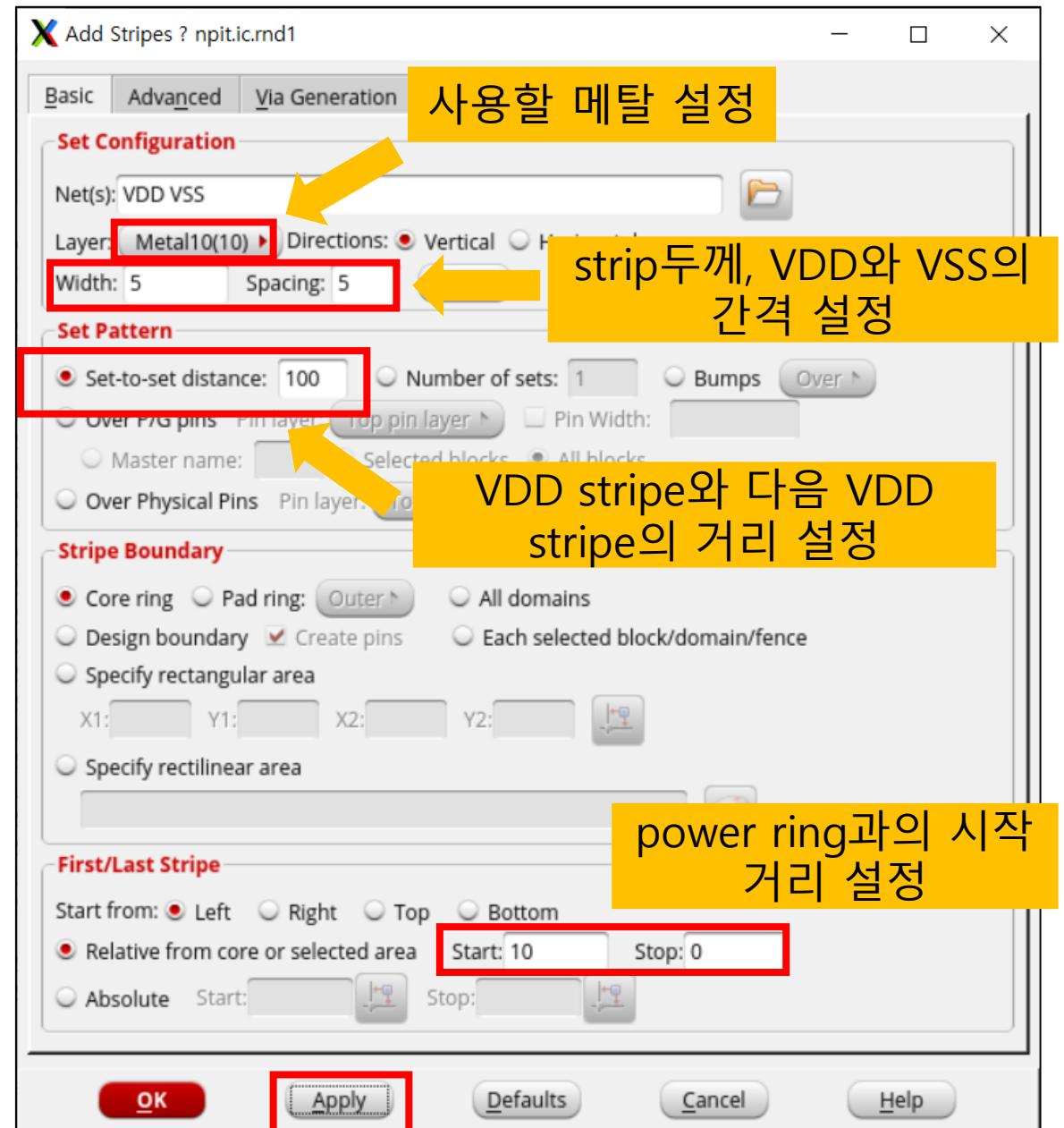
- PowerPlan
- core영역에 stripe 형성



Auto PnR

Innovus

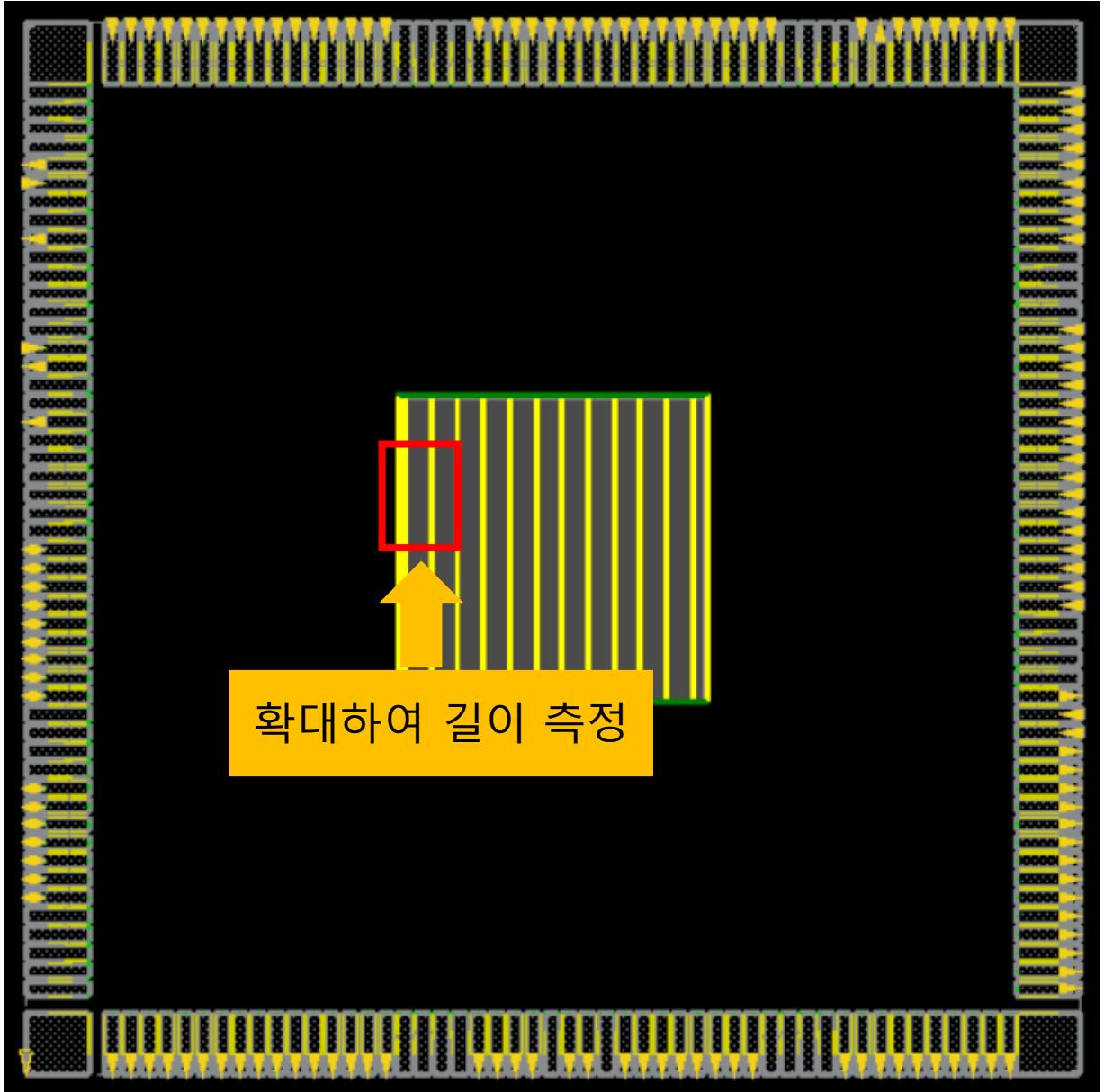
- PowerPlan
- core영역에 stripe 형성
- 오른쪽과 똑같이 설정 후 Apply



Auto PnR

Innovus

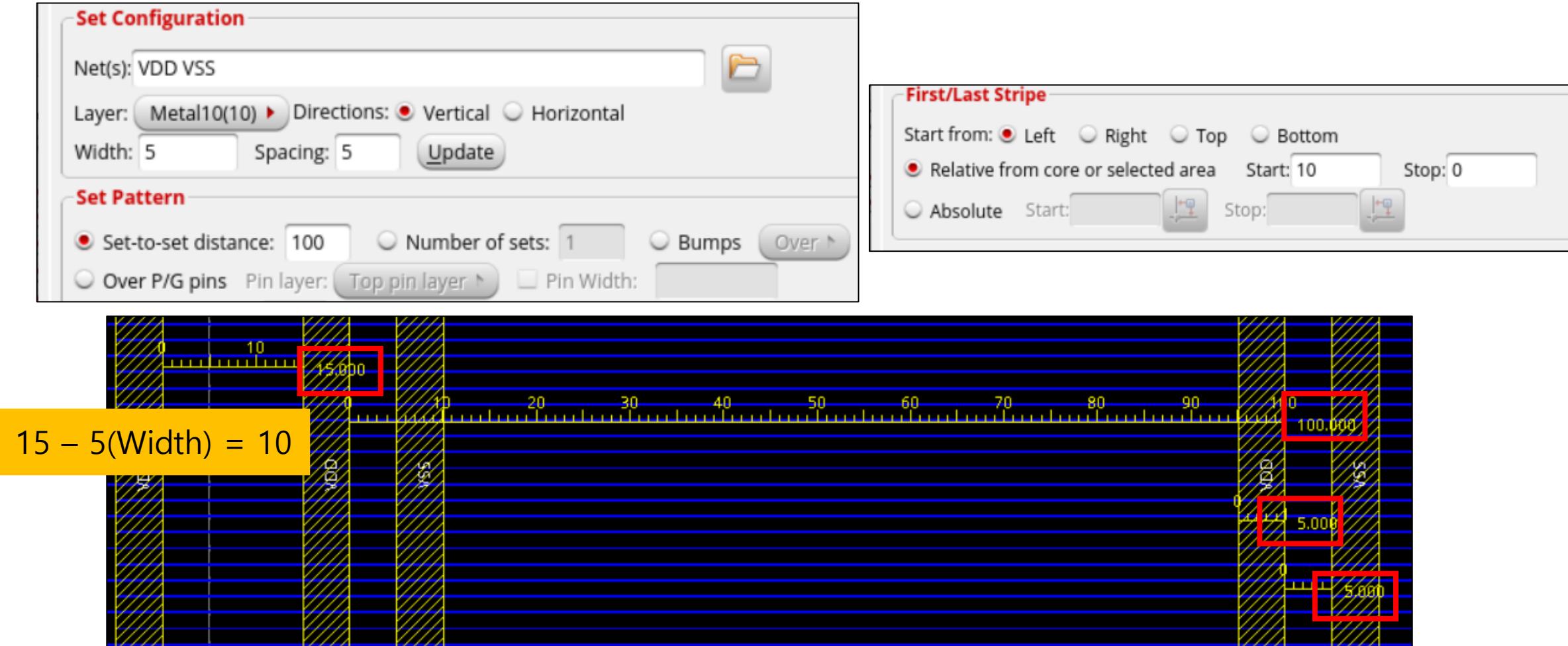
- PowerPlan
- core영역에 stripe 형성



Auto PnR

Innovus

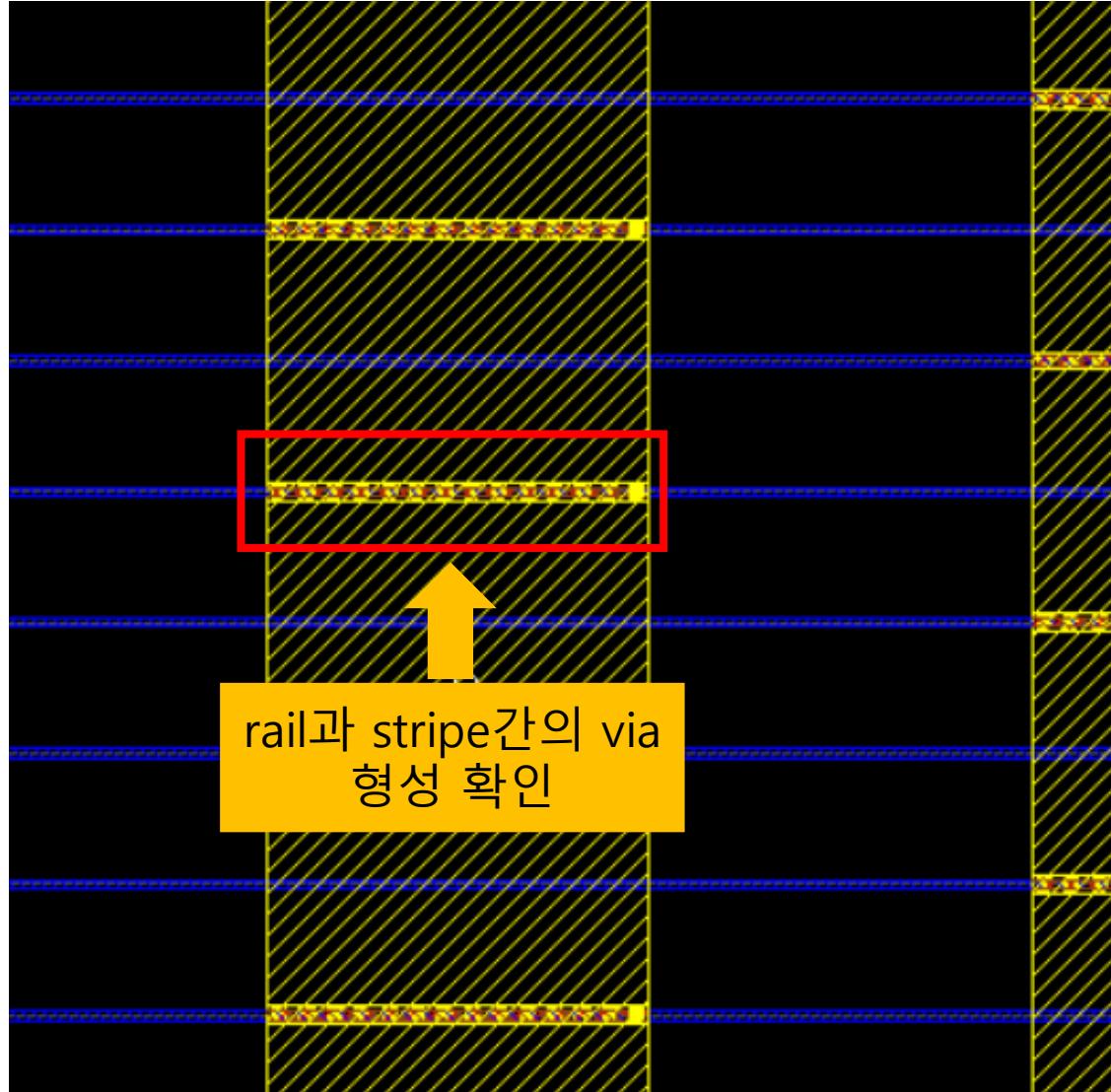
- PowerPlan
- core영역에 stripe 형성 – 설정 값과 일치함



Auto PnR

Innovus

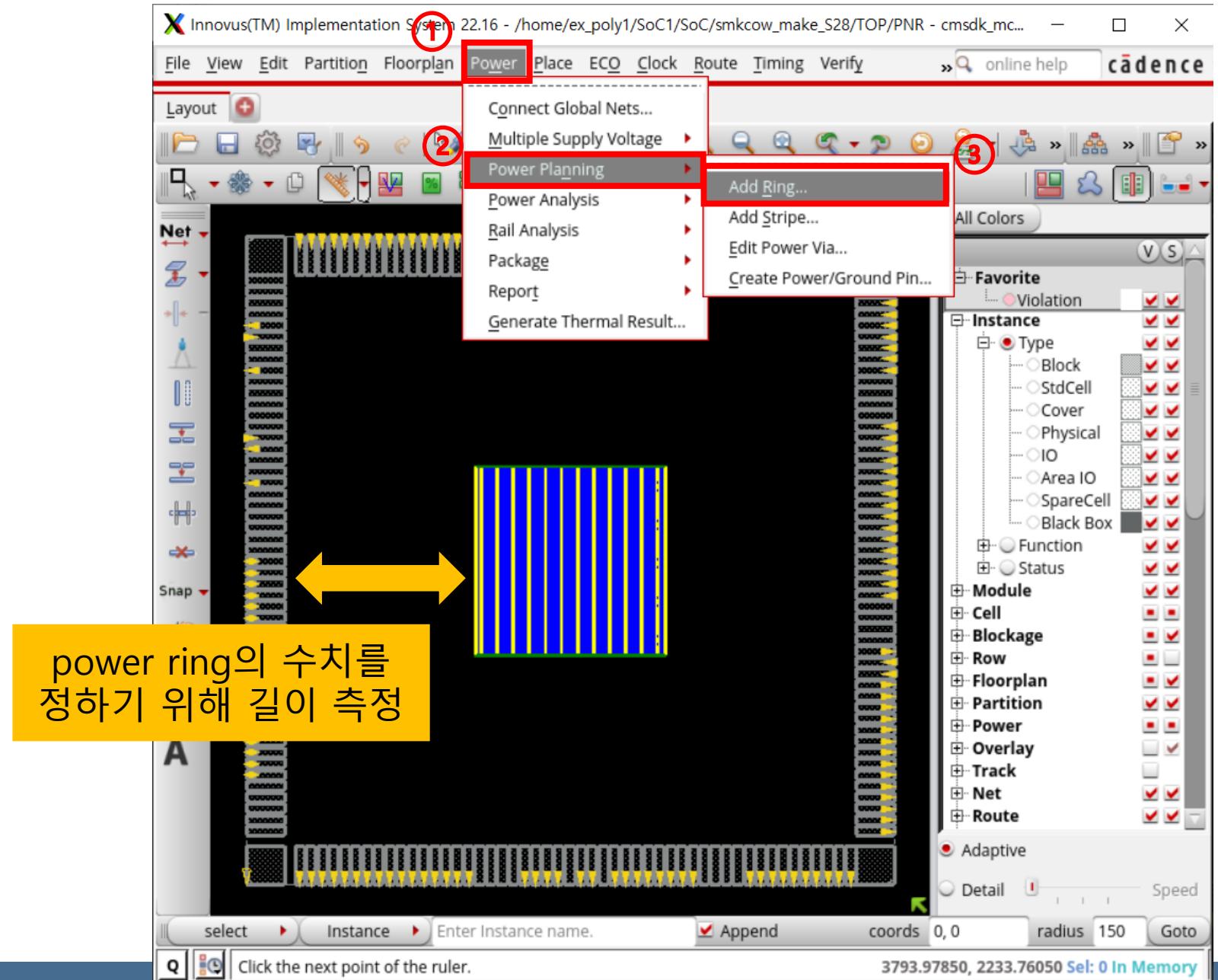
- PowerPlan
- core영역에 stripe 형성



Auto PnR

Innovus

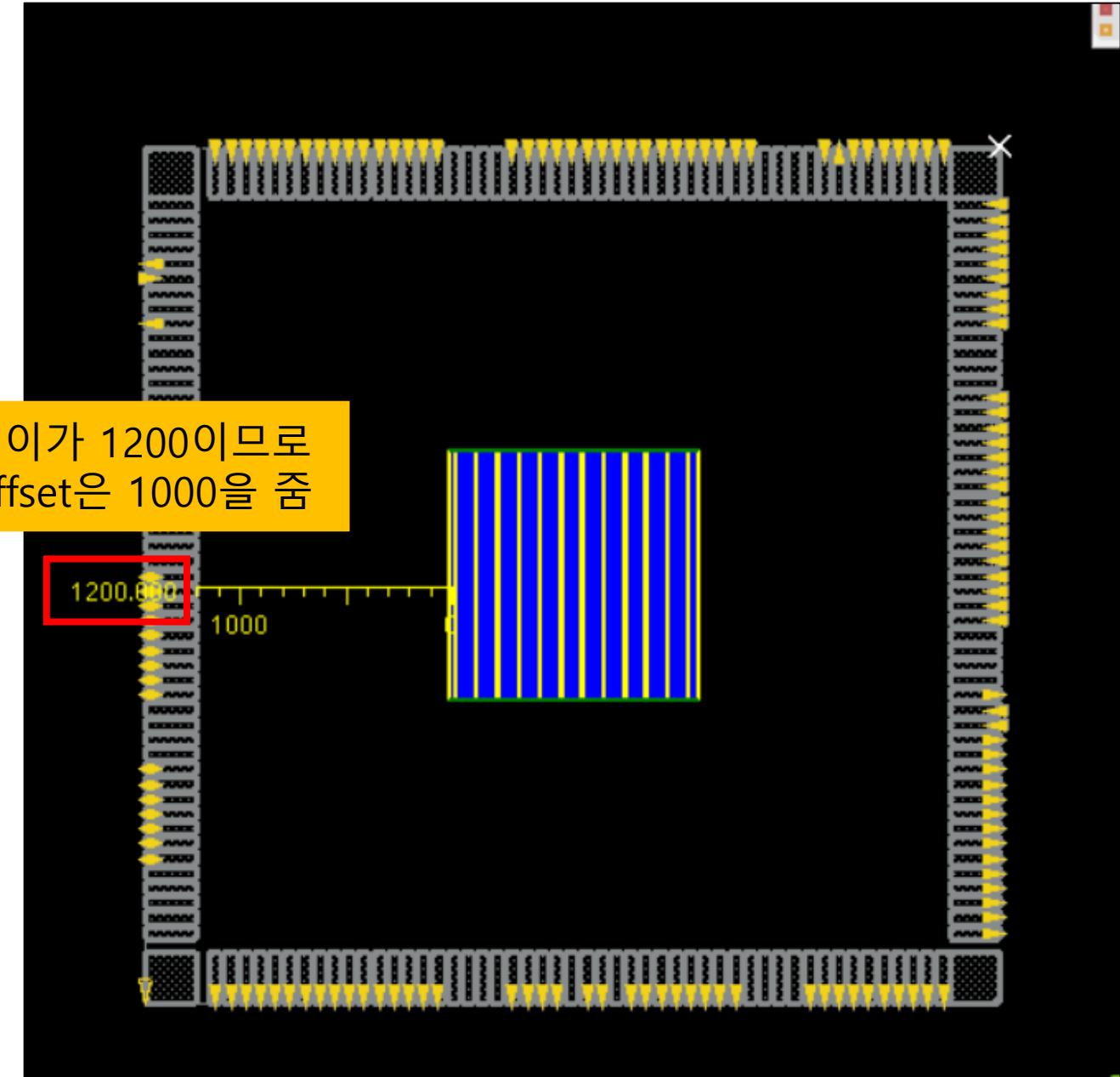
- PowerPlan
- IO주변 power ring 생성



Auto PnR

Innovus

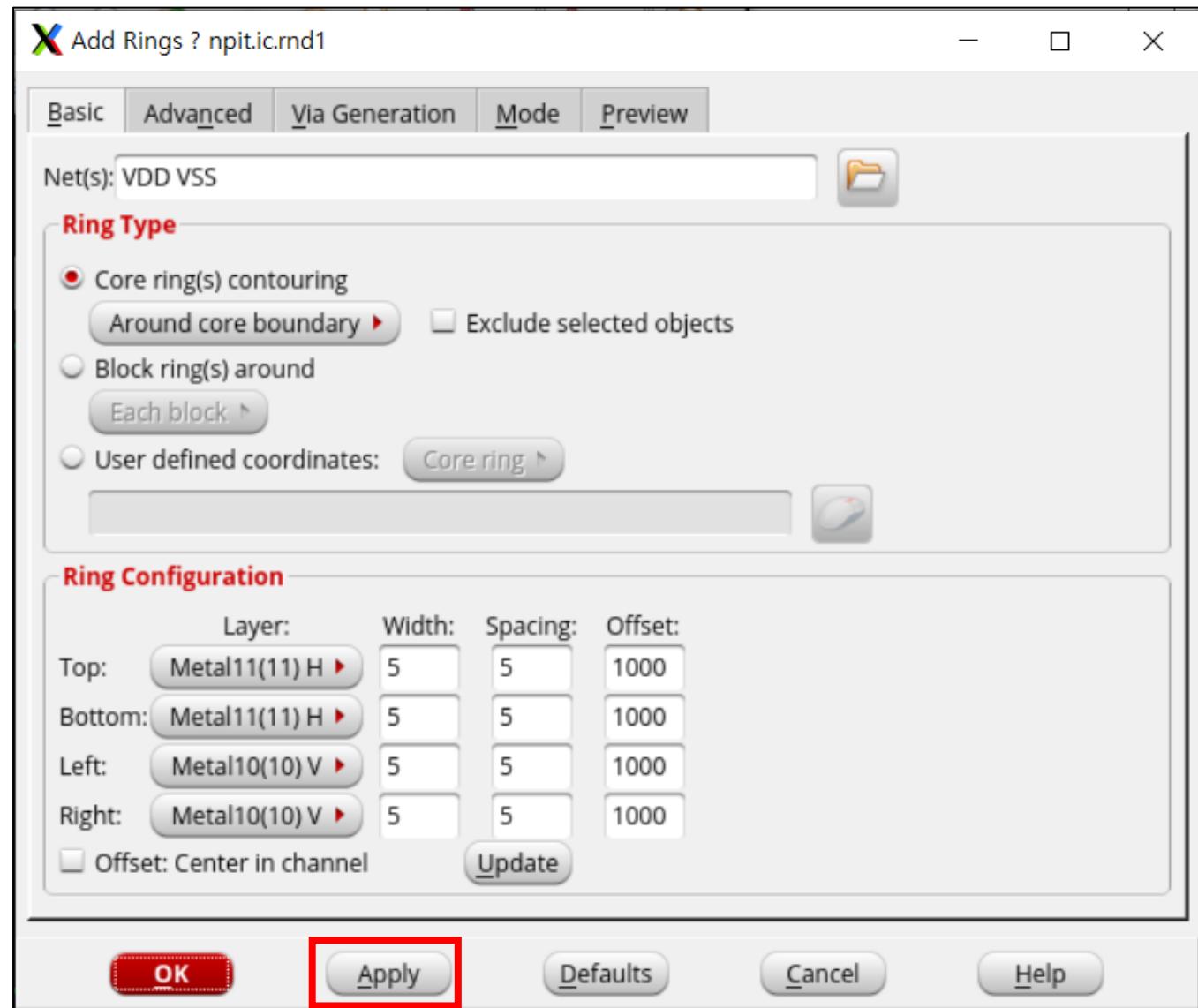
- PowerPlan
- IO주변 power ring 생성



Auto PnR

Innovus

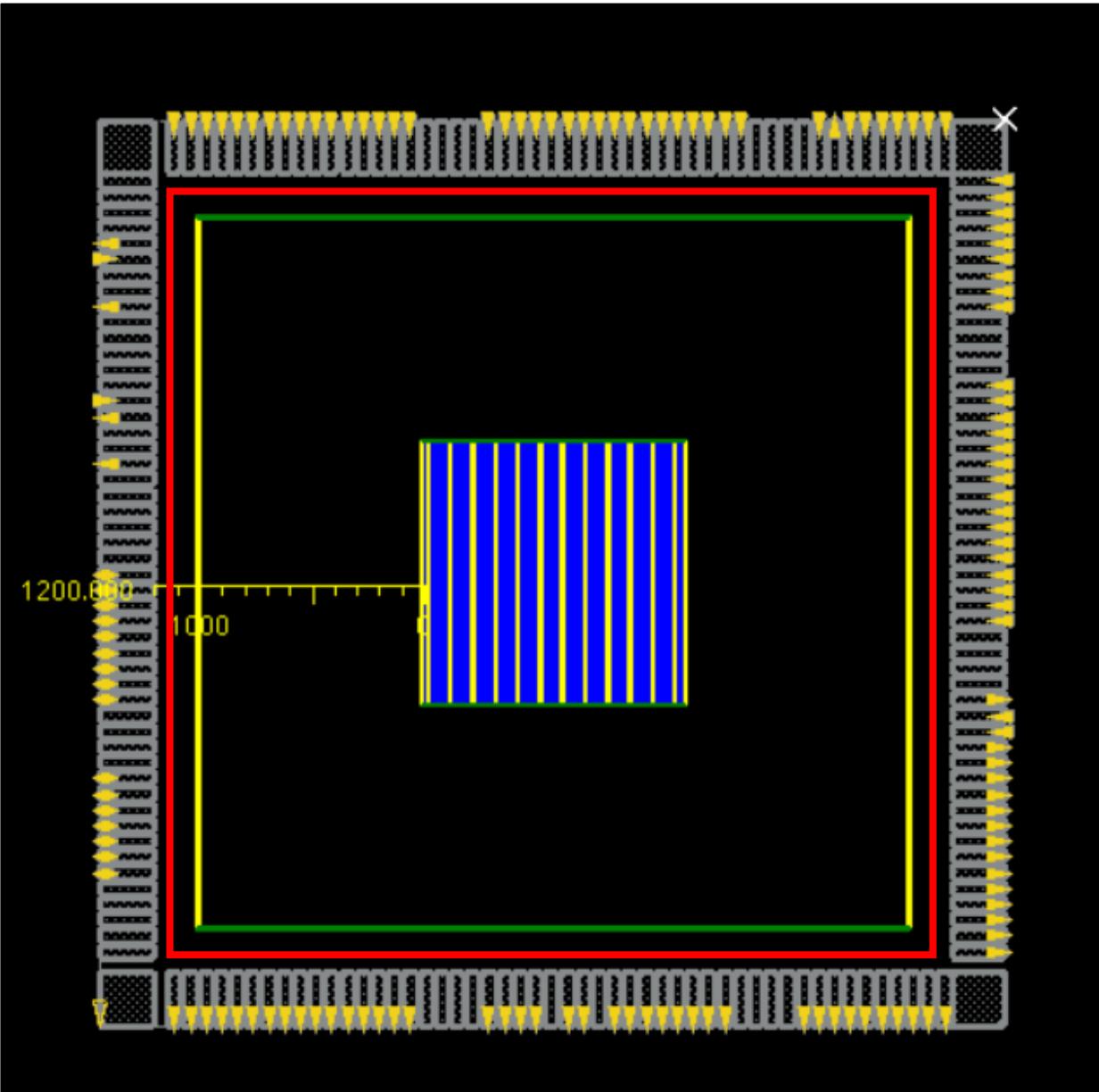
- PowerPlan
- IO주변 power ring 생성
- 오른쪽과 똑같이 설정 후 Apply



Auto PnR

Innovus

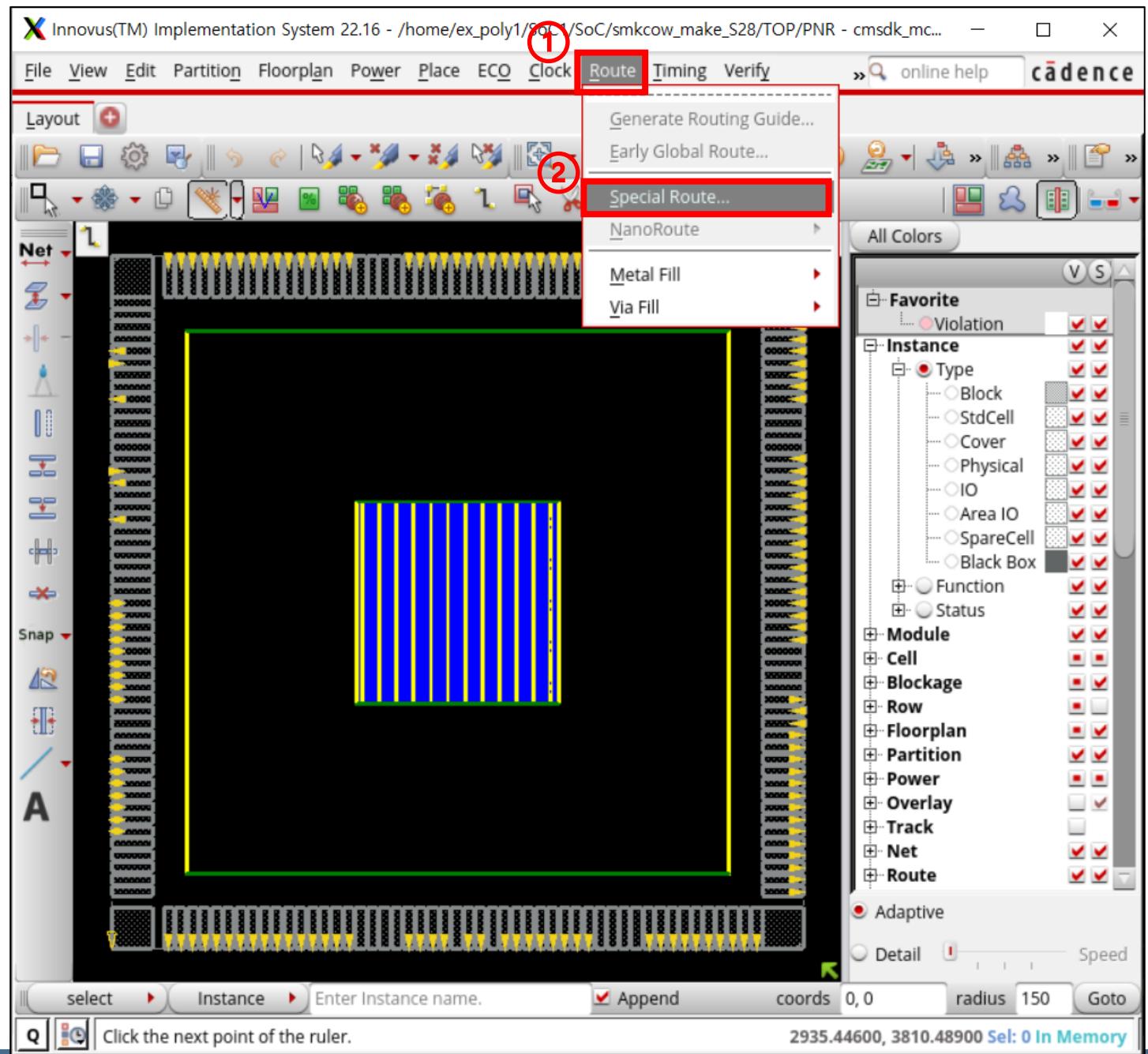
- PowerPlan
- IO주변 power ring 생성



Auto PnR

Innovus

- PowerPlan
- IO주변 Power ring과 IO cell을 연결



Auto PnR

Innovus

- **PowerPlan**
- IO주변 Power ring과 IO cell을 연결
- 오른쪽과 똑같이 설정 후 Apply

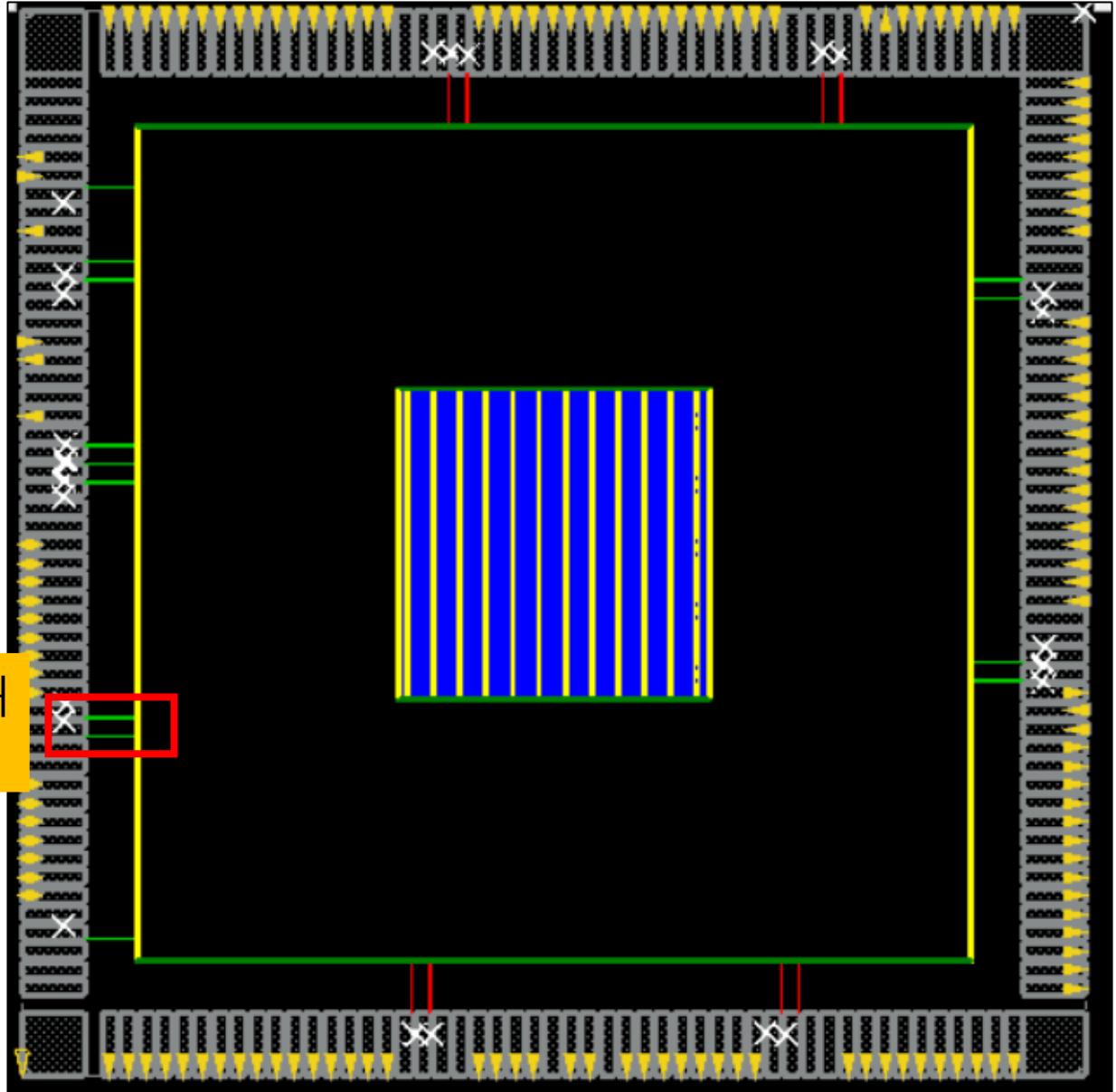


Auto PnR

Innovus

- PowerPlan
- IO주변 Power ring과 IO cell을 연결

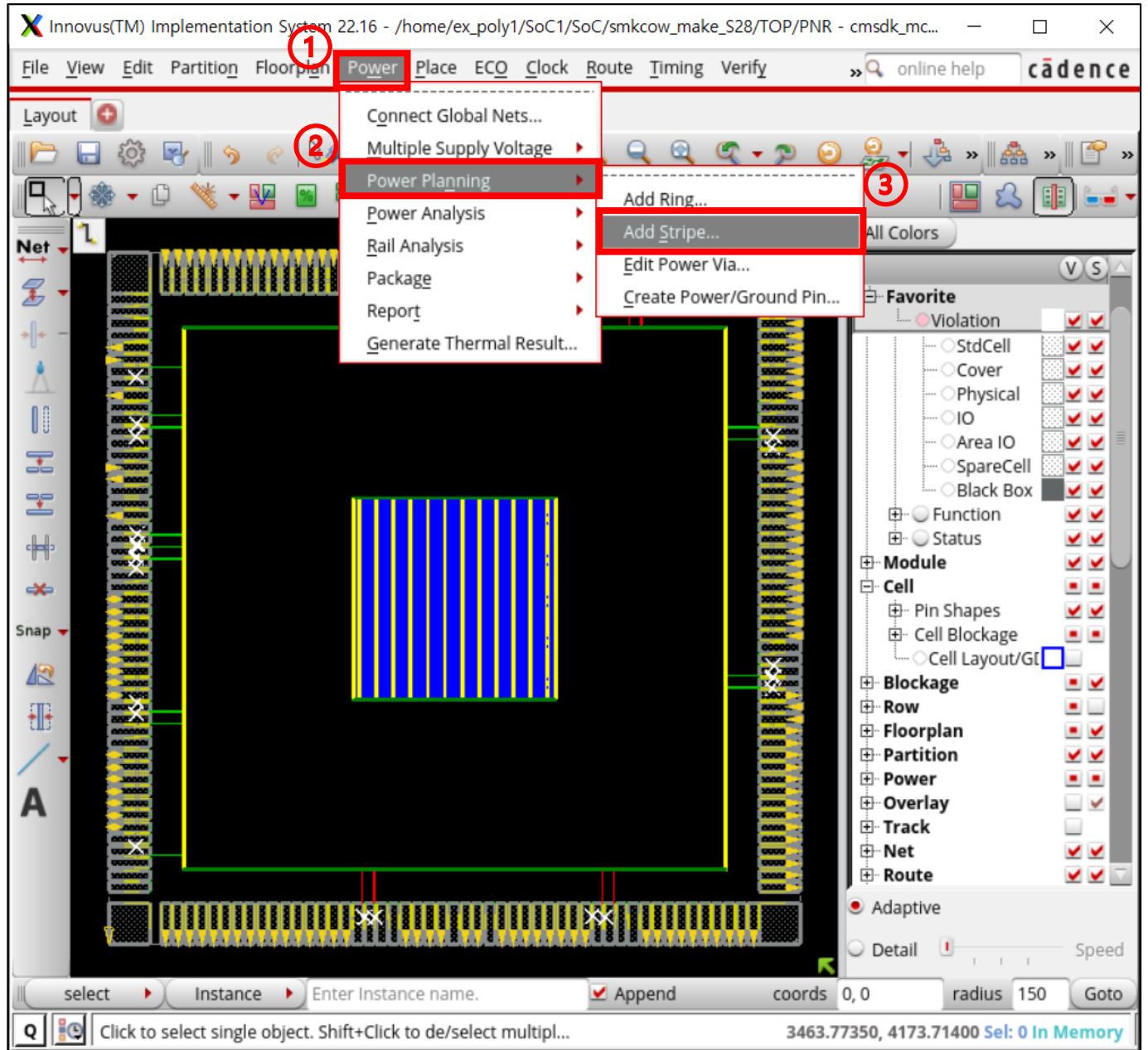
power ring과 셀을 연결해
주는 라인이 형성됨



Auto PnR

Innovus

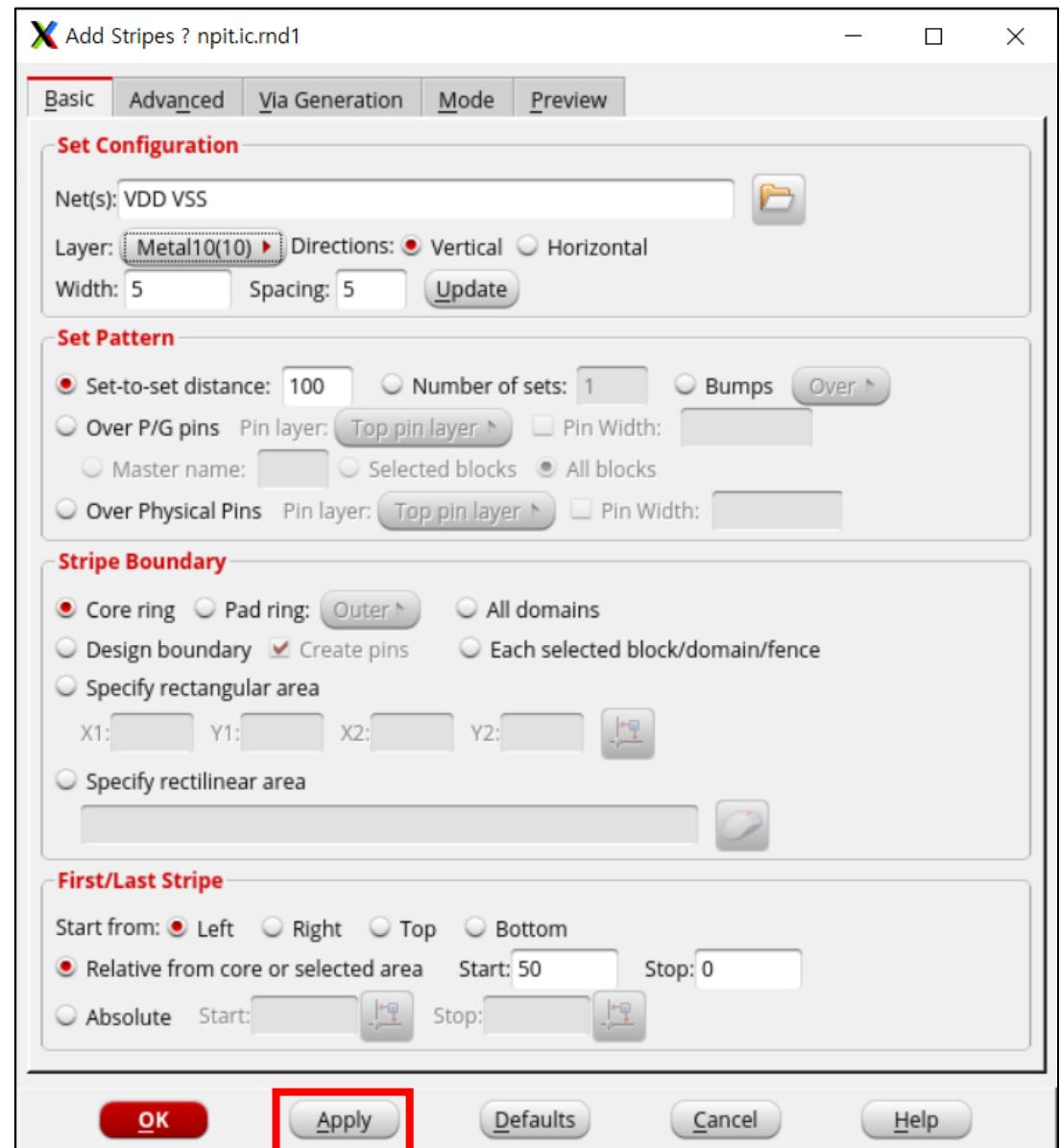
- PowerPlan
- IO 주변 power ring과 Core 주변 power ring 연결



Auto PnR

Innovus

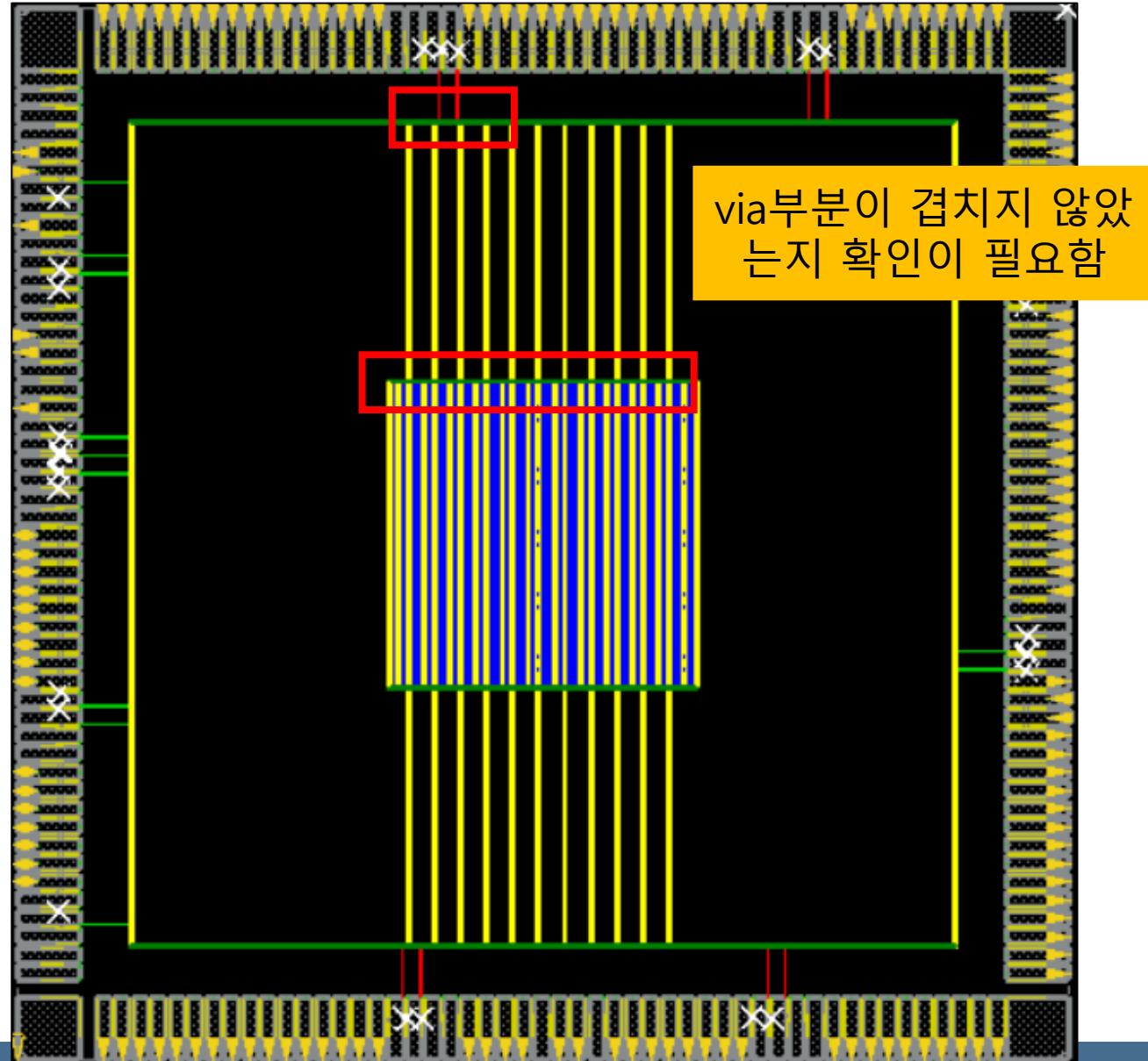
- PowerPlan
- IO 주변 power ring과 Core 주변 power ring 연결
- 오른쪽과 똑같이 설정 후 Apply



Auto PnR

Innovus

- **PowerPlan**
- IO 주변 power ring과 Core 주변 power ring 연결

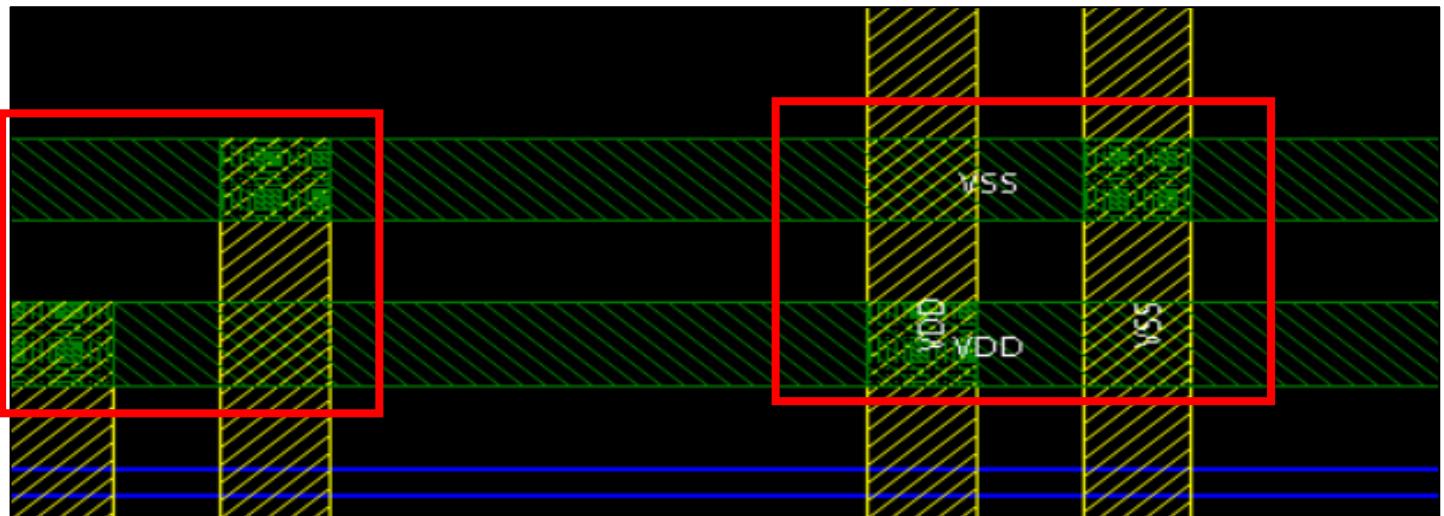
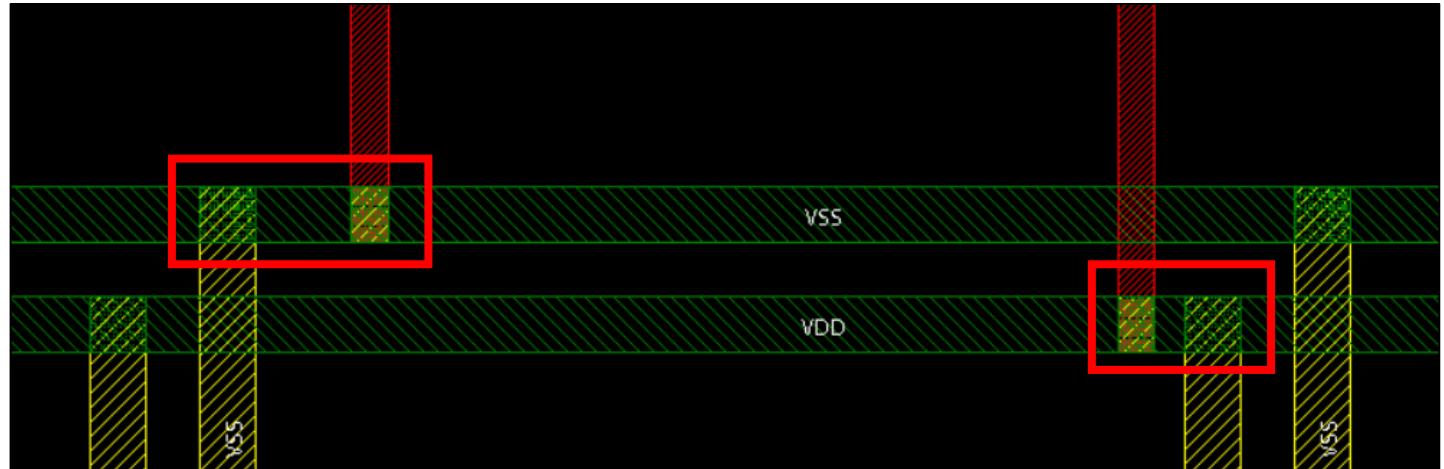


Auto PnR

Innovus

- PowerPlan
- IO 주변 power ring과 Core 주변 power ring 연결

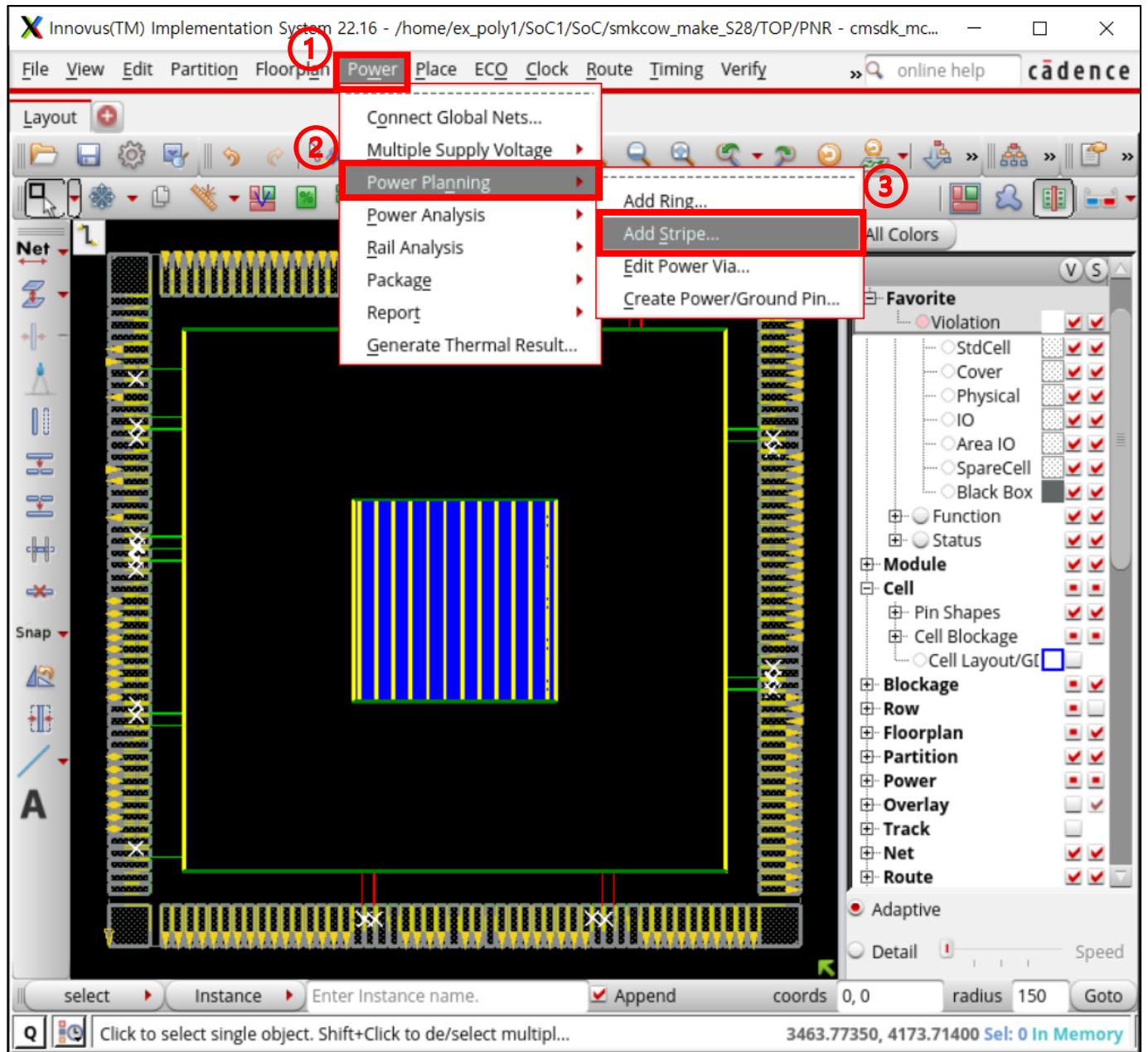
via부분이 겹치지 않음



Auto PnR

Innovus

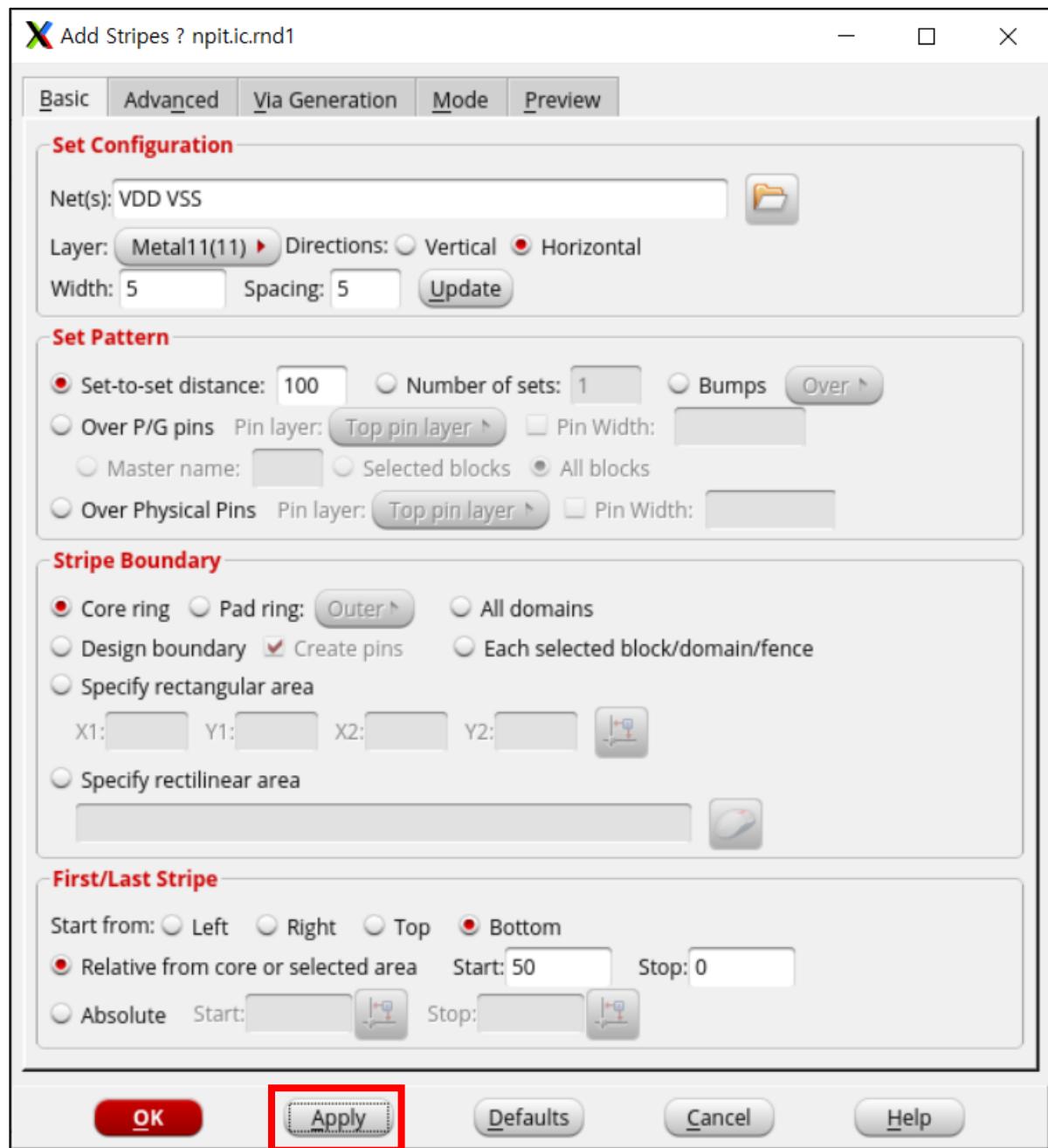
- PowerPlan
- Mesh 형성



Auto PnR

Innovus

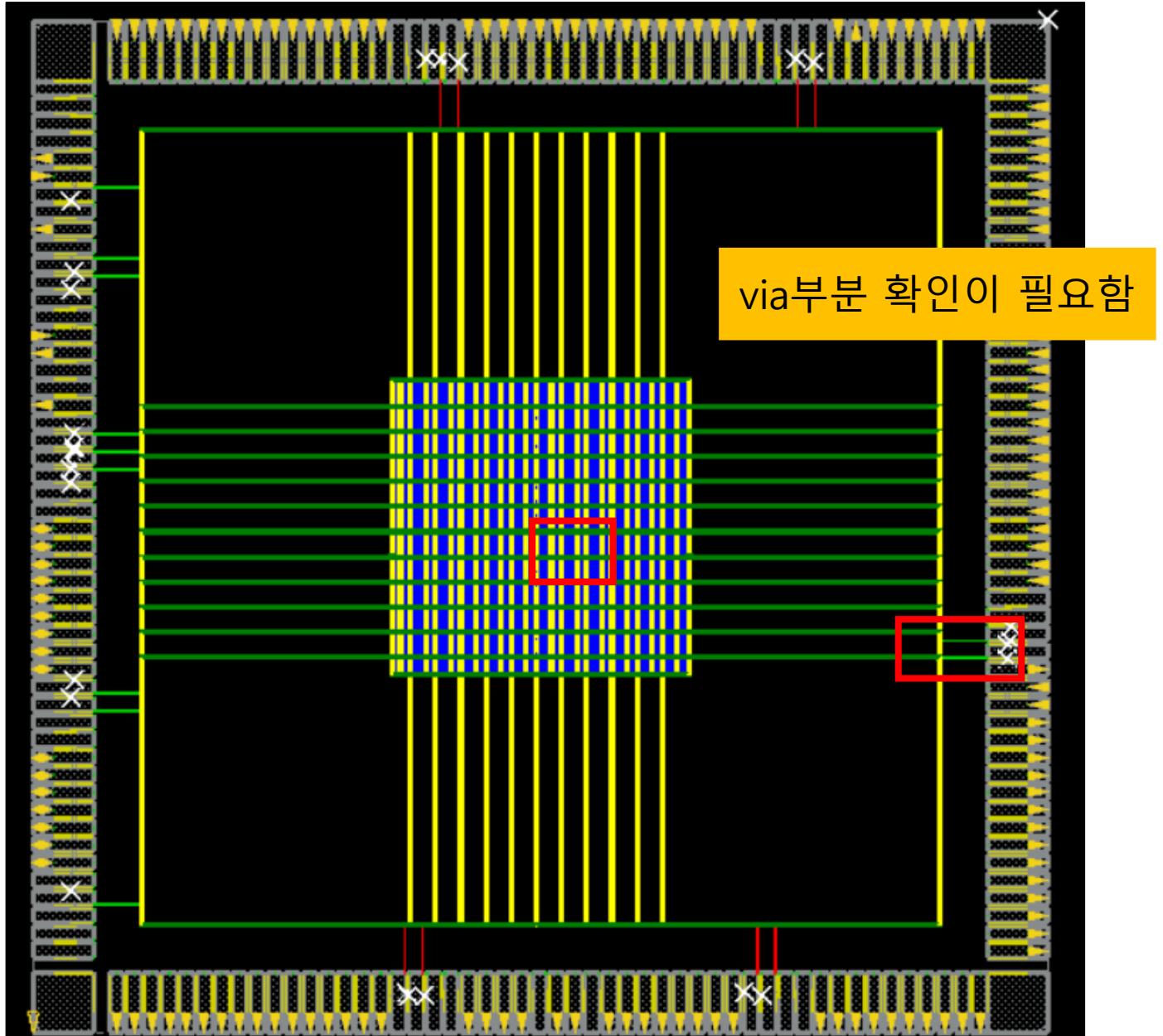
- PowerPlan
- Mesh 형성
- 오른쪽과 똑같이 설정 후 Apply



Auto PnR

Innovus

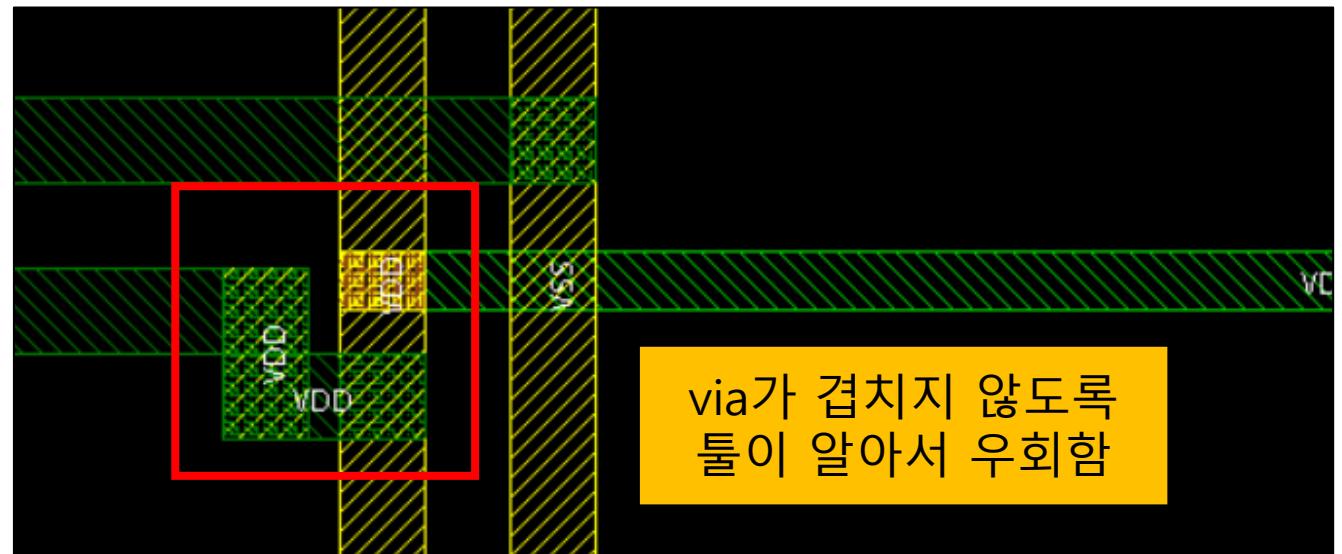
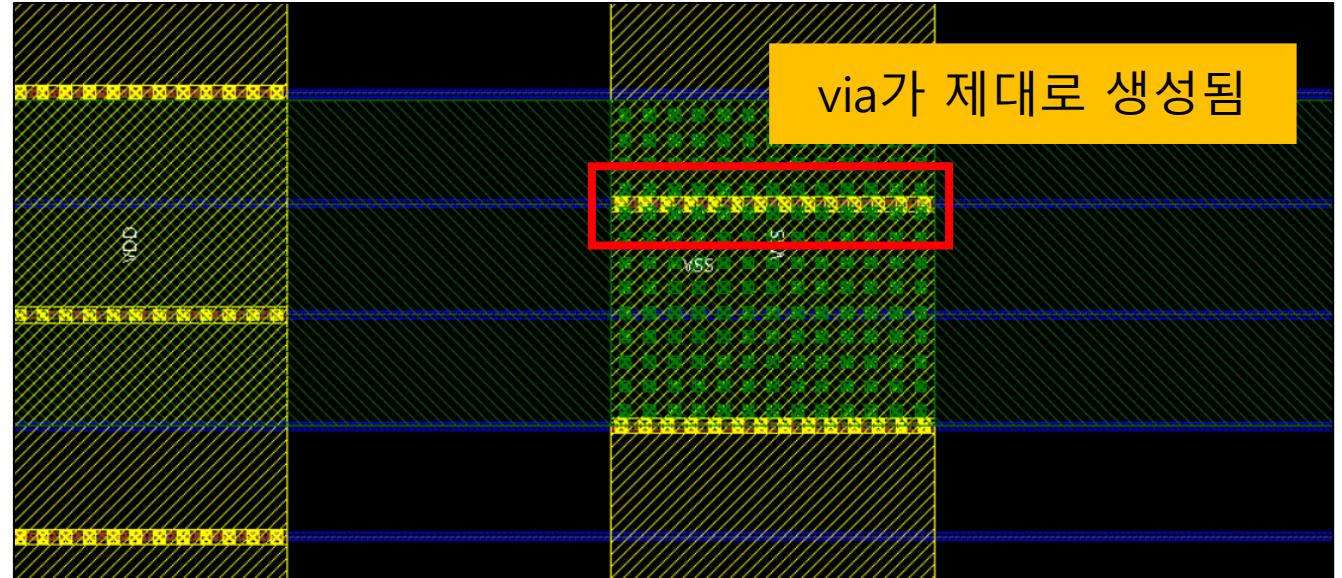
- PowerPlan
- Mesh 형성



Auto PnR

Innovus

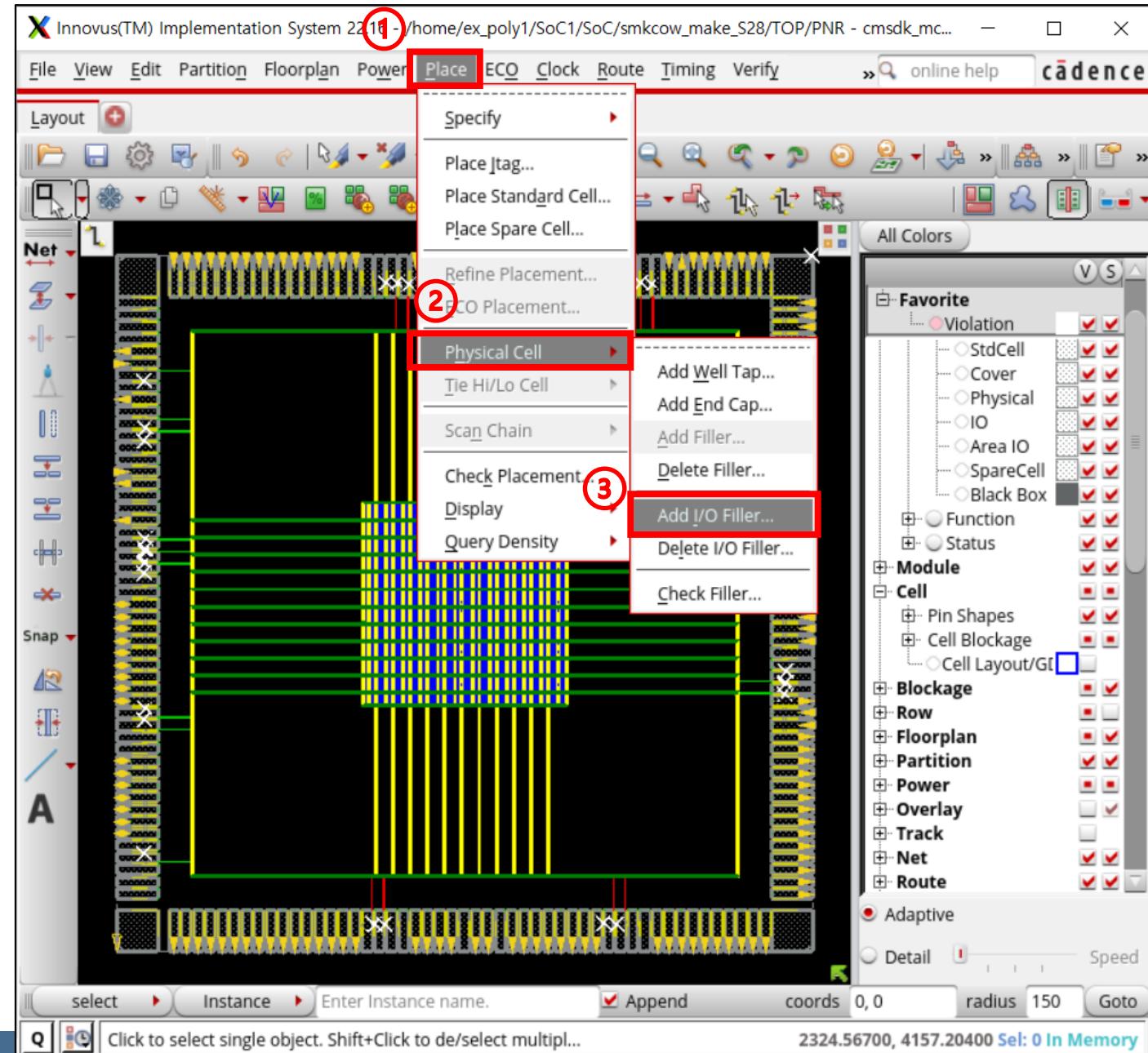
- PowerPlan
- Mesh 형성



Auto PnR

Innovus

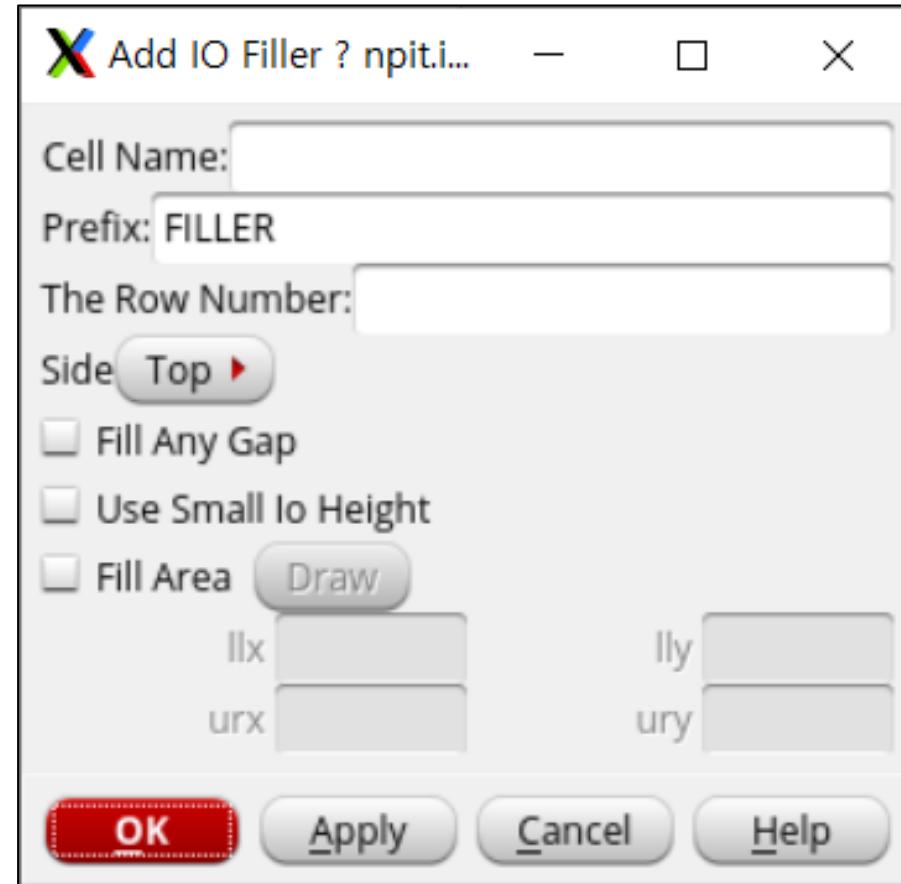
- IO Filler 채우기



Auto PnR

Innovus

- IO Filler 채우기
- Io 필러의 Cell name을 찾아야함



Auto PnR

Innovus

- IO Filler 채우기
- 전에 사용하던 나머지 터미널에서 바로 진행 가능

```
$> vi ../../..../GPDK045/digital/giolib045_v3.5/lef/giolib045.lef
```

PNR폴더에 있을 시 해당
경로로 명령어 입력

Auto PnR

Innovus

- **/MACRO padIORINGFEED** 검색하여 IO 필러 Cell name 확인
- 총 5개의 Cell name 확인 가능

```
VERSION 5.7 ;
BUSBITCHARS "[]" ;
DIVIDERCHAR "/" ;

UNITS
    DATABASE MICRONS 2000 ;
END UNITS
```

MACRO padIORINGFEED1

MACRO padIORINGFEED3

MACRO padIORINGFEED5

MACRO padIORINGFEED10

MACRO padIORINGFEED60

Auto PnR

Innovus

- **/MACRO padIORINGFEED** 검색하여 IO 필러 Cell name 확인
- 총 5개의 Cell name 확인 가능

TIP → :g,MACRO padIORINGFEED,,nu

```
VERSION 5.7 ;
BUSBITCHARS "[]" ;
DIVIDERCHAR "/" ;
UNITS
    DATABASE MICRONS 2000 ;
END UNITS
```

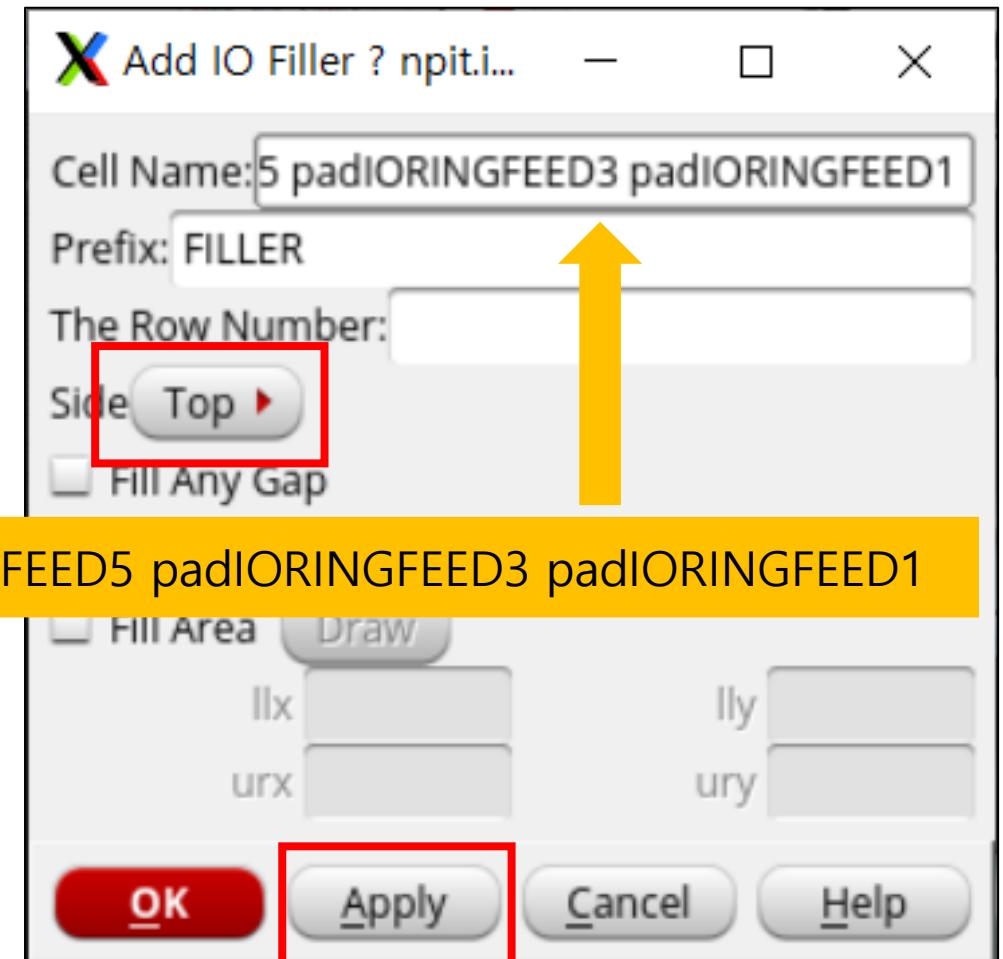
1305	MACRO	padIORINGFEED1
1378	MACRO	padIORINGFEED10
1453	MACRO	padIORINGFEED3
1528	MACRO	padIORINGFEED5
1603	MACRO	padIORINGFEED60

Auto PnR

Innovus

- **IO Filler 채우기**
- 앞서 찾은 Cell name을 크기가 큰 순으로 입력
- 입력 후 Apply 클릭

padIORINGFEED60 padIORINGFEED10 padIORINGFEED5 padIORINGFEED3 padIORINGFEED1

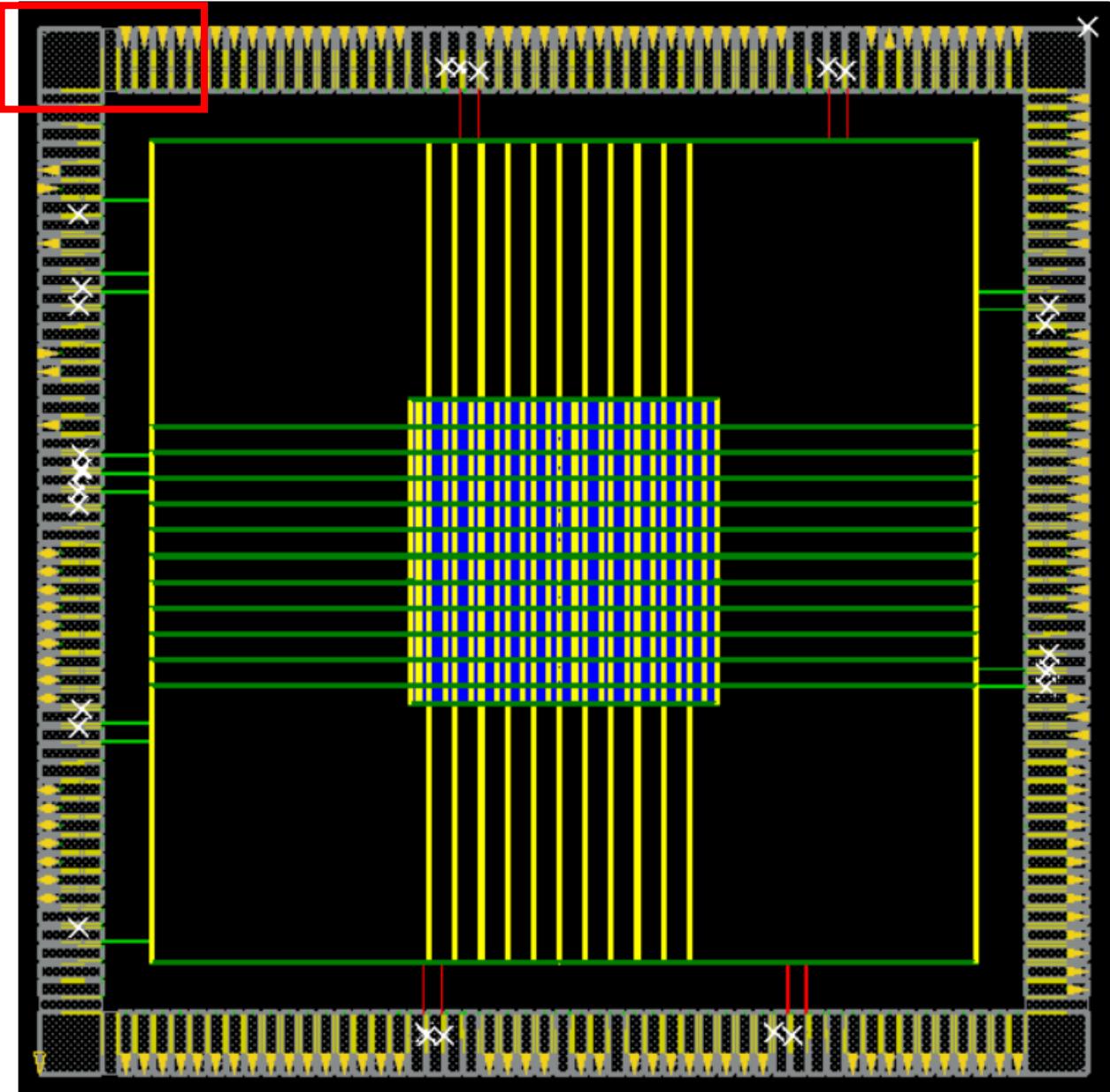


Auto PnR

TOP 확대 후 필러 확인

Innovus

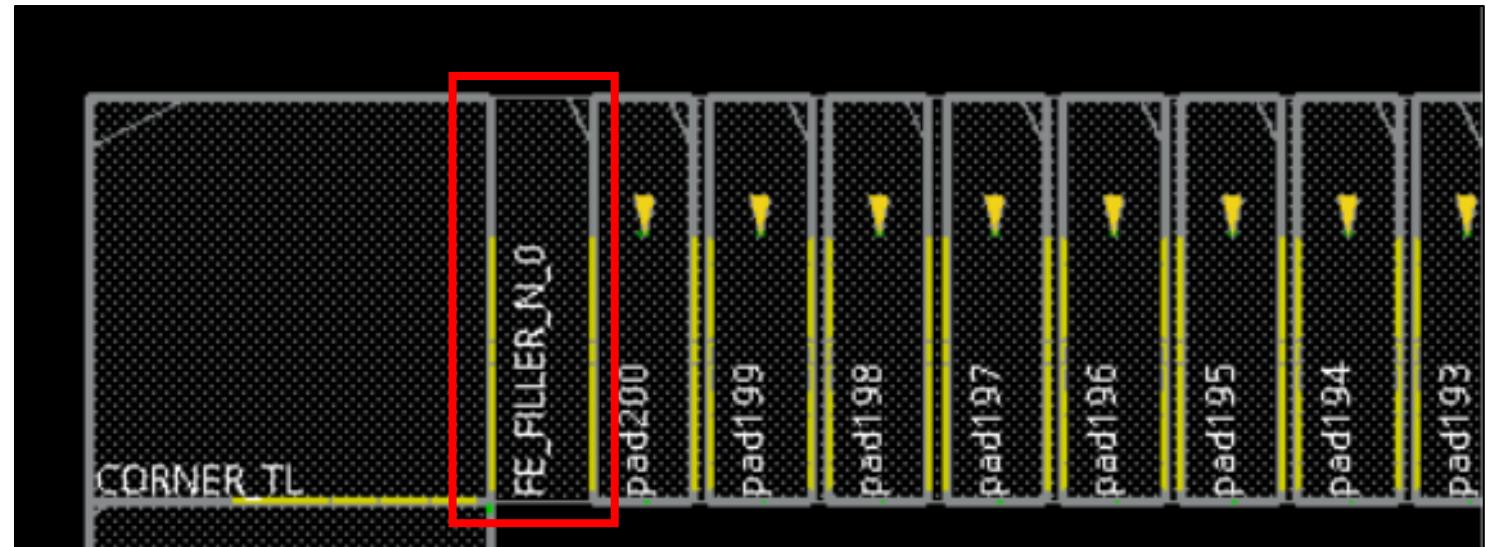
- IO Filler 채우기



Auto PnR

Innovus

- IO Filler 채우기
- 같은 방법으로 Left, Bottom, Right 진행

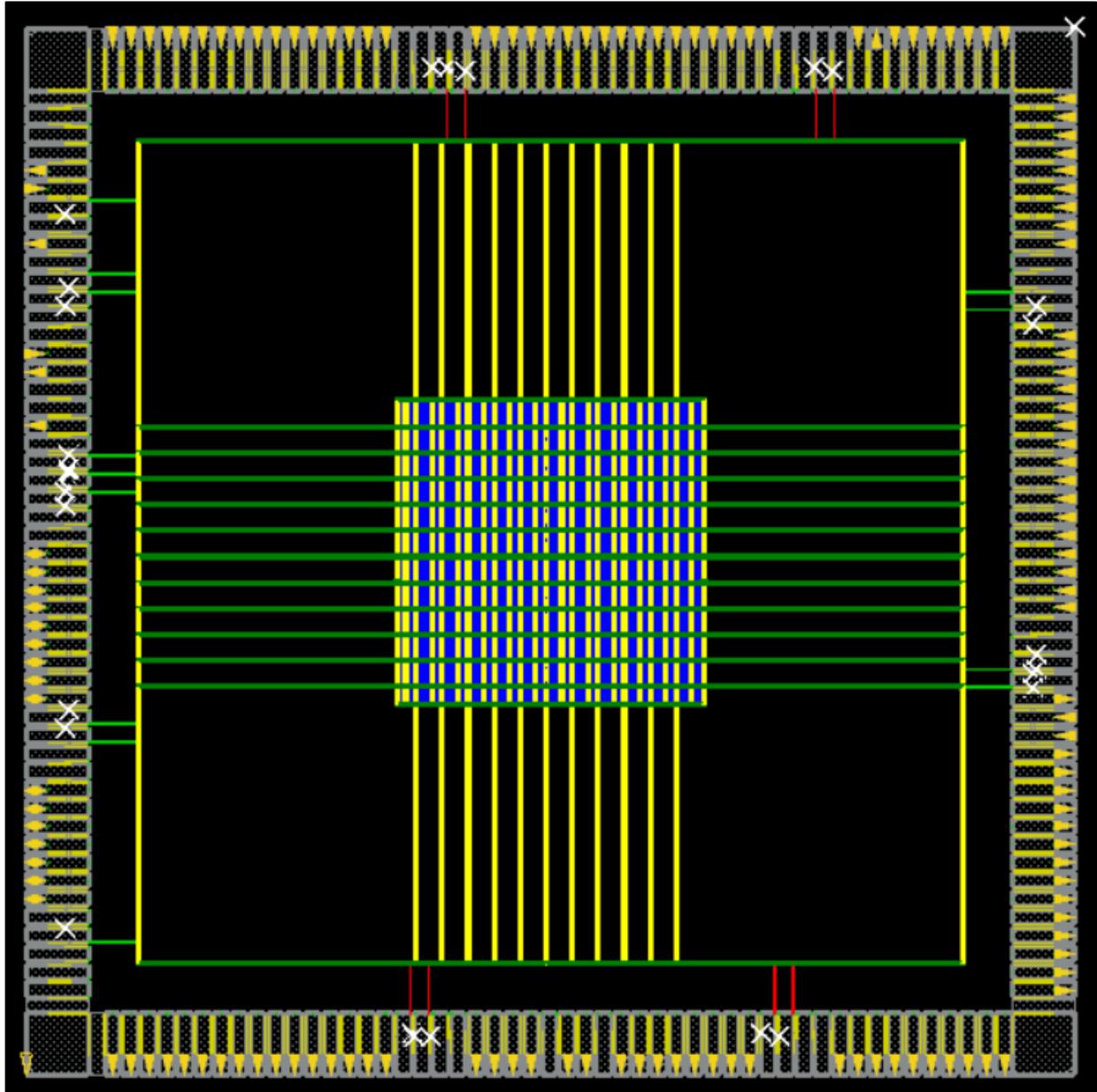


빈 공간이었던 곳이
필러로 채워짐

Auto PnR

Innovus

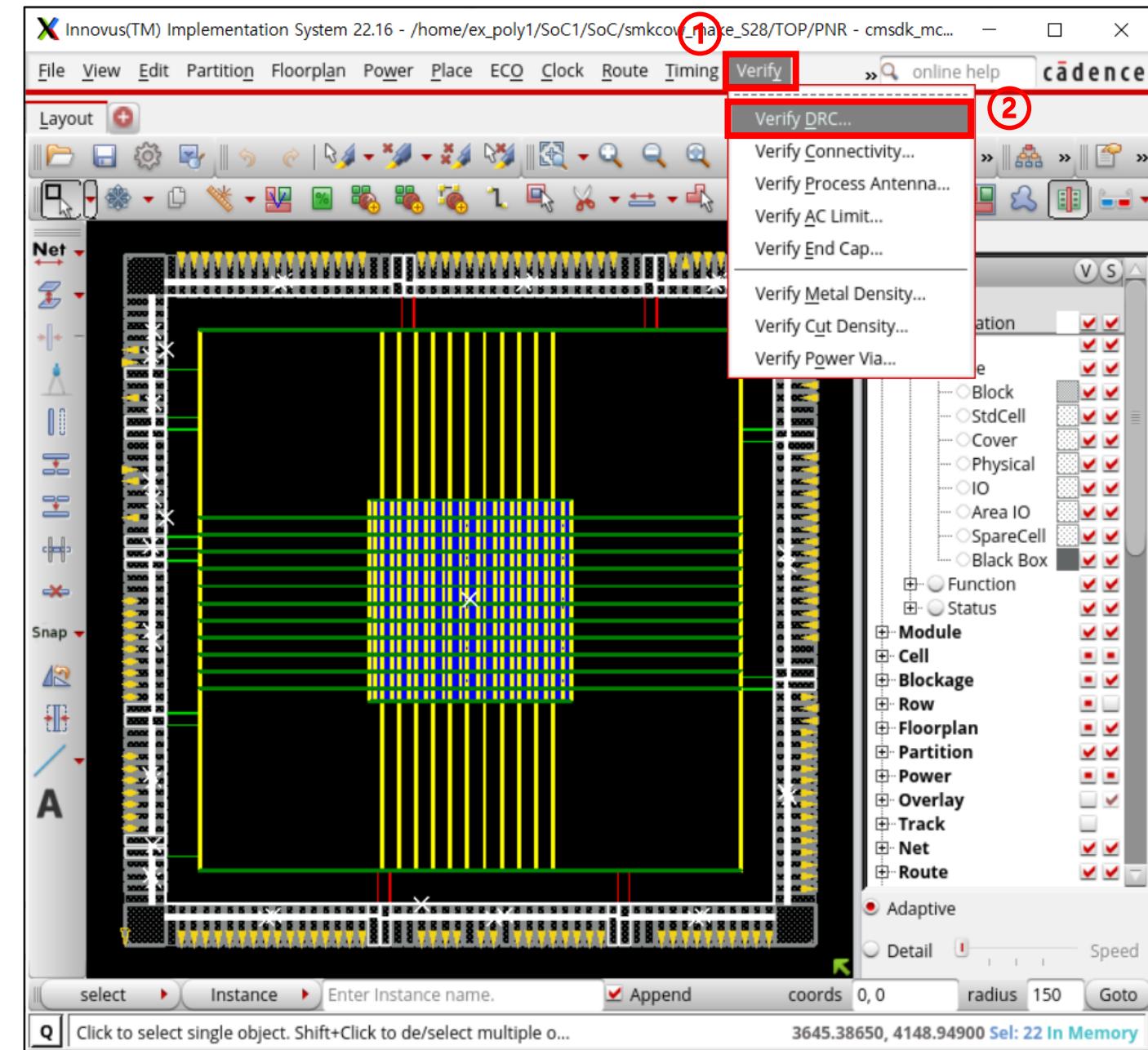
- IO Filler가 전부 채워진 것을 확인함



Auto PnR

Innovus

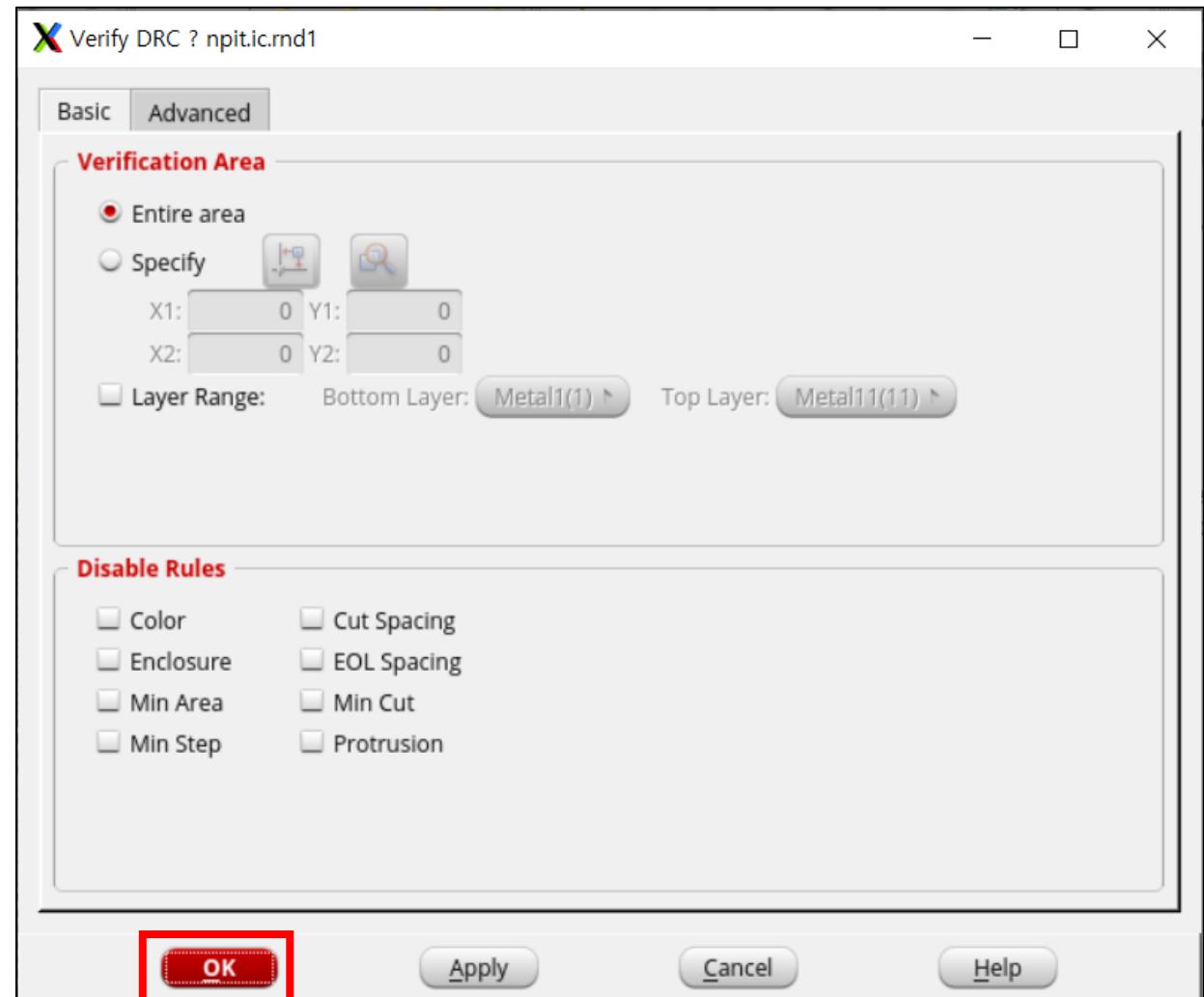
- DRC
- 디자인을 완성했으므로 Verify DRC 진행



Auto PnR

Innovus

- DRC
- OK 클릭



Auto PnR

Innovus

- **DRC**
- Viols가 0으로 이상없음

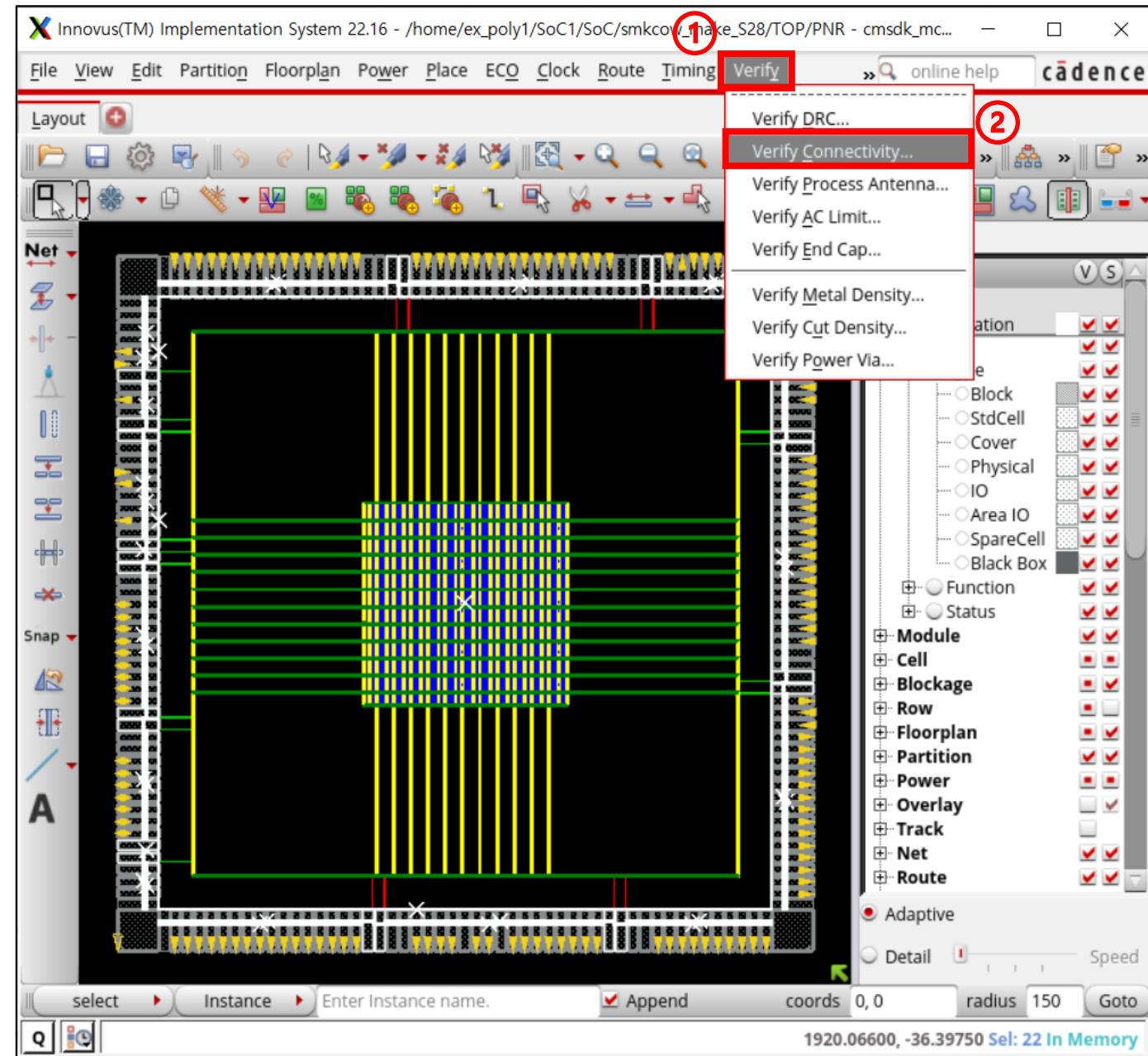
```
Verification Complete : 0 Viols.
```

```
*** End Verify DRC (CPU TIME: 0:00:13.5  ELAPSED TIME: 0:00:13.0  MEM: 264.1M) ***
```

Auto PnR

Innovus

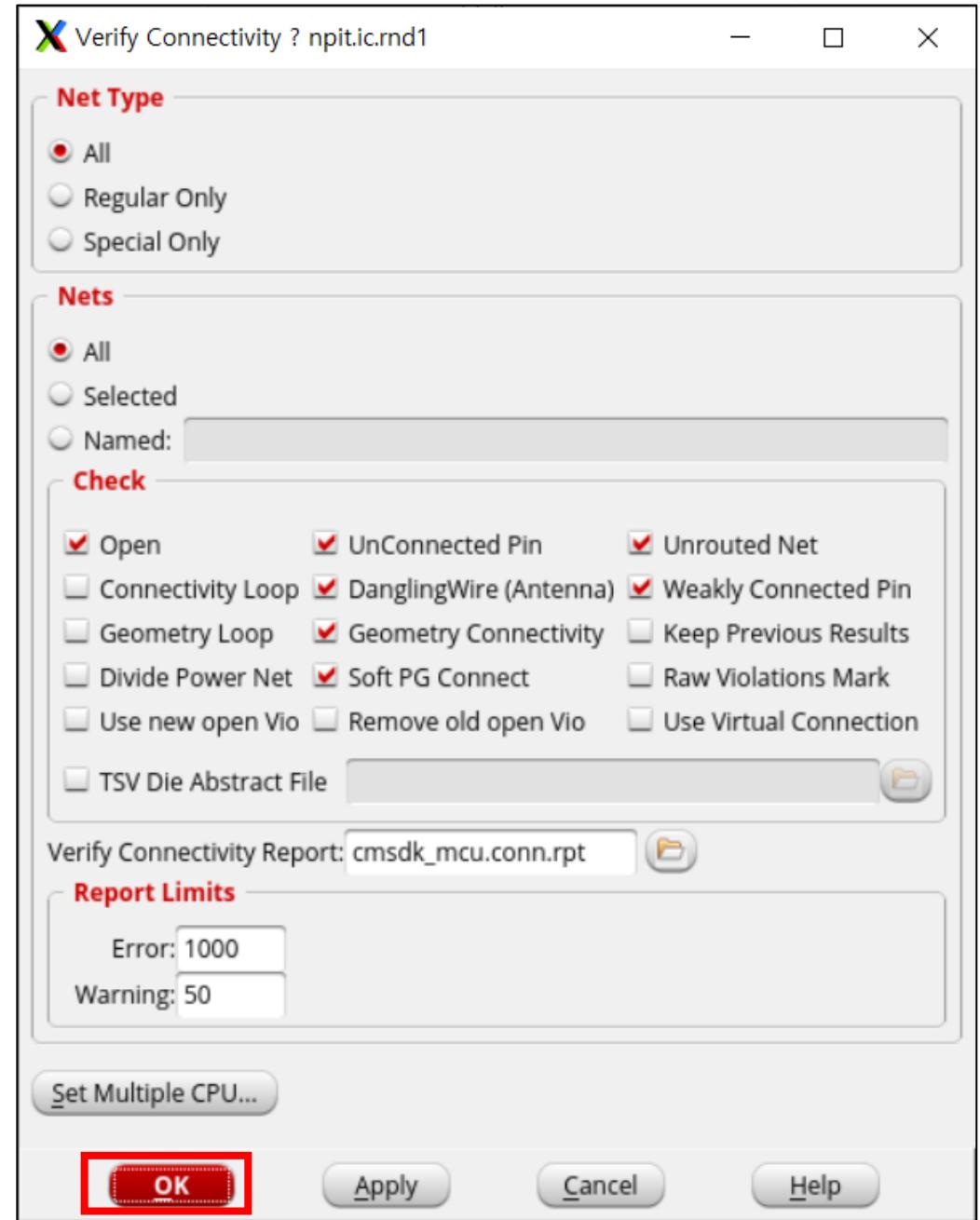
- **Connectivity**
- 디자인을 완성했으므로 Verify Connectivity 진행



Auto PnR

Innovus

- **Connectivity**
- 오른쪽과 같이 설정 후 OK 클릭



Auto PnR

Innovus

- **Connectivity**
- Viols 36개는 모두 Io셀 관련 오류이므로 현재 내 디자인에는 문제가 없음

```
Begin Summary
  1 Problem(s) (IMPVFC-98): Net has no global routing and no special routing.
  4 Problem(s) (IMPVFC-96): Terminal(s) are not connected.
  2 Problem(s) (IMPVFC-200): Special Wires: Pieces of the net are not connected together
  29 Problem(s) (IMPVFC-92): Pieces of the net are not connected together.
  36 total info(s) created.
End Summary

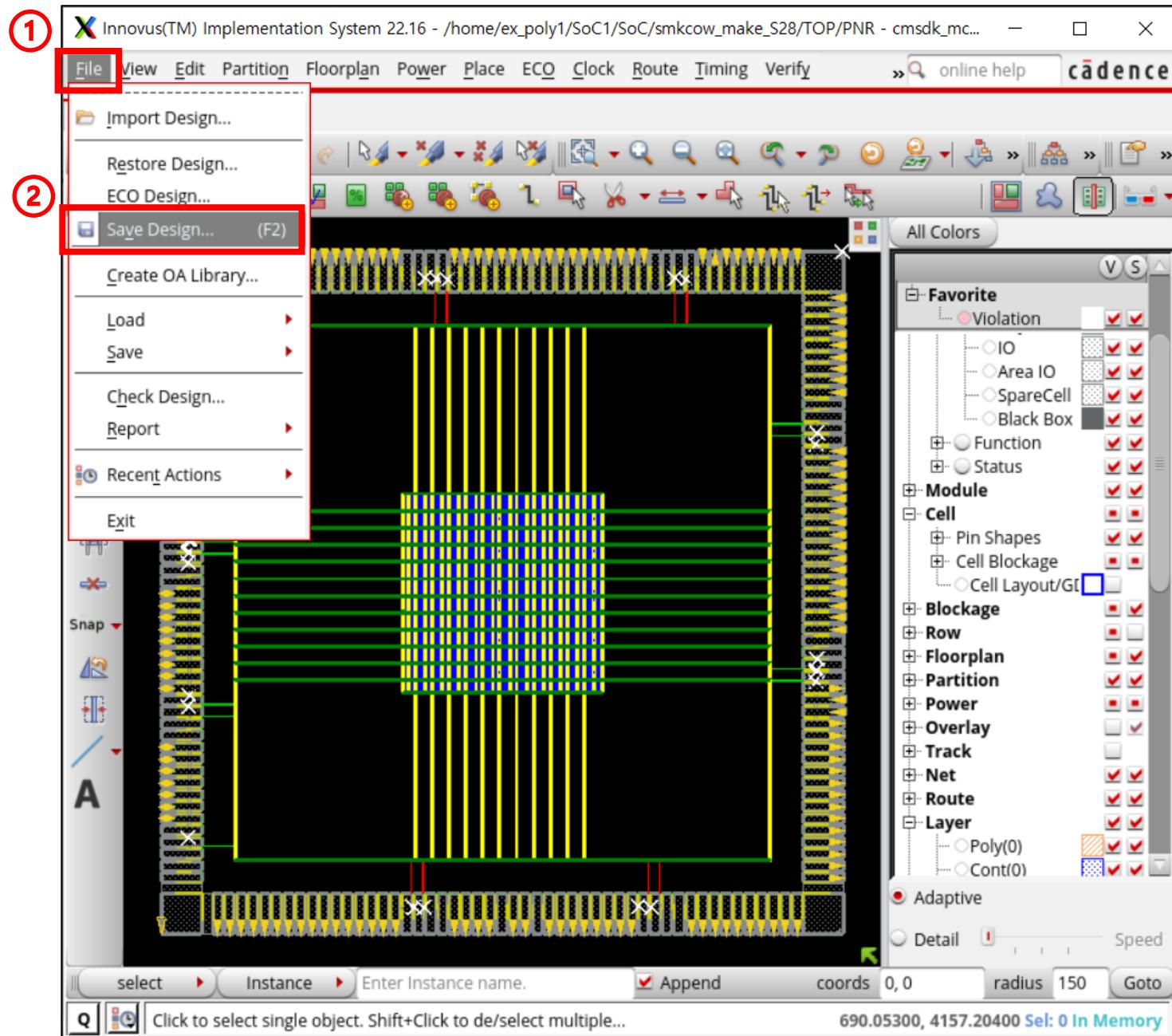
End Time: Thu Feb 27 10:43:08 2025
Time Elapsed: 0:00:01.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 36 Viols. 0 Wrngs.
(CPU Time: 0:00:00.4 MEM: -0.47/M)
```

Auto PnR

Innovus

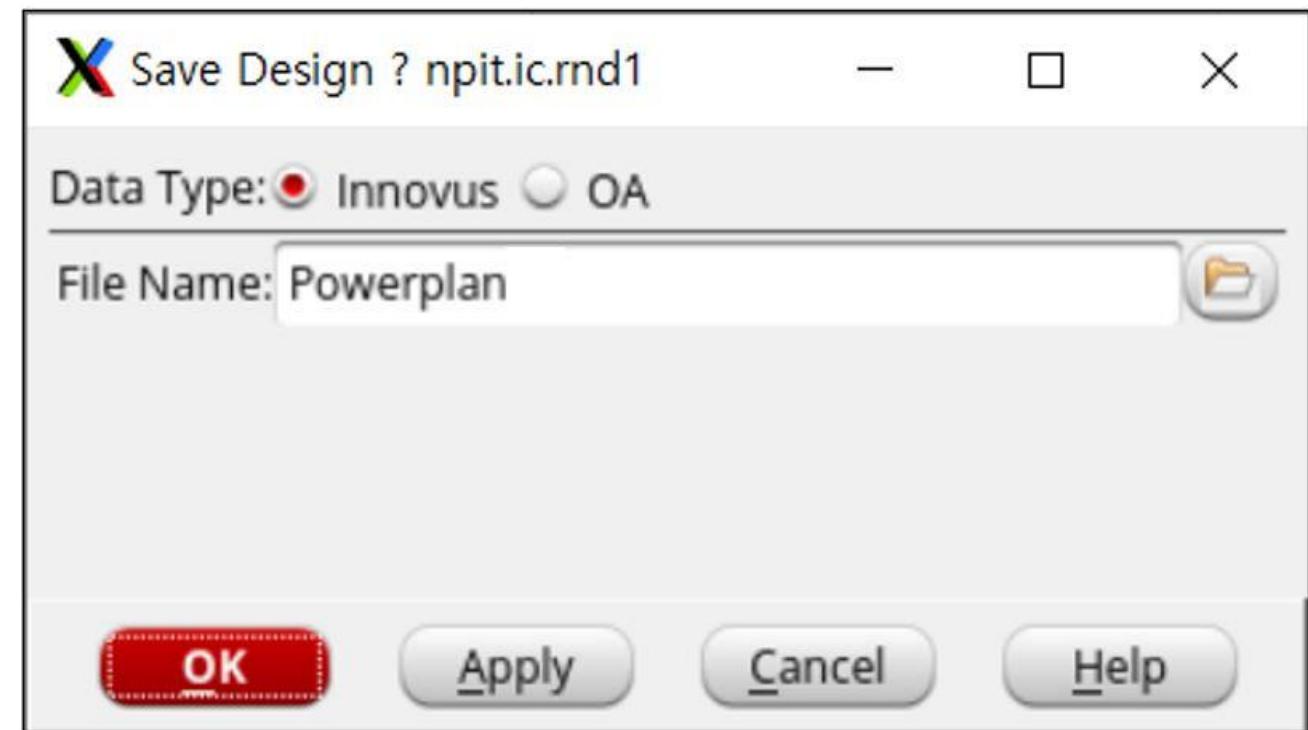
- Save Design
- 디자인에 문제가 없는 것을 확인했으므로 중간 저장함



Auto PnR

Innovus

- **Save Design**
- 디자인에 문제가 없는 것을 확인했으므로 중간 저장함



Auto PnR

Innovus

- **Save Design**
- 문제없이 저장이 완료되었으며 현재 폴더에 저장한 파일이 생성되었음

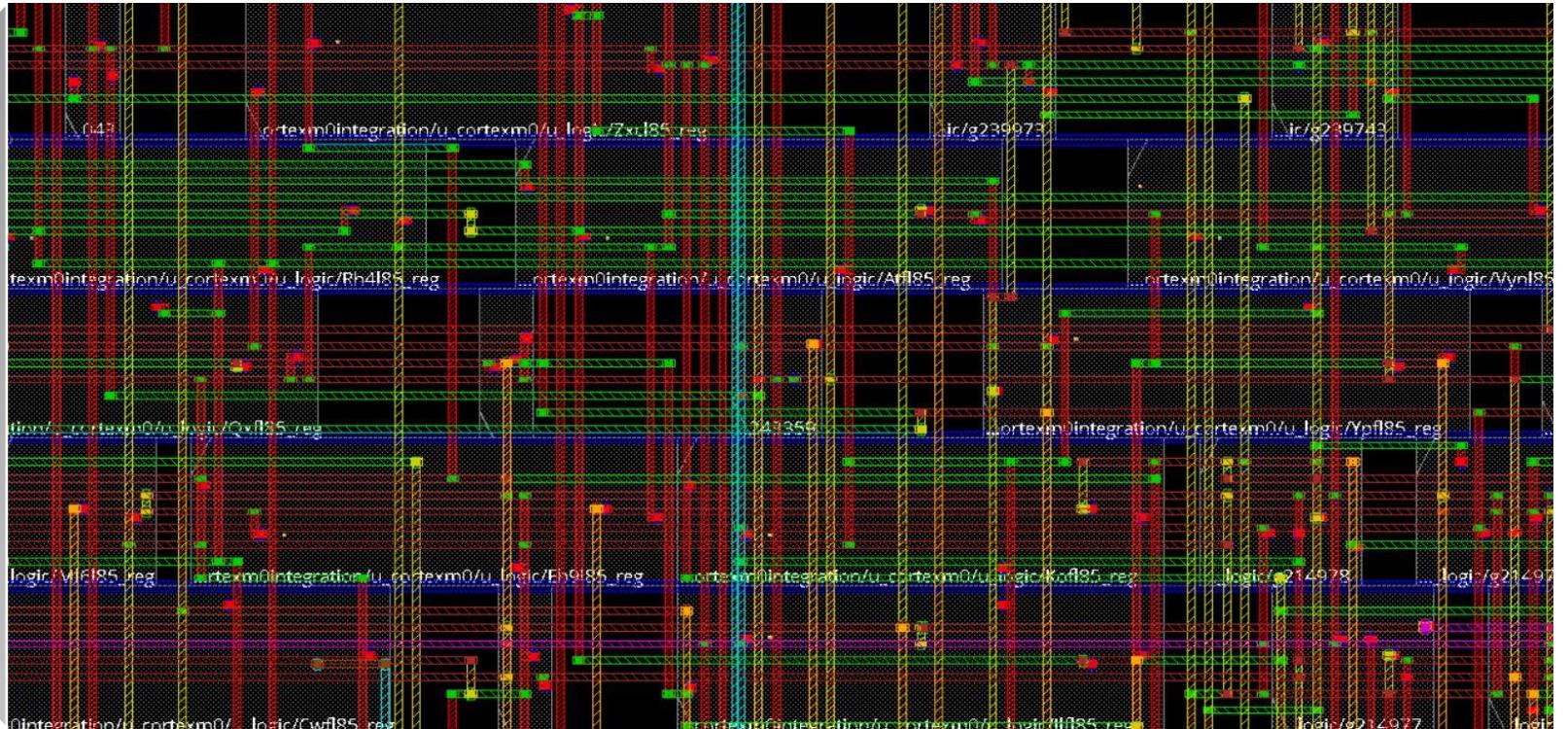
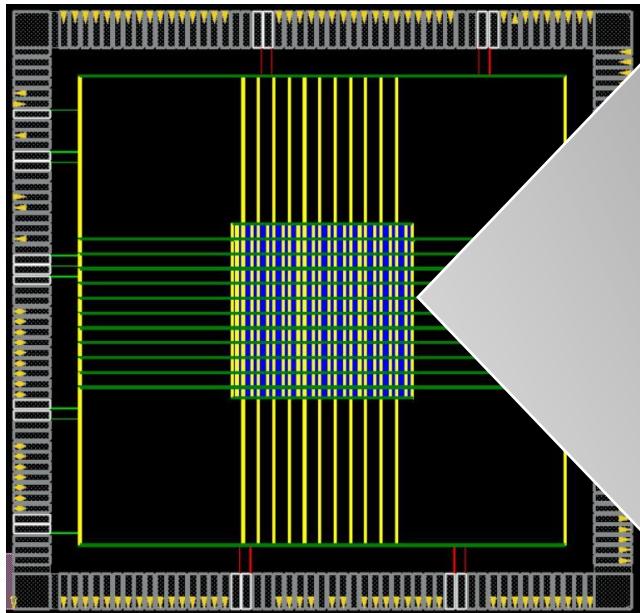
```
#% End save design ... (date=02/26 13:59:24, total cpu=0:00:00.9, real=0:00:01.0, peak re  
s=2554.8M, current mem=2551.3M)  
*** Message Summary: 0 warning(s), 0 error(s)
```

PowerPlan
PowerPlan.dat

Auto PnR

Innovus

- Place: 설계된 회로의 각 부품을 칩 내부 최적의 위치에 배치함



```
118 ## Placement
119 set_db place_global_cong_effort high
120 # First placement
121 #place_design
122 checkPlace cmsdk_mcu.checkPlace
123 # View Density Map
124 setDrawView place
125 getCTSMode -obs_engine -quiet
126 setLayerPreference densityMap -isVisible 1
127 # View Pin Density Map
128 getCTSMode -obs_engine -quiet
129 setLayerPreference pinDensityMap -isVisible 1
130 # report_timing
131 report_timing -gui
132
133 # Placement Optimization
134 place_opt_design
135 report_timing -nworst 10 -max_paths 10 -gui
136 verifyConnectivity -type all -geomConnect -error 1000 -warning 50
137 violationBrowser -all -no_display_false -displayByLayer
138 # Save placeOpt
139 saveDesign placeOpt
140
```

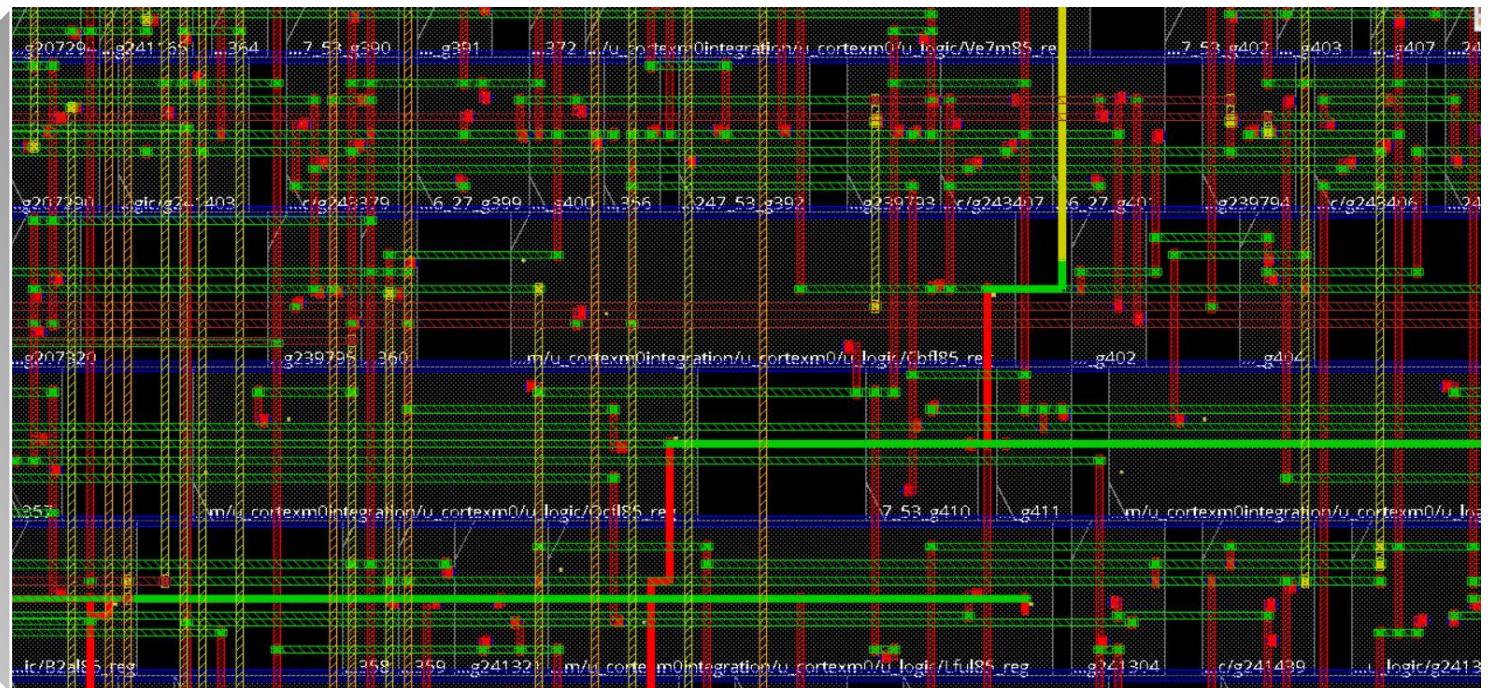
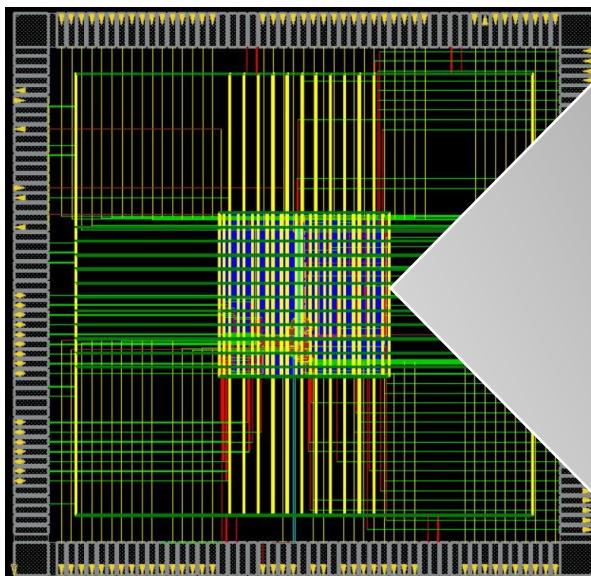
Auto PnR

Innovus

```
141 # CTS  
142 create_ccopt_clock_tree_spec  
143 ccopt_design  
144 saveDesign postCTSopt
```

- CTS: CTS를 진행하므로써 Uncertainty와 Transition, Latency가 확실해짐. (CLK 주기: 7ns)

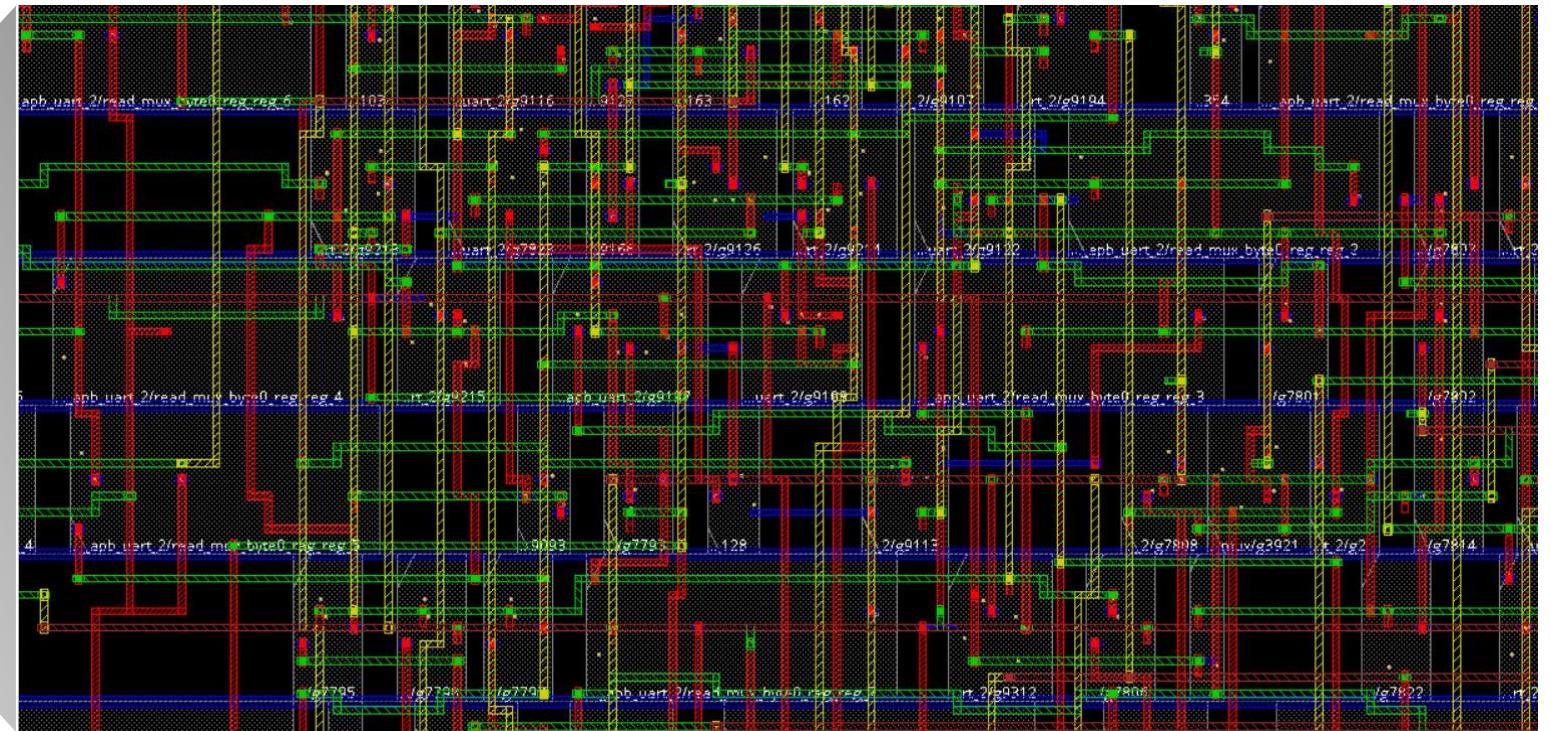
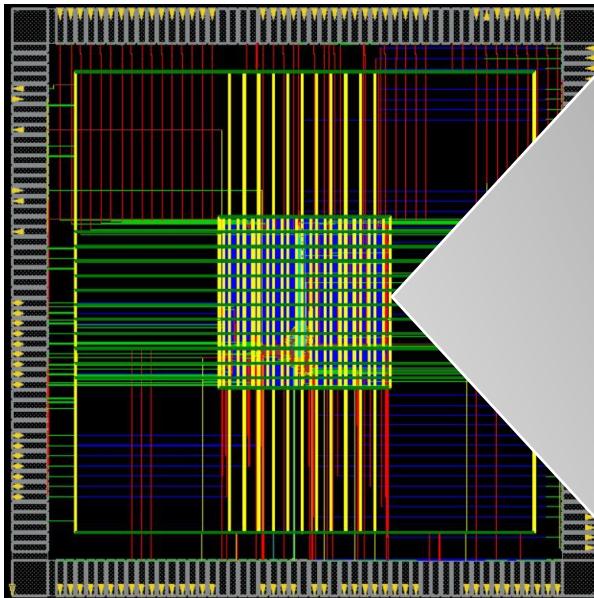
Core 부분을 확대해서 살펴보면 Place 단계에서는 없었던 CLK이 굵게 배선된 것을 확인할 수 있음



Auto PnR

Innovus

- **Routing:** 설계자가 설정한 값에 맞게 배선을 최적화 해주었음



Auto PnR

Innovus

- Operating condition → PnR → Report_timing

Constraint

```
Create_clock -period 7 MAIN_CLOK [get_ports XTAL1]
```

```
Set_clock_latency -source -max 0.2 [get_clocks MAIN_CLOCK]  
Set_clock_latency -max 0.2 [get_clocks MAIN_CLOCK]
```

```
Set_clock_uncertainty -setup 0.1 [get_clocks MAIN_CLOCK]
```

```
Set_clock_transition -setup 0.1 [get_clocks MAIN_CLOCK]
```

```
Set_input_delay -max 0.1 -clock MAIN_CLOCK [all_input]  
Set_input_delay -min 0.01 -clock MAIN_CLOCK [all_input]
```

```
Set_output_delay -min 0.01 -clock MAIN_CLOCK [all_input]  
Set_output_delay -min 0.01 -clock MAIN_CLOCK [all_input]
```

```
69 set_driving_cell -lib_cell PADDI -pin Y -library [get_libs $STD_LIB] [remove_from_collection [all_inputs] [get_ports XTAL1]]  
70  
71 #set_load [load_of $STD_LIB/PADDI/A] [get_ports {TDO XTAL2}]  
72 set_load [load_of PADDI/A] [all_outputs]
```

```
78 set_operating_conditions PVT_0P9V_125C -library [get_libs $STD_LIB] -analysis_type single
```

setup time

- timeDesign -postRoute

timeDesign Summary			
Setup views included: FUNC_SS_WORST			
Setup mode	all	reg2reg	default
WNS (ns):	0.008	0.008	0.020
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	4599	4506	846

- Report_timing -early

Path Groups: {MAIN_CLOCK}	
Analysis View: FUNC_SS_WORST	
Other End Arrival Time	0.082
- Setup	0.141
+ Phase Shift	8.000
- Uncertainty	0.100
= Required Time	7.841
- Arrival Time	7.833
= Slack Time	0.008
Clock Rise Edge	0.000
+ Clock Network Latency (Prop)	0.081
= Beginpoint Arrival Time	0.081

hold time

- timeDesign -postRoute -hold

timeDesign Summary			
Hold views included: FUNC_FF_BEST			
Hold mode	all	reg2reg	default
WNS (ns):	0.002	0.028	0.002
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	4599	4506	846

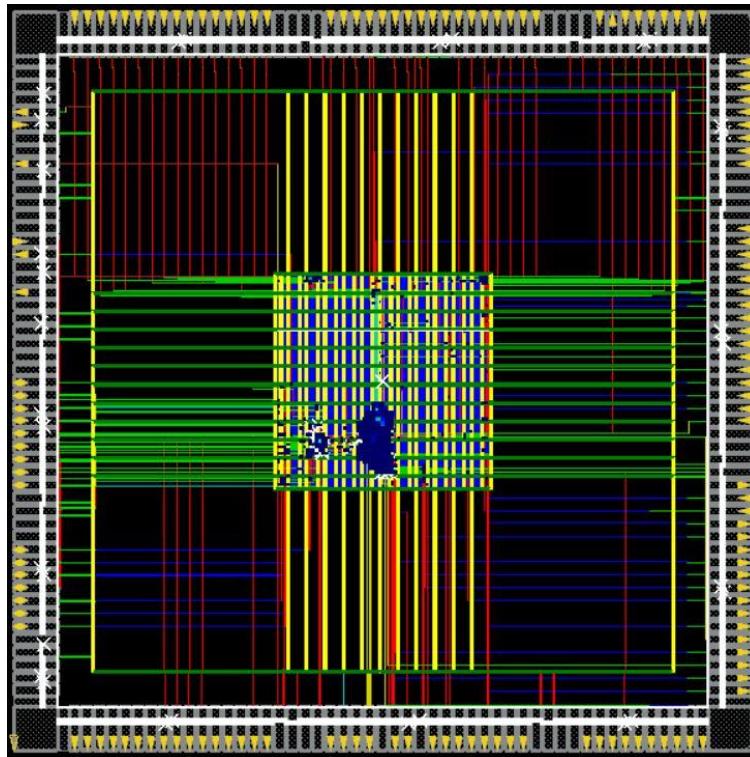
- Report_timing -late

Path Groups: {MAIN_CLOCK}	
Analysis View: FUNC_FF_BEST	
Other End Arrival Time	1.610
+ Hold	-0.000
+ Phase Shift	0.000
= Required Time	1.609
Arrival Time	1.611
Slack Time	0.002
Clock Rise Edge	0.000
+ Input Delay	0.010
+ Drive Adjustment	0.725
+ Source Insertion Delay	0.200
= Beginpoint Arrival Time	0.934

Auto PnR

Innovus

- DRC, Check connectivity: PnR 과정에서 발생한 에러 확인



- Verify 진행



Violation Type:

- CheckPlace (74/74)
 - Placement (74/74)
 - TechSite (74/74)- Verify (32/32)
 - Connectivity (32/32)
 - Open (31/31)
 - UnConnPin (1/1)
 - Metal4(4) (1/1)

Violation:

LAYER	OBJECT1	LOCATION
VDD		(3160, 3873)
VSS		(3090, 3859)
VDD		(3873.39, 29)
VSS		(3859.5, 302)
Metal4(4)	VDD	(145.5, 2329)
VDD		(145.38, 309)
VDD		(145.38, 239)
VDD		(239, 3873.3)
VSS		(159.265, 33)
VSS		(159.265, 22)
VSS		(239, 3859.5)

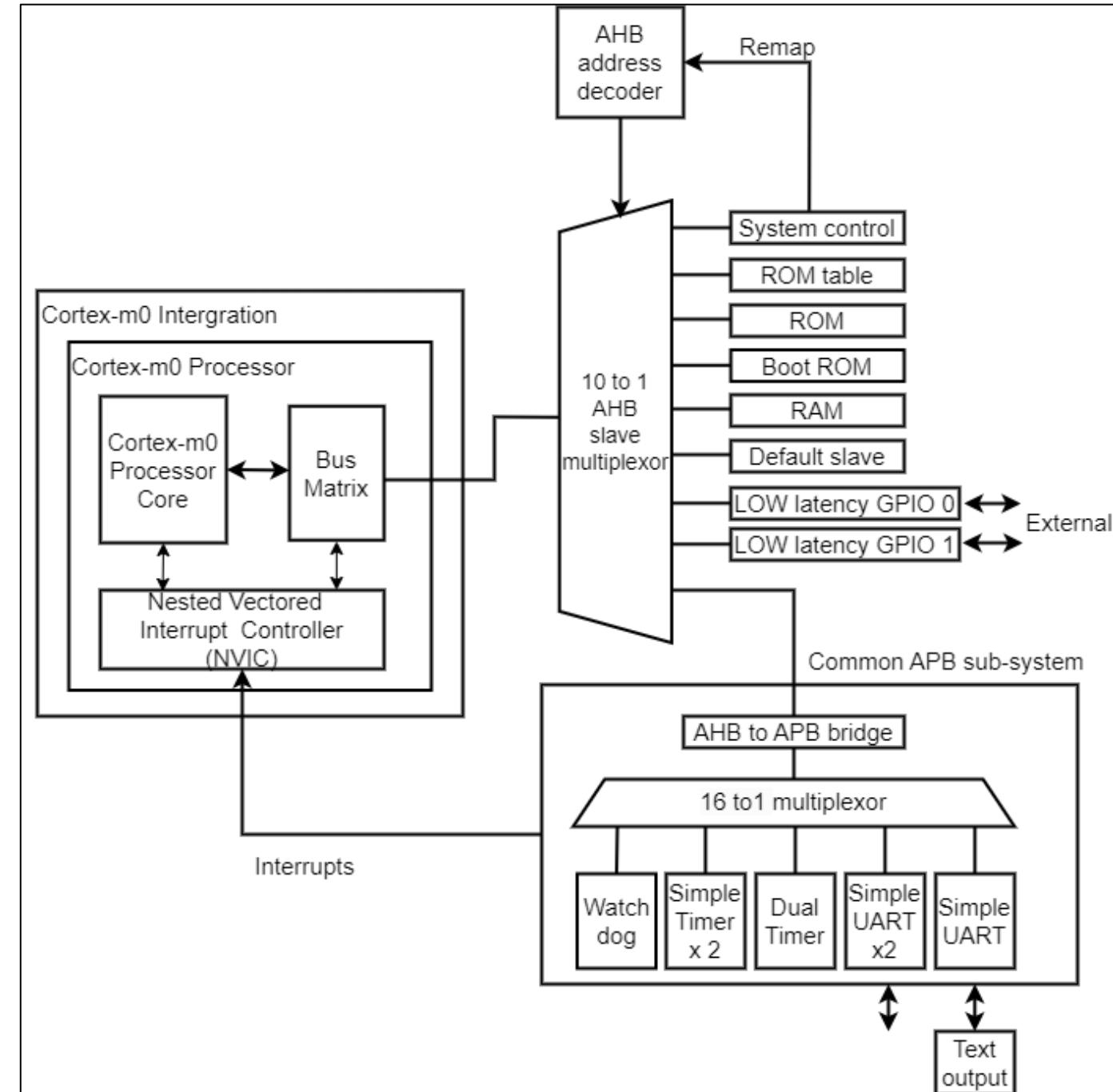
- Verify 32는 IO영역에 대한 것이기 때문에 스kip 가능하며 CheckPlace는 Place 단계에서 나온 TechSite 이슈이므로 스kip 가능하다. 또한 DRC 파트는 보이지 않으므로 해당 PnR에는 문제가 없음을 확인할 수 있다.

감사합니다

Function Simulation

ARM Cortex-M0 시스템 구조

- NVIC: 여러 개의 인터럽트가 동시에 발생할 경우, NVIC는 미리 설정된 우선순위에 따라 어떤 interrupts를 먼저 처리할지 결정
- Interrupts: 컴퓨터 시스템이 외부의 자극에 즉각적으로 반응하고, **다양한 작업을 효율적으로 처리할 수 있도록 하는 중요한 메커니즘**



Function Simulation

ARM Cortex-M0 시스템 구조

- 향후 연구과제
 - SoC의 기능을 확장하기 위해 IP들을 추가

