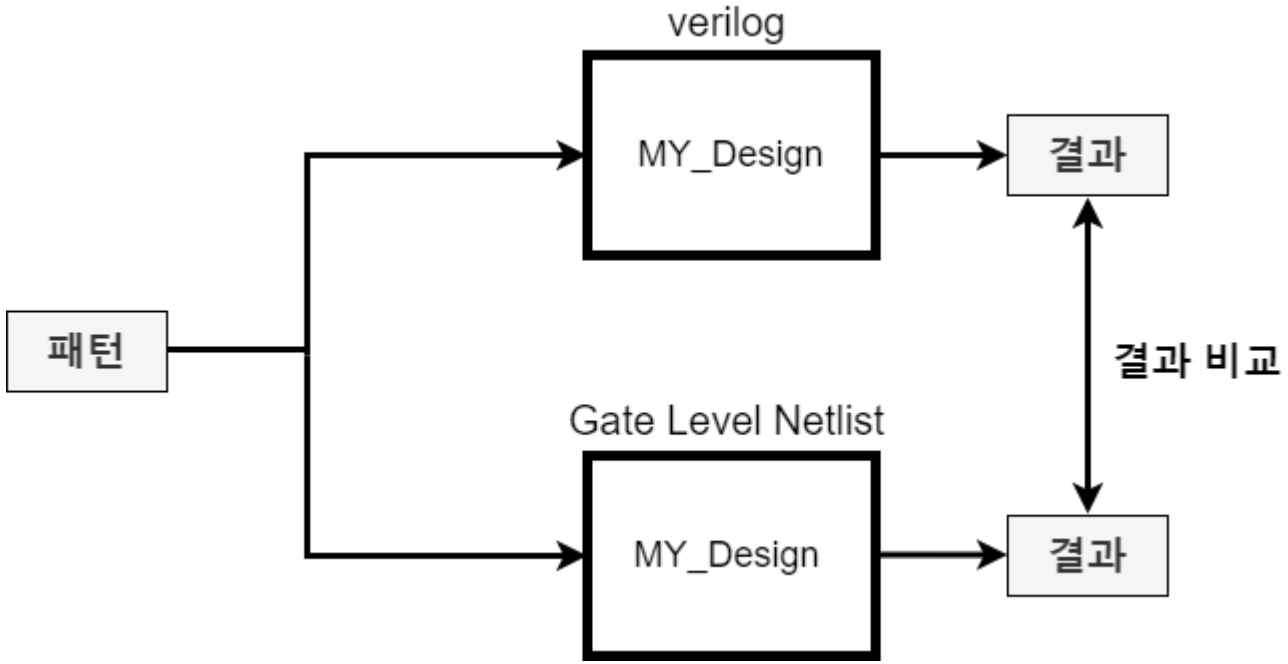
Equivalence Check

Equivalence Check

Equivalence Check란?

- 합성 전의 Verilog 소스와 합성 후의 Gate Level Netlist를 비교하는 툴 ➔ 합성 시의 오류유무 추출
- **비교방법_0:** 디자인의 input과 output, reg, net의 이름이 동일한 지의 여부를 확인
- **비교방법_1:** 동일한 임의의 패턴을 입력한 뒤 결과가 동일한 지의 여부를 확인

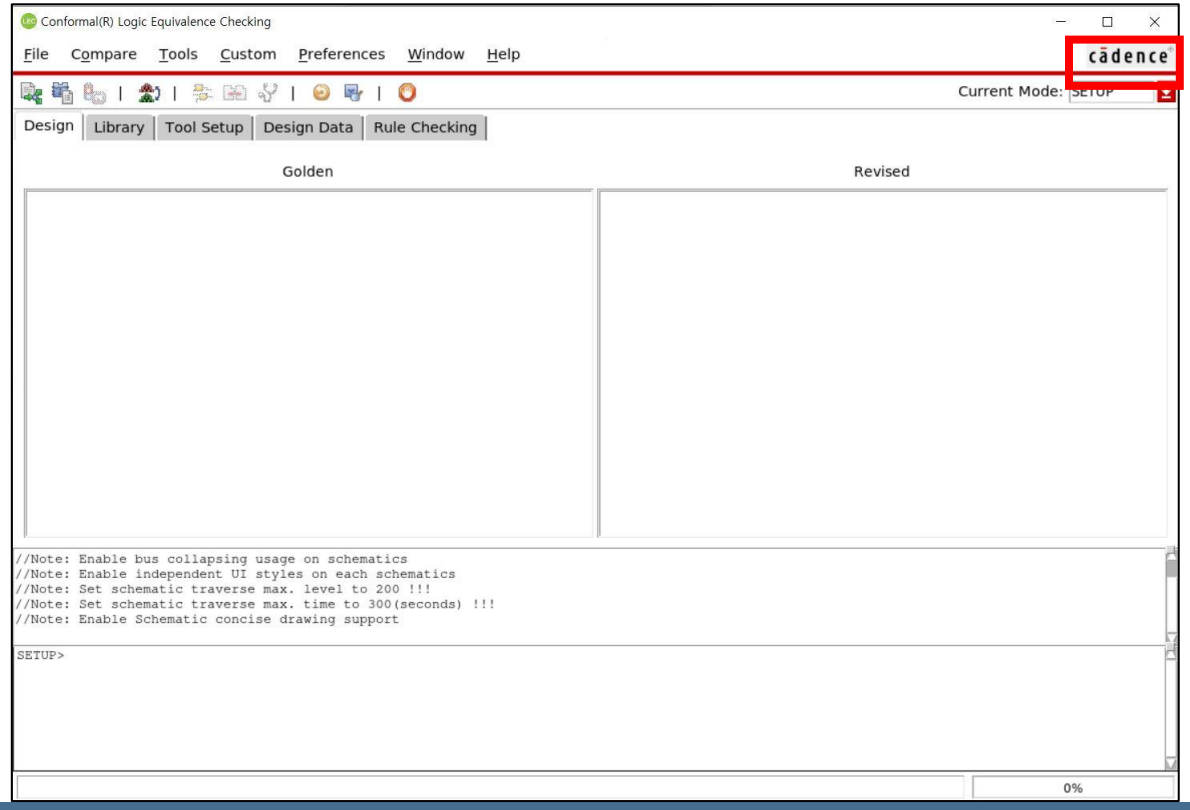


Equivalence Check

ConformaI이란?

- Equivalence Check를 하기 위해 사용하는 툴

- ConformaI을 사용하기 위해서는 lec라는 명령어를 사용함



LAB을 위한 환경설정 파일

Equivalence Check

Conformal

- 툴 사용을 위한 README 파일 확인

$> vi README_HowtoRun

```
/home/ex_poly1/SoC2/SoC/smkcow_make_S28/TOP/Equivalence_check
```

```
[ex_poly1@npit Equivalence_check]$ ls
README_HowtoRun  log  script
```

Equivalence Check

Conformal

- 툴 사용을 위한 README 파일 확인

$> vi README_HowtoRun

```
1 $> lec
2
3 After lec is invoked, type the below command at the console
4 SETUP> dofile ./script/script.tcl
```

README 파일의 내용확인

1. lec를 실행
2. lec가 뜨면 4행의 문장을 SETUP>으로 시작하는 콘솔에 입력함

Equivalence Check

Conformal

- 툴 사용을 위한 README 파일 확인

$> vi README_HowtoRun

```
1 $> lec
2
3 After lec is invoked, type the below command at the console
4 SETUP> dofile ./script/script.tcl
```

커서를 위치시킨 뒤 g+f

Synthesis

genus

- 툴 사용을 위한 README 파일 확인
- script.tcl 파일 확인

```
 1 set log file ./log/all.log -replace
 2
 3 read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045
   _all_v4.4/gsclib045/verilog/slow_vdd1v0_basicCells.v -verilog -both
 4
 5 #Below is the same with the above
 6 #read library -liberty -both \
 7     ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/timing/fast_vdd1v0_basicCells.lib \
 8     ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/timing/slow_vdd1v0_basicCells.lib \
 9     ../../../../GPDK045/digital/giolib045_v3.5/timing/pads_SS_s1vg.lib
10
11 read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.
   v ../../../cortexm0_designstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final
   .v -verilog -golden
12
13 read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
14
15 set system mode lec
16
17 add compare points -all
18
19 compare
20
21 report verification
22 report statistics
```

LAB

Equivalence Check

Conformal

$> lec

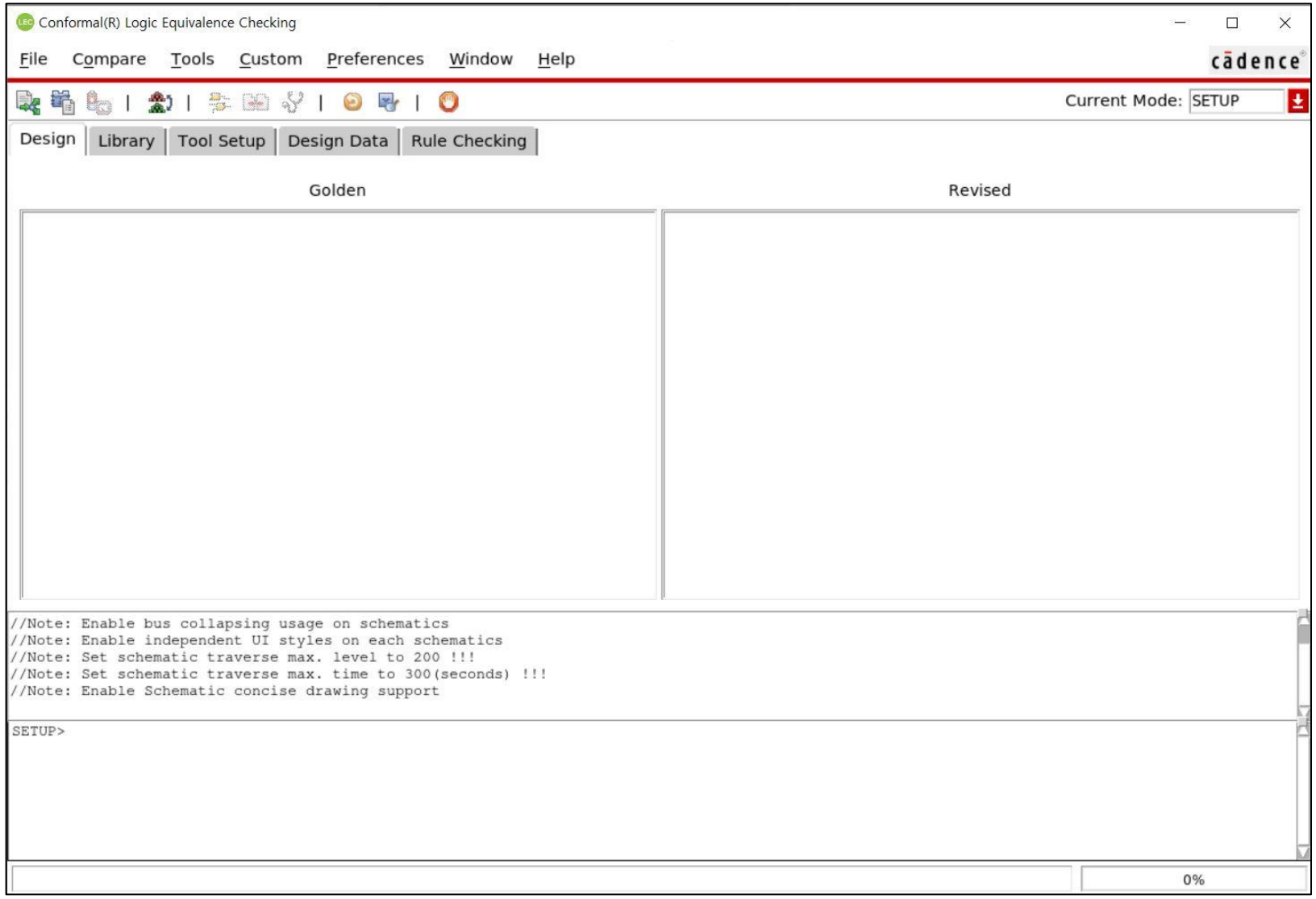
```
[ex_poly1@npit Equivalence_check]$ lec
                         CONFORMAL (R)
                  Version 22.10-s300 (29-Aug-2022) (64 bit executable)
   Copyright (c) Cadence Design Systems, Inc., 1997-2022. All Rights Reserved


This program is proprietary and confidential information belonging to
Cadence Design Systems, Inc., and may be used and disclosed only as authorized
in a license agreement controlling such use and disclosure.

// Warning: This version is 874 days old. You can download the latest version from http://downloads.cadence.com.

// Check out Conformal_Asic 22.1 license
```

Equivalence Check

Conformal

$> lec

- Gui가 뜨는 것을 확인할 수 있음

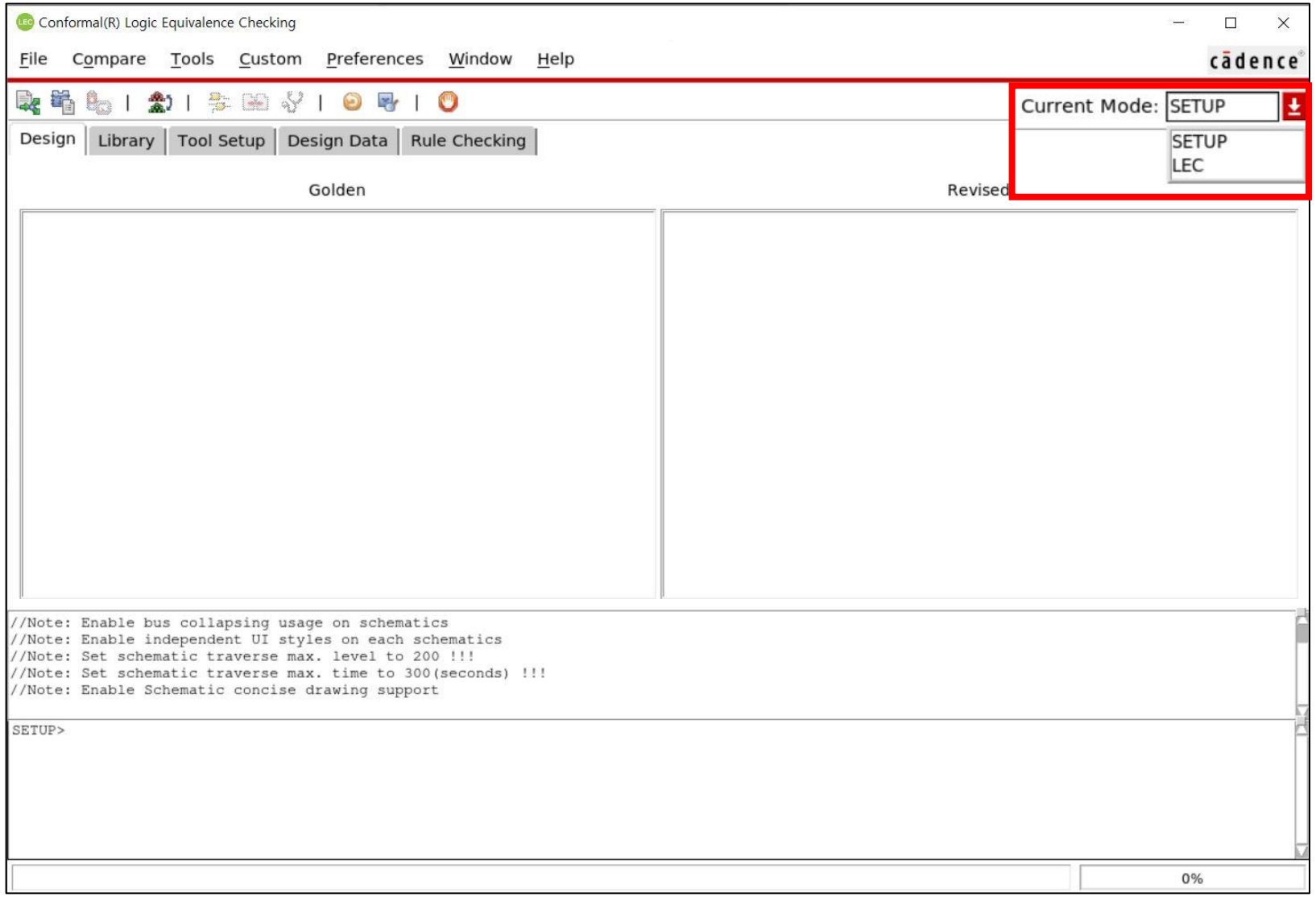


Equivalence Check

Conformal

$> lec

- Current Mode를 보면 SETUP과 LEC로 나누어져 있는 모습을 볼 수 있음
- SETUP은 Verilog 소스, 공정사에서 제공한 STD셀, Gate Level Netlist 등을 불러오는 모드
- LEC는 이름 비교와 패턴을 이용한 비교를 하는 모드임

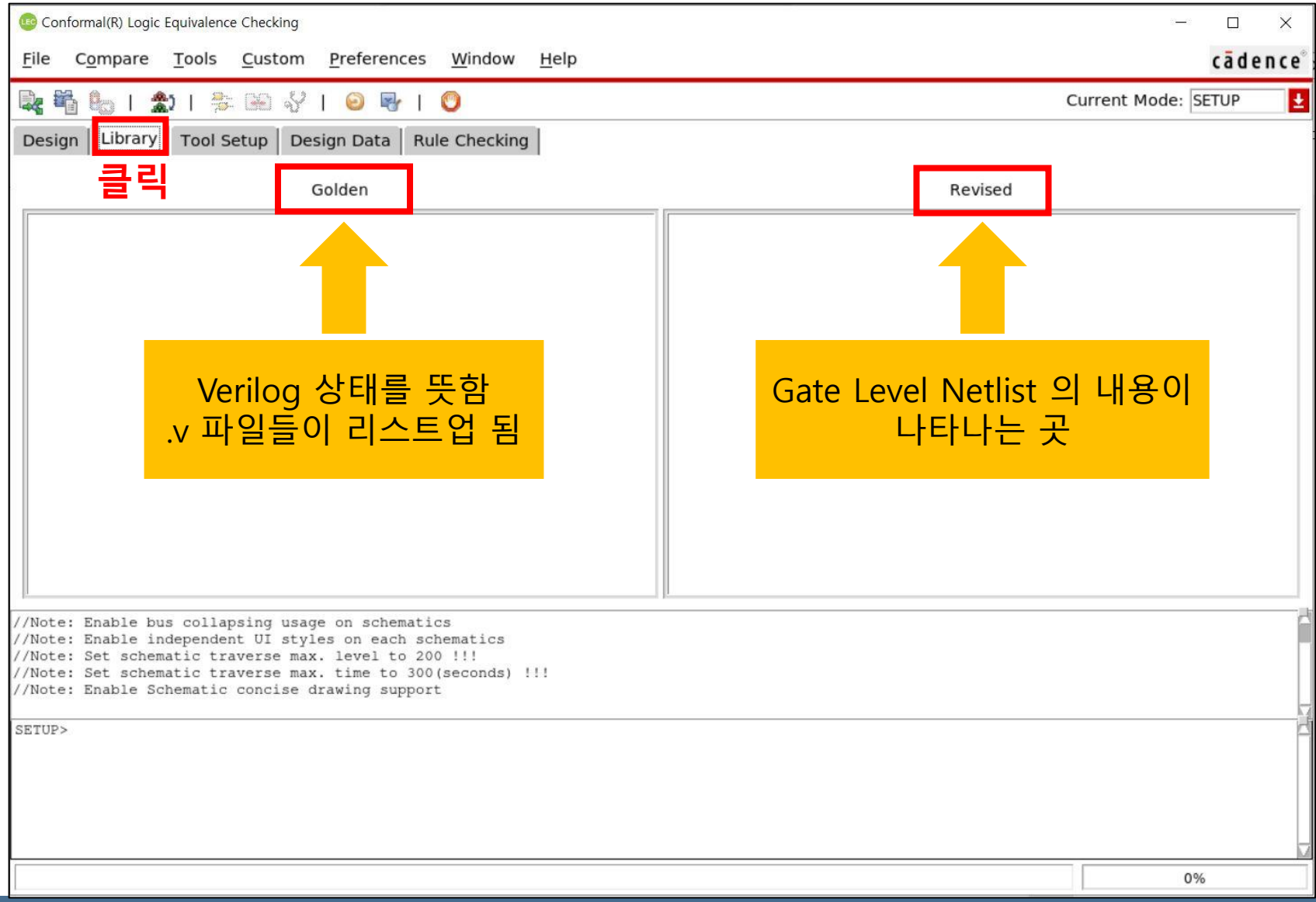


Equivalence Check

Conformal

$> lec

- Golden: 합성 전의 Verilog 소스와 관련 파일들
- Revised: 합성 후의 Gate Level Netlist와 관련 파일들

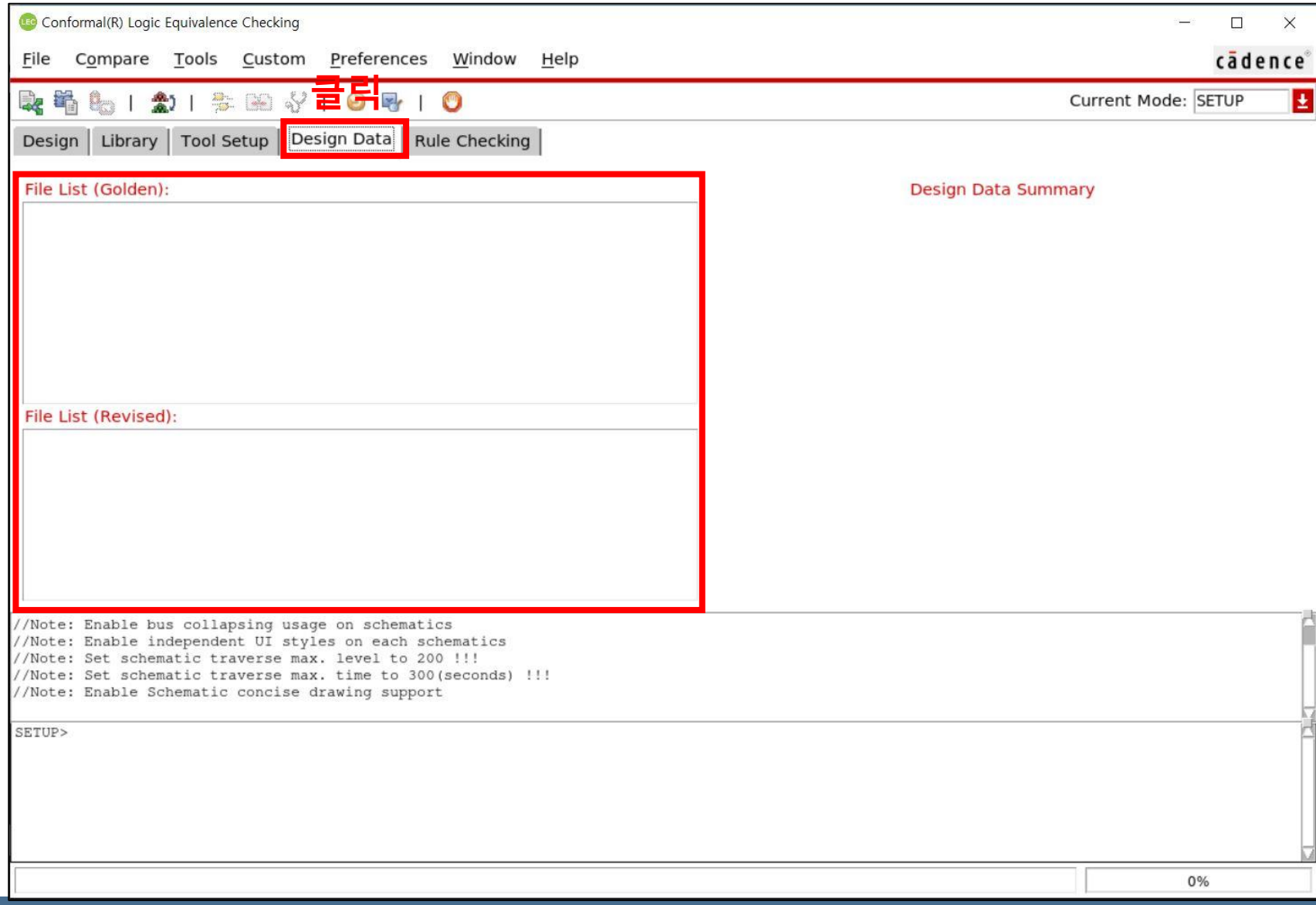


Equivalence Check

Conformal

$> lec

- Design Data: Verilog 소스와 Gate Level Netlist 가 리스트업 되는 페이지

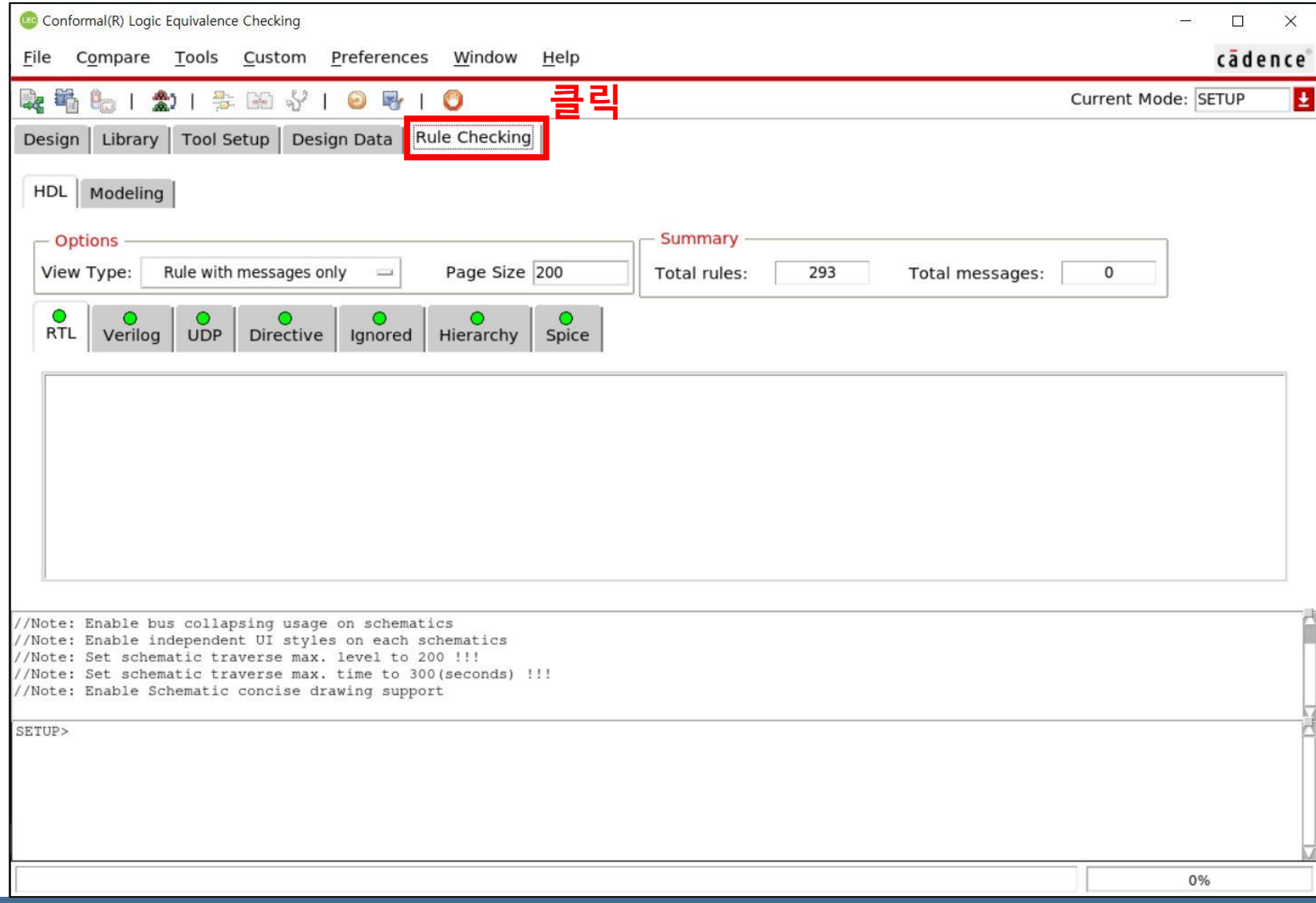


Equivalence Check

Conformal

$> lec

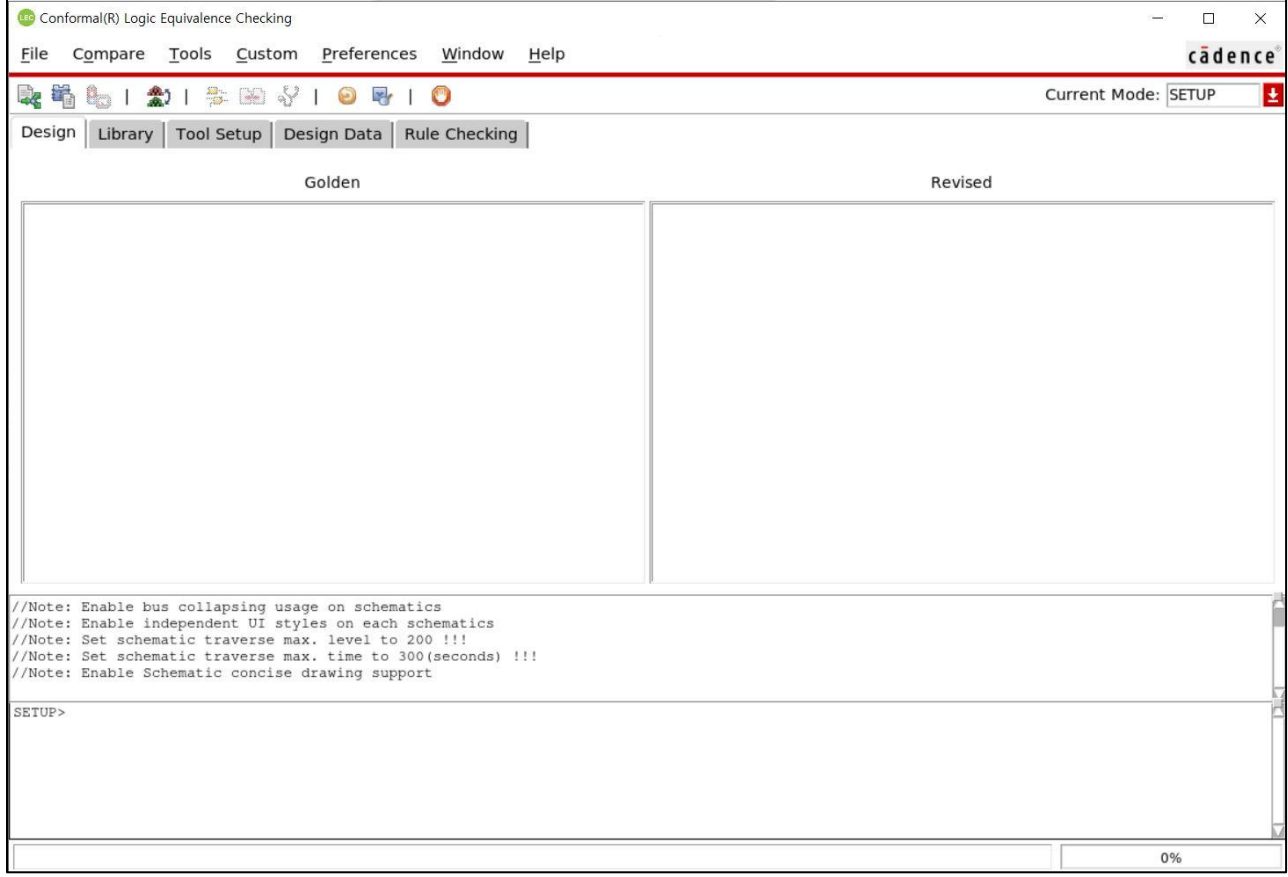
- 비교를 위한 법칙을 확인 및 수정할 수 있는 페이지



Equivalence Check

Conformal

- 터미널 두개를 사용함
- 하나는 lec, 다른 하나는 vi script/script.tcl 명령 실행

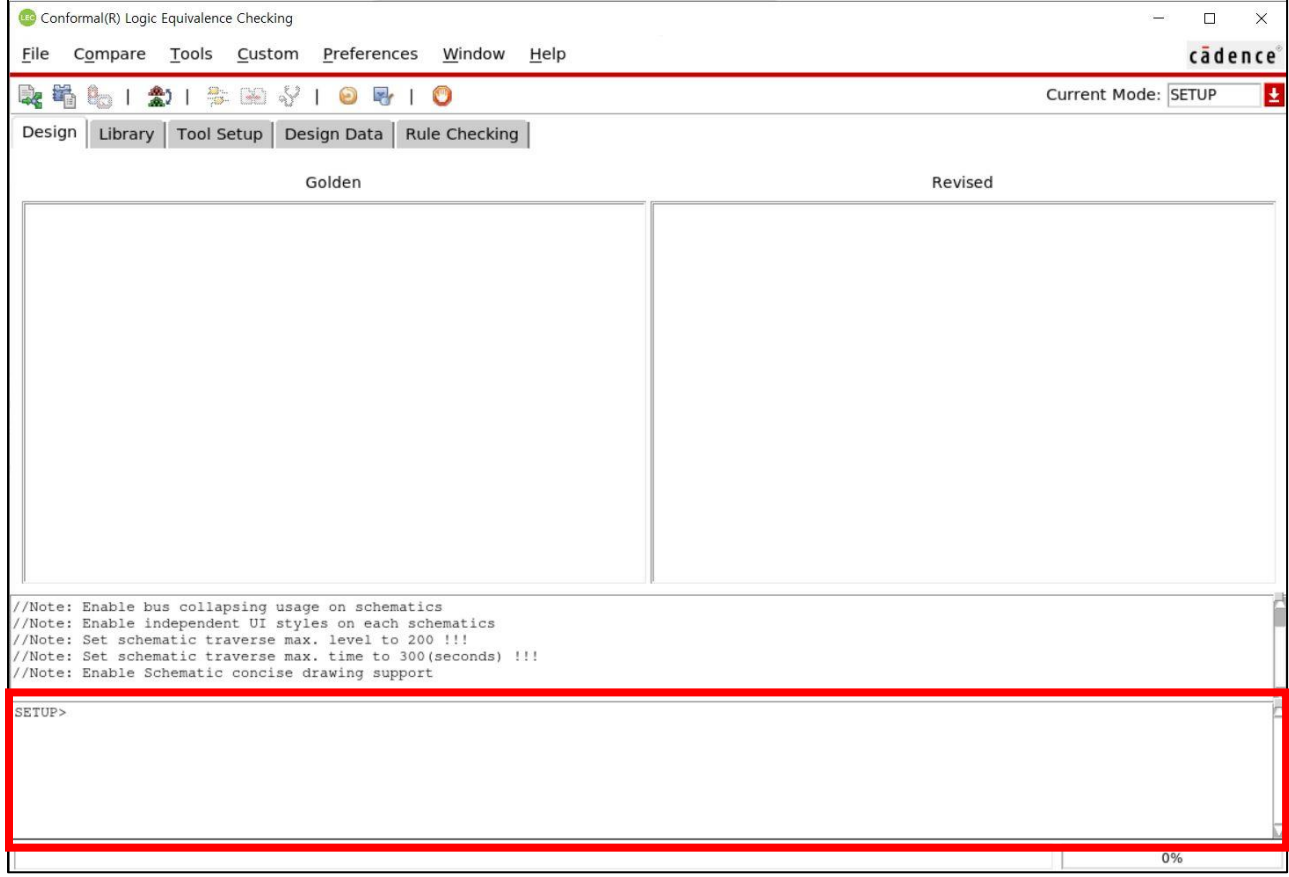



```
1 set log file ./log/all.log -replace
2
3 read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
  erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5 read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
  esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7 read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9 set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Equivalence Check

Conformal

- vi script/script.tcl 파일의 내용을 참고하여 SETUP> 에 직접 입력하는 방식으로 진행




```
1 set log file ./log/all.log -replace
2
3 read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/verilog/slow_vdd1v0_basicCells.v -verilog -both
4
5 read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_designstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7 read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9 set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Equivalence Check

Conformal

- 현재 위치에 로그 파일을 담을 예정
- 기존의 로그 파일과 교체함

툴 실행 결과

```
README_HowtoRun log/            script/

all.iog  all.log  all.log~
SETUP> set log file ./log/all.all.log -replace
// Command: set log file ./log/all.all.log -replace

SETUP>
SETUP> set log file ./log/all.all.log -replace
SETUP>
```

```
1 set log file ./log/all.log -replace
2
3 read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
  erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5 read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
  esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7 read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9 set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Equivalence Check

Conformal

- .v로 되어있는 Digital library 파일을 입력 함 (STD셀, IO셀)
- 학습을 위해 직접 입력

```
[ex_poly1@npit Equivalence_check]$ pwd
/home/ex_poly1/SoC2/SoC/smkcow_make_S28/TOP/Equivalence_check
[ex_poly1@npit Equivalence_check]$ cd ../
[ex_poly1@npit TOP]$ ls
Equivalence_check  RTL  SIM  SYN
[ex_poly1@npit TOP]$ cd ../
[ex_poly1@npit smkcow_make_S28]$ ls
TOP  fifo_uart_mem  memory_wrapper
[ex_poly1@npit smkcow_make_S28]$ cd ../
[ex_poly1@npit SoC]$ ls
cortexm0_designstart  smkcow_make_S28
[ex_poly1@npit SoC]$ cd ../
[ex_poly1@npit ~/SoC2]$ ls
GPDK045  SoC  ggw
```

현재 위치에서 상위 폴더 네 번째에 있음

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RT   msdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implem   ation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read de   k_mcu_syn_final.v -verilog -revised
8
9  set sys
10
11 add compare points -all
12
13 compare
14
15 report verification
```

GPDK045가 있는 경로 지정

Equivalence Check

Conformal

- .v로 되어있는 Digital library 파일을 입력 함 (STD셀, IO셀)

- 학습을 위해 직접 입력

read library입력 → ../ 입력 → tab키 사용 → ../ 입력 → tab키 사용..
(GPDK045 폴더를 찾을 수 있음)

```
Equivalence_check/ RTL/                    SIM/
SYN/

TOP/              fifo_uart_mem/   memory_wrapper/

cortexm0_designstart/ smkcow_make_S28/

GPDK045/ SoC/      ggw/
SETUP> read library ../../../../
```

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RT   msdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implem   ation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read de   k_mcu_syn_final.v -verilog -revised
8
9  set sys
10
11 add compare points -all
12
13 compare
14
15 report verification
```

GPDK045가 있는 경로 지정

Equivalence Check

Conformal

- lo셀 라이브러리 입력
- 경로 지정 후 tab키를 사용하여 동일한 방법으로 입력함

```
GPDK045/ SoC/     ggw/

analog/  digital/

SRAM1RW512x32.v     TEST/               giolib045_v3.5/
gsclib045_all_v4.4/

AMSFF_database_diagram.pdf   Release_Note.txt
SoftwareLicenseAgreement.pdf cdl/
cds.lib                      cdsLibEditor.log
cdsLibEditor.log.cdslck      config
display.drf                  lef/
libManager.log               libManager.log.cdslck
oa22/                        release
spectre/                     timing/
vhdl/                        vlog/

pads_FF_slvg.v pads_SS_slvg.v pads_TT_slvg.v stub.v

pads_FF_slvg.v pads_SS_slvg.v pads_TT_slvg.v

SETUP> read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_slvg.v
```

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_slvg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RT   msdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implem   ation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read    mcu_syn_final.v -verilog -revised
8
9  set sy
10
11 add compare points -all
12
13 compare
14
15 report verification
```

pads_SS_s1vg.v 까지 경로 지정

Equivalence Check

Conformal

- 위와 동일한 방식으로 STD셀 라이브러리도 입력

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revis
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

io셀 입력이 끝나면 띄어쓰기 후 연속 입력

Equivalence Check

Conformal

- Io셀, STD셀 라이브러리 모두 입력

```
3 read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
  erilog/slow_vdd1v0_basicCells.v -verilog -both
```

```
cds.lib                      config
doc/                         gsclib045/
gsclib045_backbias/          gsclib045_hvt/
gsclib045_lvt/               gsclib045_svt_v4.4/
gsclib045_tech/              release

gsclib045/          gsclib045_backbias/ gsclib045_hvt/
gsclib045_lvt/      gsclib045_svt_v4.4/ gsclib045_tech/

gsclib045/          gsclib045_backbias/ gsclib045_hvt/
gsclib045_lvt/      gsclib045_svt_v4.4/ gsclib045_tech/

AMSFF_database_diagram.pdf Release_Note.txt
cdl/                       cds.lib
celtic/                    gds/
lef/                       migration/
oa22/                      qrc/
skill/                     spectre/
spef/                      techfile/
timing/                    verilog/
vhdl/

compile_gsclib045_functional.csh fast_vdd1v0_basicCells.v
fast_vdd1v0_extvdd1v0.v          fast_vdd1v0_extvdd1v2.v
fast_vdd1v0_multibitsDFF.v       fast_vdd1v2_basicCells.v
fast_vdd1v2_extvdd1v0.v          fast_vdd1v2_extvdd1v2.v
fast_vdd1v2_multibitsDFF.v       slow_vdd1v0_basicCells.v
slow_vdd1v0_extvdd1v0.v          slow_vdd1v0_extvdd1v2.v
slow_vdd1v0_multibitsDFF.v       slow_vdd1v2_basicCells.v
slow_vdd1v2_extvdd1v0.v          slow_vdd1v2_extvdd1v2.v
slow_vdd1v2_multibitsDFF.v
```

```
SETUP> read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/verilog/slow_vdd1v0_basicCells.v
```

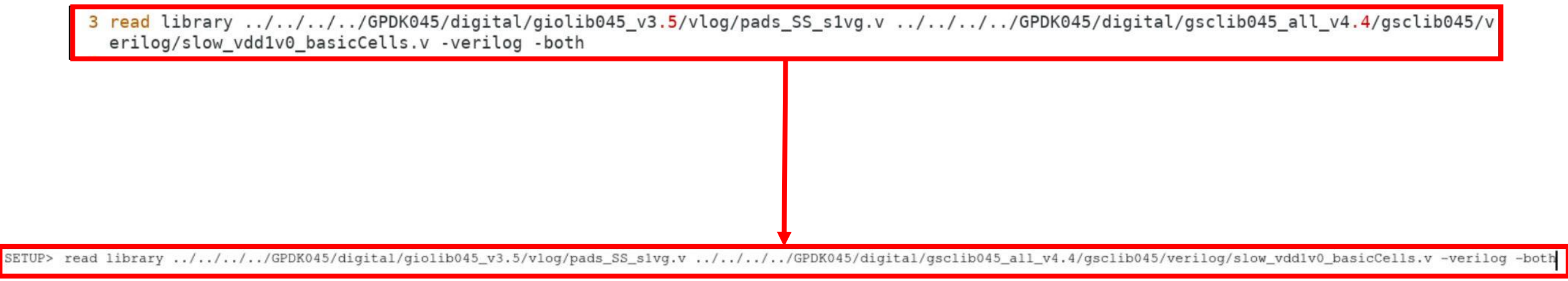
Equivalence Check

Conformal

- 경로 입력 후 마지막에 –verilog –both 옵션을 입력함

-Verilog: 파일타입(.v)에 의해 입력
-both: revised와 golden 모두에 동일하게 적용

```
3 read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
  erilog/slow_vdd1v0_basicCells.v -verilog -both
```



Equivalence Check

Conformal

- .v로 되어있는 Digital library 파일을 입력하는 명령임 (STD셀, IO셀)

툴 실행 결과

```
// Warning: (DIR6.1) Ignored compiler directive is detected (occurrence:497)
// Warning: (DIR6.2) Supported compiler directive is detected (occurrence:1036)
// Note: (DIR6.3) Conditional compiler directive clause is effective (occurrence:14)
// Warning: (HRC1.4) Module/entity is empty (blackboxed) (occurrence:2)
// Warning: (HRC3.2a) Module/entity has no I/O ports (occurrence:9)
// Warning: (HRC3.10b) An input port is declared, but it is not used. Module is empty (occurrence:1)
// Note: Read VERILOG library successfully

SETUP>
SETUP> set log file ./log/all.all.log -replace
SETUP> read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK04
```

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smk    cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_fina    -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

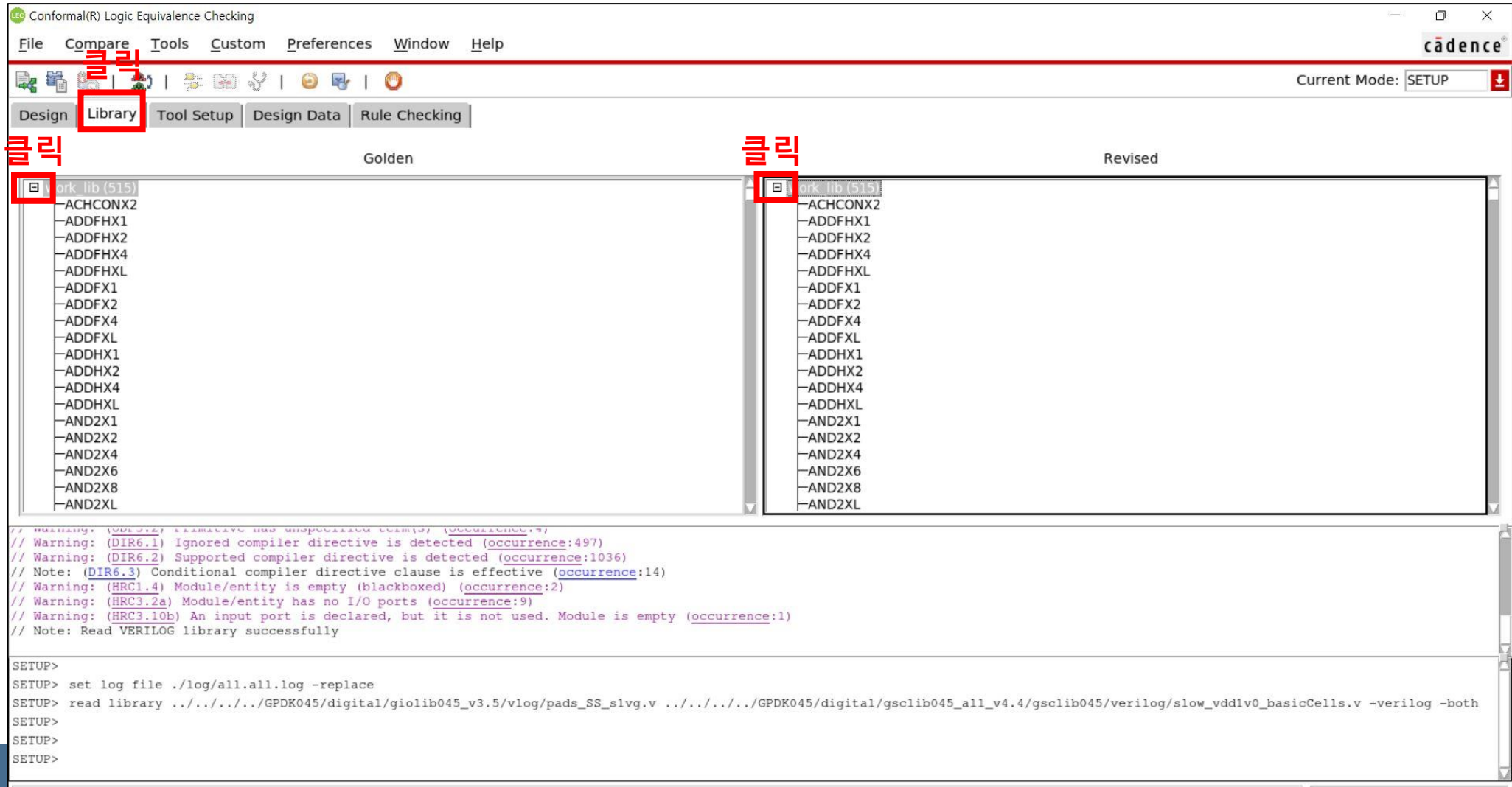
경로에 주의

Equivalence Check

Conformal

- Gui 확인
- Library tab 확인

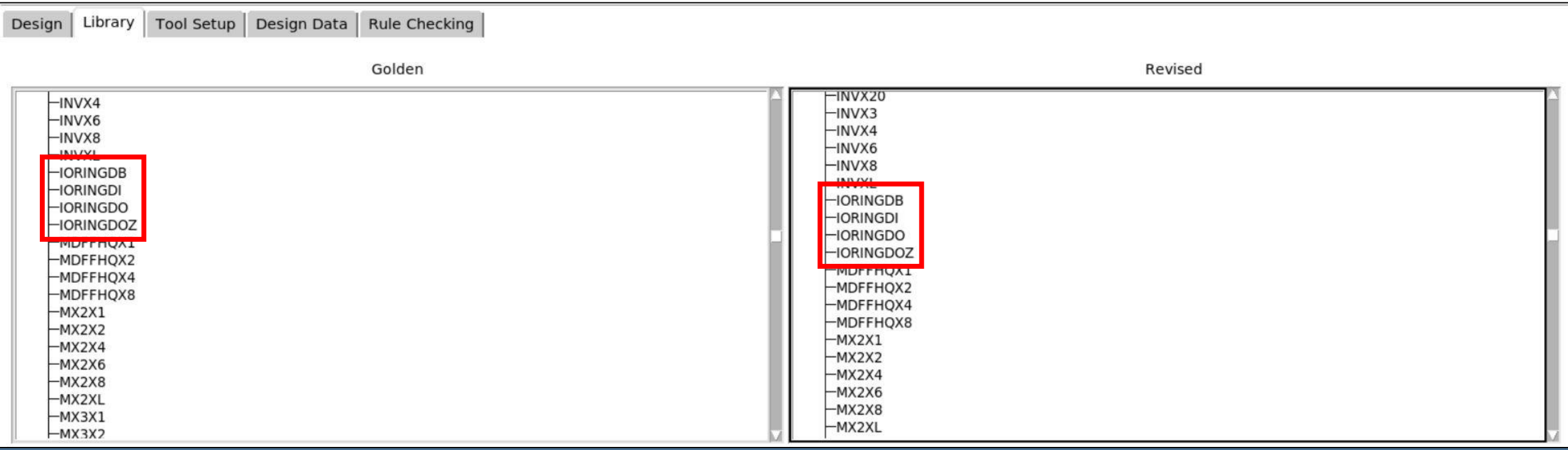
- Golden과 Revised에 대한 라이브러리가 모두 적용된 것을 확인



Equivalence Check

Conformal

- STD셀과 IO셀이 모두 리스트 업 되어있음을 확인



Equivalence Check

Conformal

- 5행의 마지막 부분의 –golden 옵션은 합성 전의 verilog 소스를 적용한다는 뜻
- 학습을 위해 직접 입력

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Equivalence Check

Conformal

- 빨간 상자에서 g+f 하여 파일 경로가 올바른지 확인

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_cl
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

아래와 같이 오픈이 되면 경로가 올바르다는 뜻

```
//-----------------------------------------------------------------------------
// The confidential and proprietary information contained in this file may
// only be used by a person authorised under and to the extent permitted
// by a subsisting licensing agreement from ARM Limited.
//
//            (C) COPYRIGHT 2010-2015  ARM Limited or its affiliates.
//                ALL RIGHTS RESERVED
//
// This entire notice must be reproduced on all copies of this file
// and copies of this file may only be made by a person if such person is
// permitted to do so under the terms of a subsisting license agreement
// from ARM Limited.
//
//  Version and Release Control Information:
//
//  File Revision       : $Revision: 275084 $
//  File Date           : $Date: 2014-03-27 15:09:11 +0000 (Thu, 27 Mar 2014) $
//
//  Release Information : Cortex-M0 DesignStart-r1p0-00rel0
//-----------------------------------------------------------------------------
// Verilog-2001 (IEEE Std 1364-2001)
//-----------------------------------------------------------------------------
//
//-----------------------------------------------------------------------------
// Abstract : Top level for example Cortex-M0 microcontroller
//-----------------------------------------------------------------------------
//

`include "cmsdk_mcu_defs.v"
```

Equivalence Check

Conformal

- 빨간 상자에서 g+f 하여 파일 경로가 올바른지 확인

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v .
   esignstart/implementation/cortex_m0_mcu_system_cadence_/ns/mapped/cmsdk_mcu
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

아래와 같이 오픈이 되면 경로가 올바르다는 뜻

```
//            (C) COPYRIGHT 2010-2015  ARM Limited or its affiliates.
//                ALL RIGHTS RESERVED
//
// This entire notice must be reproduced on all copies of this file
// and copies of this file may only be made by a person if such person is
// permitted to do so under the terms of a subsisting license agreement
// from ARM Limited.
//
//  Version and Release Control Information:
//
//  File Revision       : $Revision: 275084 $
//  File Date           : $Date: 2014-03-27 15:09:11 +0000 (Thu, 27 Mar 2014) $
//
//  Release Information : Cortex-M0 DesignStart-r1p0-00rel0
//-----------------------------------------------------------------------------
// Verilog-2001 (IEEE Std 1364-2001)
//-----------------------------------------------------------------------------
//
//-----------------------------------------------------------------------------
// Abstract : Simple clock controller for Cortex-M0 example system
//-----------------------------------------------------------------------------
// Note : Most of the clock gating are handled by the example PMU provided
//        in the Cortex-M0/Cortex-M0+ deliverable.

`include "cmsdk_mcu_defs.v"

module cmsdk_mcu_clkctrl #(
  parameter CLKGATE_PRESENT = 0)
```

Equivalence Check

Conformal

이와 같이 오픈이 되면 경로가 올바르다는 뜻

```
// and copies of this file may only be made by a person if such person is
// permitted to do so under the terms of a subsisting license agreement
// from ARM Limited.
//
//  Version and Release Control Information:
//
//  File Revision       : $Revision: 275084 $
//  File Date           : $Date: 2014-03-27 15:09:11 +0000 (Thu, 27 Mar 2014) $
//
//  Release Information : Cortex-M0 DesignStart-r1p0-00rel0
//-----------------------------------------------------------------------------
// Verilog-2001 (IEEE Std 1364-2001)
//-----------------------------------------------------------------------------
//
//-----------------------------------------------------------------------------
// Abstract : Pin multiplexing control for example Cortex-M0/Cortex-M0+
//            microcontroller
//-----------------------------------------------------------------------------
//
module cmsdk_mcu_pin_mux (
  //------------------------------------------
  // I/O ports
  //------------------------------------------

    // UART
    output wire             uart0_rxd,
    input  wire             uart0_txd,
    input  wire             uart0_txen,
    output wire             uart1_rxd,
```

- 빨간 상자에서 g+f 하여 파일 경로가 올바른지 확인

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Equivalence Check

아래와 같이 오픈이 되면 경로가 올바르다는 뜻

Conformal

- 빨간 상자에서 g+f 하여 파일 경로가 올바른지 확인

```
// Generated by Cadence Genus(TM) Synthesis Solution 22.16-s078_1
// Generated on: Jan 20 2025 09:32:59 KST (Jan 20 2025 00:32:59 UTC)

// Verification Directory fv/cmsdk_mcu_system

module
     cmsdk_mcu_addr_decode_BASEADDR_GPIO032h40010000_BASEADDR_GPIO132
TABLE32hf0000000(haddr,
     remap_ctrl, boot_hsel, flash_hsel, sram_hsel, apbsys_hsel,
     gpio0_hsel, gpio1_hsel, sysctrl_hsel, sysrom_hsel, defslv_hsel,
     hselmtb, hselram, hselsfr);
  input [31:0] haddr;
  input remap_ctrl;
  output boot_hsel, flash_hsel, sram_hsel, apbsys_hsel, gpio0_hsel,
       gpio1_hsel, sysctrl_hsel, sysrom_hsel, defslv_hsel, hselmtb,
       hselram, hselsfr;
```

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Equivalence Check

Conformal

툴 실행 결과

```
// Warning: (DIR4.2) Design includes one or more HDL directives or pragmas that Conformal supports (occurrence:2)
// Note: (HRC3.5b) Open output port connection is detected (occurrence:2)
// Warning: (HRC3.10a) An input port is declared, but it is not completely used in the module (occurrence:1310)
// Warning: (HRC3.16) A wire is declared, but not used in the module (occurrence:5)
// Warning: There are 1179 undriven nets in Golden
// Warning: There are 1179 undriven pins in Golden
// Note: Read VERILOG design successfully
```

- 파일 경로가 올바른 것을 확인했으면 SETUP>에 read design 입력 후 경로 입력
- 5행의 마지막 부분의 –golden 명령은 .v로 된 verilog 소스임을 명시함

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

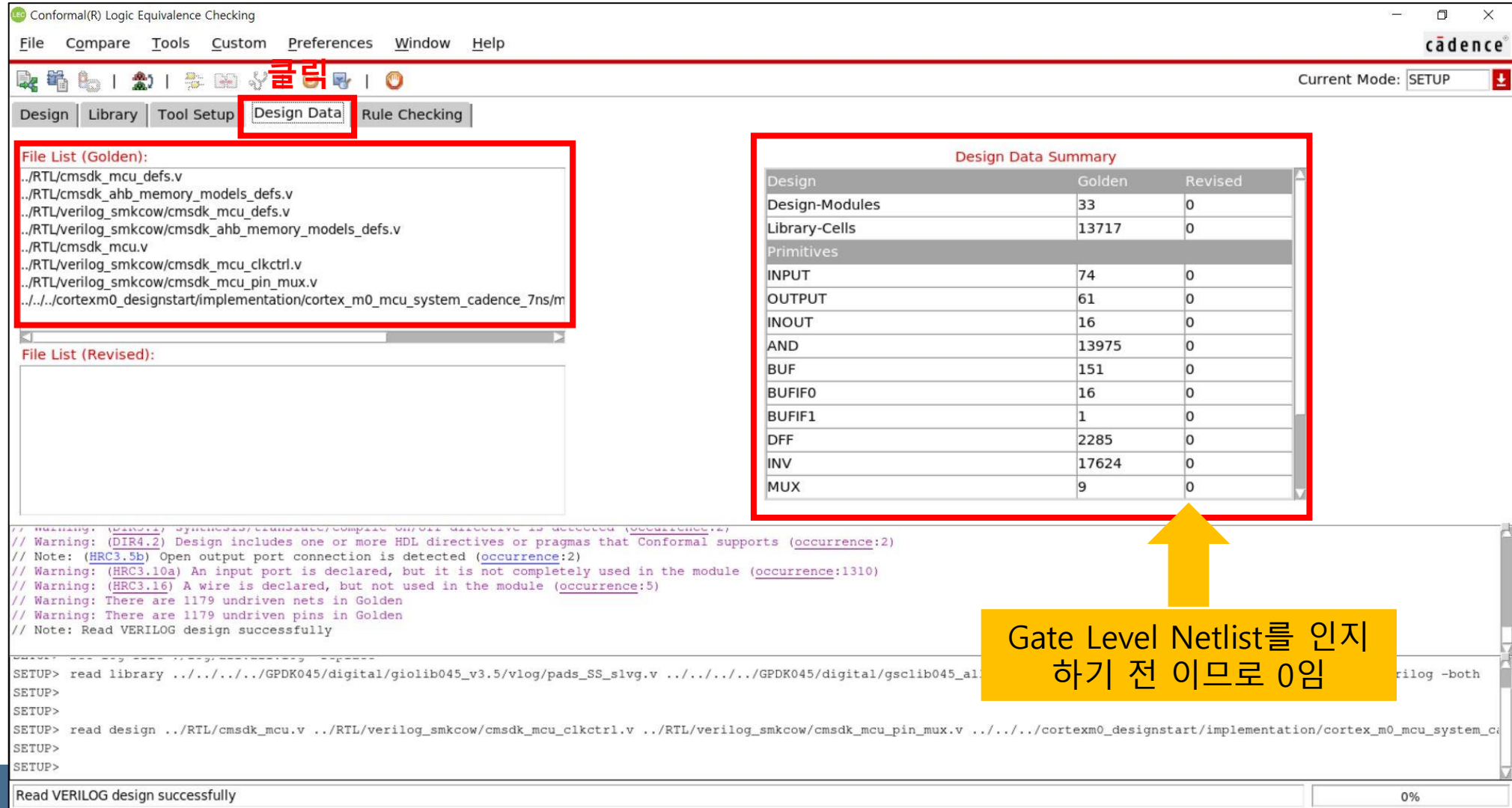
중간중간의 띄어쓰기 주의

Equivalence Check

Conformal

- gui 확인
- Design Data 탭 확인

- Golden에 .v 파일들이 리스트 업 된 것을 볼 수 있음



Equivalence Check

Conformal

- 7행의 마지막 부분의 –revised 옵션은 Gate Level Netlist를 적용한다는 뜻
- 학습을 위해 직접 입력

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_S
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkc
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/c
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Tab키를 활용하여 경로 입력

```
Equivalence_check/ RTL/                SIM/
SYN/

RTL_LIST.tcl     Result/          cds_syn_runtime  const/
env/             fv/              genus.cmd        genus.cmd1
genus.cmd2       genus.log        genus.log1       genus.log2
log/             mapped/          report/          run_syn
script/          top.mtarpt       unmapped/

cmsdk_mcu_incr.db
cmsdk_mcu_m.default_emulate_constraint_mode.sdc
cmsdk_mcu_m.dont_touch.sdc
cmsdk_mcu_m.g
cmsdk_mcu_m.genus_init.tcl
cmsdk_mcu_m.genus_setup.tcl
cmsdk_mcu_m.lec.taf.gz
cmsdk_mcu_m.metrics.json
cmsdk_mcu_m.mmmc.tcl
cmsdk_mcu_m.preserve.tcl
cmsdk_mcu_m.root.g
cmsdk_mcu_m.safety.taf.gz
cmsdk_mcu_m.v
cmsdk_mcu_map.db
cmsdk_mcu_rtl_2_lec_map.v
cmsdk_mcu_syn_final.sdc
cmsdk_mcu_syn_final.v
rtl_2_lec_final.do
rtl_2_lec_map.do
SETUP> read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
```

Equivalence Check

Conformal

툴 실행 결과

```
// Command: read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
// Parsing file ../SYN/mapped/cmsdk_mcu_syn_final.v ...
// Revised root module is set to 'cmsdk_mcu'
// Warning: (RTL2.2) Variable is referenced but never assigned (occurrence:133)
// Warning: (RTL2.5) Net is referenced without an assignment. Design verification will be based on set_undriven_signal setting (occurrence:133)
// Warning: (RTL2.13) Undriven pin is detected (occurrence:105)
// Warning: (RTL14) Signal has input but it has no output (occurrence:1919)
// Warning: (RTL14.1) Fanout load of the signal is removed (occurrence:171)
// Warning: (HRC3.10a) An input port is declared, but it is not completely used in the module (occurrence:1412)
// Warning: There are 105 undriven nets in Revised
// Warning: There are 105 undriven pins in Revised
// Note: Read VERILOG design successfully
```

- 7행의 마지막 부분의 –revised 명령은 Gate Level Netlist를 적용함

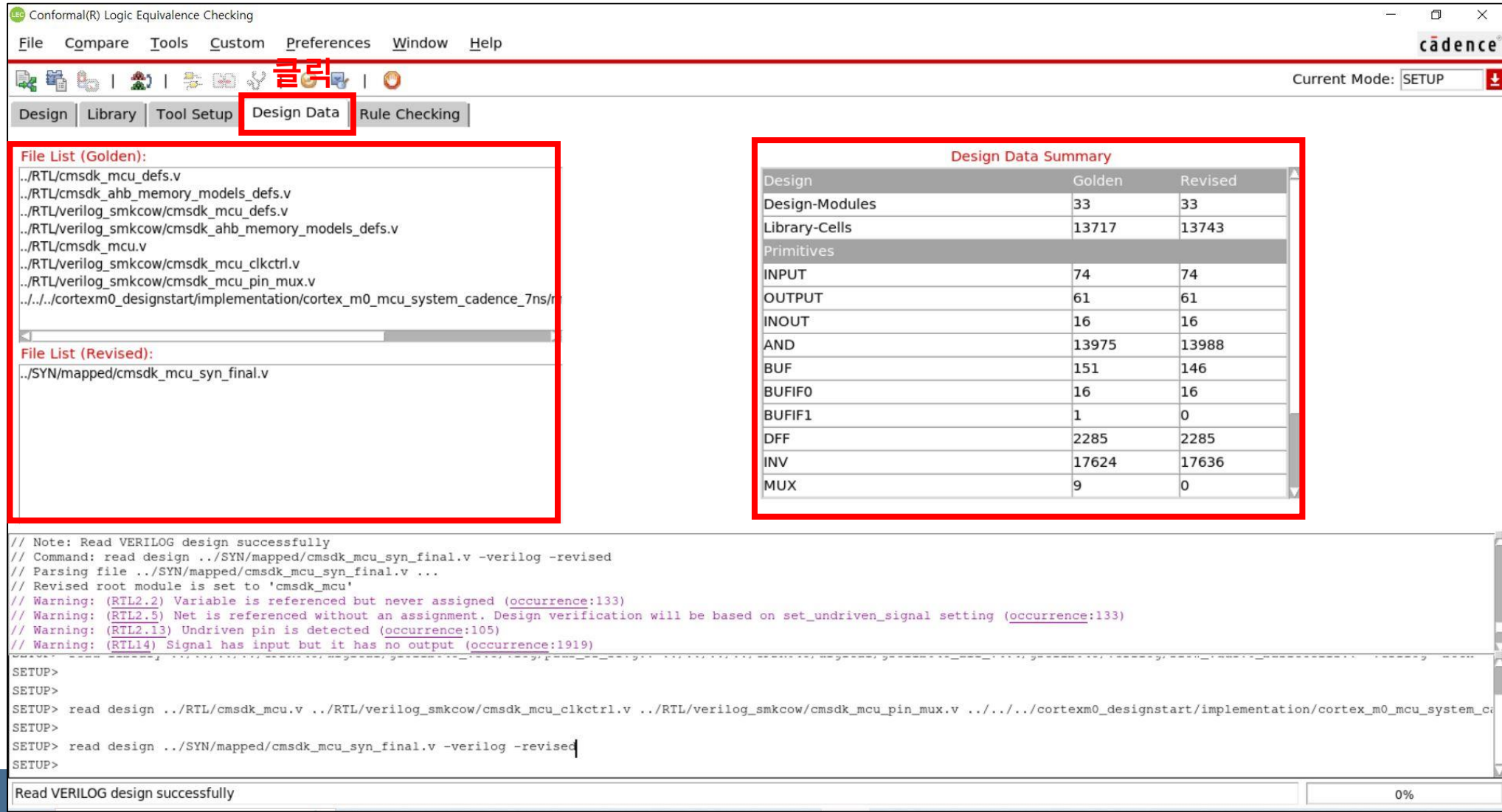
```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Equivalence Check

Conformal

- gui 확인
- Design Data 탭 확인

- 모든 파일이 리스트 업 된 것을 확인할 수 있음
- 비교에 필요한 모든 파일 입력완료



Equivalence Check

Conformal

- 비교준비: LEC Mode 준비

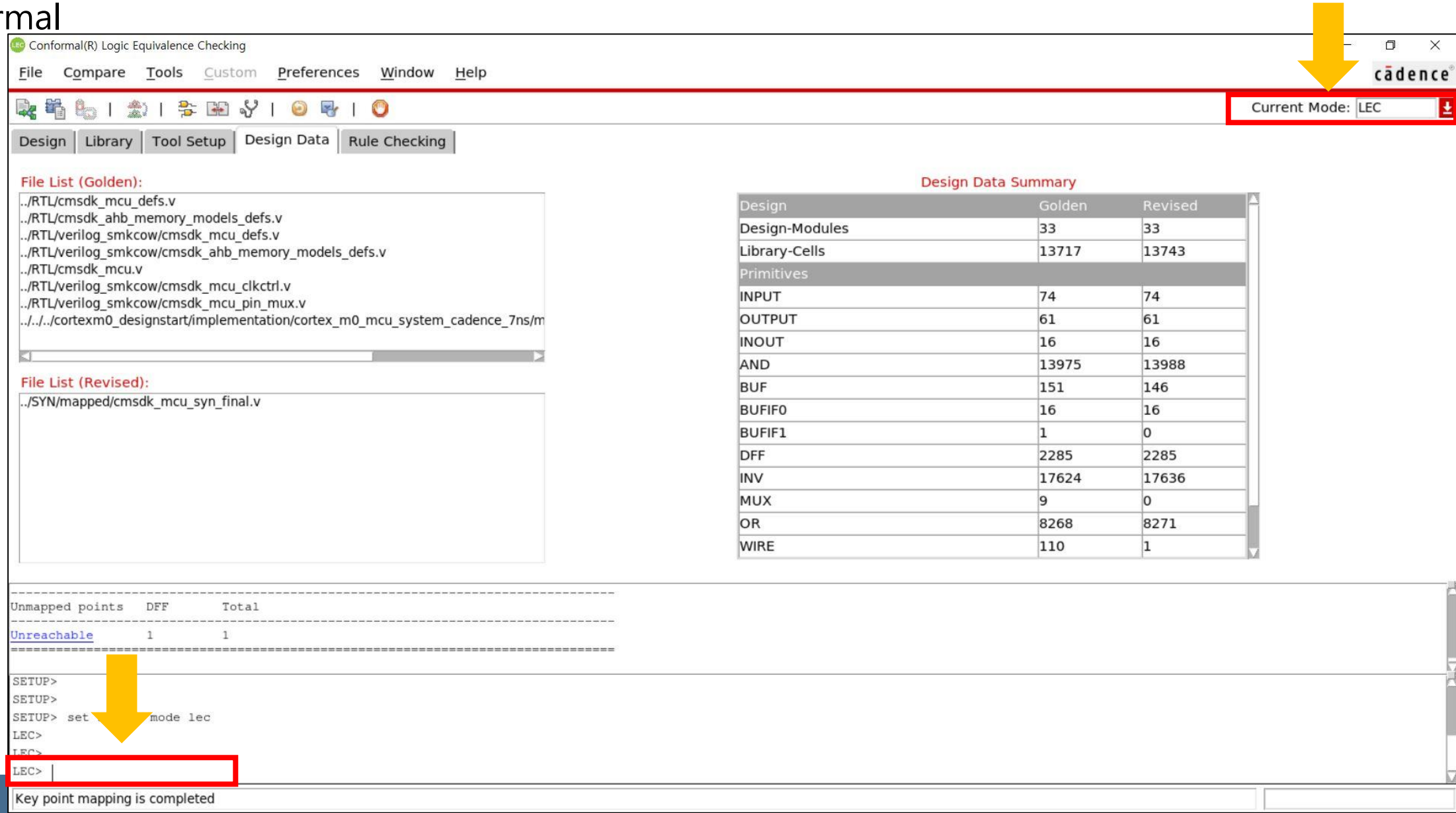
```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ..
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

툴 실행 결과

```
// Modeling Golden ...
// (F1) Created 16 wire resolution gate(s) due to multiple-driven net(s)
// (F39) Added 16 output Z gates
// (F28) Converted 1180 internal output port(s) to inout port(s)
// Processing Revised ...
// Modeling Revised ...
// (F1) Created 16 wire resolution gate(s) due to multiple-driven net(s)
// (F39) Added 16 output Z gates
// (F28) Converted 105 internal output port(s) to inout port(s)
CPU time      : 6.61    seconds
Elapse time   : 5055    seconds
Memory usage : 178.58  M bytes
// Mapping key points ...
================================================================================
Mapped points: SYSTEM class
--------------------------------------------------------------------------------
Mapped points      PI      PO      DFF     Z          Total
--------------------------------------------------------------------------------
Golden             106     77      2284    32         2499
--------------------------------------------------------------------------------
Revised            106     77      2284    32         2499
================================================================================
Unmapped points:
================================================================================
Golden:
--------------------------------------------------------------------------------
Unmapped points    DFF         Total
--------------------------------------------------------------------------------
Unreachable        1           1
================================================================================
Revised:
--------------------------------------------------------------------------------
Unmapped points    DFF         Total
--------------------------------------------------------------------------------
Unreachable        1           1
================================================================================
```

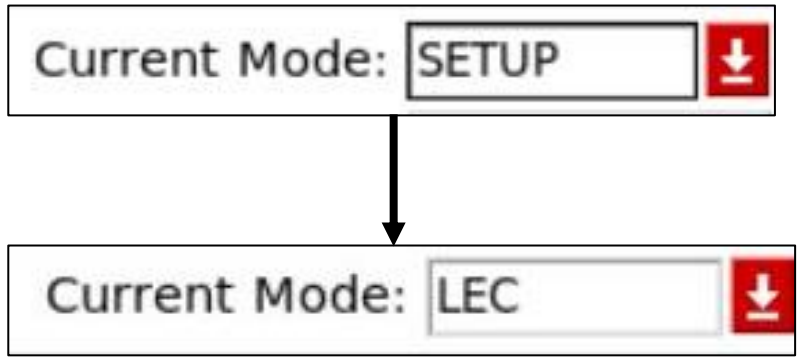
Equivalence Check

Conformal

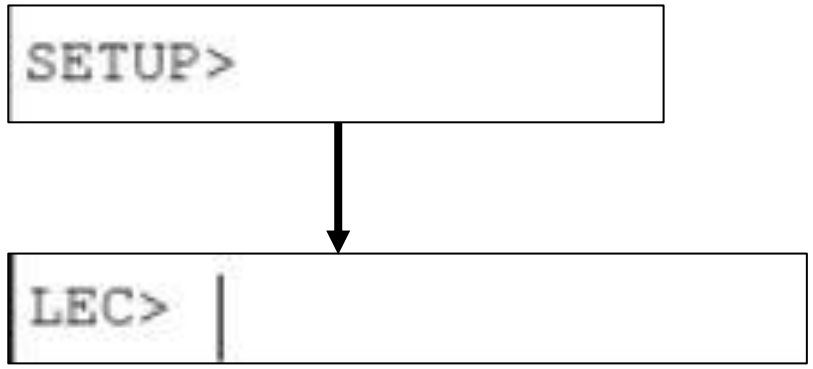


Equivalence Check

Conformal



- Current Mode: SETUP ➔ LEC
- SETUP> ➔ LEC>



Equivalence Check

Conformal

툴 실행 결과

```
LEC> add compare points -all
// Command: add compare points -all
// 2361 compared points added to compare list
```

- 비교 전 필수 Command

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Equivalence Check

Conformal

툴 실행 결과

```
LEC> compare
// Command: compare
================================================================================
Compared points       PO      DFF       Total
--------------------------------------------------------------------------------
Equivalent            77      2284      2361
--------------------------------------------------------------------------------
```

만약 일치하지 않으면 Equivalence 아래에 Non Equivalent를 포함하여 많은 항목들이 추가됨

- Verilog 소스와 Gate Level Netlist 간의 Input, output, reg, net 이름 비교

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/v
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_d
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

Equivalence Check

Conformal

- Verification report를 확인할 수 있음
- 임의의 패턴을 생성 후 입력하여 결과가 동일한지의 여부 확인

툴 실행 결과

```
// Command: report verification
================================================================================
                              Verification Report
--------------------------------------------------------------------------------
Category                                                                  Count
--------------------------------------------------------------------------------
1. Non-standard modeling options used:                                        0
--------------------------------------------------------------------------------
2. Incomplete verification:                                                   0
--------------------------------------------------------------------------------
3. User modification to design:                                               0
--------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:   0
--------------------------------------------------------------------------------
5. Design ambiguity:                                                          0
--------------------------------------------------------------------------------
6. Compare Results:                                                        PASS
```

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045_all_v4.4/
   erilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.v ../../..
   esignstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
```

비교 결과 일치

Equivalence Check

Conformal

- 툴 실행 결과를 보기 쉽게 정리해 줌

툴 실행 결과

```
// Command: report statistics
Mapping and compare statistics
================================================================================
                    Compare Result       Golden              Revised
--------------------------------------------------------------------------------
Root module name                         cmsdk_mcu           cmsdk_mcu

Primary inputs                             106                 106
   Mapped                                  106                 106

Tri-state (Z) key points                    32                  32
   Mapped                                   32                  32

Primary outputs                             77                  77
   Mapped                                   77                  77
      Equivalent              77

State key points                          2285                2285
   Mapped                                 2284                2284
      Equivalent           2284
   Unmapped                                  1                   1
      Unreachable                            1                   1
================================================================================
```

```
1  set log file ./log/all.log -replace
2
3  read library ../../../../GPDK045/digital/giolib045_v3.5/vlog/pads_SS_s1vg.v ../../../../GPDK045/digital/gsclib045
   _all_v4.4/gsclib045/verilog/slow_vdd1v0_basicCells.v -verilog -both
4
5  read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/verilog_smkcow/cmsdk_mcu_pin_mux.
   v ../../../cortexm0_designstart/implementation/cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final
   .v -verilog -golden
6
7  read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised
8
9  set system mode lec
10
11 add compare points -all
12
13 compare
14
15 report verification
16 report statistics
```

Equivalence Check

Conformal

- Conformal 재 실행 시 유용하도록 스크립트를 생성 후 자동 실행해 보자
- 사용할 my_script.tcl 파일 생성

$> cd script

```
[ex_poly1@npit Equivalence_check]$ ls
log  README_HowtoRun  script
```

$> vi my_script.tcl

```
[ex_poly1@npit script]$ vi my_script.tcl
```

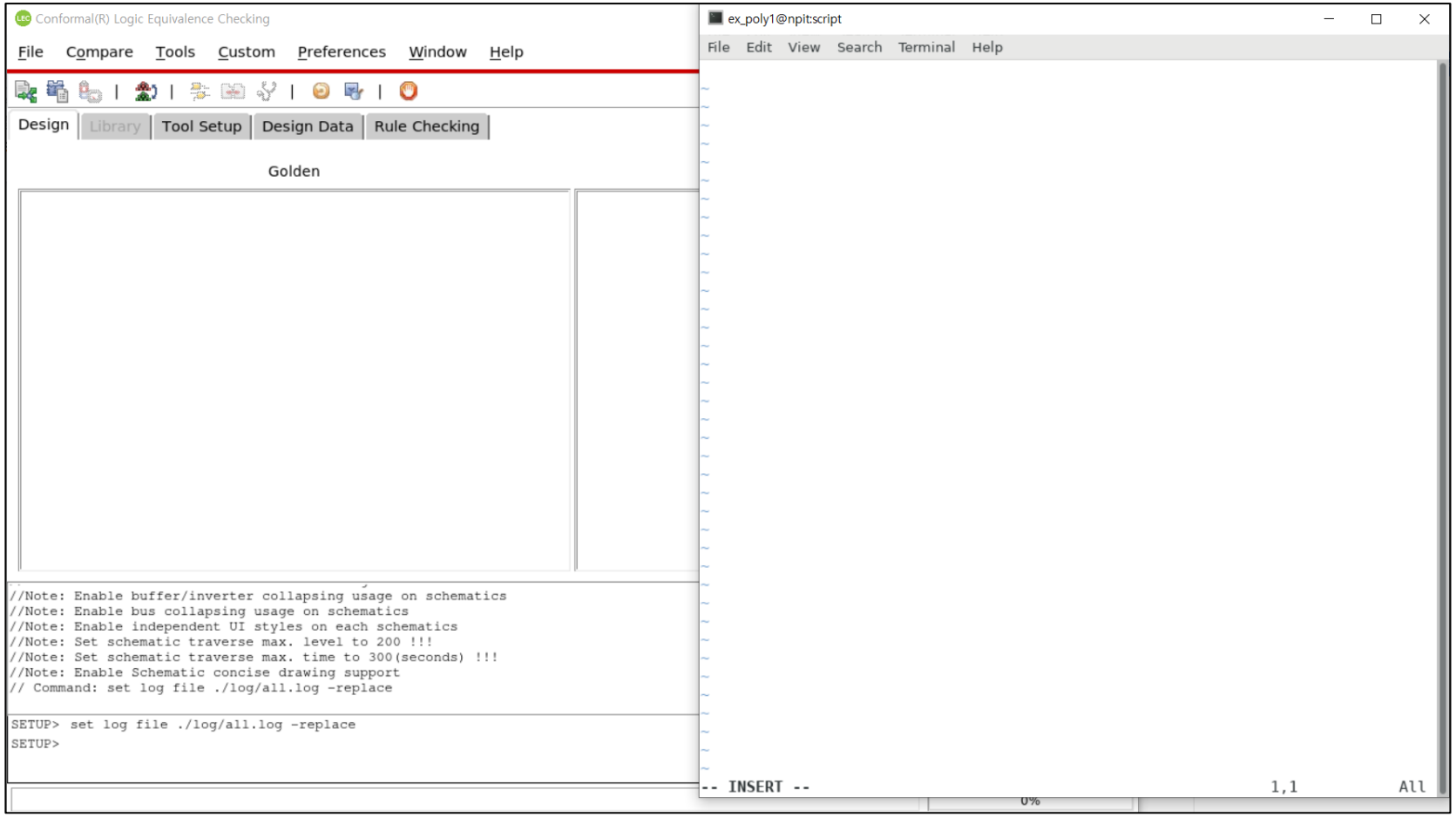
Equivalence Check

Conformal

$> lec

$> vi my_script.tcl

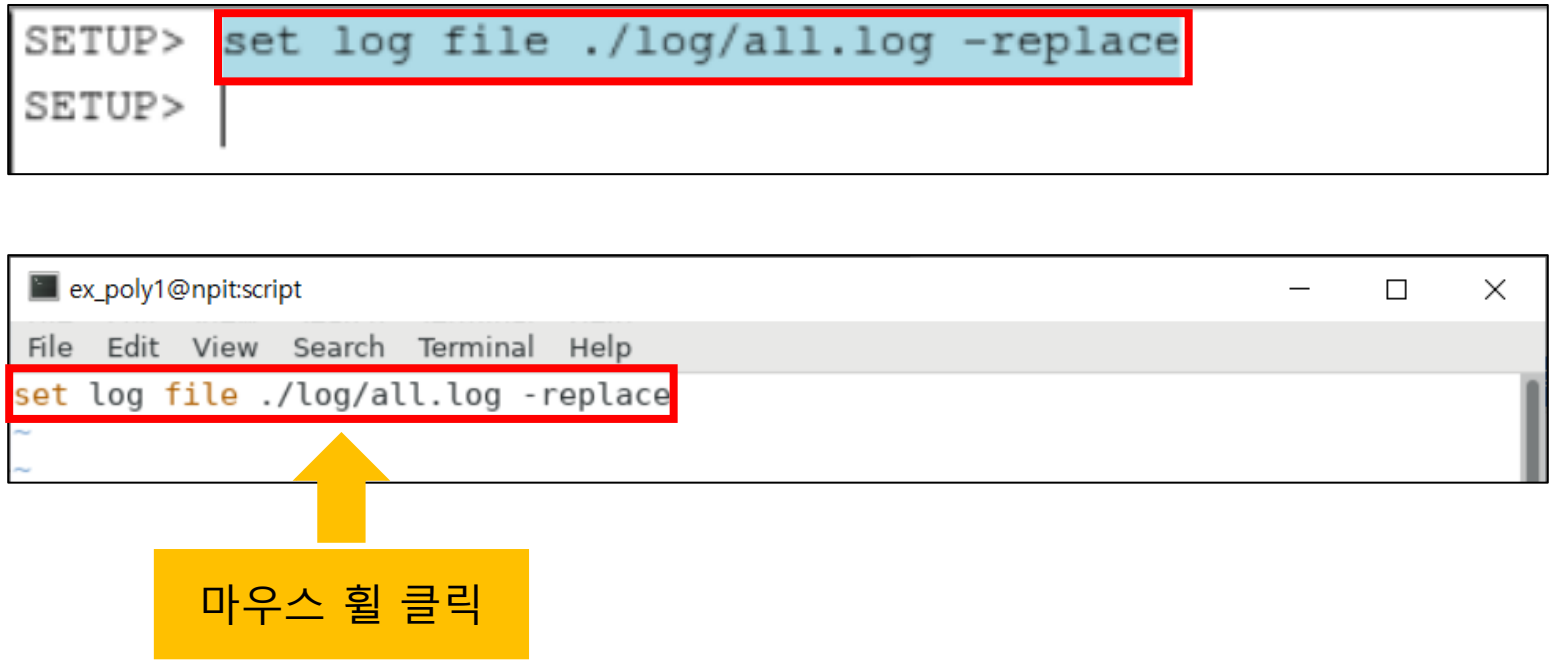
- 두개의 터미널 사용
- 이전에 진행했던 lec 유지



Equivalence Check

Conformal

- SETUP>에 입력했던 명령어를 선택 후 vi 창에 붙여넣기
- 아래의 그림과 같은 방법으로 모든 명령어 진행



Equivalence Check

Conformal

- 모든 입력을 완료했으면 vi 종료를 위해 **esc ➔ :wq**
- 툴 사용을 위해 lec 종료

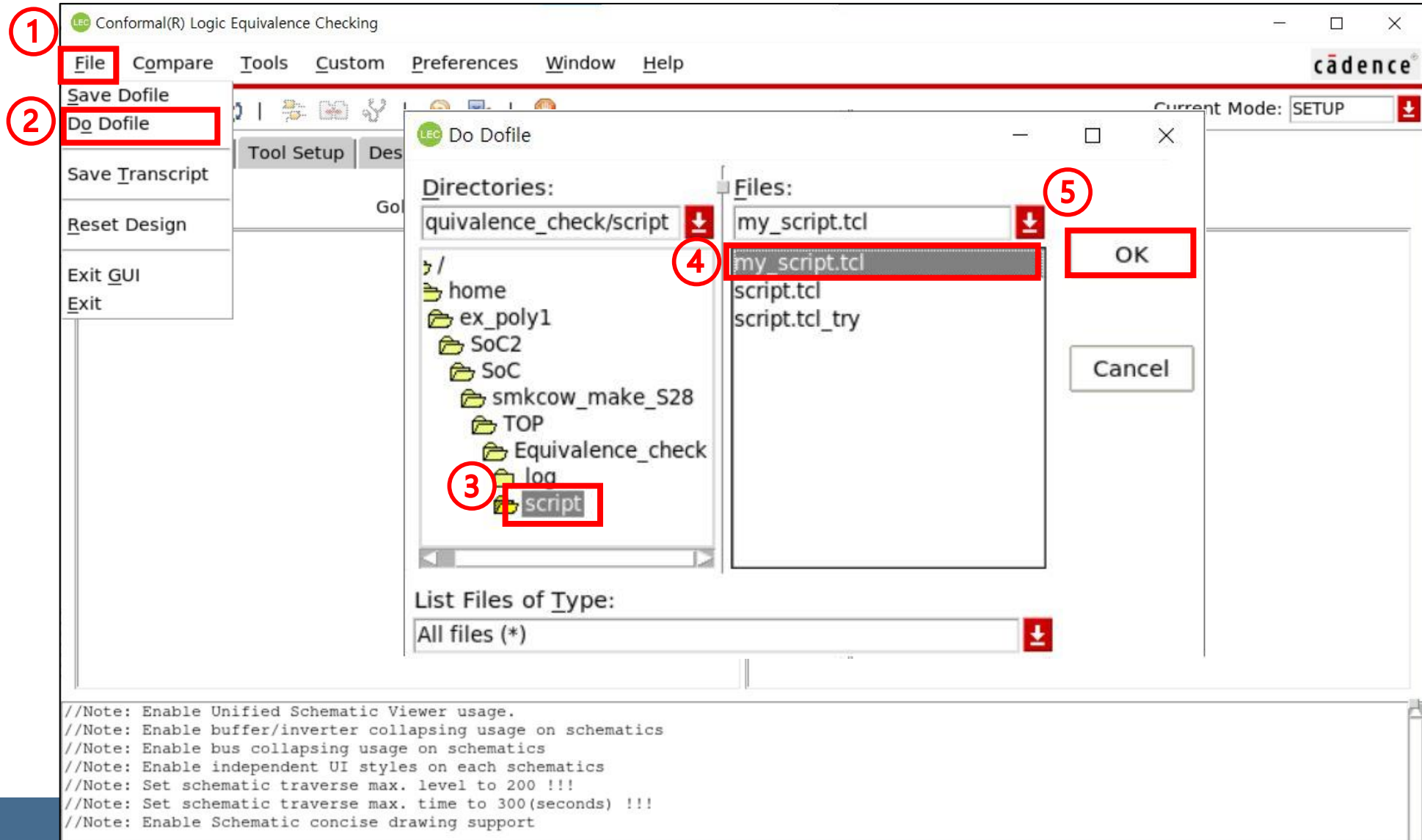
```
set log file ./log/all.log -replace

read library -liberty -both \
   ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/timing/fast_vdd1v0_b
asicCells.lib \
   ../../../../GPDK045/digital/gsclib045_all_v4.4/gsclib045/timing/slow_vdd1v0_b
asicCells.lib \
    ../../../../GPDK045/digital/giolib045_v3.5/timing/pads_SS_s1vg.lib

read design ../RTL/cmsdk_mcu.v ../RTL/verilog_smkcow/cmsdk_mcu_clkctrl.v ../RTL/
verilog_smkcow/cmsdk_mcu_pin_mux.v ../../../cortexm0_designstart/implementation/
cortex_m0_mcu_system_cadence_7ns/mapped/cmsdk_mcu_system_syn_final.v -verilog -g
olden

read design ../SYN/mapped/cmsdk_mcu_syn_final.v -verilog -revised

set system mode lec

add compare points -all

compare

report verification
report statistics
```

Equivalence Check

Conformal

$> lec

- Conformal 재 실행 시 유용하도록 스크립트를 생성 후 자동 실행



Equivalence Check

Conformal

- Dofile 실행 결과: 이전 결과와 같음

Dofile 실행 결과

```
Elapse time  : 129      seconds
Memory usage : 181.36  M bytes
// Command: add compare points -all
// 2361 compared points added to compare list
// Command: compare
================================================================================
Compared points      PO      DFF       Total
--------------------------------------------------------------------------------
Equivalent           77      2284      2361
================================================================================
// Command: report verification
================================================================================
                            Verification Report
--------------------------------------------------------------------------------
Category                                                                  Count
--------------------------------------------------------------------------------
1. Non-standard modeling options used:                                      0
--------------------------------------------------------------------------------
2. Incomplete verification:                                                 0
--------------------------------------------------------------------------------
3. User modification to design:                                             0
--------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:  0
--------------------------------------------------------------------------------
5. Design ambiguity:                                                        0
================================================================================
6. Compare Results:                                                      PASS
================================================================================
```

```
// Command: report statistics
Mapping and compare statistics
================================================================================
                      Compare Result        Golden             Revised
--------------------------------------------------------------------------------
Root module name                            cmsdk_mcu          cmsdk_mcu

Primary inputs                                106                106
   Mapped                                     106                106

Tri-state (Z) key points                       32                 32
   Mapped                                      32                 32

Primary outputs                                77                 77
   Mapped                                      77                 77
      Equivalent                77

State key points                             2285               2285
   Mapped                                    2284               2284
      Equivalent             2284
   Unmapped                                     1                  1
      Unreachable                               1                  1
================================================================================
```