

# Synthesis Report

# Synthesis

## Genus 툴 실행 결과

genus

```
Warning: Library 'fast_vdd1v0' found in multiple domains.  
Info: Use -domain to uniquify.  
Info: Selecting library 'fast_vdd1v0' in domain '-1'  
Warning: Library 'giolib045' found in multiple domains.  
Info: Use -domain to uniquify.  
Info: Selecting library 'giolib045' in domain '-1'  
Warning: Library 'slow_vdd1v0' found in multiple domains.  
Info: Use -domain to uniquify.  
Info: Selecting library 'slow_vdd1v0' in domain '-1'  
Info : Joules engine is used. [RPT-16]  
      : Joules engine is being used for the command report_power.  
Output file: ./report/18_cmsdk_mcu_SYN_pwr.rpt  
@file(cortexm0_45nm.tcl) 178: report_qor  
@file(cortexm0_45nm.tcl) 179: report_timing -nworst 100 -net  
@file(cortexm0_45nm.tcl) 180: report_summary  
> ${RPT_DIR}/19_${TOP DESIGN}_SYN_qor.rpt  
> ${RPT_DIR}/20_${TOP DESIGN}_SYN_timing.rpt  
> ${RPT_DIR}/21_${TOP DESIGN}_SYN_summary.rpt
```

- report 폴더에 여러가지 report를 저장함

```
161 #####  
162 ## REPORTS  
163 #####  
164  
165 report_analysis_views -type all      > ${RPT_DIR}/08_${TOP DESIGN}_SYN_analysis_view.rpt  
166 report_area                          > ${RPT_DIR}/09_${TOP DESIGN}_SYN_area.rpt  
167 report_clocks                        > ${RPT_DIR}/10_${TOP DESIGN}_SYN_clock.rpt  
168 report_clocks -generated           >> ${RPT_DIR}/10_${TOP DESIGN}_SYN_clock.rpt  
169 report_datapath                      > ${RPT_DIR}/11_${TOP DESIGN}_SYN_datapath.rpt  
170 report_design_rules                 > ${RPT_DIR}/12_${TOP DESIGN}_SYN_design_rules.rpt  
171 report_gates                         > ${RPT_DIR}/13_${TOP DESIGN}_SYN_gate.rpt  
172 report_gates -power                 >> ${RPT_DIR}/13_${TOP DESIGN}_SYN_gate.rpt  
173 report_hierarchy                     > ${RPT_DIR}/14_${TOP DESIGN}_SYN_hier.rpt  
174 report_memory_cells                > ${RPT_DIR}/15_${TOP DESIGN}_SYN_mem_cell.rpt  
175 report_messages -all               > ${RPT_DIR}/16_${TOP DESIGN}_SYN_message.rpt  
176 report_nets -hierarchical          > ${RPT_DIR}/17_${TOP DESIGN}_SYN_net.rpt  
177 report_power                         > ${RPT_DIR}/18_${TOP DESIGN}_SYN_pwr.rpt  
178 report_qor                           > ${RPT_DIR}/19_${TOP DESIGN}_SYN_qor.rpt  
179 report_timing -nworst 100 -net       > ${RPT_DIR}/20_${TOP DESIGN}_SYN_timing.rpt  
180 report_summary                      > ${RPT_DIR}/21_${TOP DESIGN}_SYN_summary.rpt
```

# Synthesis

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## Genus 툴 실행 결과

```
@genus:root: 102> write_design -basename ${MAPPED_DIR}/${TOP DESIGN}_mapped  
(write_design): Writing Genus content. Constraint interface is 'smsc'  
Exporting design data for 'cmsdk_mcu' to ./mapped/cmsdk_mcu_mapped...  
%# Begin write_design (01/26 23:33:34, mem=1909.54M)  
      flow.cputime  flow.realtime  timing.setup.tns  timing.setup.wns  snapshot  
UM:*                                         write_design  
Setting attribute of root '/': 'set_boundary_change' =  
No scan chains were found.  
File ./mapped/cmsdk_mcu_mapped.mmmc.tcl has been written.  
Finished SDC export (command execution time mm:ss (real) = 00:00).  
Info: file ./mapped/cmsdk_mcu_mapped.default_emulate_constraint_mode.sdc has been written  
Info: file ./mapped/cmsdk_mcu_mapped.default_emulate_constraint_mode.sdc has been written  
** To load the database source ./mapped/cmsdk_mcu_mapped.genus_setup.tcl in an Genus(TM) Synthesis Solution session.  
Finished exporting design data for 'cmsdk_mcu' (command execution time mm:ss cpu = 00:01, real = 00:05).  
. .  
%# End write_design (01/26 23:33:39, total cpu=17:00:01, real=17:00:05, peak res=1016.40M, current me m=1909.54M)
```

- mapped 폴더에 TOP 디자인의 이름을 활용한 디자인 폴더를 생성

```
182 #####  
183 ## write Innovus file set (verilog, SDC, config, etc.)  
184 #####  
185  
186 #source -echo ./script/report syn.tcl  
187 write_design -basename ${MAPPED_DIR}/${TOP DESIGN}_mapped  
188 write_hdl > ${MAPPED_DIR}/${TOP DESIGN}_syn_final.v  
189 write_sdc > ${MAPPED_DIR}/${TOP DESIGN}_syn_final.sdc  
190 write_sdf -timescale ns -nonegchecks -recrrem split -edges check_edge  
-setuphold split > ${MAPPED_DIR}/${TOP DESIGN}_delays.sdf
```

# Synthesis

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## Genus 툴 실행 결과

```
@genus:root: 103> write_hdl > ${MAPPED_DIR}/${TOP DESIGN}_syn_final.v
@genus:root: 104> write_sdc > ${MAPPED_DIR}/${TOP DESIGN}_syn_final.sdc
Finished SDC export (command execution time mm:ss (real) = 00:01).
@genus:root: 105> write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge
                     -setuphold split > ${MAPPED_DIR}/${TOP DESIGN}_delays.sdf
Warning : No delay description exists for an instance. [WSDF-201]
          : Cell u_cmsdk_mcu_system/u_apb_subsystem/u_ahb_to_apb/g1363.
          : The timing arc of the instance does not exist or is disabled by disable_t
imeing or constant value. The delay information will not be generated for the instance
. The instance could be a loop breaker or its inputs could be driven by constant
Warning : No delay description exists for an instance. [WSDF-201]
          : Cell pad5.
Warning : No delay description exists for an instance. [WSDF-201]
          : Cell pad71.
```

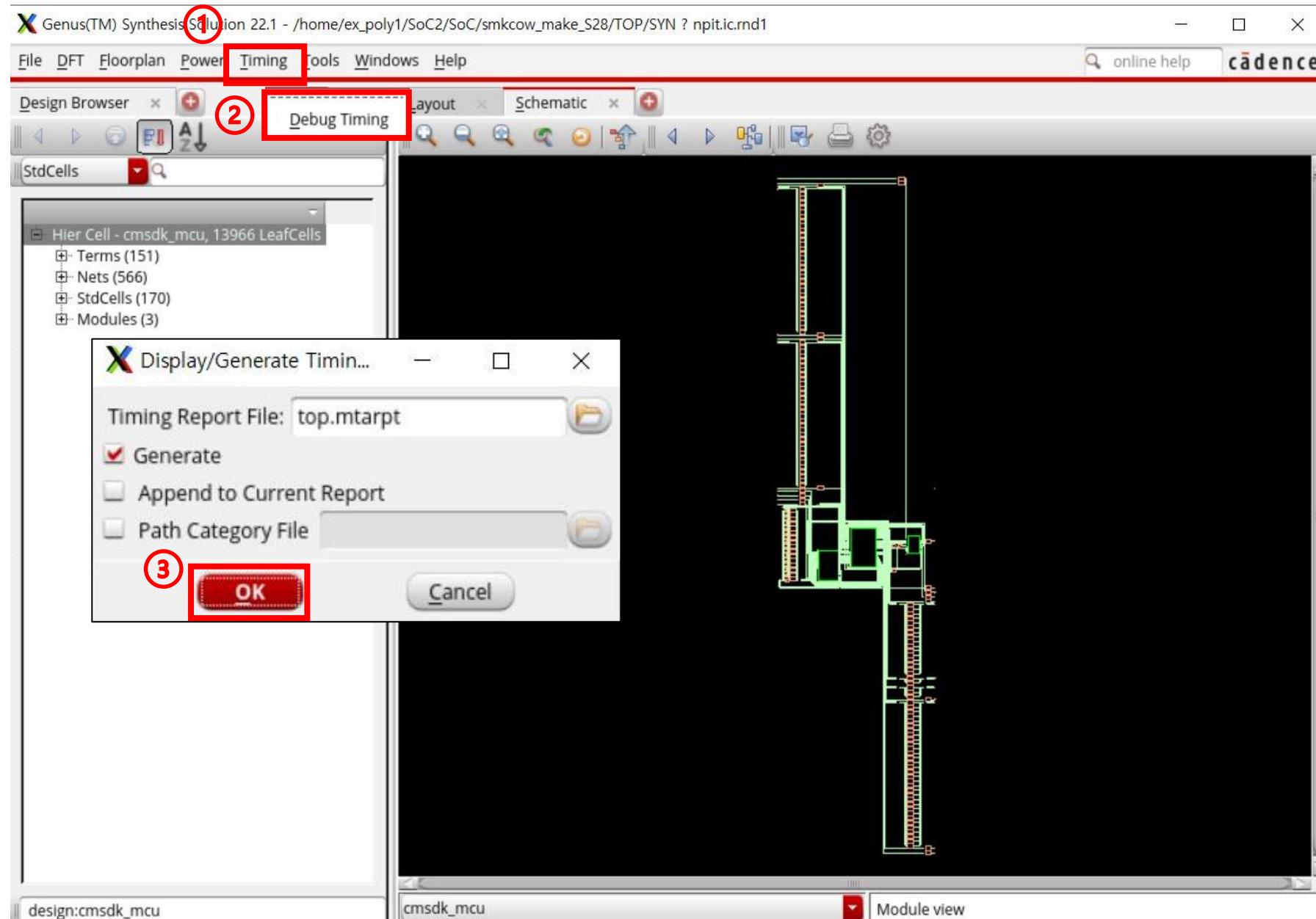
- 188행은 Gate\_Level\_Netlist를 최종적으로 뽑아내며, 이 파일은 다음 단계 툴에 사용 됨
- 189행은 툴이 constrain를 기억한 후 다음 툴을 위해 write out
- 190행의 sdf는 Standard Delay Format의 약자로 cell이 동작하는데 걸린 시간을 저장

```
182 #####
183 ## write Innovus file set (verilog, SDC, config, etc.)
184 #####
185
186 #source -echo ./script/report_syn.tcl
187 write_design -basename ${MAPPED_DIR}/${TOP DESIGN}_mapped
188 write_hdl > ${MAPPED_DIR}/${TOP DESIGN}_syn_final.v
189 write_sdc > ${MAPPED_DIR}/${TOP DESIGN}_syn_final.sdc
190 write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge
           -setuphold split > ${MAPPED_DIR}/${TOP DESIGN}_delays.sdf
```

# Synthesis

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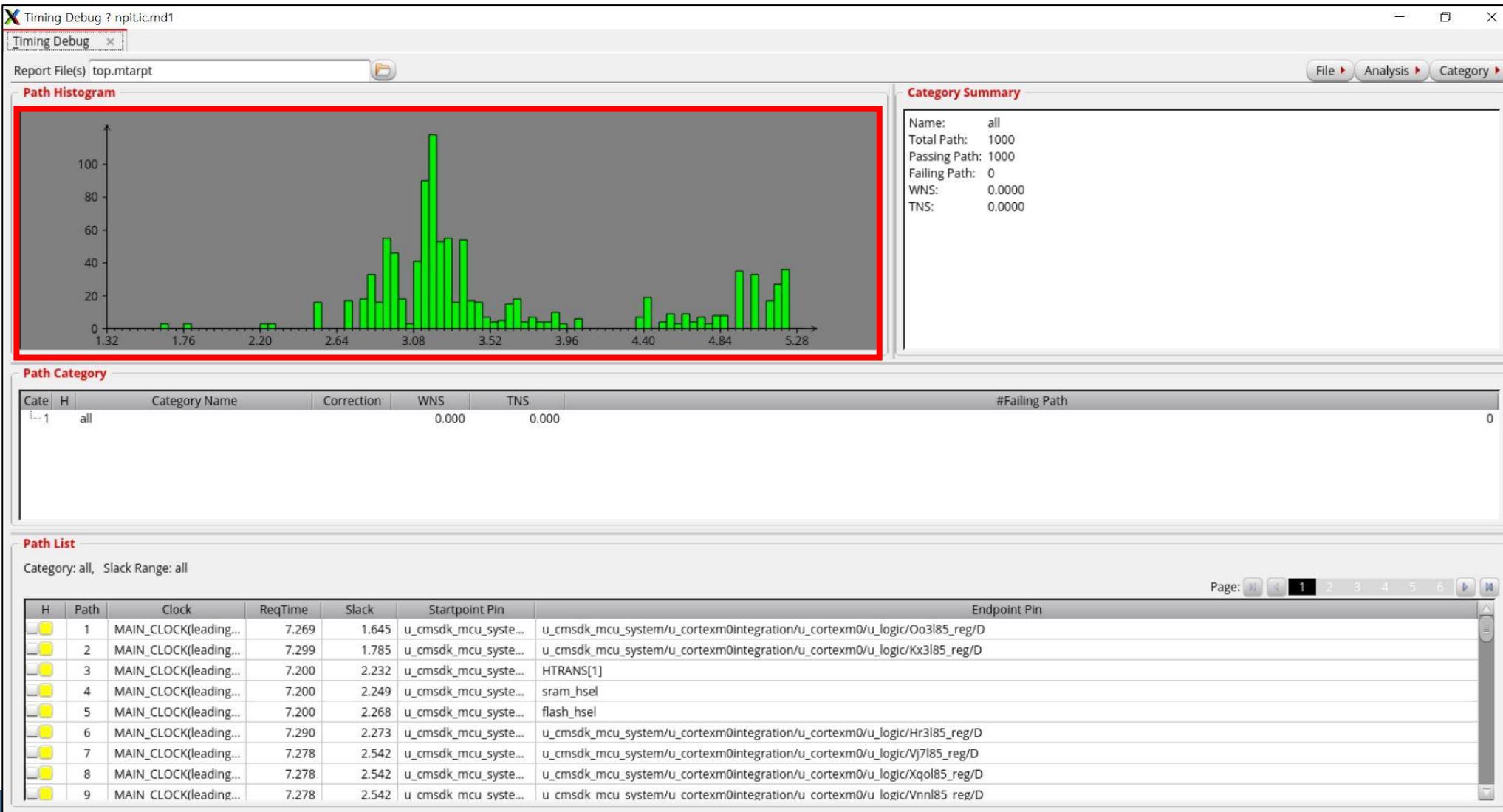
- Debug Timing



# Synthesis

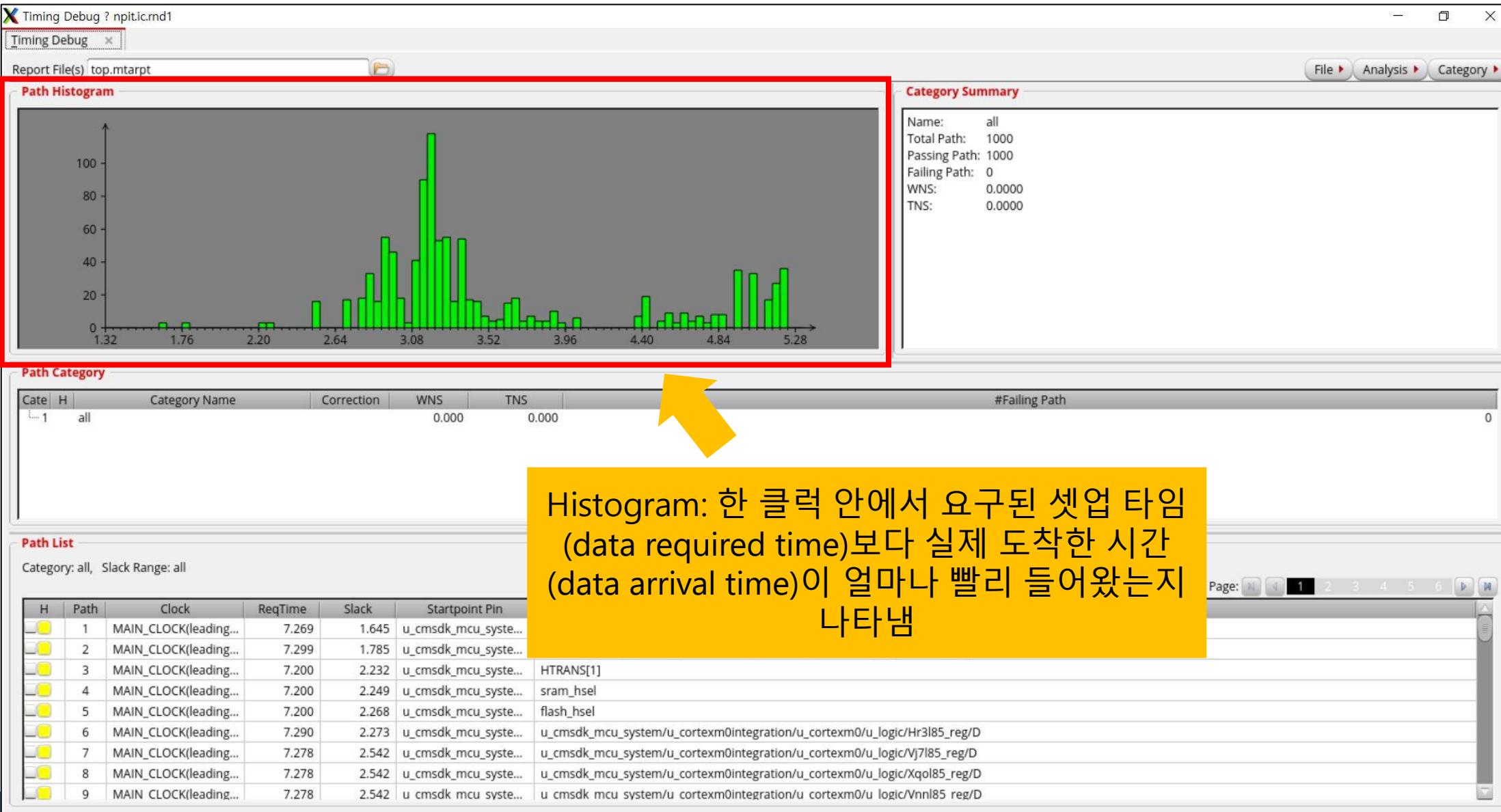
genus

- Debug Timing: 텍스트로 확인했던 정보를 그래픽으로 확인
- Path가 모두 녹색이므로 이상 없음(문제 발생 시 빨간색으로 표시됨)



# Synthesis

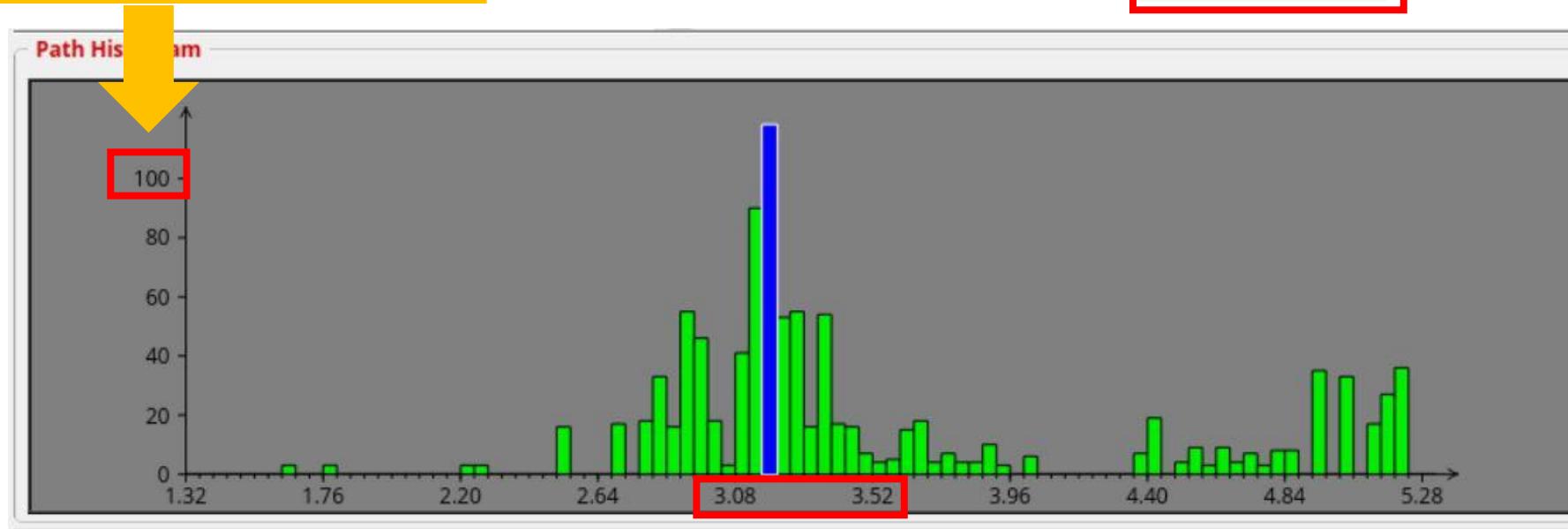
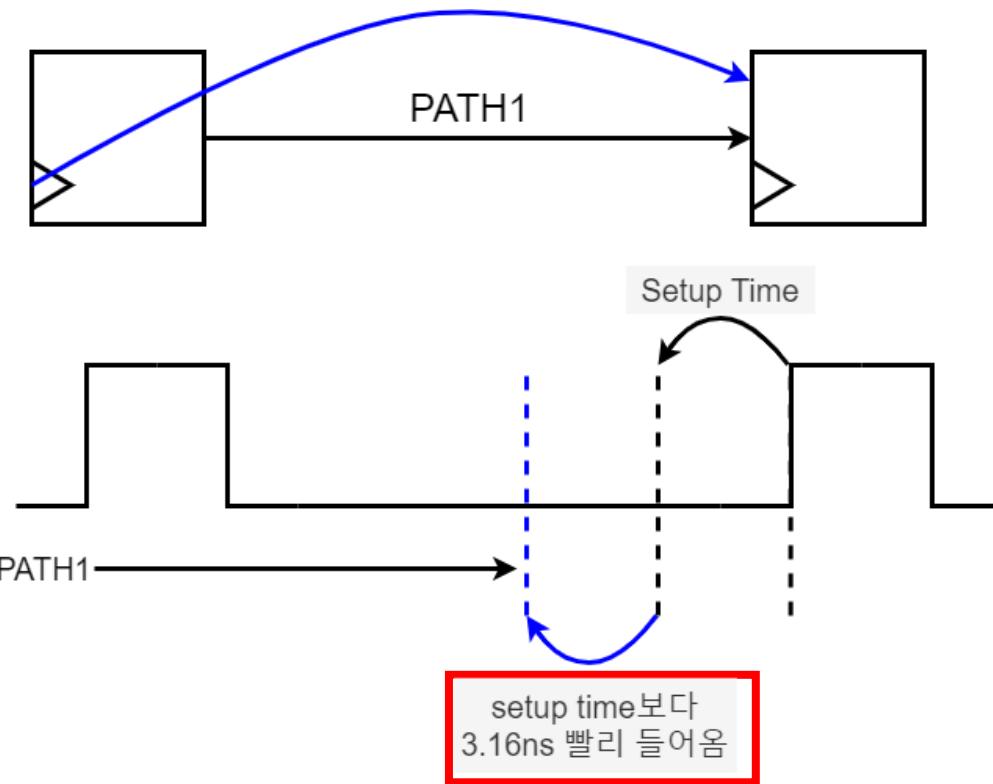
genus



# Synthesis

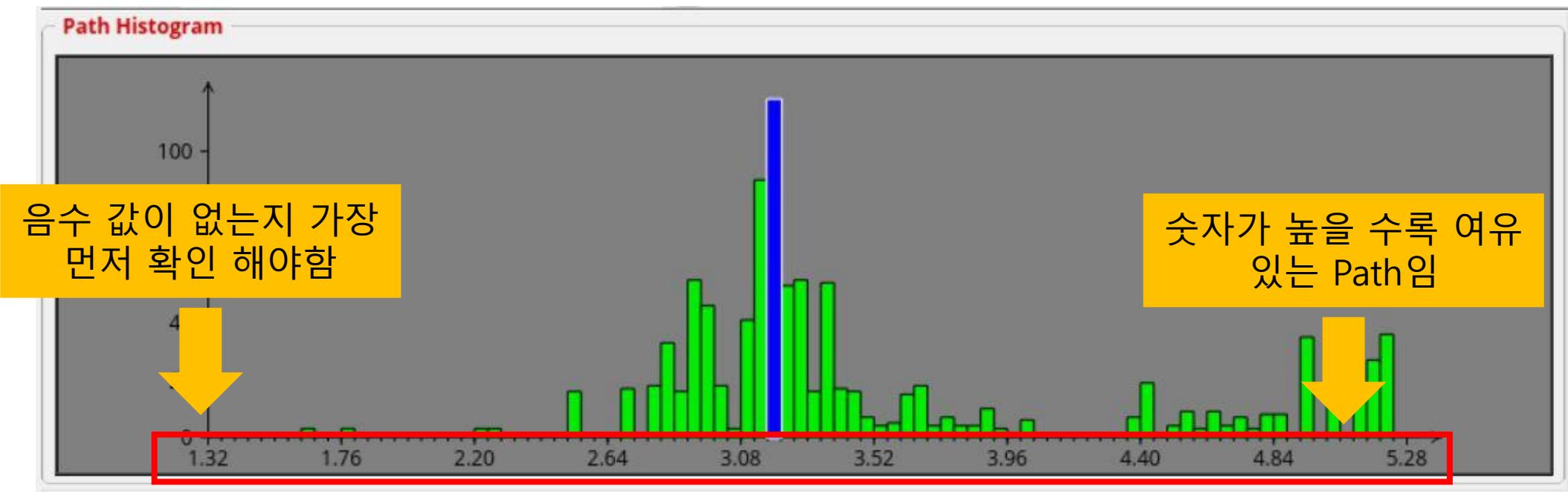
genus

3.16ns 일찍 도착한 Path가 100개 이상 된다는 것을 알 수 있음



# Synthesis

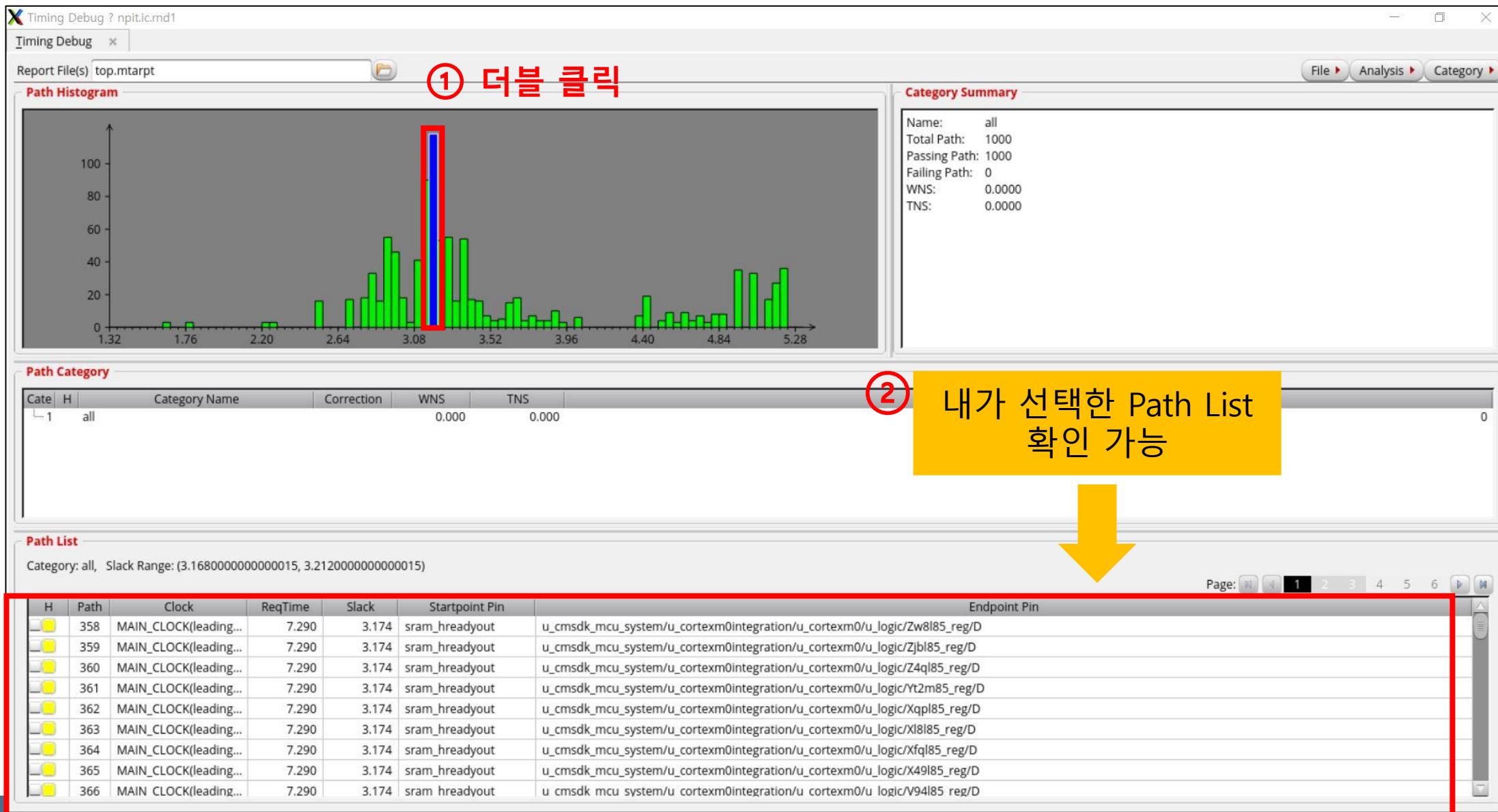
genus



# Synthesis

- Histogram의 세부내용 확인 방법

genus



# Synthesis

## genus

- Histogram의 세부내용 확인 방법
- Start point와 Endpoint 확인 가능함

Path List

Category: all, Slack Range: (3.1680000000000015, 3.2120000000000015)

Page: 1 2 3 4 5 6

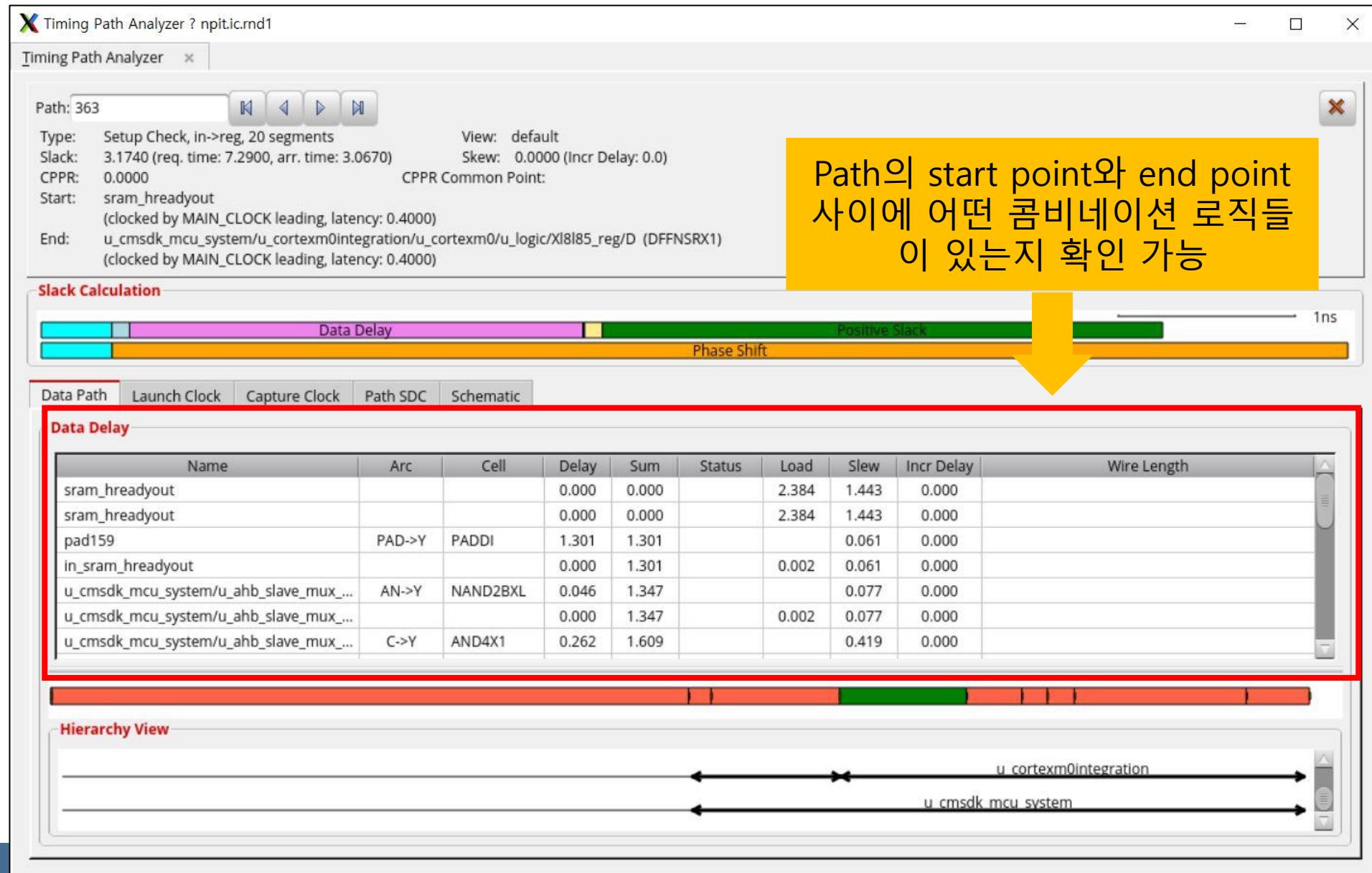
H	Path	Clock	ReqTime	Slack	Startpoint Pin	Endpoint Pin
358	MAIN_CLOCK(leading...		7.290	3.174	sram_nreadyout	u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Zw8l85_reg/D
359	MAIN_CLOCK(leading...		7.290	3.174	sram_hreadyout	u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Zjbl85_reg/D
360	MAIN_CLOCK(leading...		7.290	3.174	sram_hreadyout	u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Z4ql85_reg/D
361	MAIN_CLOCK(leading...		7.290	3.174	sram_hreadyout	u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Yt2m85_reg/D
362	MAIN_CLOCK(leading...		7.290	3.174	sram_breadyout	u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Vqpl85_reg/D
363	MAIN_CLOCK(leading...		7.290	3.174	sram_hreadyout	u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Xl8l85_reg/D
364	MAIN_CLOCK(leading...		7.290	3.174	sram_nreadyout	u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Xlql85_reg/D
365	MAIN_CLOCK(leading...		7.290	3.174	sram_hreadyout	u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/X49l85_reg/D
366	MAIN CLOCK(leading...		7.290	3.174	sram hreadyout	u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/V94l85_reg/D

① 더블 클릭

# Synthesis

- Histogram의 세부내용 확인 방법

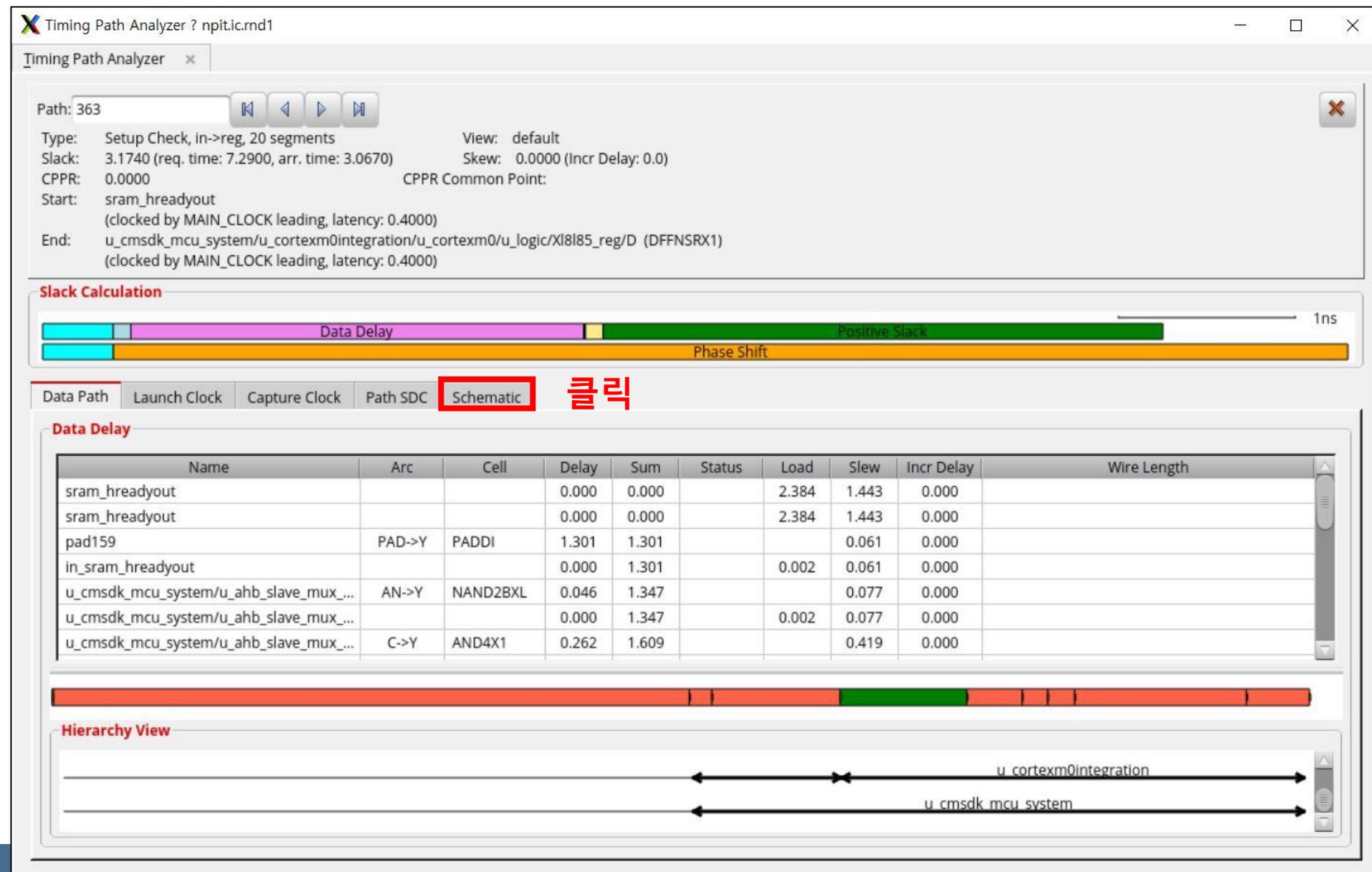
genus



# Synthesis

- Histogram의 세부내용 확인 방법

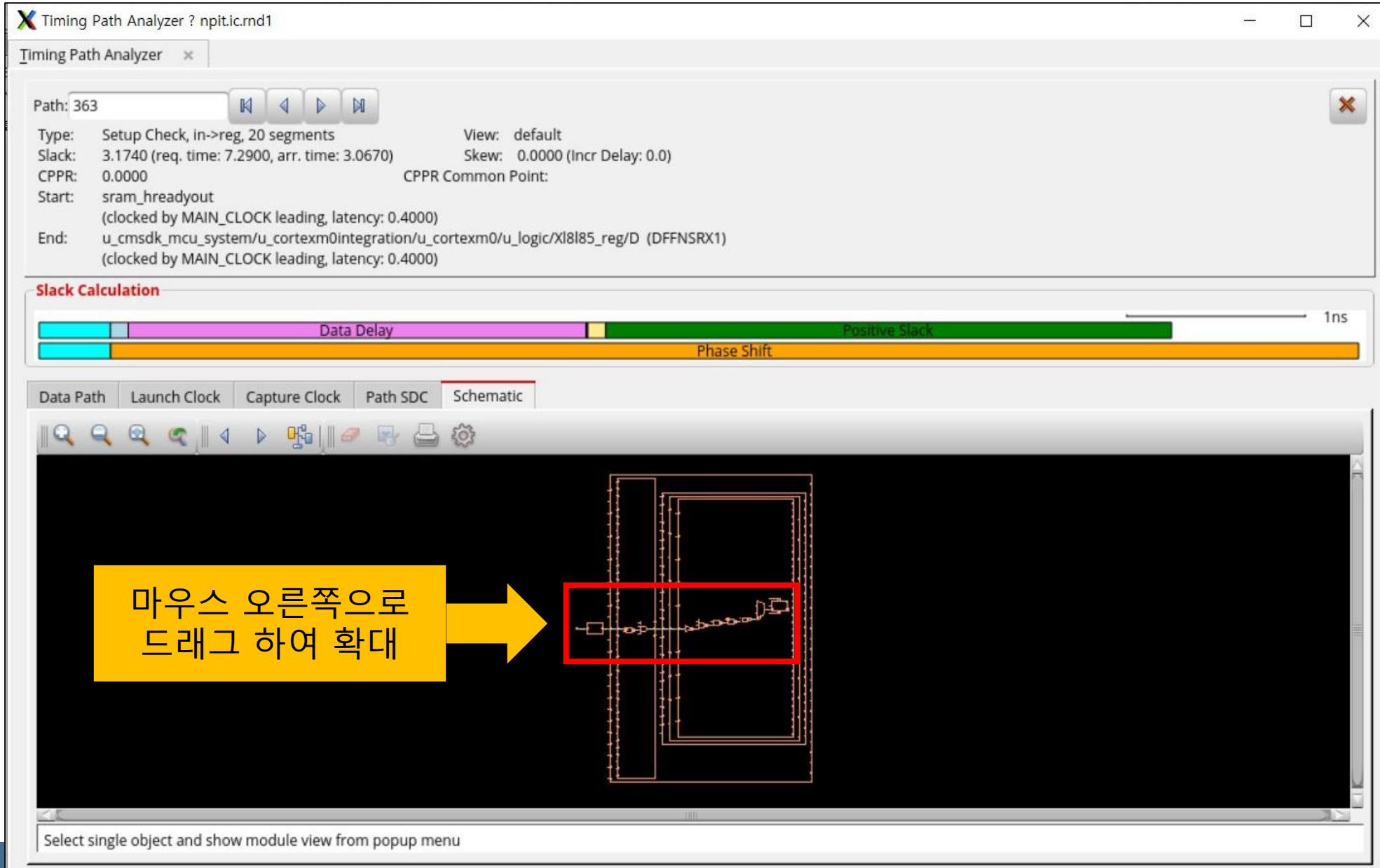
genus



# Synthesis

genus

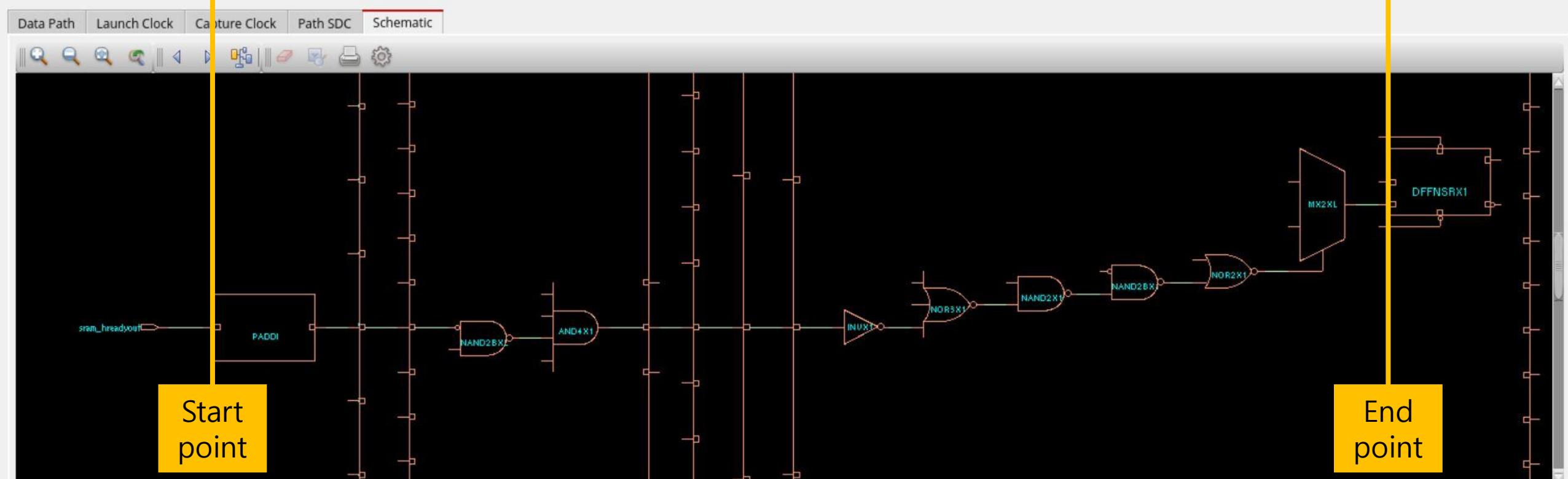
- Schematic 확인 가능



# Synthesis

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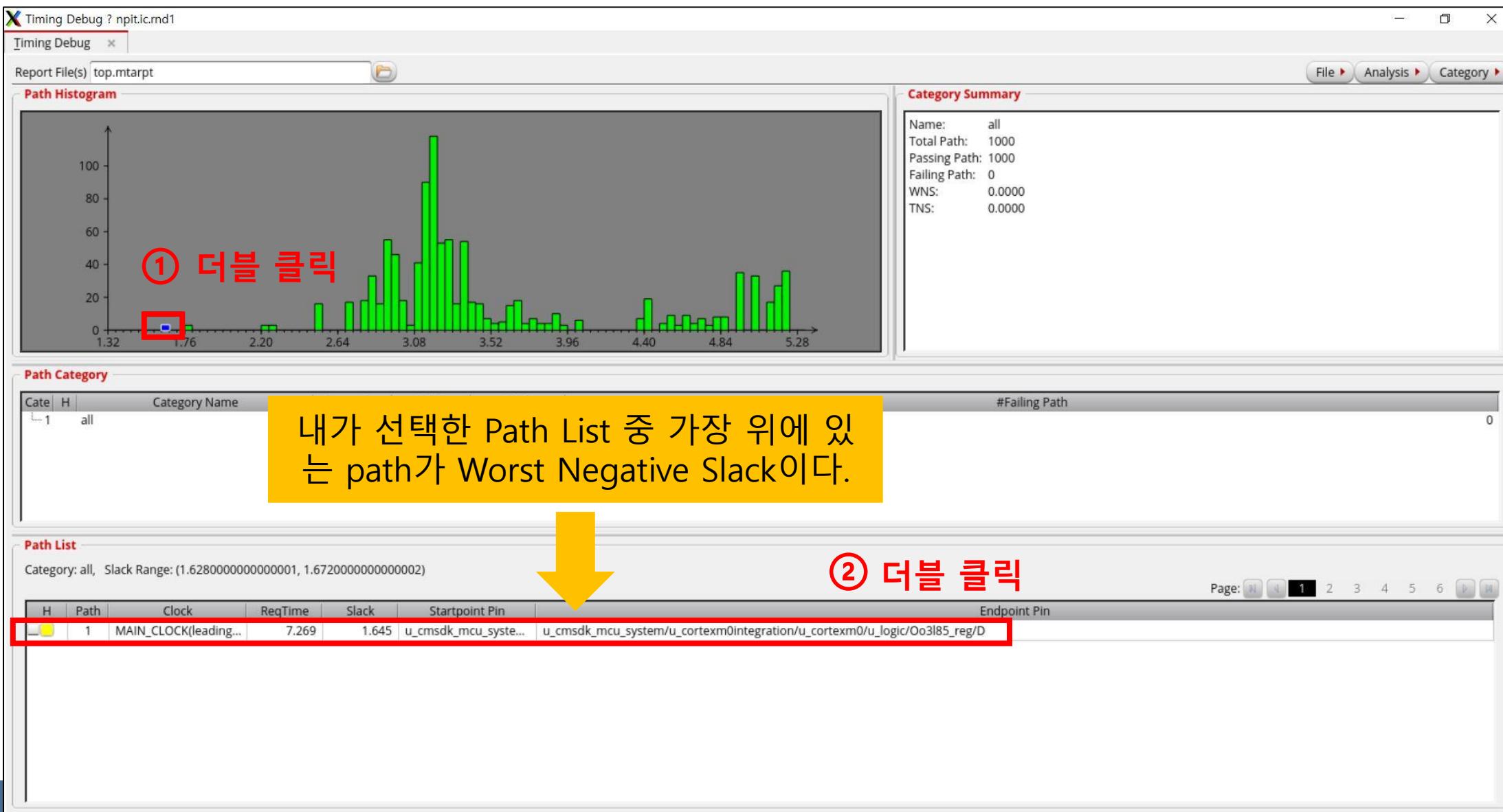
Path와 Path 사이의 start point, end point, 콤비네이션 로직을 schematic으로 확인할 수 있음



# Synthesis

genus

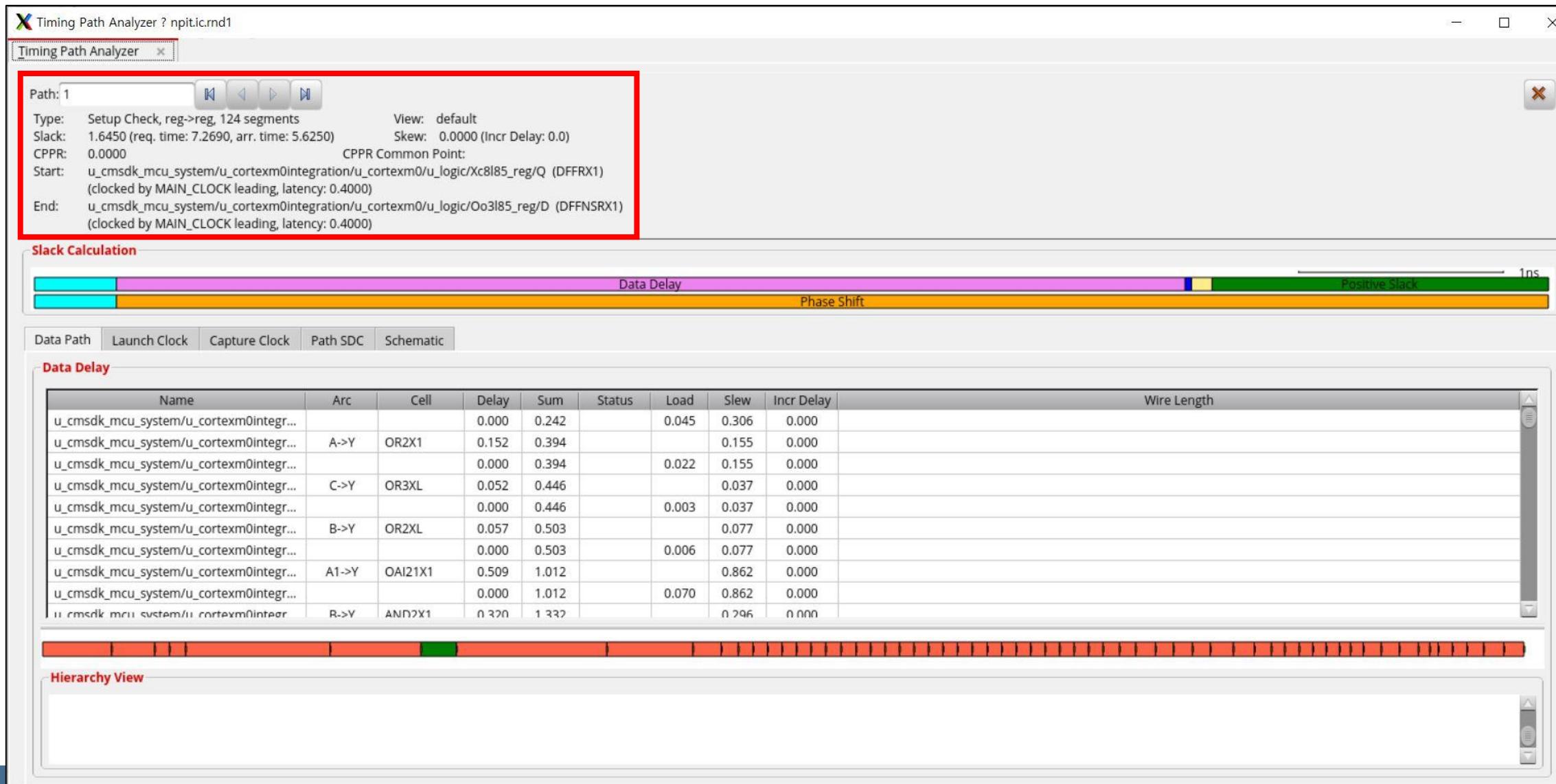
- Histogram을 이용한 worst negative Slack 확인



# Synthesis

genus

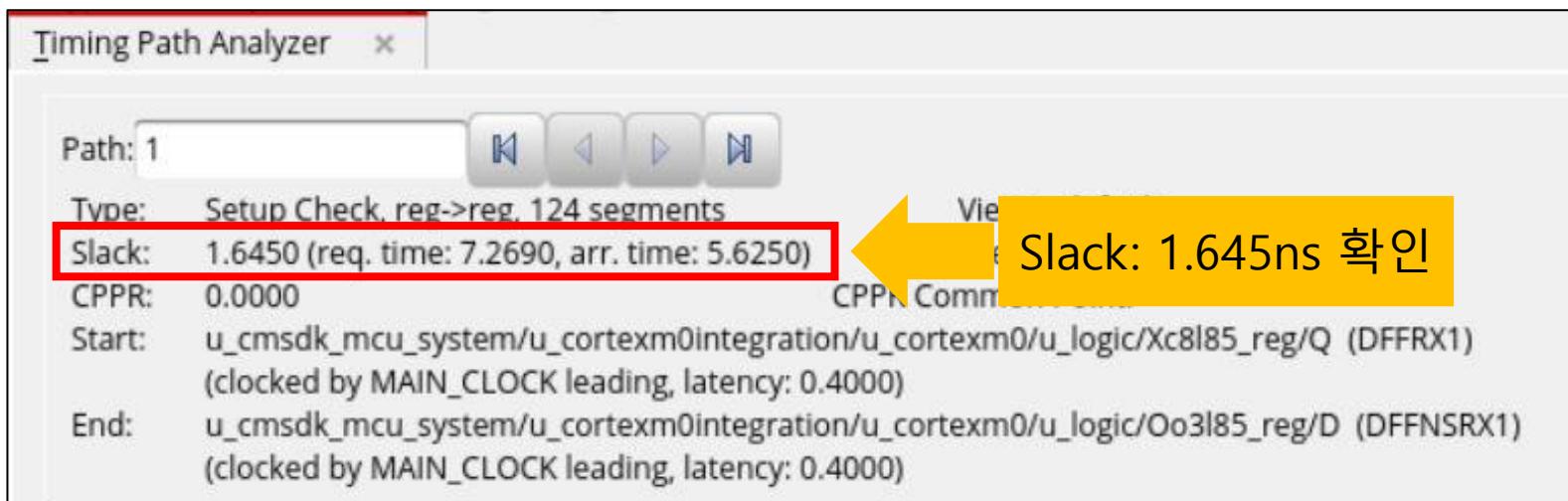
- Histogram을 이용한 worst negative Slack 확인



# Synthesis

## genus

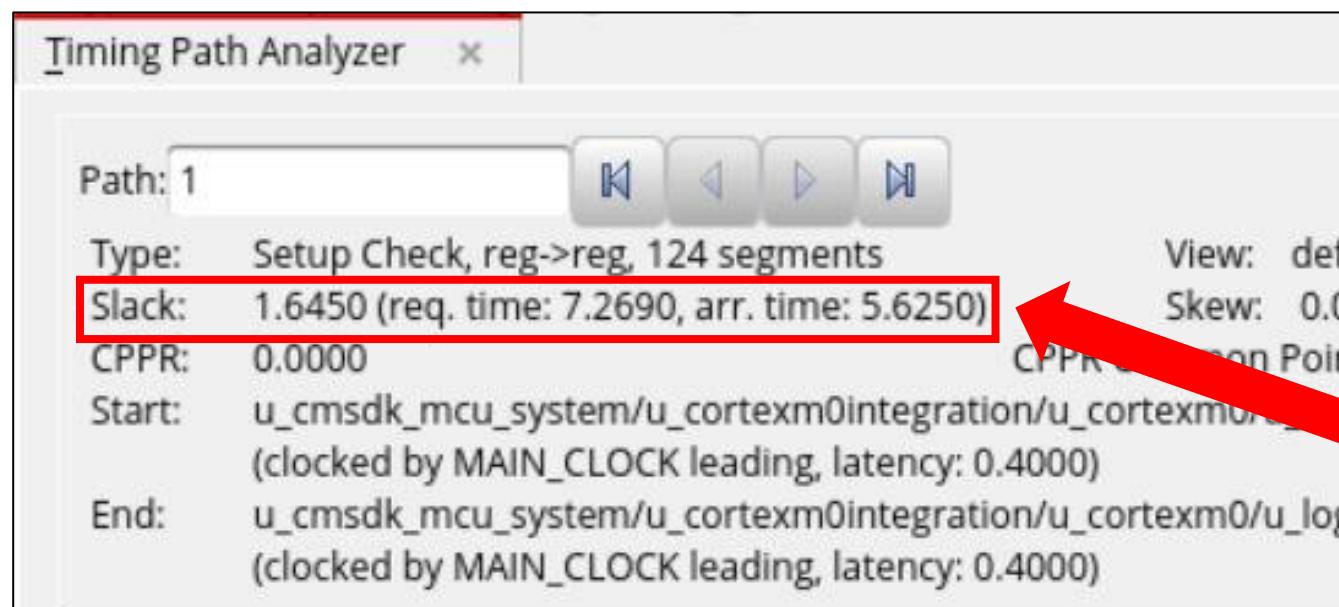
- Histogram을 이용한 worst negative Slack 확인



# Synthesis

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- Histogram을 이용해 total negative Slack을 확인한 결과 report timing 결과와 같음
- Slack이 양수이므로 문제없음



report timing 결과

Path 1: MET (1645 ps) Setup Check with Pin u\_cmse

Group: MAIN\_CLOCK

Startpoint: (R) u\_cmsdk\_mcu\_system/u\_cortexm0/integration/u\_cortexm0/u\_log

Clock: (R) MAIN\_CLOCK

Endpoint: (F) u\_cmsdk\_mcu\_system/u\_cortexm0/integration/u\_cortexm0/u\_log

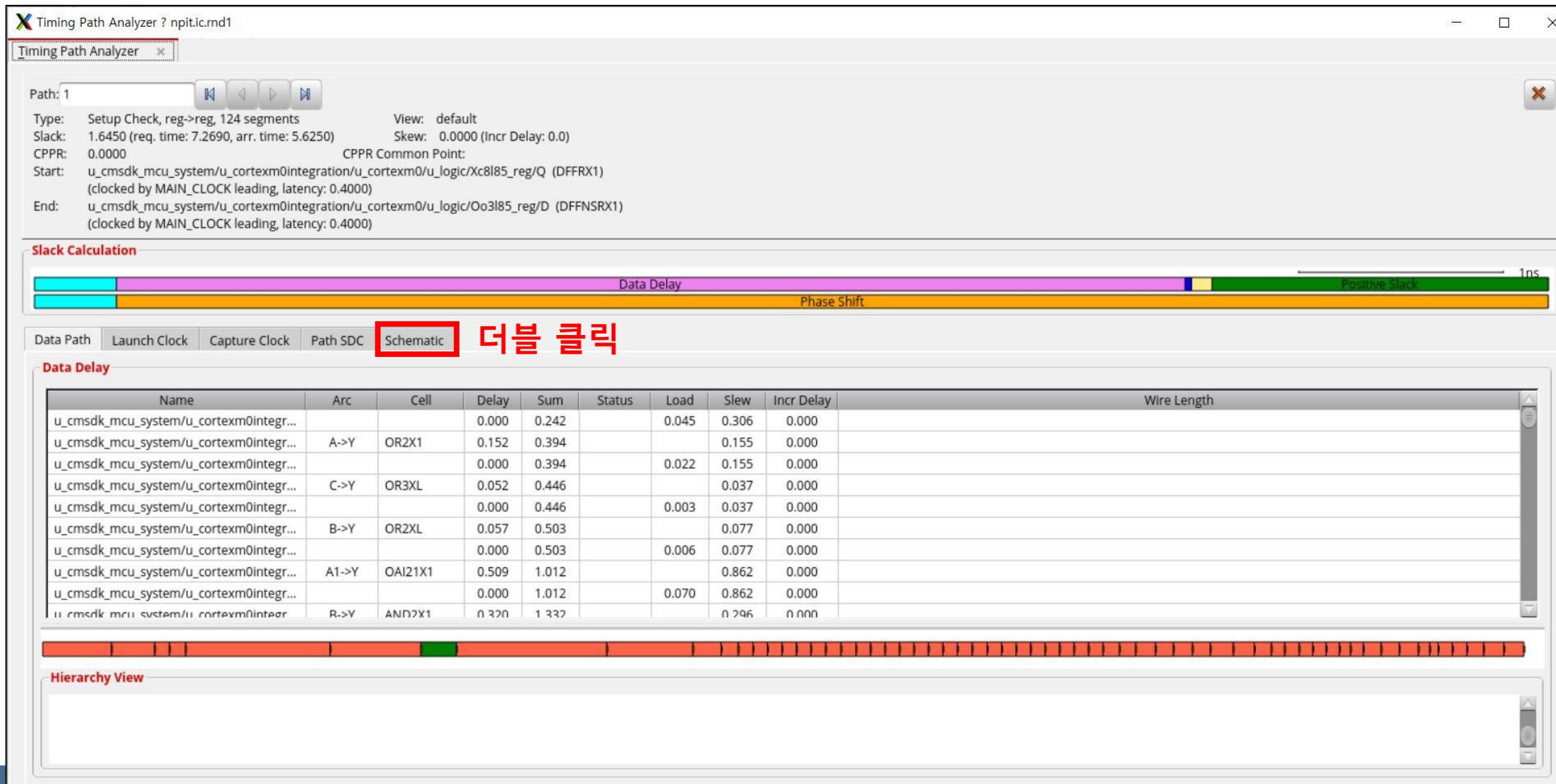
Clock: (R) MAIN\_CLOCK

	Capture	Launch
Clock Edge:+	7000	0
Src Latency:+	200	200
Net Latency:+	200 (I)	200 (I)
Arrival:=	7400	400
Setup:-	31	
Uncertainty:-	100	
Required Time:=	7269	
Launch Clock:-	400	
Data Path:-	5225	
Slack:=	1645	

# Synthesis

genus

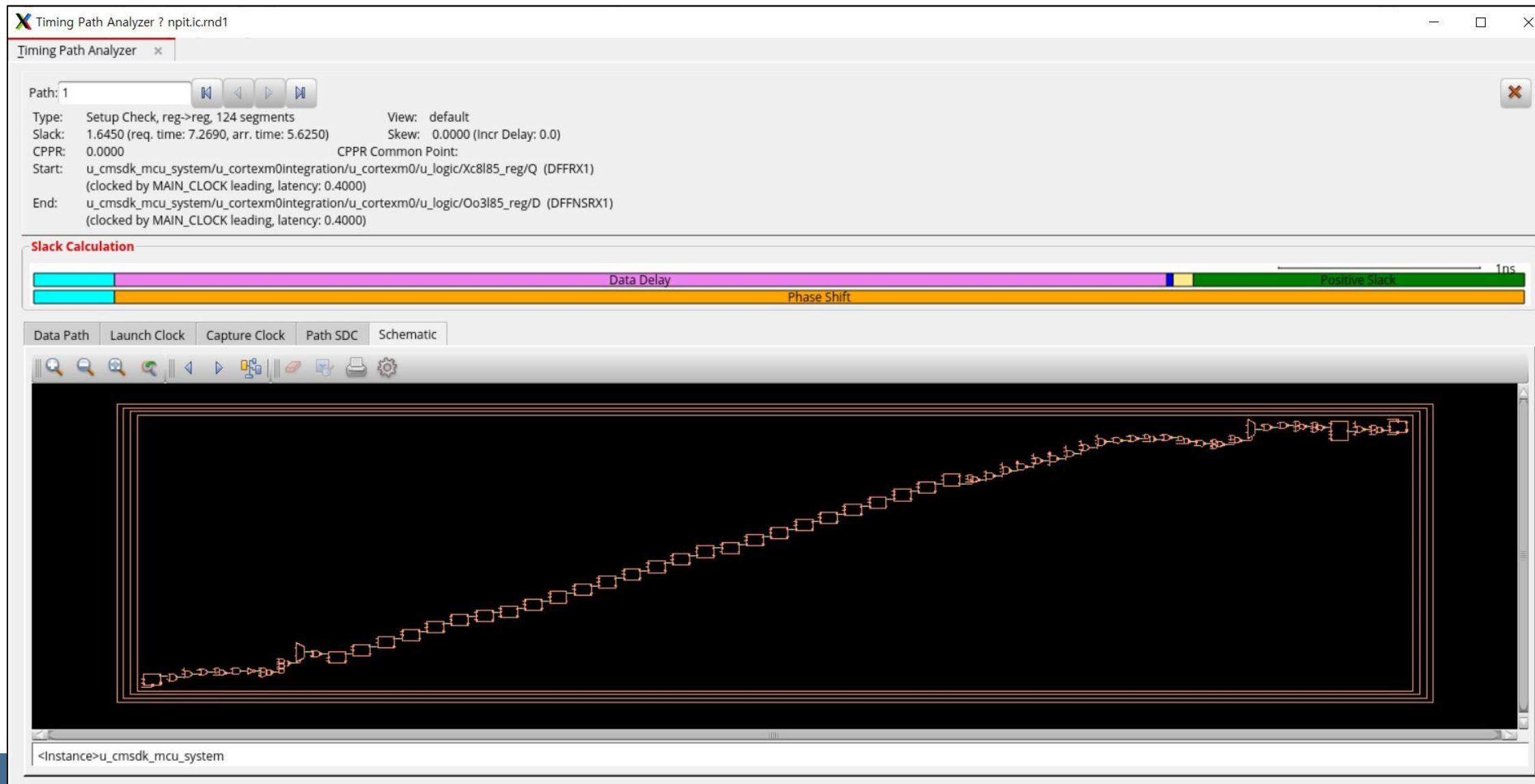
- Histogram을 이용한 worst negative Slack 확인



# Synthesis

genus

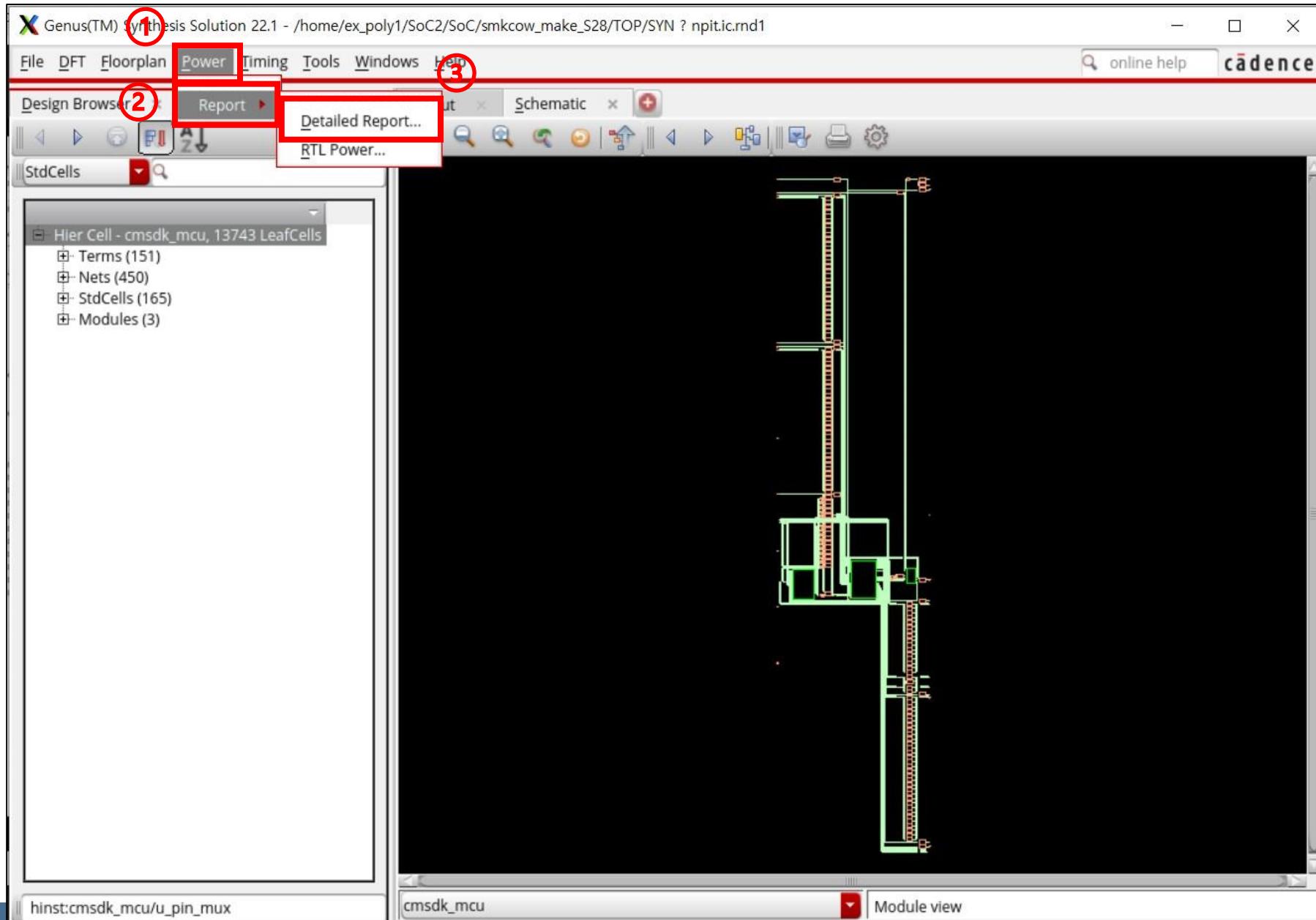
- Histogram을 이용해 worst negative Slack의 schematic 확인 가능



# Synthesis

genus

- Power를 통해 전력 소모량을 알 수 있음



# Synthesis

genus

각 instance의 전력 소모량을 알 수 있음

TOP 모듈을 보면 총 누적 전력 소모량을 알 수 있음

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_test_slave.u_apb_test_slave	170	21.198	23.65.246	411.187	411.6.478
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_timer_0.u_apb_timer_0	383	59.581	62674.151	3337.701	66011.852
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_timer_1.u_apb_timer_1	383	59.589	62679.337	3336.089	66015.426
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_uart_0.u_apb_uart_0	481	80.187	88276.954	5172.004	93448.958
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_uart_1.u_apb_uart_1	481	80.322	88257.579	5172.971	93430.550
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_uart_2.u_apb_uart_2	480	80.331	88267.739	5168.302	93436.041
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog	469	84.528	82159.548	9836.187	91995.734
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog_frc	342	63.021	58141.882	9572.026	67713.908
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/u_ahb_to_apb	140	30.587	40682.143	3066.842	43748.985
cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/u_apb_slave_mux	16	16.303	317.111	383.158	700.269
cmsdk_mcu/u_cmsdk_mcu_system/u_cmsdk_mcu_stclkctrl	5.830	7558.270	254.603	7812.873	
cmsdk_mcu/u_cmsdk_mcu_system/u_cmsdk_mcu_sysctrl	12.999	12803.600	571.532	13375.132	
cmsdk_mcu/u_cmsdk_mcu_system/u_cortexm0integration	1193.780	932151.657	303284.851	1235436.508	
cmsdk_mcu/u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0	7790	1193.780	932151.657	303284.851	1235436.508
cmsdk_mcu/u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic	7790	1193.780	932151.657	303284.851	1235436.508
cmsdk_mcu/u_cmsdk_mcu_system/u_system_rom_table	42	6.357	4884.568	203.913	5088.480
cmsdk_mcu/u_pin_mux	6	0.892	248.572	260.794	509.366
cmsdk_mcu	13743	5817237.115	91854993.074	2949871.304	94804864.378

# Synthesis

genus

```
$> ./clean.tcl
```

```
$> ./run_synthesis
```

지금부터는 run\_synthesis를 실행하여 전체 스크립트를 자동 배치모드로 한번에 진행

①

```
[ex_poly1@npit SYN]$ ./clean.tcl
```

②

```
[ex_poly1@npit SYN]$ ./run_synthesis
```

# Synthesis

genus를 사용 준비

```
/home/ex_poly1/SoC2/SoC/smkcov_make_S28/TOP/SYN
```

- 두개의 터미널 사용 (위의 경로에서 진행)
- 하나는 `./run_synthesis` 명령실행, 나머지는 report 파일의 생성을 확인

The image shows two terminal windows side-by-side. The left window, titled 'ex\_poly1@npit:SYN', displays the command history for running synthesis:

```
[ex_poly1@npit SYN]$ pwd  
/home/ex_poly1/SoC2/SoC/smkcov_make_S28/TOP/SYN  
[ex_poly1@npit SYN]$ ./clean.tcl  
[ex_poly1@npit SYN]$ ./run_synthesis
```

The right window, also titled 'ex\_poly1@npit:SYN', shows the directory structure and the list of generated report files after synthesis:

```
File Edit View Search Terminal Help  
[ex_poly1@npit SYN]$ ls  
lean.tcl cons fv log mapped report run_synthesis script unmapped  
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
0_check_design.rpt  
1_check_timing.rpt  
2_report_port.rpt  
3_report_datapath_generic.rpt  
4_report_datapath_map.rpt  
5_default_post_syn_map.rpt  
5_MAIN_CLOCK_post_syn_map.rpt  
final.rpt  
[ex_poly1@npit report]$
```

On the far right of the right window, there are several small report files listed vertically:

```
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt
```

# Synthesis

## genus

```
$> ./run_synthesis
```

- `./run_synthesis` 명령으로 합성의 모든 과정이 진행됨

## Genus 툴 실행 결과

# Synthesis

genus

\$> cd report

- 합성 진행상황을 report 폴더에서 실시간으로 확인

```
[ex_poly1@npit SYN]$ ls  
clean.tcl  cons  fv  log  mapped  report  run_synthesis  script  unmapped
```

# Synthesis

genus

\$> //

- 합성 //
- 명령어를 활용하여 report가 실시간으로 생성되는지 확인함
- 각 report의 결과가 정상적으로 나왔는지 확인함

합성 전

```
[ex_poly1@npit report]$ ll  
total 0
```

합성 후

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_men_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt  
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

# Synthesis

genus

\$> vi 00\_check\_design.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt  
  
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

큰 문제가 없음을  
확인함

- RTL소스의 무결성을 확인함

Name	Total
2 Check Design Report (c)	
3 -----	
4 -----	
5 Summary	
6 -----	
7 -----	
8 -----	
9 -----	
10 Unresolved References	0
11 Empty Modules	0
12 Unloaded Port(s)	0
13 Unloaded Sequential Pin(s)	0
14 Unloaded Combinational Pin(s)	11
15 Assigns	137
16 Undriven Port(s)	0
17 Undriven Leaf Pin(s)	0
18 Undriven hierarchical pin(s)	1241
19 Multidriven Port(s)	0
20 Multidriven Leaf Pin(s)	0
21 Multidriven hierarchical Pin(s)	0
22 Multidriven unloaded net(s)	0
23 Constant Port(s)	0
24 Constant Leaf Pin(s)	880
25 Constant hierarchical Pin(s)	56
26 Preserved leaf instance(s)	13566
27 Preserved hierarchical instance(s)	30
28 Feedthrough Modules(s)	0
29 Libcells with no LEF cell	4
30 Physical (LEF) cells with no libcell	107
31 Subdesigns with long module name	0
32 Physical only instance(s)	0
33 Logical only instance(s)	0
34 -----	
35 Done Checking the design.	

# Synthesis

genus

\$> vi 01\_check\_timing.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00 check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

• 내가 입력한 constraint에 문제가 없음을 확인함

1	=	Generated by:	Genus(TM) Synthesis Solution 22.16-s078_1
2		Generated on:	Feb 01 2025 11:35:18 pm
3		Module:	cmsdk_mcu
4		Technology libraries:	fast_vdd1v0 1.0 slow_vdd1v0 1.0 giolib045 physical_cells
5		Operating conditions:	PVT_0P9V_125C
6		Interconnect mode:	global
7		Area mode:	physical library
8			=====
9			
10			
11			
12			
13			
14			
15		Lint summary	
16		Unconnected/logic driven clocks	0
17		Sequential data pins driven by a clock signal	0
18		Sequential clock pins without clock waveform	0
19		Sequential clock pins with multiple clock waveforms	0
20		Generated clocks without clock waveform	0
21		Generated clocks with incompatible options	0
22		Generated clocks with multi-master clock	0
23		Generated clocks with master clock not reaching the generated clock target	0
24		Paths constrained with different clocks	0
25		Loop-breaking cells for combinational feedback	0
26		Nets with multiple drivers	0
27		Timing exceptions with no effect	0
28		Suspicious multi_cycle exceptions	0
29		Pins/ports with conflicting case constants	0
30		Inputs without clocked external delays	0
31		Outputs without clocked external delays	0
32		Inputs without external driver/transition	0
33		Outputs without external load	0
34		Exceptions with invalid timing start-/endpoints	0
35			0
36			0
37			0
		Total:	0

# Synthesis

genus

\$> vi 02\_report\_port.rpt

- External Driver에 원하는 cell이 입력되어 있는지 확인하는 것이 중요

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

```
1 ======  
2 Generated by: Genus(TM) Synthesis Solution 22.16-s078_1  
3 Generated on: Feb 01 2025 11:35:18 pm  
4 Module: cmsdk_mcu  
5 Technology libraries: fast_vdd1v0 1.0  
6 slow_vdd1v0 1.0  
7 giolib045  
8 physical_cells  
9 Operating conditions: PVT_0P9V_125C  
10 Interconnect mode: global  
11 Area mode: physical library  
12 ======  
13  
14  
15 External Delays & Exceptions  
16 -----  
17 Port Dir Clock Rise Fall Ext Delay Exception  
18 19 Object Object/Type  
20 XTAL1 in N/A N/A N/A N/A N/A N/A  
21 NRST in MAIN_CLOCK 100.0 100.0 in_del N/A N/A  
22 in MAIN_CLOCK no_value no_value in_del_89_1 N/A  
23 nTRST in MAIN_CLOCK 100.0 100.0 in_del_1_1 N/A  
24 in MAIN_CLOCK no_value no_value in_del_90_1 N/A  
25 SWCLKTCK in MAIN_CLOCK 100.0 100.0 in_del_2_1 N/A  
26 in MAIN_CLOCK no_value no_value in_del_91_1 N/A  
27 TDI in MAIN_CLOCK 100.0 100.0 in_del_3_1 N/A  
28 in MAIN_CLOCK no_value no_value in_del_92_1 N/A  
29 SWDIOTMS in MAIN_CLOCK 100.0 100.0 in_del_4_1 N/A
```

# Synthesis

genus

\$> vi 02\_report\_port.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

- /External Driver 명령어를 사용하여 검색
- PADDI와 같이 내가 원하는 셀이 입력되어 있음

External Driver/Slew							
Port	Dir	External	External	Slew	Slew	Timing Case	Timing Ideal
		Driver	Driver				
XTAL1	in			0.0	0.0		false
NRST	in	PADDI/Y	PADDI/Y	0.0	0.0		false
nTRST	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
SWCLKTCK	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
TDI	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
SWDIOTMS	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hreadyout	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[31]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[30]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[29]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[28]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[27]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[26]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[25]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[24]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[23]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[22]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[21]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[20]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
flash_hrdata[19]	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false

# Synthesis

genus

\$> vi 03\_report\_datapath\_generic.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
1 Command: report datapath > ./report/03_report_datapath_generic.rpt  
2 Warning: '-sort' is not specified. By default, 'report datapath' orders the components based on instance name  
3 =====  
4 Generated by: Genus(TM) Synthesis Solution 22.16-s078_1  
5 Generated on: Feb 01 2025 11:35:31 pm  
6 Module: cmsdk_mcu  
7 Technology libraries: fast_vdd1v0 1.0  
8 slow_vdd1v0 1.0  
9 giolib045  
10 physical_cells  
11 fast_vdd1v0 1.0  
12 slow_vdd1v0 1.0  
13 giolib045  
14 physical_cells  
15 Operating conditions: PVT_0P9V_125C  
16 Interconnect mode: global  
17 Area mode: physical library  
18 =====  
19  
20  
21 Type CellArea Percentage  
22 -----  
23 datapath modules 0.00 0.00  
24 external muxes 0.00 0.00  
25 others 2139958.05 100.00  
26  
27 total 2139958.05 100.00
```

Total의 숫자가 작을수록 critical path가 적고 area가 작아짐

# Synthesis

genus

\$> vi 04\_report\_datapath\_map.rpt

- syn\_generic → syn\_map 진행 후 datapath 비교

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
1 Command: report datapath > ./report/04_report_datapath_map.rpt  
2 Warning: '-sort' is not specified. By default, 'report datapath' orders the components based on instance name  
3 =====  
4 Generated by: Genus(TM) Synthesis Solution 22.16-s078_1  
5 Generated on: Feb 01 2025 11:35:53 pm  
6 Module: cmsdk_mcu  
7 Technology libraries: fast_vdd1v0 1.0  
8 slow_vdd1v0 1.0  
9 giolib045  
10 physical_cells  
11 fast_vdd1v0 1.0  
12 slow_vdd1v0 1.0  
13 giolib045  
14 physical_cells  
15 Operating conditions: PVT_0P9V_125C  
16 Interconnect mode: global  
17 Area mode: physical library  
18 =====  
19  
20  
21 Type CellArea Percentage  
22 -----  
23 datapath modules 0.00 0.00  
24 external muxes 0.00 0.00  
25 others 2139890.38 100.00  
26  
27 total 2139890.38 100.00
```

Total의 숫자가 작을수록 critical path가 적고 area가 작아짐

# Synthesis

genus

\$> vi 05\_MAIN\_CLOCK\_post\_syn\_map.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_svn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
1 =====  
2 Generated by: Genus(TM) Synthesis Solution 22.16-s078_1  
3 Generated on: Feb 01 2025 11:35:54 pm  
4 Module: cmsdk_mcu  
5 Operating conditions: PVT_OP9V_125C  
6 Interconnect mode: global  
7 Area mode: physical library  
8 =====  
9  
10  
11 Path 1: MET (1644 ps) Setup Check with Pin u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/0o3l85_reg/CKN->D  
12 Group: MAIN_CLOCK  
13 Startpoint: (R) u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Xc8l85_reg/CK  
14 Clock: (R) MAIN_CLOCK  
15 Endpoint: (F) u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/0o3l85_reg/D  
16 Clock: (R) MAIN_CLOCK  
17  
18 Capture Launch  
19 Clock Edge:+ 7000 0  
20 Src Latency:+ 200 200  
21 Net Latency:+ 200 (I) 200 (I)  
22 Arrival:= 7400 400  
23  
24 Setup:- 31  
25 Uncertainty:- 100  
26 Required Time:= 7269  
27 Launch Clock:- 400  
28 Data Path:- 5225  
29 Slack:= 1644
```

Slack에 문제 없음

# Synthesis

genus

\$> vi 06\_report\_constraint.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MATN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

- Constraint에 만족하는 디자인이 나왔는지 검증

```
1 =====  
2 Generated by:          Genus(TM) Synthesis Solution 22.16-s078_1  
3 Generated on:          Feb 01 2025  11:36:03 pm  
4 Module:                cmsdk_mcu  
5 Operating conditions:  PVT A09V 125C  
Setup Timing, clock_period,  
pulse_width에 문제 없음  
=====  
11 Checking for violation type : Setup Timing Slack  
12 -----  
13 No timing slack violation found.  
14 -----  
15 Checking for violation type : clock_period  
16 -----  
17 No paths found.  
18 -----  
19 Checking for violation type : pulse_width  
20 -----  
21 No paths found.  
22 -----  
23 Checking for violation type : max_capacitance  
24 -----  
25 -----  
26 |   Pin    | Required|Actual |Slack | Mode |  
27 |           | Load   | Load   | Load  |  
28 |           | (ff)  | (ff)  | (ff) |  
29 -----
```

# Synthesis

\$> vi 06\_report\_constraint.rpt

genus

- max\_capacitance에 Required Load보다 Actual Load가 크게 걸림
- Io셀을 이미 넣은 상황이기 때문에 **수정 불가**
- BE과정에서 개선의 여지가 있기 때문에 일단 유지

Checking for violation type : max\_capacitance

Pin	Required Load (ff)	Actual Load (ff)	Slack Load (ff)	Mode
port:cmsdk_mcu/P1[0]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[1]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[2]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[3]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[4]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[5]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[6]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[7]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[8]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[9]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[10]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[11]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[12]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[13]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[14]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/P1[15]	888.30	2388.40	-1500.10	default
port:cmsdk_mcu/flash_hrdraft[14]	888.30	2385.40	-1497.10	default
port:cmsdk_mcu/sram_hrdraft[13]	888.30	2385.40	-1497.10	default
port:cmsdk_mcu/sram_hrdraft[12]	888.30	2385.40	-1497.10	default
port:cmsdk_mcu/sram_hrdraft[11]	888.30	2385.40	-1497.10	default
port:cmsdk_mcu/sram_hrdraft[10]	888.30	2385.40	-1497.10	default
port:cmsdk_mcu/sram_hrdraft[9]	888.30	2385.40	-1497.10	default
port:cmsdk_mcu/sram_hrdraft[8]	888.30	2385.40	-1497.10	default
port:cmsdk_mcu/sram_hrdraft[7]	888.30	2385.40	-1497.10	default

# Synthesis

\$> vi 06\_report\_constraint.rpt

genus

- max\_transition에 Required slew보다 Actual slew가 크게 걸림
- 같은 셀 중 드라이브 스트레스가 높은 셀을 찾아 수정 가능

Checking for violation type : max_transition				
	Pin	Required Slew (ps)	Actual Slew (ps)	Slack Slew (ps)
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4850/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4851/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4852/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4853/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4854/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4855/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4856/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4857/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4858/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4859/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4860/B1	280	915	-635
	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subsystem/gen_apb_watchdog.u_apb_watchdog/u_apb_watchdog_frc/g 4861/B1	280	915	-635

No max\_fanout rule violations.

fanout 문제 없음

# Synthesis

genus

\$> vi 07\_MAIN\_CLOCK\_post\_syn\_opt.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
1 =====  
2 Generated by: Genus(TM) Synthesis Solution 22.16-s078_1  
3 Generated on: Feb 01 2025 11:36:09 pm  
4 Module: cmsdk_mcu  
5 Operating conditions: PVT_OP9V_125C  
6 Interconnect mode: global  
7 Area mode: physical library  
8 =====  
9  
10  
11 Path 1: MET (1645 ps) Setup Check with Pin u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/0o3l85_reg/CKN->D  
12 Group: MAIN_CLOCK  
13 Startpoint: (R) u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Xc8l85_reg/CK  
14 Clock: (R) MAIN_CLOCK  
15 Endpoint: (F) u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/0o3l85_reg/D  
16 Clock: (R) MAIN_CLOCK  
17  
18 Capture Launch  
19 Clock Edge:+ 7000 0  
20 Src Latency:+ 200 200  
21 Net Latency:+ 200 (I) 200 (I)  
22 Arrival:= 7400 400  
23  
24 Setup:- 31  
25 Uncertainty:- 100  
26 Required Time:= 7269  
27 Launch Clock:- 400  
28 Data Path:- 5225  
29 Slack:= 1645
```

Slack에 문제 없음

# Synthesis

genus

\$> vi 08\_cmsdk\_mcu\_SYN\_analysis\_view.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
1 Multi-Mode Analysis View Report  
2 _____  
3  
4 + ALL Views  
5 |  
6 + Analysis View: default_emulate_view  
7 |  
8 + Delay Calc Corner: default_emulate_delay_corner  
9 |  
10 + timing_condition: default_emulate_timing_cond_max  
11 |  
12 + library_sets: default_emulate_libset_max  
13 |  
14 + timing: /home/ex_poly1/SoC2/SoC/smkcowl_make_S28/TOP/SYN/../../../../GPKD045/digital/gsclib045_all_v4.4/gsclib045/tim  
ing/fast_vdd1v0_basicCells.lib  
15 /home/ex_poly1/SoC2/SoC/smkcowl_make_S28/TOP/SYN/../../../../GPKD045/digital/gsclib045_all_v4.4/gsclib045/  
timing/slow_vdd1v0_basicCells.lib  
16 /home/ex_poly1/SoC2/SoC/smkcowl_make_S28/TOP/SYN/../../../../GPKD045/digital/giolib045_v3.5/timing/pads_SS  
_slvg.lib  
17 |  
18 |  
19 |  
20 + rc_corner: default_emulate_rc_corner  
21 |  
22 + postRoute_res: 1.0 1.0 1.0  
23 |  
24 + postRoute_cap: 1.0 1.0 1.0  
25 |  
26 + postRoute_xcap: 1.0 1.0 1.0  
27 |  
28 + postRoute_clkcap: 1.0 1.0 1.0  
29 |  
30 + postRoute_clkres: 1.0 1.0 1.0  
31 |
```

# Synthesis

genus

\$> vi 09\_cmsdk\_mcu\_SYN\_area.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

1	=====	Generated by:	Genus(TM) Synthesis Solution 22.16-s078_1	2	Cell Count	Cell Area	Net Area	Total Area
3	=====	Generated on:	Feb 01 2025 11:36:11 pm	4				
5	=====	Module:	cmsdk_mcu	6				
7	=====	Operating conditions:	PVT_0P9V_125C	8				
9	=====	Interconnect mode:	global	10	Instance	Module		
11	=====	Area mode:	physical library	12	cmsdk_mcu			
13	=====	u_cmsdk_mcu_clockctrl	cmsdk_mcu_clockctrl_preserve	14	u_cmsdk_mcu_system	cmsdk_mcu_system	13566	37429.164 18046.327 55475.491
15	=====	u_addr_decode	cmsdk_mcu_addr_decode_BASEADDR_GPIO0032h40010000_BA	16	u_ahb_default_slave_1	cmsdk_ahb_default_slave	5	46.170 23.187 69.357
17	=====	u_ahb_gpio_0	cmsdk_ahb_gpio_ALTERNATE_FUNC_MASK16h0000_ALTERNAT	18	u_ahb_to_ip	cmsdk_ahb_to_ip	625	1794.474 694.475 2488.949
19	=====	u_iop_gpio	cmsdk_iop_gpio_ALTERNATE_FUNC_MASK16h0000_ALTERNAT	20	u_ahb_gpio_1	cmsdk_ahb_gpio_ALTERNATE_FUNC_MASK16h002a_ALTERNAT	607	1688.454 647.549 2336.003
21	=====	u_ahb_to_gpio	cmsdk_mcu_system_cmsdk_ahb_to_ip_1	22	u_iop_gpio	cmsdk_iop_gpio_ALTERNATE_FUNC_MASK16h002a_ALTERNAT	643	1832.094 731.175 2563.269
23	=====	u_ahb_slave_mux_sys_bus	cmsdk_ahb_slave_mux_PORT0_ENABLE1_PORT1_ENABLE1_PO	24	u_apb_subsystem	cmsdk_apb_subsystem_APB_EXT_PORT12_ENABLE0_APB_EXT	127	271.890 128.537 400.427
25	=====	gen_apb_dualtimers_2.u_apb_dualtimers_2	cmsdk_apb_dualtimers	26	u_apb_timer_frc_1	cmsdk_apb_dualtimers_frc	1095	3471.642 1389.577 4861.219
27	=====	u_apb_timer_frc_2	cmsdk_mcu_system_cmsdk_apb_dualtimers_frc_1	28	gen_apb_test_slave.u_apb_test_slave	cmsdk_apb_test_slave	490	1549.602 621.340 2170.942
29	=====	gen_apb_timer_0.u_apb_timer_0	cmsdk_apb_timer	30	gen_apb_timer_1.u_apb_timer_1	cmsdk_mcu_system_cmsdk_apb_timer_1	120	361.836 101.681 463.517
31	=====	gen_apb_uart_0.u_apb_uart_0	cmsdk_apb_uart	32	gen_apb_uart_1.u_apb_uart_1	cmsdk_mcu_system_cmsdk_apb_uart_1	481	1341.324 546.210 1887.534
33	=====	gen_apb_uart_2.u_apb_uart_2	cmsdk_mcu_system_cmsdk_apb_uart_2	34	gen_apb_watchdog.u_apb_watchdog	cmsdk_apb_watchdog	480	1340.982 545.469 1886.451
35	=====	u_apb_watchdog_frc	cmsdk_apb_watchdog_frc	36	u_ahb_to_apb	cmsdk_ahb_to_apb_ADDRWIDTH16_REGISTER_RDATA1_REGIS	469	1535.238 546.761 2081.999
37	=====	u_apb_slave_mux	cmsdk_apb_slave_mux_PORT0_ENABLE1_PORT1_ENABLE1_PO	38	u_cmsdk_mcu_stclkctrl	cmsdk_mcu_stclkctrl_DIV_RATIO18h003e8	342	1172.034 424.097 1596.131
39	=====	u_cmsdk_mcu_sysctrl	cmsdk_mcu_sysctrl_BE0	40	u_cortexm0integration	CORTEXM0INTEGRATION	140	504.108 94.060 598.168
41	=====	u_cortexm0	CORTEXM0DS	42	u_logic	cortexm0ds_logic	157	303.354 87.769 391.123
							30	93.708 31.626 125.334
							81	222.300 85.165 307.465
							7790	20730.330 10901.048 31631.378
							7790	20730.330 10901.048 31631.378
							7790	20730.330 10901.048 31631.378

디자인 전체의  
Area 확인

# Synthesis

genus

\$> vi 10\_cmsdk\_mcu\_SYN\_clock.rpt

- Clock에 대한 정보를 확인함

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

```
1 =====  
2 Generated by: Genus(TM) Synthesis Solution 22.16-s078_1  
3 Generated on: Feb 01 2025 11:36:11 pm  
4 Module: cmsdk_mcu  
5 Operating conditions: PVT_0P9V_125C  
6 Interconnect mode: global  
7 Area mode: physical library  
8 =====  
9  
10 11 Clock Description  
12 -----  
13  
14 15 Clock  
15 Name Period Rise Fall Clock Source No of  
16 Domain Pin/Port Registers  
17 MAIN_CLOCK 7000.0 0.0 3500.0 domain_1 XTAL1 2285  
18  
19 20 Clock Network Latency / Setup Uncertainty  
21  
22 23 Network Network Source Source Setup Setup  
23 Clock Latency Latency Latency Latency Uncertainty Uncertainty  
24 Name Rise Fall Rise Fall Rise Fall  
25  
26 MAIN_CLOCK 200.0 200.0 200.0 200.0 100.0 100.0  
27  
28 29 Clock Relationship (with uncertainty & latency)  
29 -----
```

# Synthesis

genus

\$> vi 11\_cmsdk\_mcu\_SYN\_datapath.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock_rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

- syn\_map → syn\_opt 진행 후 datapath 비교

```
1 Command: report datapath > ./report/11_cmsdk_mcu_SYN_datapath.rpt  
2 Warning: '-sort' is not specified. By default, 'report datapath' orders the components based on instance name  
3 =====  
4 Generated by: Genus(TM) Synthesis Solution 22.16-s078_1  
5 Generated on: Feb 01 2025 11:36:11 pm  
6 Module: cmsdk_mcu  
7 Operating conditions: PVT_0P9V_125C  
8 Interconnect mode: global  
9 Area mode: physical library  
10 =====  
11  
12  
13      Type          CellArea  Percentage  
14 -----  
15  datapath modules    0.00     0.00  
16  external muxes     0.00     0.00  
17  others             2139913.64 100.00  
18  
19  total              2139913.64 100.00  
20
```

Total의 숫자가 작을수록 critical path가 적고 area가 작아짐

# Synthesis

genus

\$> vi 12\_cmsdk\_mcu\_SYN\_design\_rulse.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

## DRC: Design Rule Check

- /Max 검색하여 DRC 관련 정보를 확인함
- Max capacitance, Max fanout, Max transition 확인

```
1 =====  
2 Generated by:          Genus(TM) Synthesis Solution 22.16-s078_1  
3 Generated on:          Feb 01 2025 11:36:11 pm  
4 Module:                cmsdk_mcu  
5 Operating conditions: PVT_0P9V_125C  
6 Interconnect mode:    global  
7 Area mode:             physical library  
8 =====  
9  
10 Max_transition design rule (violation total = 1034288)  
11 Pin                      Slew      Max      Violation  
12 -----  
13 u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/g207479/B  
         912        280       632  
14   --> Other violations on net  
           40422  
15 u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/g207480/B  
         912        280       632  
16   --> Other violations on net  
           40422  
17 u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/g207481/B  
         912        280       632  
18   --> Other violations on net  
           40422  
19 u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/g207482/B  
         912        280       632
```

# Synthesis

genus

\$> vi 13\_cmsdk\_mcu\_SYN\_gate.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

1	=====	2	Generated by:	Genus(TM) Synthesis Solution 22.16-s078_1
2		3	Generated on:	Feb 01 2025 11:36:12 pm
4		5	Module:	cmsdk_mcu
6		7	Operating conditions:	PVT_0P9V_125C
8		9	Interconnect mode:	global
10		11	Area mode:	physical library
11	Gate	Instances	Area	Library
12	-----			
13	ADDFX1	215	1102.950	fast_vdd1v0
14	ADDHX1	7	26.334	fast_vdd1v0
15	AND2X1	134	183.312	fast_vdd1v0
16	AND2XL	164	224.352	fast_vdd1v0
17	AND3XL	15	30.780	fast_vdd1v0
18	AND4X1	5	11.970	fast_vdd1v0
19	AND4XL	11	26.334	fast_vdd1v0
20	A021X1	3	7.182	fast_vdd1v0
21	A021XL	12	28.728	fast_vdd1v0
22	A022X1	1	2.736	fast_vdd1v0
23	A022XL	173	473.328	fast_vdd1v0
24	AOI211X1	2	4.788	fast_vdd1v0
25	AOI211XL	22	45.144	fast_vdd1v0
26	AOI21X1	84	143.640	fast_vdd1v0
27	AOI21XL	141	241.110	fast_vdd1v0
28	AOI221X1	386	924.084	fast_vdd1v0
29	AOI222X1	169	520.182	fast_vdd1v0

- 내 디자인에서 사용된 cell에 대한 정보를 확인함

# Synthesis

genus

\$> vi 14\_cmsdk\_mcu\_SYN\_hier.rpt

- 내 디자인의 계층 구조를 확인함

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt  
  
1 =====  
2 Generated by: Genus(TM) Synthesis Solution 22.16-s078_1  
3 Generated on: Feb 01 2025 11:36:13 pm  
4 Module: cmsdk_mcu  
5 Operating conditions: PVT_OP9V_125C  
6 Interconnect mode: global  
7 Area mode: physical library  
8 =====  
9  
10  
11 Hierarchy Report Format :  
12  
13 level instance ( module ) <status>  
14  
15 status : preserve_<value> -- indicating preserve hierarchy or inherited_preserve value  
16 : blackbox -- indicating unresolved instance  
17  
18 =====  
19  
20 0 cmsdk_mcu  
21 1 u_cmsdk_mcu_clkctrl ( cmsdk_mcu_clkctrl_CLKGATE_PRESENT0 )  
22 1 u_cmsdk_mcu_system ( cmsdk_mcu_system ) preserve_true  
23 2 u_addr_decode ( cmsdk_mcu_addr_decode_BASEADDR_GPIO032h40010000_BASEADDR_GPIO132h40011000_BOOT_LOADER_PRESENT1h0_BASEADDR_SYSROMTABLE32hf0000000 ) preserve_true
```

# Synthesis

genus

\$> vi 15\_cmsdk\_mcu\_SYN\_mem\_cell.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

- 메모리 관련 정보 확인 가능

```
1 =====  
2 # Generated by: Cadence Genus(TM) Synthesis Solution 22.16-s078_1  
3 # Generated on: Feb 1 2025 23:36:13  
4  
5 Library : fast_vdd1v0  
6 No memory cells found  
7  
8 Library : slow_vdd1v0  
9 No memory cells found  
10  
11 Library : giolib045  
12 No memory cells found
```

내 디자인에 메모리가  
없음을 확인함

# Synthesis

genus

\$> vi 16\_cmsdk\_mcu\_SYN\_message.rpt

```
[ex_poly1@npit SYN]$ cd report/  
[ex_poly1@npit report]$ ls  
00_check_design.rpt  
01_check_timing.rpt  
02_report_port.rpt  
03_report_datapath_generic.rpt  
04_report_datapath_map.rpt  
05_default_post_syn_map.rpt  
05_MAIN_CLOCK_post_syn_map.rpt  
06_report_constraint.rpt  
07_default_post_syn_opt.rpt  
07_MAIN_CLOCK_post_syn_opt.rpt  
08_cmsdk_mcu_SYN_analysis_view.rpt  
09_cmsdk_mcu_SYN_area.rpt  
10_cmsdk_mcu_SYN_clock.rpt  
11_cmsdk_mcu_SYN_datapath.rpt  
12_cmsdk_mcu_SYN_design_rules.rpt  
13_cmsdk_mcu_SYN_gate.rpt  
14_cmsdk_mcu_SYN_hier.rpt  
15_cmsdk_mcu_SYN_mem_cell.rpt  
16_cmsdk_mcu_SYN_message.rpt
```

```
17_cmsdk_mcu_SYN_net.rpt  
18_cmsdk_mcu_SYN_pwr.rpt  
19_cmsdk_mcu_SYN_qor.rpt  
20_cmsdk_mcu_SYN_timing.rpt  
final.rpt  
syn_generic_cmsdk_mcu.db  
syn_generic_qor.rpt  
syn_generic_time.rpt  
syn_map_area.rpt  
syn_map_cmsdk_mcu.db  
syn_map_gates.rpt  
syn_map_qor.rpt  
syn_map_time.rpt  
syn_opt_area.rpt  
syn_opt_cmsdk_mcu.db  
syn_opt_gates.rpt  
syn_opt_qor.rpt  
syn_opt_time.rpt
```

- 합성과정에서 나온 정보를 메시지로 확인할 수 있음

한 개의 사용하지 않는 register를 삭제한다는 메시지

```
1 ======  
2 Message S  
3 ======  
4 -----  
5 |0 ...| Sev  
6 -----  
7 |CDFG-508|Warning| 1|Removing unused register.  
8 ||||| Genus removes the flip flop or  
9 ||||| latch inferred for an unused  
10 ||||| signal or variable. To preserve  
11 ||||| the flip-flop or latch, set the  
12 ||||| hdl_preserve_unused_registers  
13 ||||| attribute to true or use a  
14 ||||| pragma in the RTL.  
15 |CDFG-818|Warning| 1|Using default parameter value  
16 ||||| for module elaboration.  
17 |CFM-1|Info | 1|Wrote dofile.  
18 |CFM-5|Info | 1|Wrote formal verification  
19 ||||| information.  
20 |DPOPT-5|Info | 1|Skipping datapath optimization.  
21 |DPOPT-6|Info | 1|Pre-processed datapath logic.  
22 |ELAB-1|Info | 1|Elaborating Design.  
23 |ELAB-3|Info | 1|Done Elaborating Design.  
24 |ELABUTL-123|Warning| 20|Undriven module output port.  
25 |ELABUTL-127|Warning| 20|Undriven module input port.  
26 ||||| Run check_design to check  
27 ||||| 'Undriven Port(s)/Pin(s)  
28 ||||| ' section for all undriven  
29 ||||| module input ports. It is
```

# Synthesis

genus

\$> vi 17\_cmsdk\_mcu\_SYN\_net.rpt

- Wire에 대한 정보를 담고 있음

```
17_cmsdk_mcu_SYN_net.rpt
18_cmsdk_mcu_SYN_pwr.rpt
19_cmsdk_mcu_SYN_qor.rpt
20_cmsdk_mcu_SYN_timing.rpt
final.rpt
syn_generic_cmsdk_mcu.db
syn_generic_qor.rpt
syn_generic_time.rpt
syn_map_area.rpt
syn_map_cmsdk_mcu.db
syn_map_gates.rpt
syn_map_qor.rpt
syn_map_time.rpt
syn_opt_area.rpt
syn_opt_cmsdk_mcu.db
syn_opt_gates.rpt
syn_opt_qor.rpt
syn_opt_time.rpt
```

Net	Loads	Drivers	Wire Cap(fF)	Wire Res(k-ohm)	Wireload Model
APBACTIVE	0	1	0.0	0.000	
FCLK	8	1	0.0	0.000	
LOCKUP	2	1	5.5	0.024	
LOCKUPRESET	2	1	4.8	0.021	
PMUENABLE	0	1	0.0	0.000	
PORESETn	1	1	0.0	0.000	
PRESETn	1	1	0.0	0.000	
SLEEPING	0	1	0.0	0.000	
SYSRESETREQ	1	1	3.2	0.014	
WDGRESETREQ	1	1	2.4	0.010	
cmsdk_SYSRESETREQ	1	1	1.6	0.007	
i_swclkck	0	1	0.0	0.000	
i_swditms	0	1	0.0	0.000	
i_tdi	0	1	0.0	0.000	
i_trst_n	0	1	0.0	0.000	
in_NRST	1	1	0.0	0.000	
in_flash_hrdata[0]	1	1	1.6	0.007	
in_flash_hrdata[1]	1	1	1.6	0.007	
in_flash_hrdata[2]	1	1	1.6	0.007	
in_flash_hrdata[3]	1	1	1.6	0.007	

# Synthesis

genus

\$> vi 18\_cmsdk\_mcu\_SYN\_pwr.rpt

- Power 소모 관련 정보를 담고 있음

```
17_cmsdk_mcu_SYN_net.rpt
18_cmsdk_mcu_SYN_pwr.rpt
19_cmsdk_mcu_SYN_qor.rpt
20_cmsdk_mcu_SYN_timing.rpt
final.rpt
syn_generic_cmsdk_mcu.db
syn_generic_qor.rpt
syn_generic_time.rpt
syn_map_area.rpt
syn_map_cmsdk_mcu.db
syn_map_gates.rpt
syn_map_qor.rpt
syn_map_time.rpt
syn_opt_area.rpt
syn_opt_cmsdk_mcu.db
syn_opt_gates.rpt
syn_opt_qor.rpt
syn_opt_time.rpt
```

Category	Leakage	Internal	Switching	Total	Row%
	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
memory	9.44624e-07	1.52379e-03	3.23107e-04	1.84784e-03	1.82%
register	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
latch	1.23094e-06	4.65504e-04	1.02382e-03	1.49055e-03	1.47%
logic	4.37853e-10	7.33379e-07	3.20881e-04	3.21615e-04	0.32%
bbox	5.81506e-03	8.98785e-02	2.26011e-03	9.79537e-02	96.40%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	5.81724e-03	9.18686e-02	3.92791e-03	1.01614e-01	100.01%
Subtotal	5.72%	90.41%	3.87%	100.00%	100.00%
Percentage					

# Synthesis

genus

\$> vi 19\_cmsdk\_mcu\_SYN\_qor.rpt

```
17_cmsdk_mcu_SYN_net.rpt
18_cmsdk_mcu_SYN_pwr.rpt
19_cmsdk_mcu_SYN_qor.rpt
20_cmsdk_mcu_SYN_timing.rpt
final.rpt
syn_generic_cmsdk_mcu.db
syn_generic_qor.rpt
syn_generic_time.rpt
syn_map_area.rpt
syn_map_cmsdk_mcu.db
syn_map_gates.rpt
syn_map_qor.rpt
syn_map_time.rpt
syn_opt_area.rpt
syn_opt_cmsdk_mcu.db
syn_opt_gates.rpt
syn_opt_qor.rpt
syn_opt_time.rpt
```

qor: quality of results

- 전체적인 통계를 확인할 수 있음

```
1 =====
2 Generated by:           Genus(TM) Synthesis Solution 22.16-s078_1
3 Generated on:          Feb 01 2025 11:36:16 pm
4 Module:                cmsdk_mcu
5 Operating conditions: PVT_0P9V_125C
6 Interconnect mode:    global
7 Area mode:             physical library
8 =====
9
10 Timing
11 -----
12
13   Clock   Period
14 -----
15 MAIN_CLOCK 7000.0
16
17
18   Cost      Critical      Violating
19   Group     Path Slack   TNS    Paths
20 -----
21 default      No paths   0.0
22 MAIN_CLOCK   1644.7    0.0      0
23 -----
24 Total         0.0        0
25
26 Instance Count
27 -----
28 Leaf Instance Count           13777
29 Physical Instance count       0
30 Sequential Instance Count     2285
31 Combinational Instance Count 11492
32 Hierarchical Instance Count   32
33
34 Area
```

# Synthesis

genus

\$> vi 20\_cmsdk\_mcu\_SYN\_timing.rpt

```
17_cmsdk_mcu_SYN_net.rpt
18_cmsdk_mcu_SYN_pwr.rpt
19_cmsdk_mcu_SYN_qor.rpt
20_cmsdk_mcu_SYN_timing.rpt
final.rpt
syn_generic_cmsdk_mcu.db
syn_generic_qor.rpt
syn_generic_time.rpt
syn_map_area.rpt
syn_map_cmsdk_mcu.db
syn_map_gates.rpt
syn_map_qor.rpt
syn_map_time.rpt
syn_opt_area.rpt
syn_opt_cmsdk_mcu.db
syn_opt_gates.rpt
syn_opt_qor.rpt
syn_opt_time.rpt
```

```
1 =====
2 Generated by:      Genus(TM) Synthesis Solution 22.16-s078_1
3 Generated on:      Feb 01 2025 11:36:17 pm
4 Module:           cmsdk_mcu
5 Operating conditions: PVT_0P9V_125C
6 Interconnect mode: global
7 Area mode:        physical library
8 =====
9
10
11 Path 1: MET (1645 ps) Setup Check with Pin u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/0o3l85_reg/CKN->D
12     Group: MAIN_CLOCK
13     Startpoint: (R) u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/Xc8l85_reg/CK
14     Clock: (R) MAIN_CLOCK
15     Endpoint: (F) u_cmsdk_mcu_system/u_cortexm0integration/u_cortexm0/u_logic/0o3l85_reg/D
16     Clock: (R) MAIN_CLOCK
17
18     Capture          Launch
19     Clock Edge:+    7000          0
20     Src Latency:+   200           200
21     Net Latency:+  200 (I)      200 (I)
22     Arrival:=       7400          400
23
24     Setup:-         31
25     Uncertainty:-  100
26     Required Time:= 7269
27     Launch Clock:- 400
28     Data Path:-    5225
29     Slack:=        1645
30
31 #
32 #               Timing Point
33 #                                     Flags Arc Edge Cell Fanout Load Trans Delay Arrival Instance
34 #                                         (fF) (ps) (ps) (ps) Location
35 u_cmsdk_mcu_system/u_cortexm0/u_logic/Xc8l85_reg/CK - - R (arrival) 1445 - 100 0 400 (-,-)
36 u_cmsdk_mcu_system/u_cortexm0/integration/u_cortexm0/u_logic/Xc8l85_reg/Q (P) CK->Q R DFFRX1 37 45.0 306 242 642 (-,-)
37 u_cmsdk_mcu_system/u_cortexm0/integration/u_cortexm0/u_logic/Xc8l85 - - - (net) - - - - - (-,-)
38 u_cmsdk_mcu_system/u_cortexm0/integration/u_cortexm0/u_logic/g215877/Y (P) A->Y R OR2X1 19 22.5 155 152 794 (-,-)
39 u_cmsdk_mcu_system/u_cortexm0/integration/u_cortexm0/u_logic/n_5666 - - - (net) - - - - - (-,-)
40 u_cmsdk_mcu_system/u_cortexm0/integration/u_cortexm0/u_logic/g207746/Y (P) C->Y R OR3XL 2 3.0 38 52 847 (-,-)
41 u_cmsdk_mcu_system/u_cortexm0/integration/u_cortexm0/u_logic/n_5665 - - - (net) - - - - - (-,-)
42 u_cmsdk_mcu_system/u_cortexm0/integration/u_cortexm0/u_logic/g207696/Y (P) B->Y R OR2XL 5 6.5 77 57 904 (-,-)
```

Slack에 문제 없음

# Synthesis

genus

\$> cd log

- log 폴더에 툴의 시작부터 종료까지의 메시지가 모두 저장되어 있음

```
[ex_poly1@npit SYN]$ ls  
clean.tcl  cons  fv  log  mapped  report  run_synthesis  script  unmapped
```

# Synthesis

## genus

```
$> vi all.log
```

- all.log 파일은 툴의 시작부터 종료까지의 메시지가 모두 저장되어 있는 파일

```
[ex_poly1@npit log]$ ls  
all.cmd all.log
```

# Synthesis

genus

\$> vi all.log

```
Cadence Genus(TM) Synthesis Solution.  
Copyright 2024 Cadence Design Systems, Inc. All rights reserved worldwide.  
Cadence and the Cadence logo are registered trademarks and Genus is a trademark  
of Cadence Design Systems, Inc. in the United States and other countries.  
  
[00:12:47.440177] Configured Lic search path (22.01-s003): 35266@npit-service1.ptime.org  
  
Version: 22.16-s078_1, built Sun Jun 09 22:32:57 PDT 2024  
Options: -files ./script/cortexm0_45nm.tcl -log ./log/all.log  
Date: Mon Feb 03 00:12:47 2025  
Host: npit.ic.rnd1 (x86_64 w/Linux 3.10.0-1160.119.1.el7.x86_64) (20cores*80cpus*  
2physical cpus*Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz 30720KB) (395262912KB)  
PID: 33843  
OS Linux Server release 7.9 (Maipo)  
Che 2937줄이 생성된 것을 알 수 있음 Genus_Synthesis  
[00:12:47.028131] Lic Lic check successful  
[00:12:47.028131] Feature usage summary:  
"all.log" 2937L, 199957C
```

# Synthesis

genus

- **/Error** 명령어를 통해 툴 사용 전반의 에러유무를 확인함
- 이전 report에서 확인했던 사항들을 다시 확인할 수 있음

\$> vi all.log

```
Info    : PWRA-0002 Finished power computation.
Info    : PWRA-0007 [PwrInfo] Completed successfully.
          : Info=6, Warn=2, Error=0, Fatal=0
Finished exporting design database to file './report/syn_map_cmsdk_mcu.db' for 'cmsdk_mcu' (command execution time mm:ss cpu = 00:01, real = 00:02).
Finished generating snapshot at stage syn_map (command execution time mm:ss cpu = 00:00, real = 00:04).
%# End write_snapshot (02/03 00:13:51, total cpu=17:00:00, real=17:00:04, peak res=962.80M, current mem=1837.57M)
@file(cortexm0_45nm.tcl) 132: write_db -to_file ${MAPPED_DIR}/syn_map.db
Finished exporting design database to file './mapped/syn_map.db' for 'cmsdk_mcu' (command execution time mm:ss cpu = 00:01, real = 00:01).
@file(cortexm0_45nm.tcl) 138: syn_opt ; #This command can't write report by using the mark '>'
Current PLE settings:

Aspect ratio      : 1.000
Shrink factor     : 1.000
Scale of res/length : 1.000
search hit BOTTOM, continuing at TOP
```

검색 결과를 전부  
확인했다는 뜻임

# Synthesis

## genus

- mapped 폴더에서 합성 최종 결과 파일들을 확인할 수 있음

```
$> cd mapped
```

```
[ex_poly1@npit SYN]$ ls  
clean.tcl  cons  fv  log  mapped  report  run_synthesis  script  unmapped
```

# Synthesis

genus

\$> //

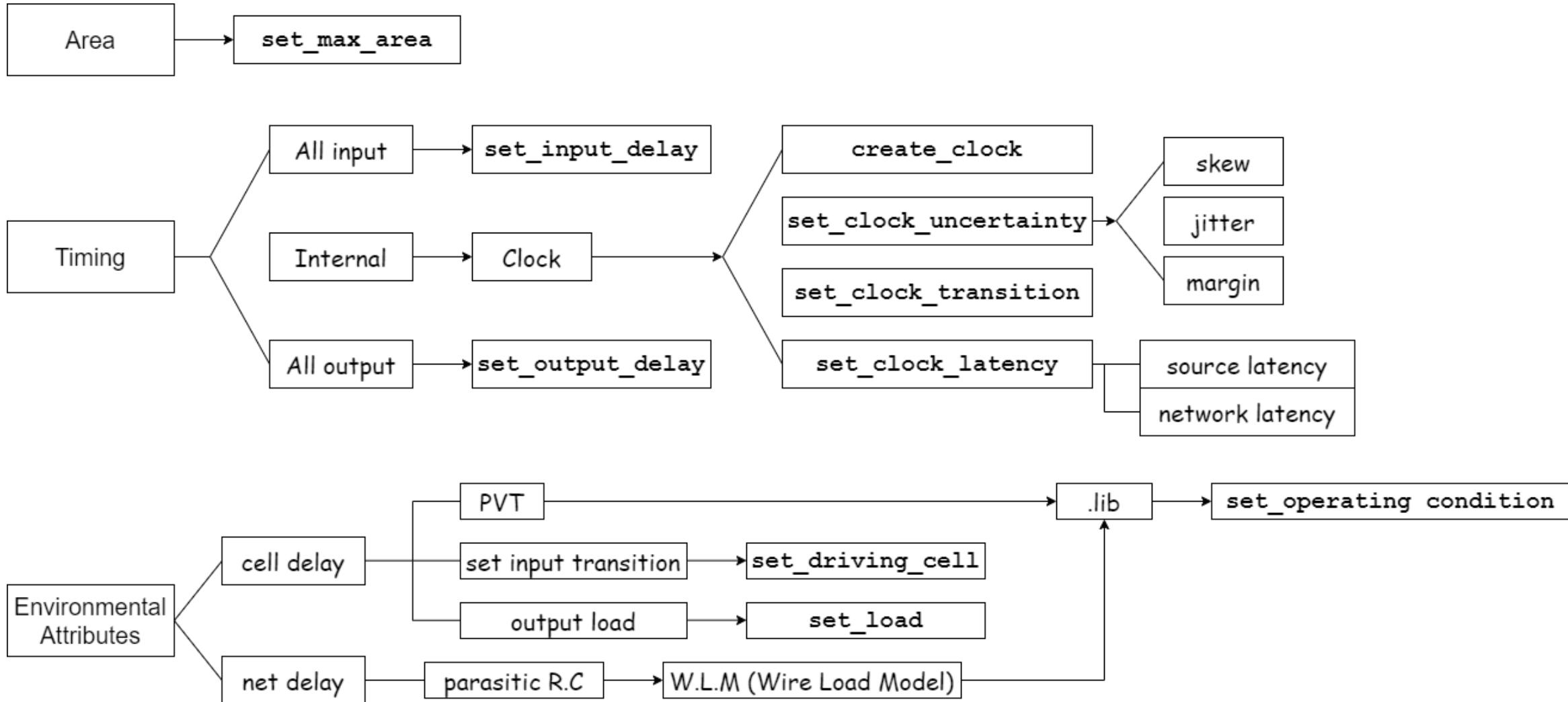
- mapped 내용 확인
- 합성 후 마지막에 write out했던 파일을 확인할 수 있음
- mapped의 파일들을 다음 단계 툴에서 입력으로 사용함

```
182 #####
183 ## write Innovus file set (verilog, SDC, config, etc.)
184 #####
185
186 #source -echo ./script/report_syn.tcl
187 write design -basename ${MAPPED_DIR}/${TOP DESIGN} mapped
188 write_hdl > ${MAPPED_DIR}/${TOP DESIGN}_syn_final.v
189 write_sdc > ${MAPPED_DIR}/${TOP DESIGN}_syn_final.sdc
190 write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge
    -setuphold split > ${MAPPED_DIR}/${TOP DESIGN}_delays.sdf
```

```
[ex_poly1@npit mapped]$ ll
total 12468
-rw-r--r-- 1 ex_poly1 rnd 6276538 Feb 3 15:42 cmsdk_mcu_delays.sdf
-rw-r--r-- 1 ex_poly1 rnd 54926 Feb 3 15:42 cmsdk_mcu_mapped.default_emulate_constraint_mode.sdc
-rw-r--r-- 1 ex_poly1 rnd 3949 Feb 3 15:42 cmsdk_mcu_mapped.dont_touch.sdc
-rw-r--r-- 1 ex_poly1 rnd 2102131 Feb 3 15:42 cmsdk_mcu_mapped.g
-rw-r--r-- 1 ex_poly1 rnd 783 Feb 3 15:42 cmsdk_mcu_mapped.genus_init.tcl
-rw-r--r-- 1 ex_poly1 rnd 4414 Feb 3 15:42 cmsdk_mcu_mapped.genus_setup.tcl
-rw-r--r-- 1 ex_poly1 rnd 27106 Feb 3 15:42 cmsdk_mcu_mapped.lec.taf.gz
-rw-r--r-- 1 ex_poly1 rnd 56638 Feb 3 15:42 cmsdk_mcu_mapped.metrics.json
-rw-r--r-- 1 ex_poly1 rnd 2399 Feb 3 15:42 cmsdk_mcu_mapped.mmmc.tcl
-rw-r--r-- 1 ex_poly1 rnd 5379 Feb 3 15:42 cmsdk_mcu_mapped.preserve.tcl
-rw-r--r-- 1 ex_poly1 rnd 11002 Feb 3 15:42 cmsdk_mcu_mapped.root.g
-rw-r--r-- 1 ex_poly1 rnd 20 Feb 3 15:42 cmsdk_mcu_mapped.safety.taf.gz
-rw-r--r-- 1 ex_poly1 rnd 1475673 Feb 3 15:42 cmsdk_mcu_mapped.v
-rw-r--r-- 1 ex_poly1 rnd 54926 Feb 3 15:42 cmsdk_mcu_syn_final.sdc
-rw-r--r-- 1 ex_poly1 rnd 1475673 Feb 3 15:42 cmsdk_mcu_syn_final.v
-rw-r--r-- 1 ex_poly1 rnd 586856 Feb 3 15:42 syn_map.ab
-rw-r--r-- 1 ex_poly1 rnd 588392 Feb 3 15:42 syn_opt.db
```

# Synthesis(정리 및 요약)

## Constraint



# Synthesis(정리 및 요약)

## 합성 검증 4단계

1. **check\_timing –intent**
2. **report\_port**
3. **report\_constraint**
4. **report\_timing**

합성 후 반드시 확인해야 할 결과임

①

Total: 0

②

External Driver/Slew							
Port	Dir	External Driver Max-Rise	External Driver Max-Fall	External Slew Max-Rise	External Slew Max-Fall	Timing Case Value	Timing Ideal Driver
XTAL1	in			0.0	0.0		false
NRST	in	PADDI/Y	PADDI/Y	0.0	0.0		false
nTRST	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false
SWCLKTCK	in	PADDI/Y	PADDI/Y	3317.1	1443.3		false

# Synthesis(정리 및 요약)

## 합성 검증 4단계

1. check\_timing\_intent
2. report\_port
3. report\_constraint
4. report\_timing

③

Checking for violation type : Setup Timing Slack	←																				
No timing slack violation found.	←																				
Checking for violation type : clock_period	←																				
No paths found.	←																				
Checking for violation type : pulse_width	←																				
No paths found.	←																				
Checking for violation type : max_transition	←																				
<table border="1"><thead><tr><th>Pin</th><th>Required Slew (ps)</th><th>Actual Slew (ps)</th><th>Slack (ps)</th><th>Mode</th></tr></thead><tbody><tr><td>pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subs_ystem/gen_apb_watchdog.u_apb_watchdog/u_ap_b_watchdog_frc/g4850/B1</td><td>280</td><td>915</td><td>-635</td><td>default</td></tr><tr><td>pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subs_ystem/gen_apb_watchdog.u_apb_watchdog/u_ap_b_watchdog_frc/g4850/B1</td><td>280</td><td>915</td><td>-635</td><td>default</td></tr></tbody></table>	Pin	Required Slew (ps)	Actual Slew (ps)	Slack (ps)	Mode	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subs_ystem/gen_apb_watchdog.u_apb_watchdog/u_ap_b_watchdog_frc/g4850/B1	280	915	-635	default	pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subs_ystem/gen_apb_watchdog.u_apb_watchdog/u_ap_b_watchdog_frc/g4850/B1	280	915	-635	default	←					
Pin	Required Slew (ps)	Actual Slew (ps)	Slack (ps)	Mode																	
pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subs_ystem/gen_apb_watchdog.u_apb_watchdog/u_ap_b_watchdog_frc/g4850/B1	280	915	-635	default																	
pin:cmsdk_mcu/u_cmsdk_mcu_system/u_apb_subs_ystem/gen_apb_watchdog.u_apb_watchdog/u_ap_b_watchdog_frc/g4850/B1	280	915	-635	default																	
Checking for violation type : max_capacitance	←																				
<table border="1"><thead><tr><th>Pin</th><th>Required Load (ff)</th><th>Actual Load (ff)</th><th>Slack Load (ff)</th><th>Mode</th></tr></thead><tbody><tr><td>port:cmsdk_mcu/P1[0]</td><td>888.30</td><td>2388.40</td><td>-1500.10</td><td>default</td></tr><tr><td>port:cmsdk_mcu/P1[1]</td><td>888.30</td><td>2388.40</td><td>-1500.10</td><td>default</td></tr><tr><td>port:cmsdk_mcu/P1[2]</td><td>888.30</td><td>2388.40</td><td>-1500.10</td><td>default</td></tr></tbody></table>	Pin	Required Load (ff)	Actual Load (ff)	Slack Load (ff)	Mode	port:cmsdk_mcu/P1[0]	888.30	2388.40	-1500.10	default	port:cmsdk_mcu/P1[1]	888.30	2388.40	-1500.10	default	port:cmsdk_mcu/P1[2]	888.30	2388.40	-1500.10	default	←
Pin	Required Load (ff)	Actual Load (ff)	Slack Load (ff)	Mode																	
port:cmsdk_mcu/P1[0]	888.30	2388.40	-1500.10	default																	
port:cmsdk_mcu/P1[1]	888.30	2388.40	-1500.10	default																	
port:cmsdk_mcu/P1[2]	888.30	2388.40	-1500.10	default																	
No max_fanout rule violations.	←																				

합성 후 반드시 확인해야 할 결과임

# Synthesis(정리 및 요약)

## 합성 검증 4단계

1. **check\_timing –intent**
2. **report\_port**
3. **report\_constraint**
4. **report\_timing**

④

Setup:-	31
Uncertainty:-	100
Required Time:=	7269
Launch Clock:-	400
Data Path:-	5225
<b>Slack:=</b>	<b>1645</b>

합성 후 반드시 확인해야 할 결과임