

Auto PnR

Auto PnR

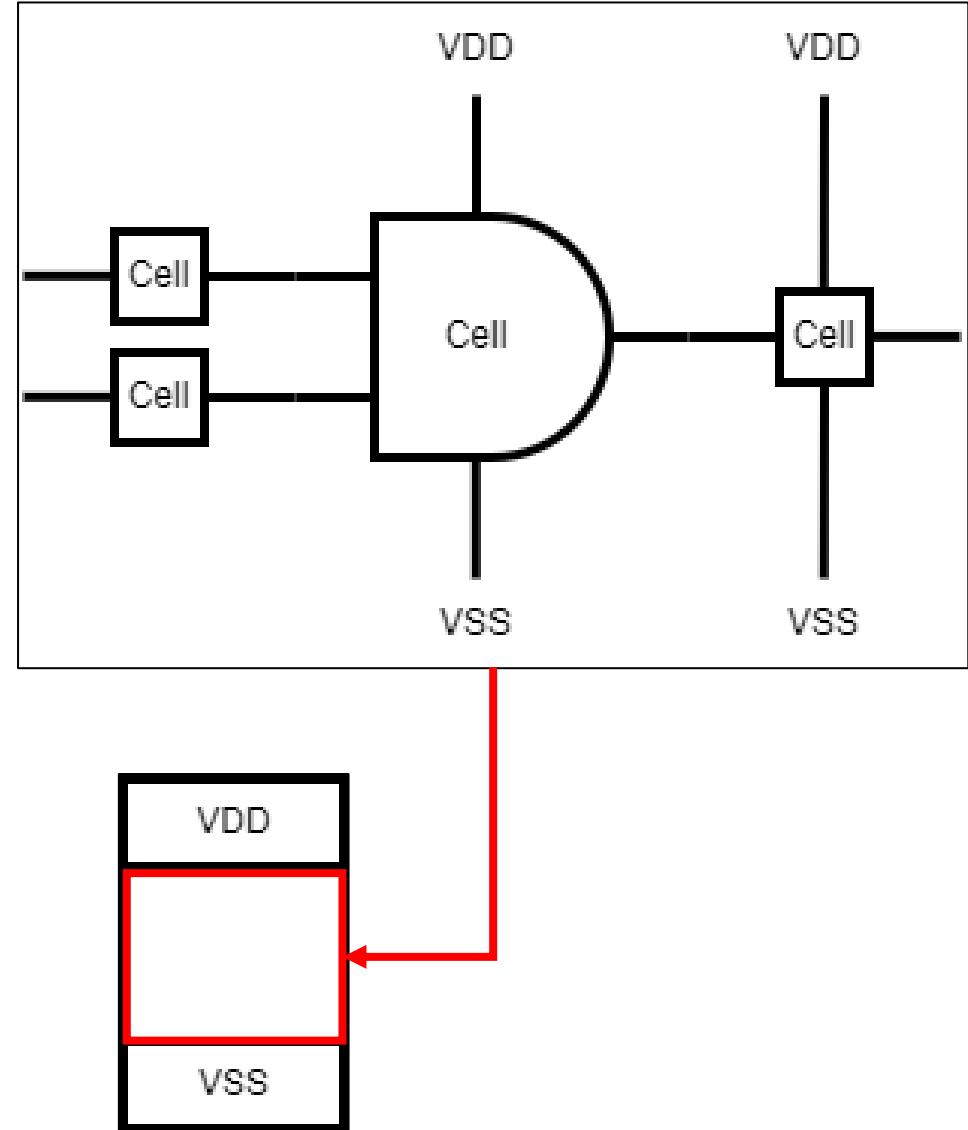
PnR 순서

1. **Floor plan:** 땅 펼치기, Io(FE 앞 부분에서 미리 설계를 해놓고 RTL소스를 작성), macro place
2. **Power plan:** power 구성(tech file에서 공정사의 룰 확인), IR드랍에 주의
3. **Place:** STD셀 자동위치(setup time, hold time을 고려함)
4. **CTS(Clock Tree Synthesis):** 클럭이 트리모양으로 보내지며 클럭 버퍼가 생성되므로 uncertainty, transition, latency값이 확실해짐
5. **Routing:** 툴이 자동으로 배선을 해주며 setup time violation, hold time violation을 툴이 알아서 잡아 줌
6. **DRC, Check connectivity :** Design Rule Check와 Check connectivity 진행(오류 발생시 툴이 자동으로 수정)

Auto PnR

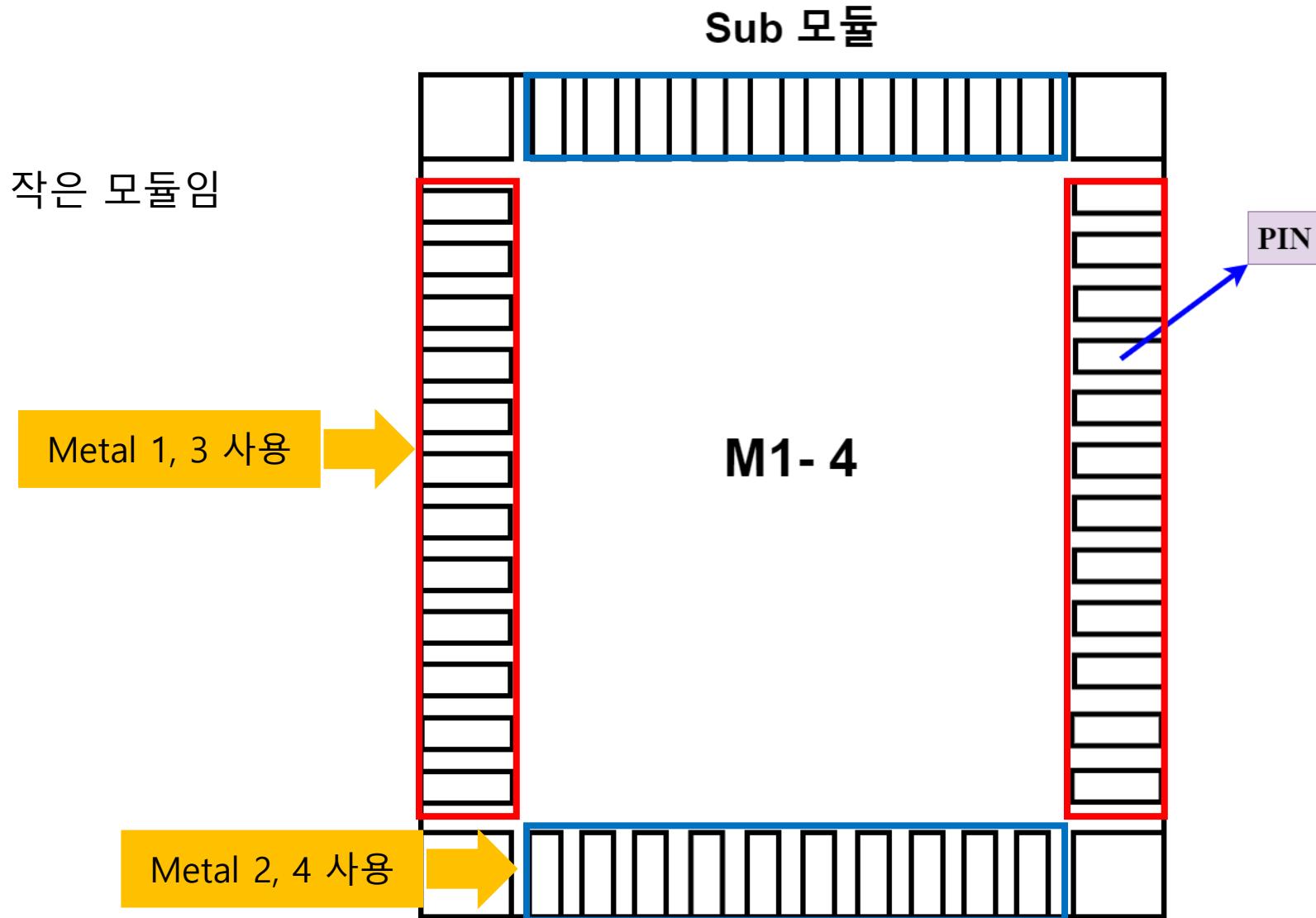
STD 셀

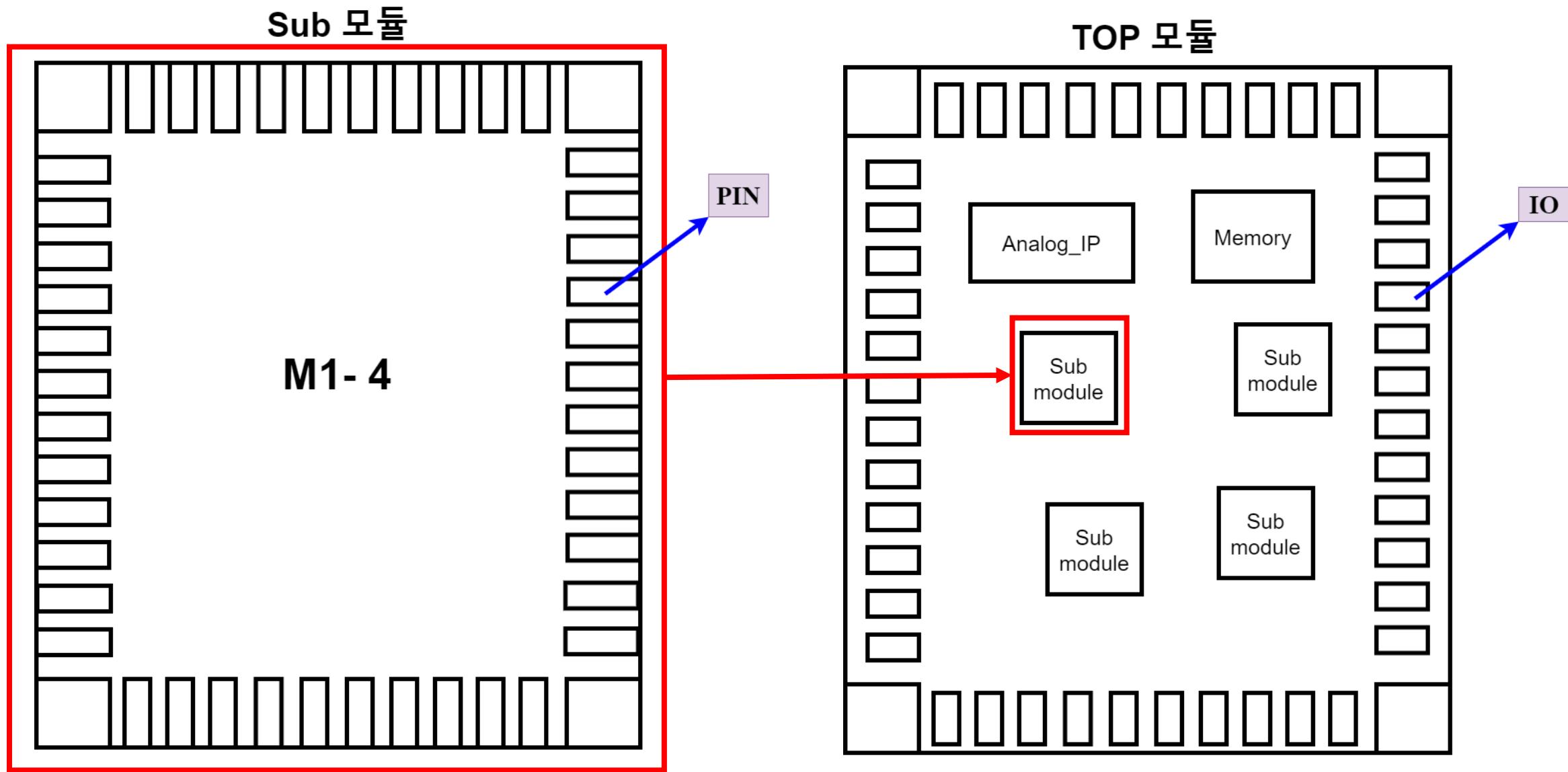
- 스탠다드 셀의 전원을 공통 단자로 연결하기 위해 아래의 그림과 같이 팬텀 셀을 사용함



모듈에 대한 설명

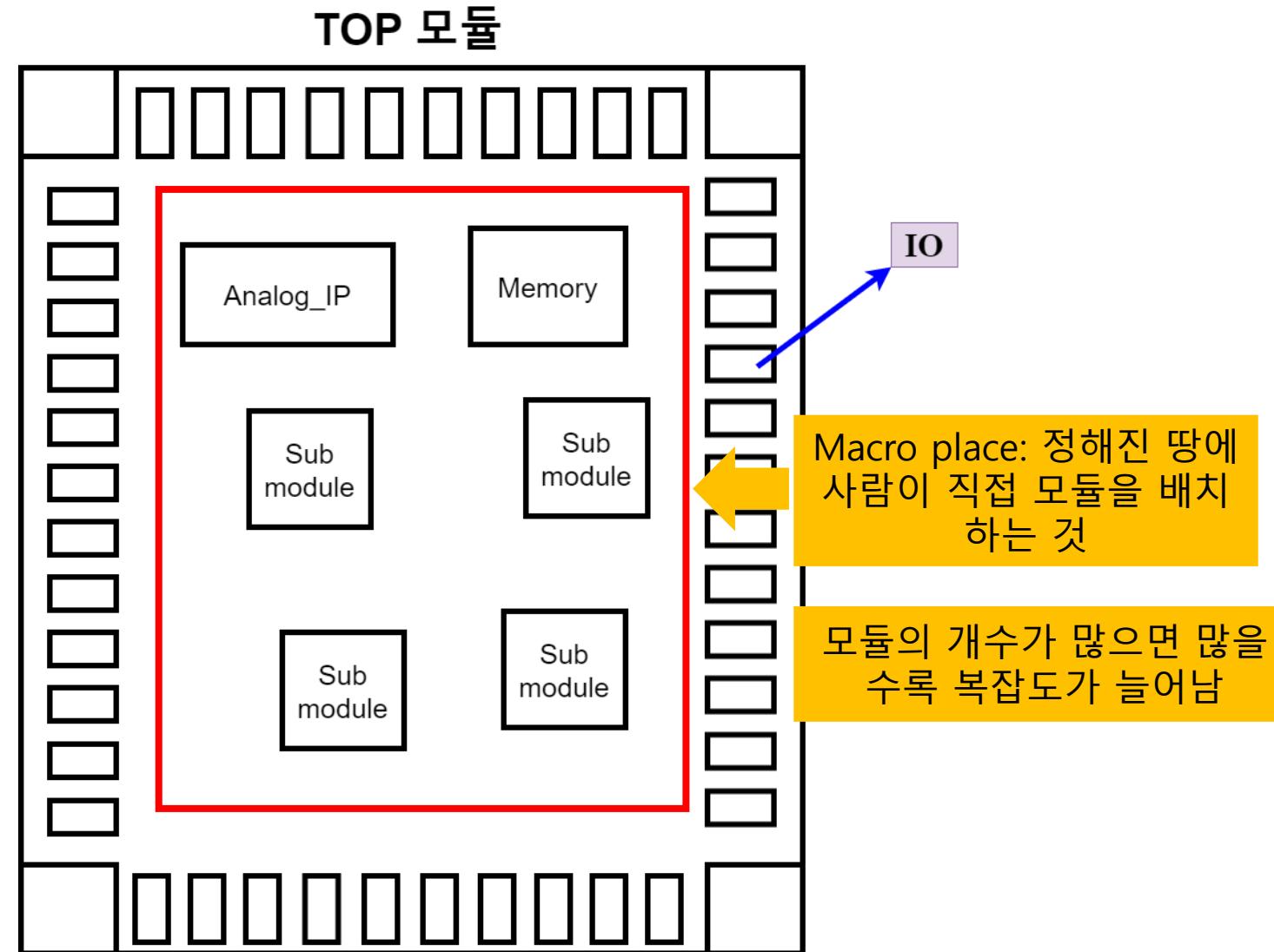
- Sub 모듈은 TOP 디자인에 들어가는 작은 모듈임
- IO셀이 아닌 PIN을 사용함



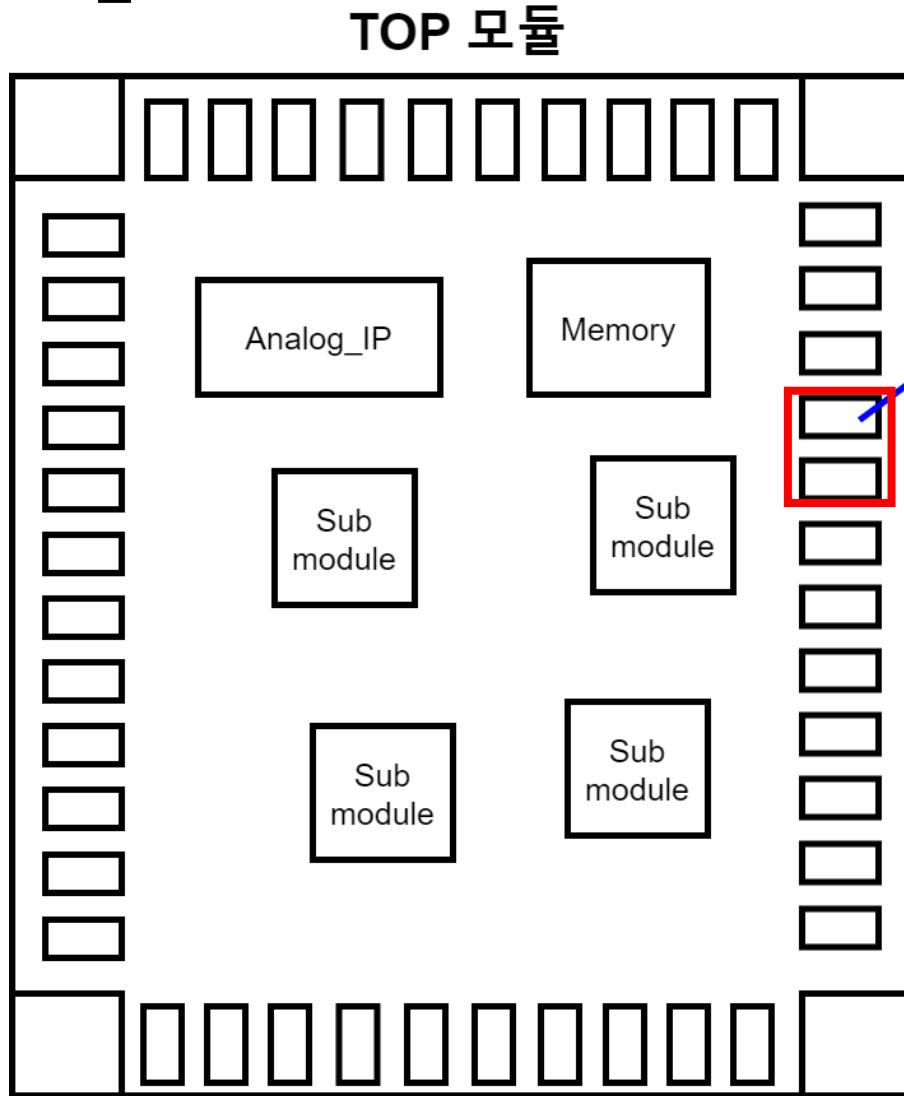


모듈에 대한 설명

- 많은 sub 모듈과 아날로그 IP, 메모리 등이 배치 되어있음
- IO셀을 사용함

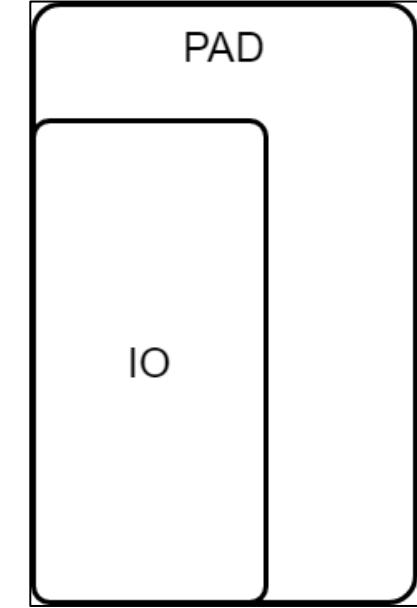
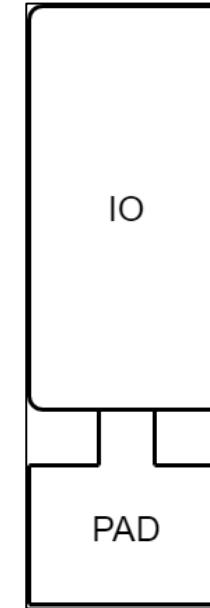


IO 셀



ESD: ElectroStatic
Discharge
정전기 방전 회로

PAD의 종류



In-line

Cup – circuit
under pad

IO 셀

- **Io cell의 종류**

- Signal Io: 입력 셀(PADDI), 출력 셀(PADDO), 양방향 셀(PADDB), ESD 기능
- Power Io: VDD, VSS, VDDIOR, VSSIOR, ESD 기능, AVDD, AVSS, AIOVDD, AIOVSS

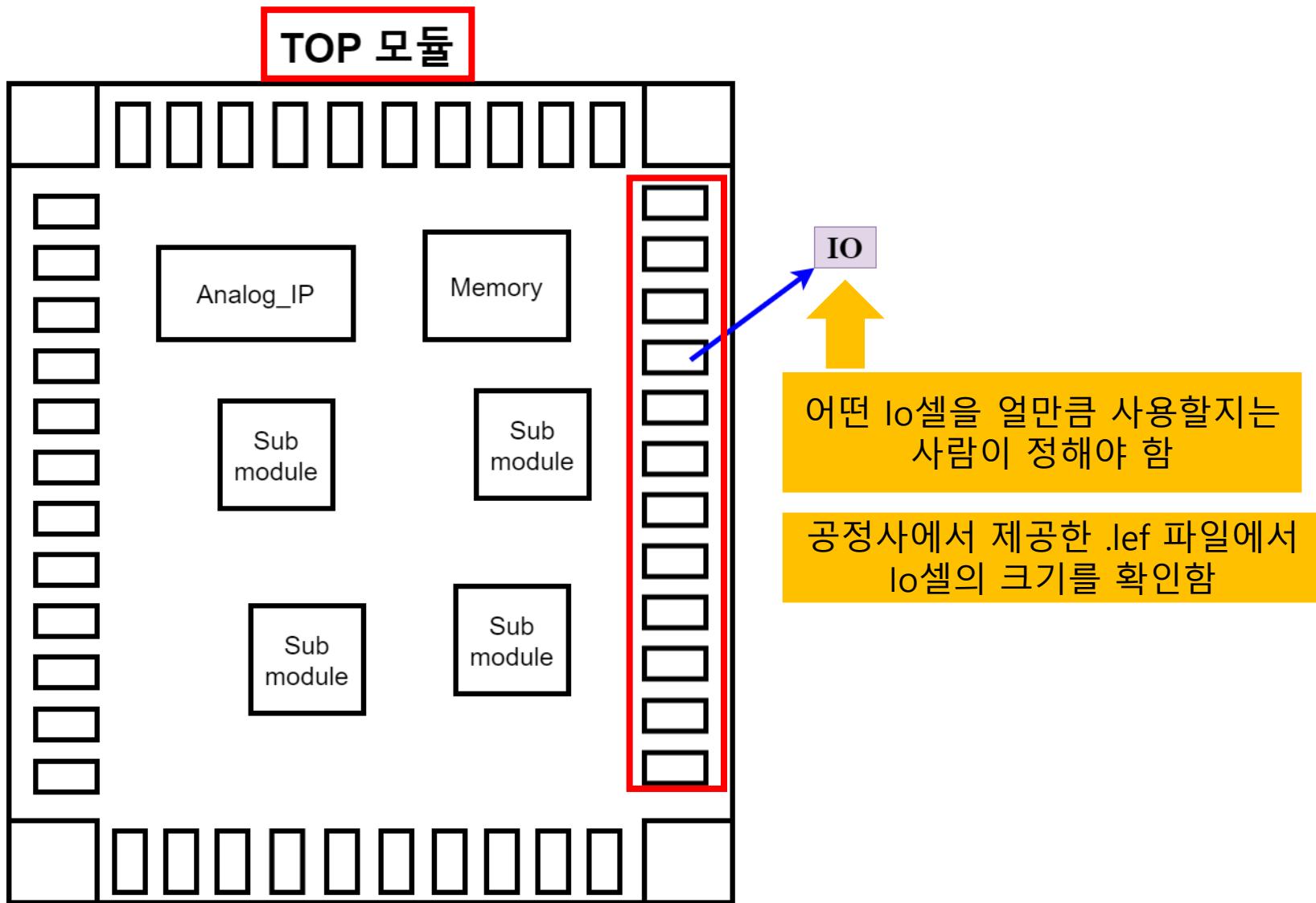
아날로그 Io셀을 위한 전원

STD셀을 위한 전원

Io셀을 위한 전원

아날로그 STD셀을 위한 전원

IO 셀

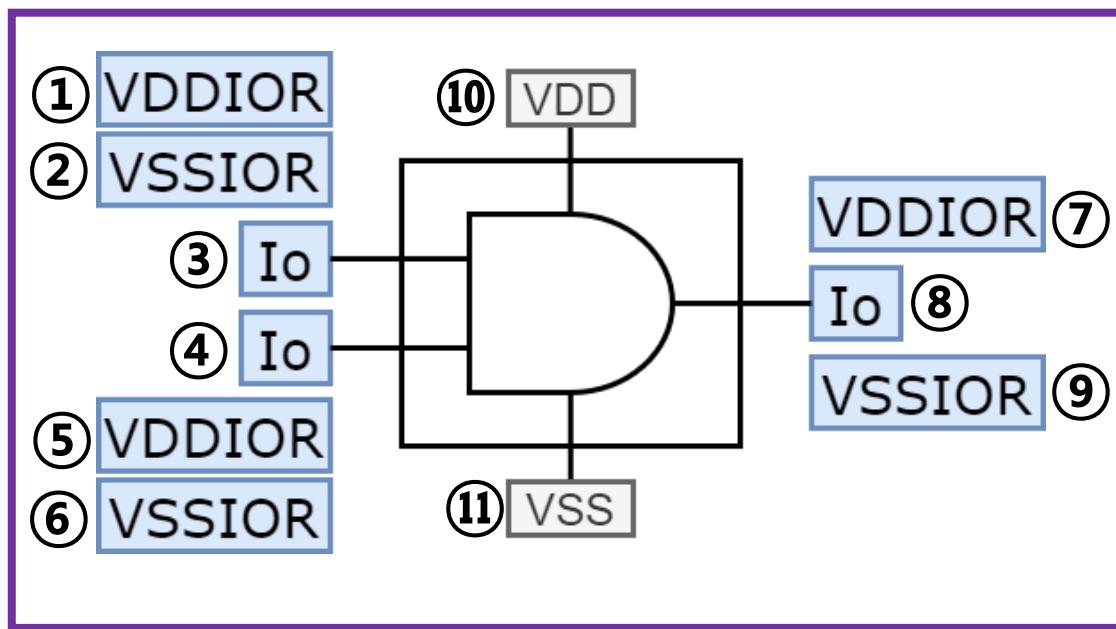


Floor plan란?

- 내가 디자인한 TOP 모듈의 Io셀, sub모듈, 메모리 등의 배치(place)를 사람이 직접 진행하는 것

Floor plan

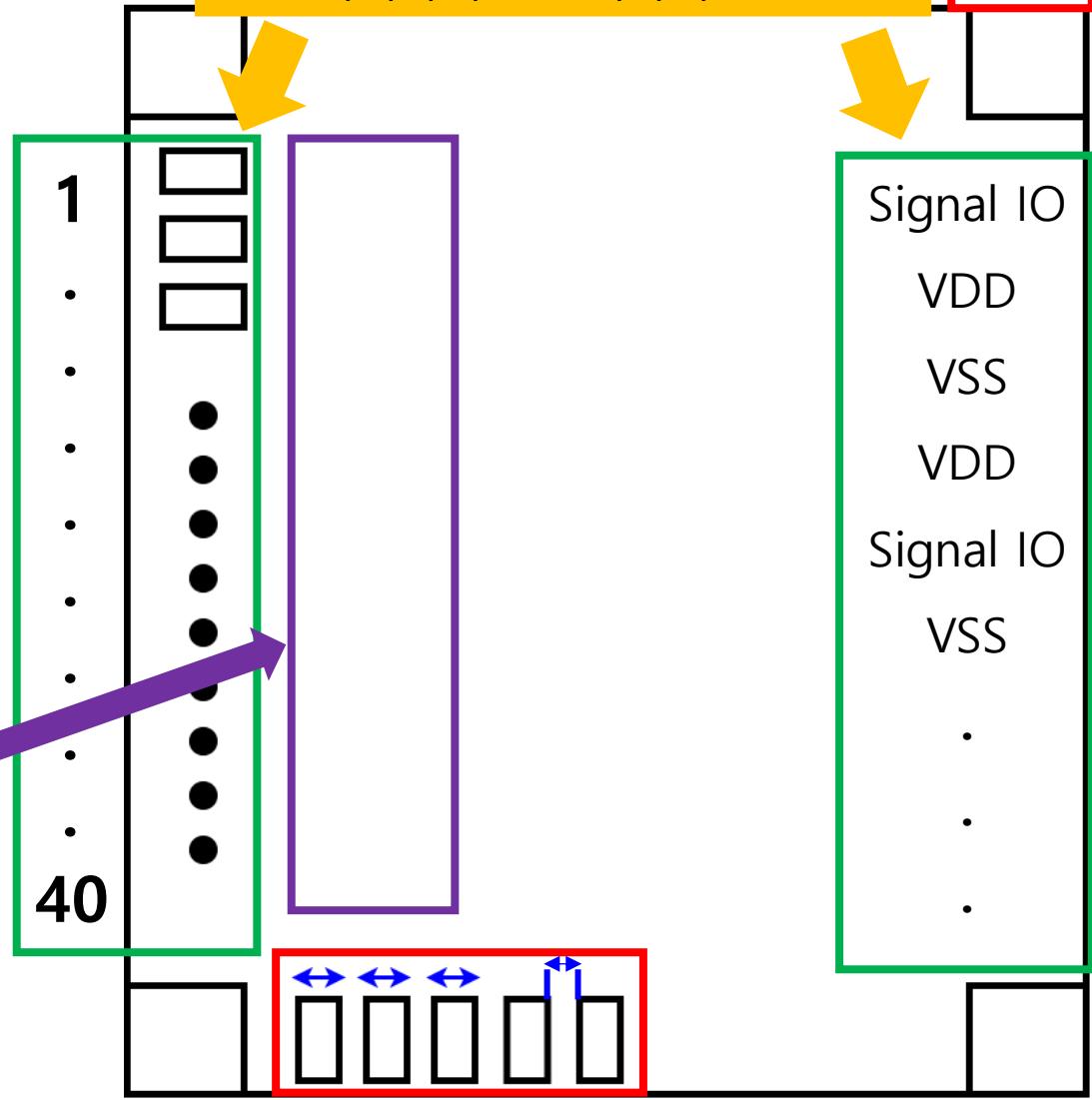
좌측 변에 1에서 40까지의 Io셀이 들어간다고 가정하면 보라색 상자에 있는 모듈은 TOP모듈의 좌측에 위치하는 것이 배선 측면에서 유리함



한 줄에 몇 개의 Io셀을 넣을 것인지
어떤 Io셀을 넣을 것인지 설계자가
여러가지를 고려하여 결정

총 크기
결정

(? , ?)



(0, 0)

공정사가 제공한 .lef 파일에서 io셀 크기 확인, TDF 파일에서 io셀 간의 거리 확인

power plan란?

- Floor plan 진행 후 sub 모듈과 메모리, 아날로그 IP 등에 대한 전원 공급방법을 사람이 직접 구성하는 것
- Stripe와 Mesh, Rectangular ring을 주로 사용하며 IR Drop이 일어나지 않도록 주의해야 함
- Tech file을 참고하여 전원연결에 어떤 Metal을 사용할 것인지 결정

Innovus

Tech file (Power)

Signal routing: 신호 연결선

M1-M9는 signal routing에 사용

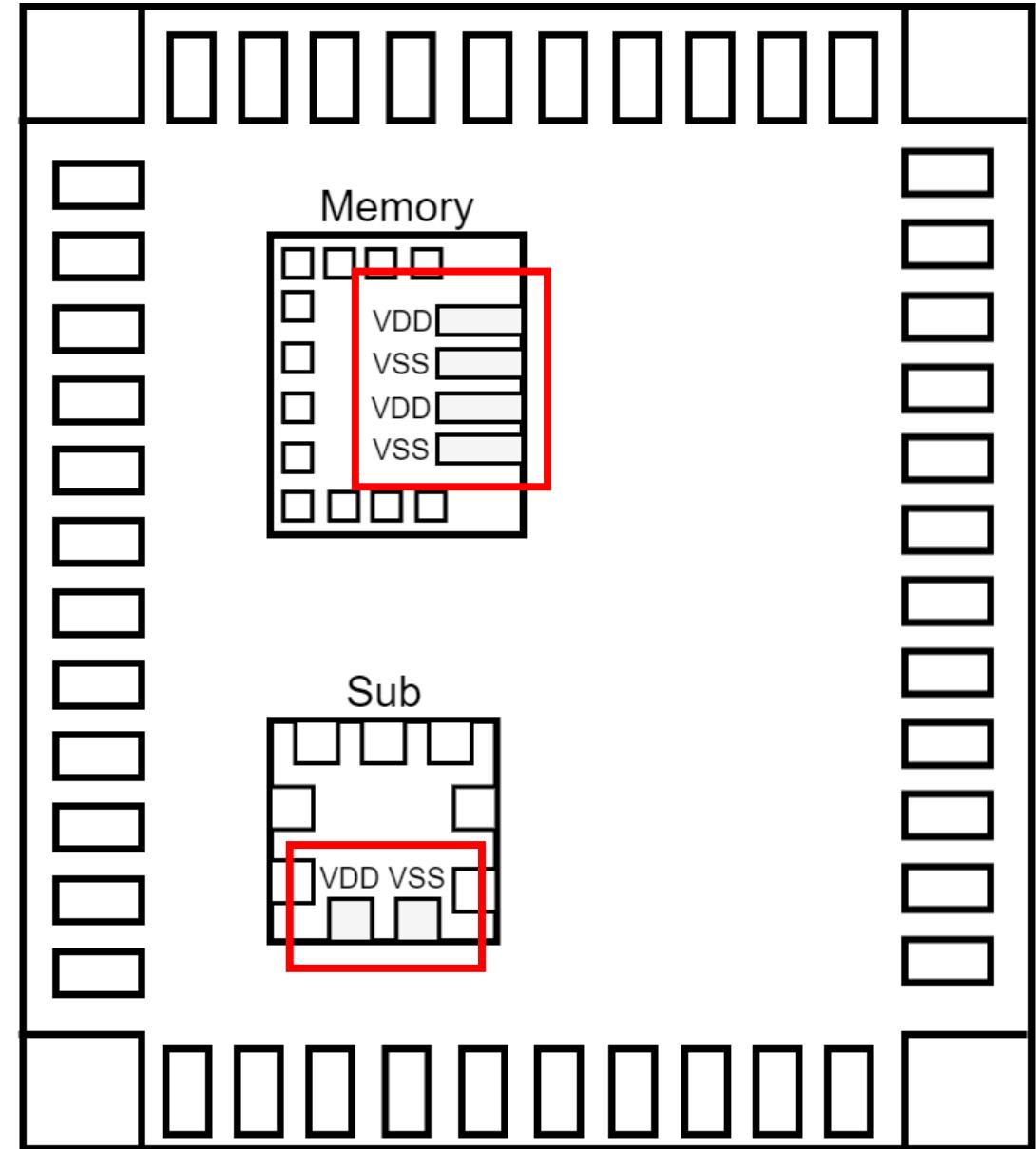
Mesh: 그물 모양의 파워 라인

M10-M11은 Mesh로 사용,
signal routing에 사용되는
M1-M9보다 Min width가 두배
이상 큼

	Direction	Horizontal Pitch	Vertical Pitch	Horizontal Offset	Vertical Offset	Min width	Max Width
M1	H	0.2	0.19	0.1	0.095	0.06	6.0
M2	V	0.2	0.19	0.1	0.095	0.08	6.0
M3	H	0.2	0.19	0.1	0.095	0.08	6.0
M4	V	0.2	0.19	0.1	0.095	0.08	6.0
M5	H	0.2	0.19	0.1	0.095	0.08	6.0
M6	V	0.2	0.19	0.1	0.095	0.08	6.0
M7	H	0.2	0.19	0.1	0.095	0.08	6.0
M8	V	0.2	0.19	0.1	0.095	0.08	6.0
M9	H	0.2	0.19	0.1	0.095	0.08	6.0
M10	V	0.5	0.19	0.6	0.095	0.22	6.0
M11	H	0.5	0.475	0.6	0.57	0.22	6.0

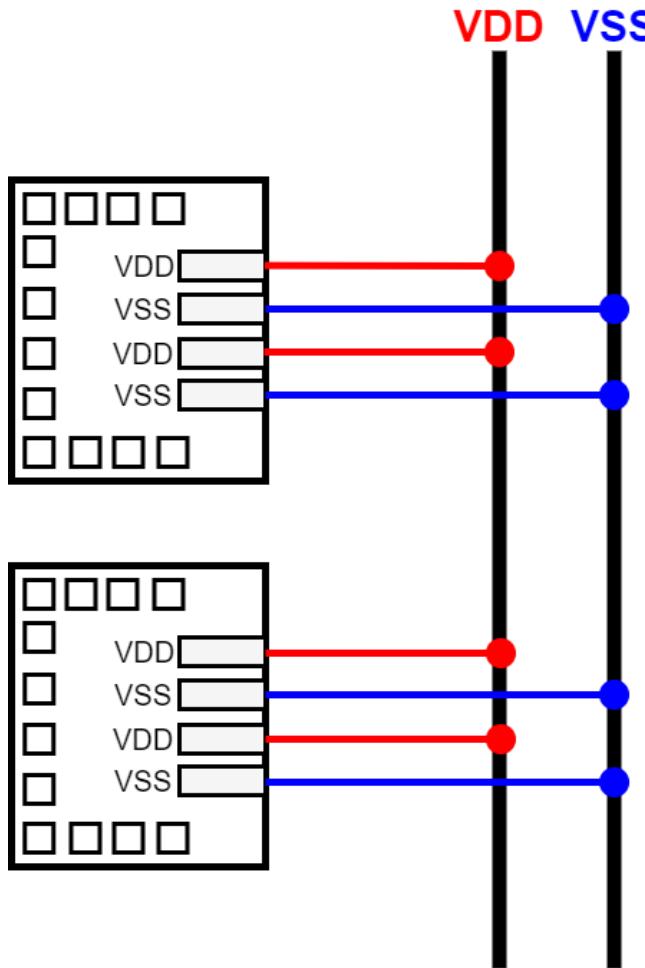
power plan

- 메모리와 sub모듈 등에 VDD와 VSS를 어떻게 공급해 줄 것인가 대한 생각이 필요함

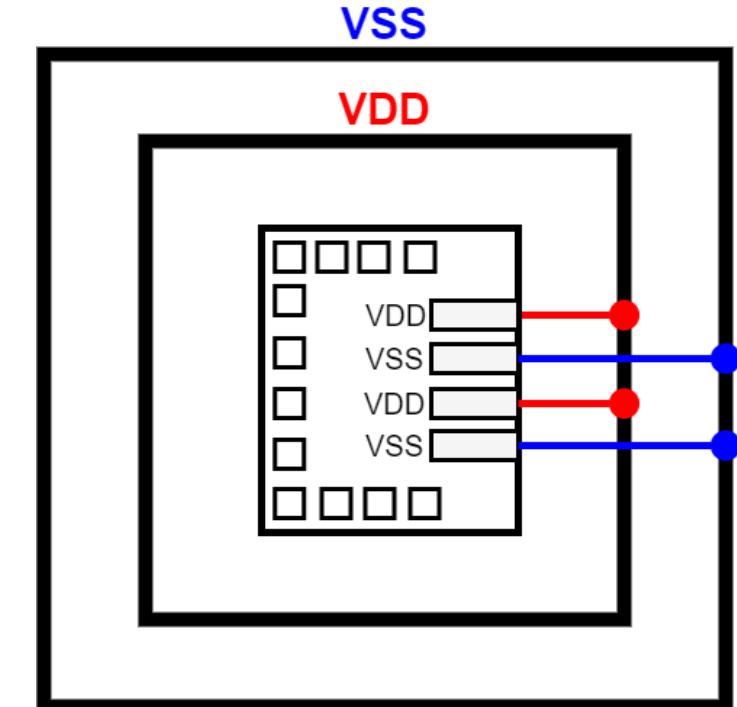


- 셀에 전원을 공급하는 방법

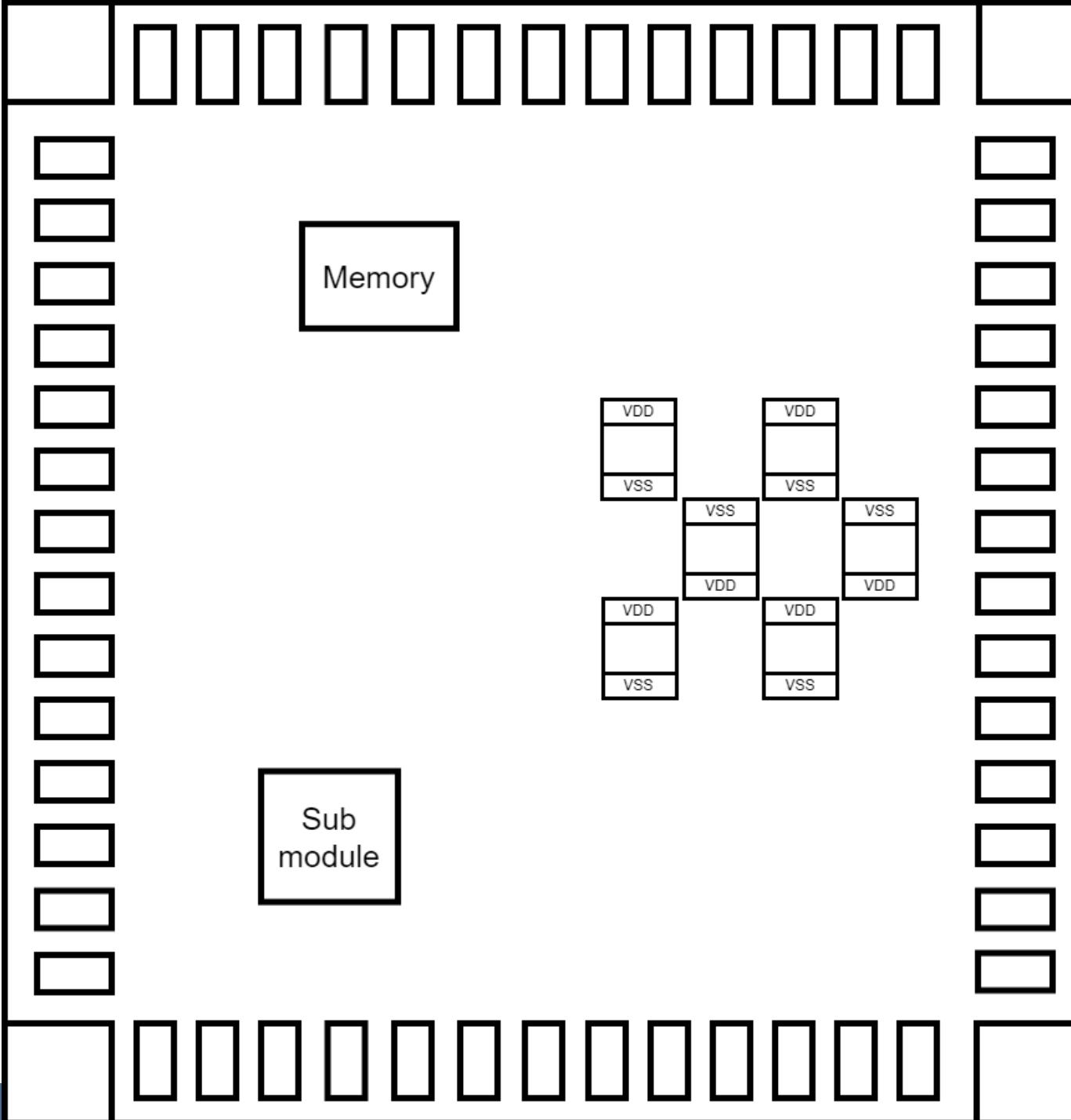
power plan



Strap: 전원을 공통
단자로 묶어서 연결



Rectangular ring: 전원선을 모듈에
사각형 모양으로 두른 후 연결



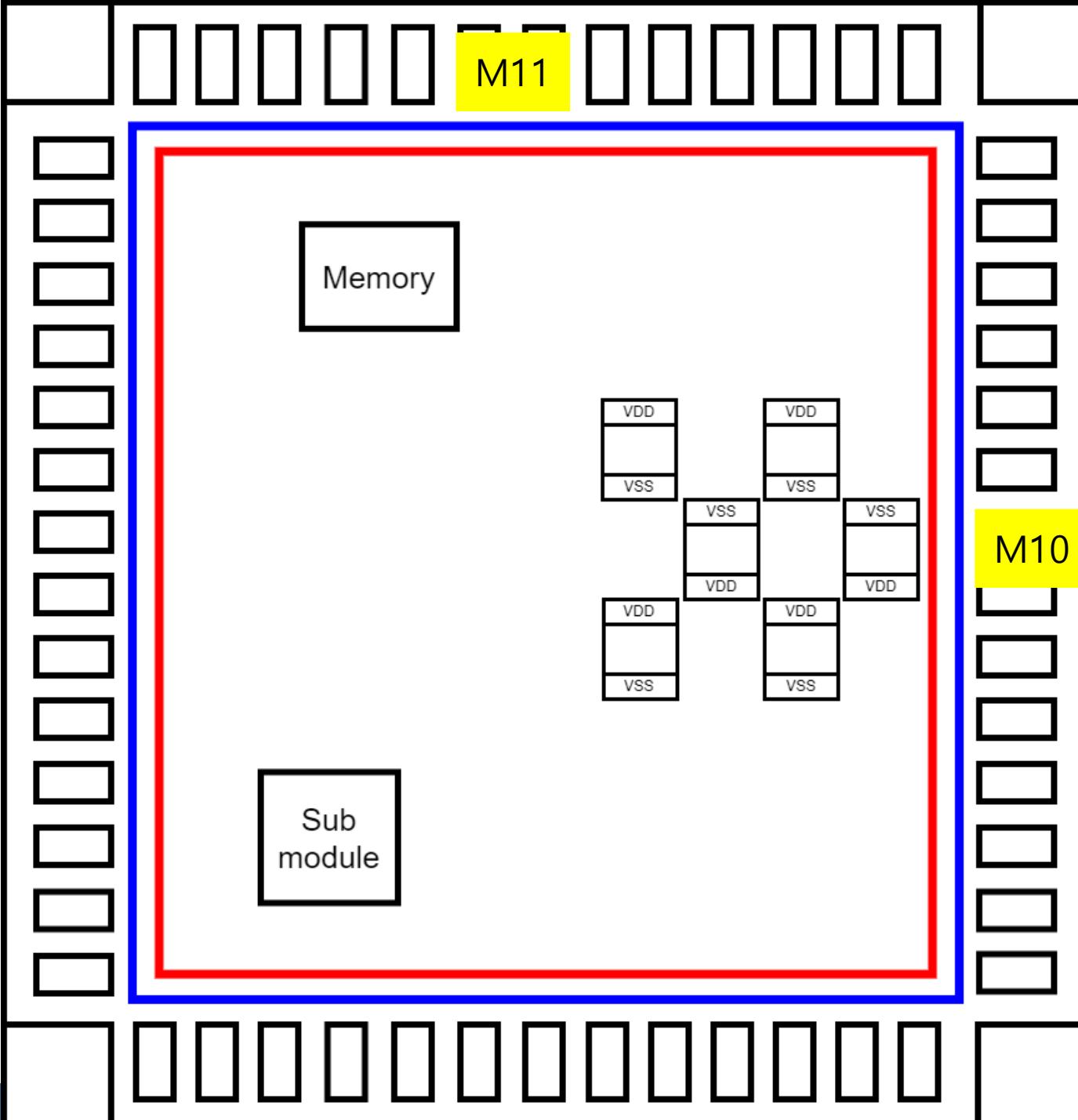
Floorplan: 메모리, 서브 모듈, 스탠다드 셀 등을 배치

VDD

VSS

M10 (V)

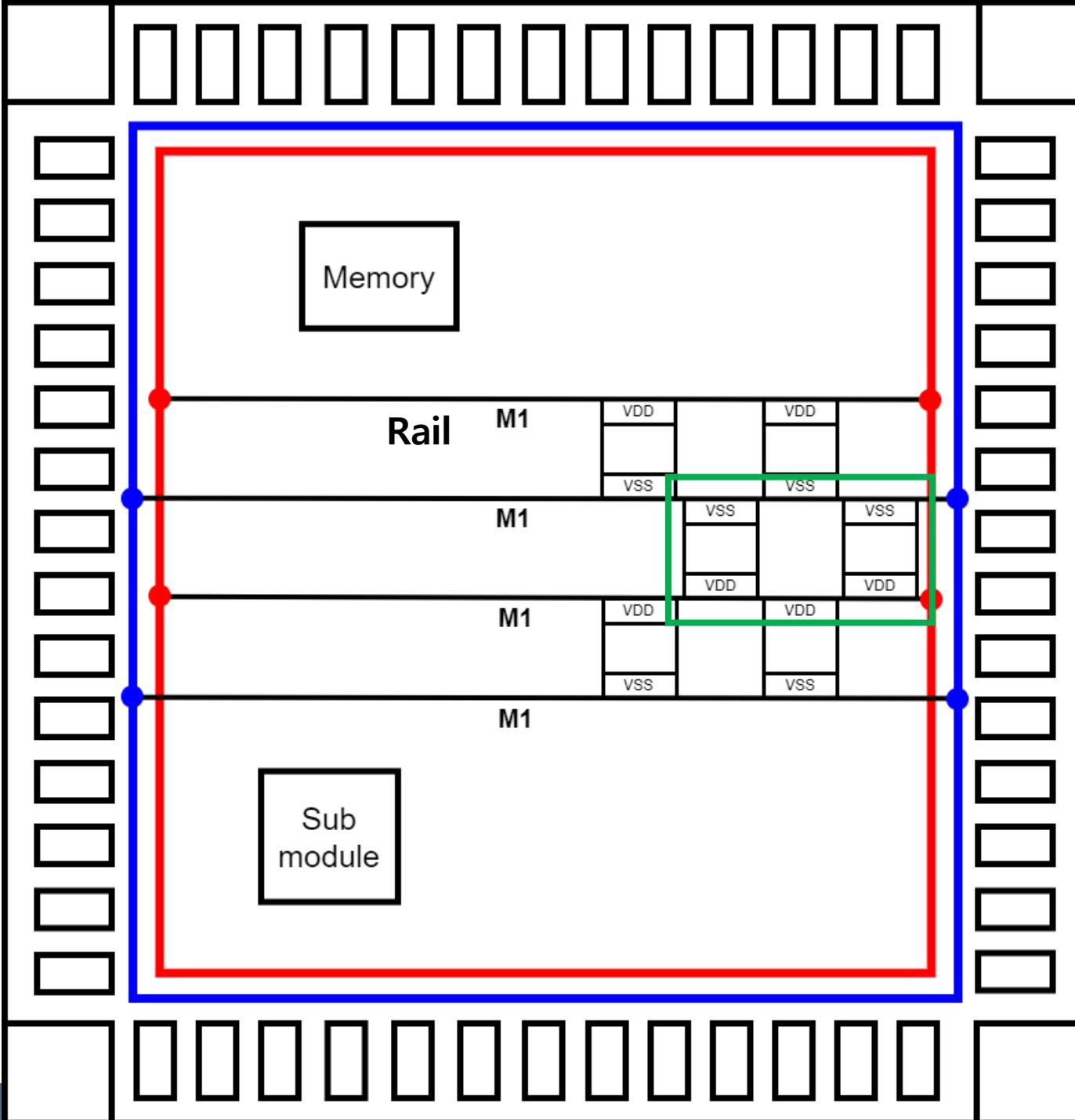
M11 (H)



TOP 디자인의
Rectangular ring
배치

VDD

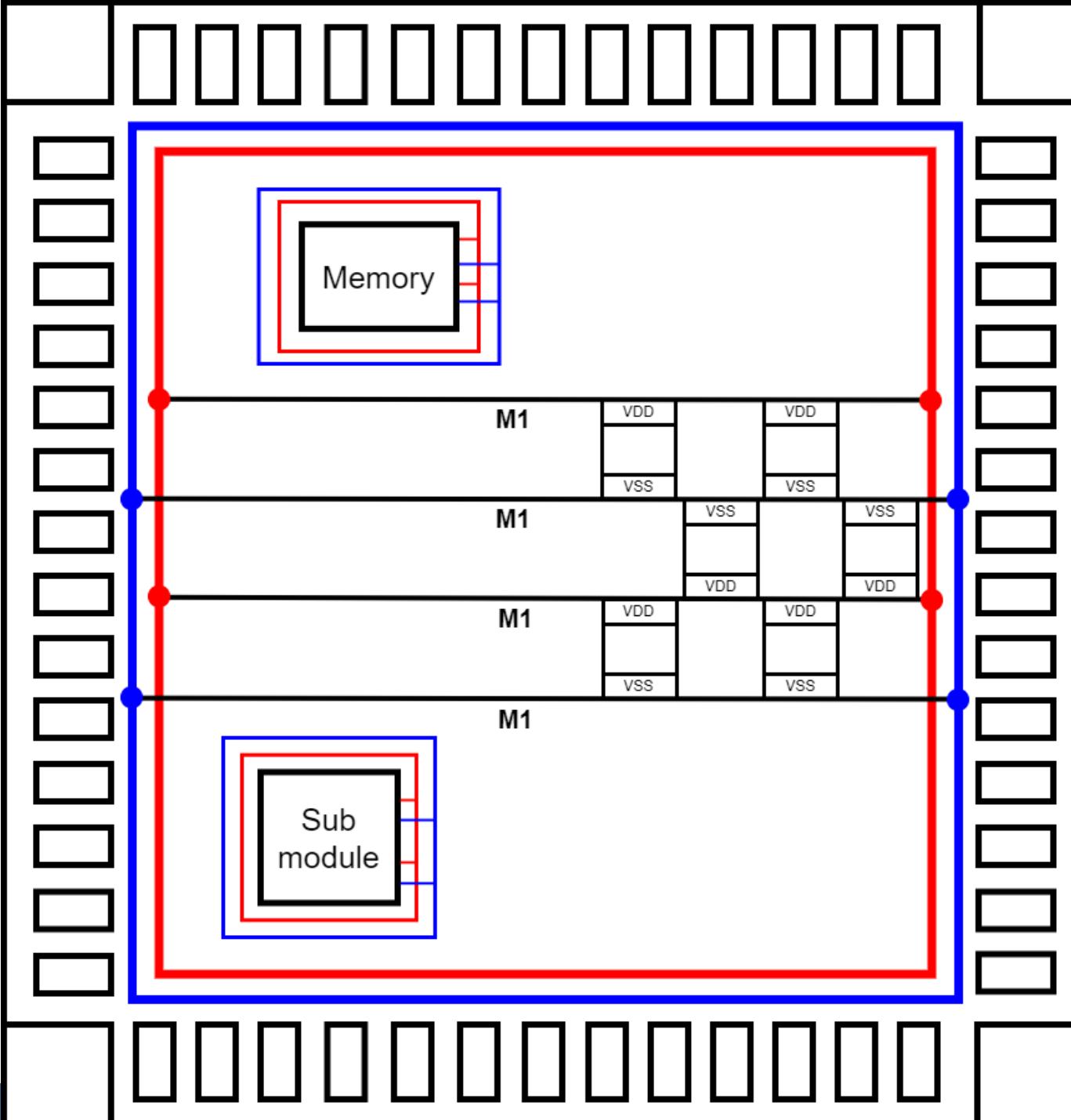
VSS



스탠다드 셀의 전원
공급을 위한
Rail(M1) 배치

초록색 상자안의 셀은 Area
를 최대한 줄이기 위해 셀을
flip하여 전원을 연결

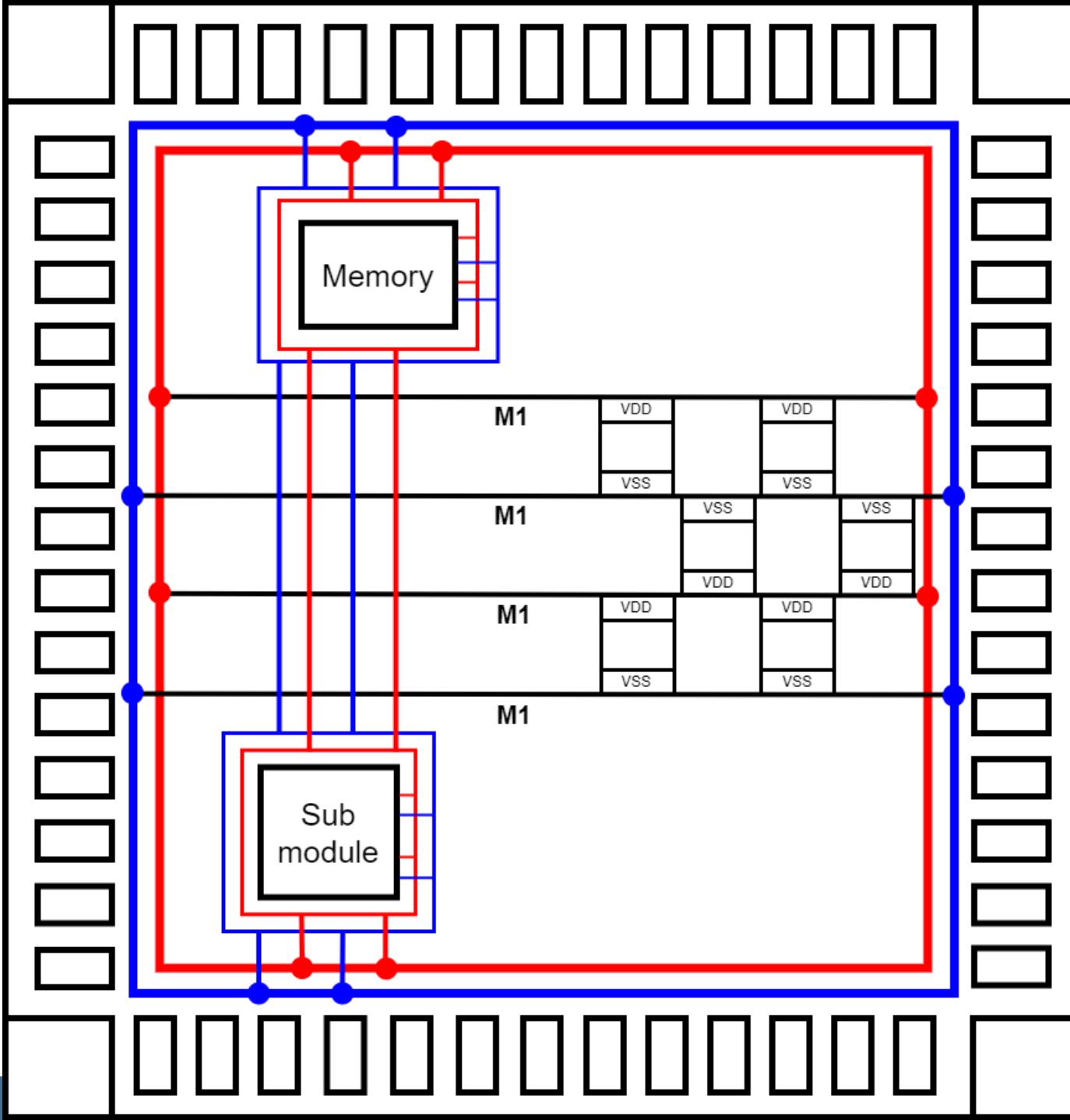
■ VDD
■ VSS



메모리와 서브 모듈
전원 공급을 위한
Rectangular ring 배치

모듈이 M1-M4까지 사용한
다면 sub모듈, 메모리의
Rectangular ring은 M5
이상으로 사용함

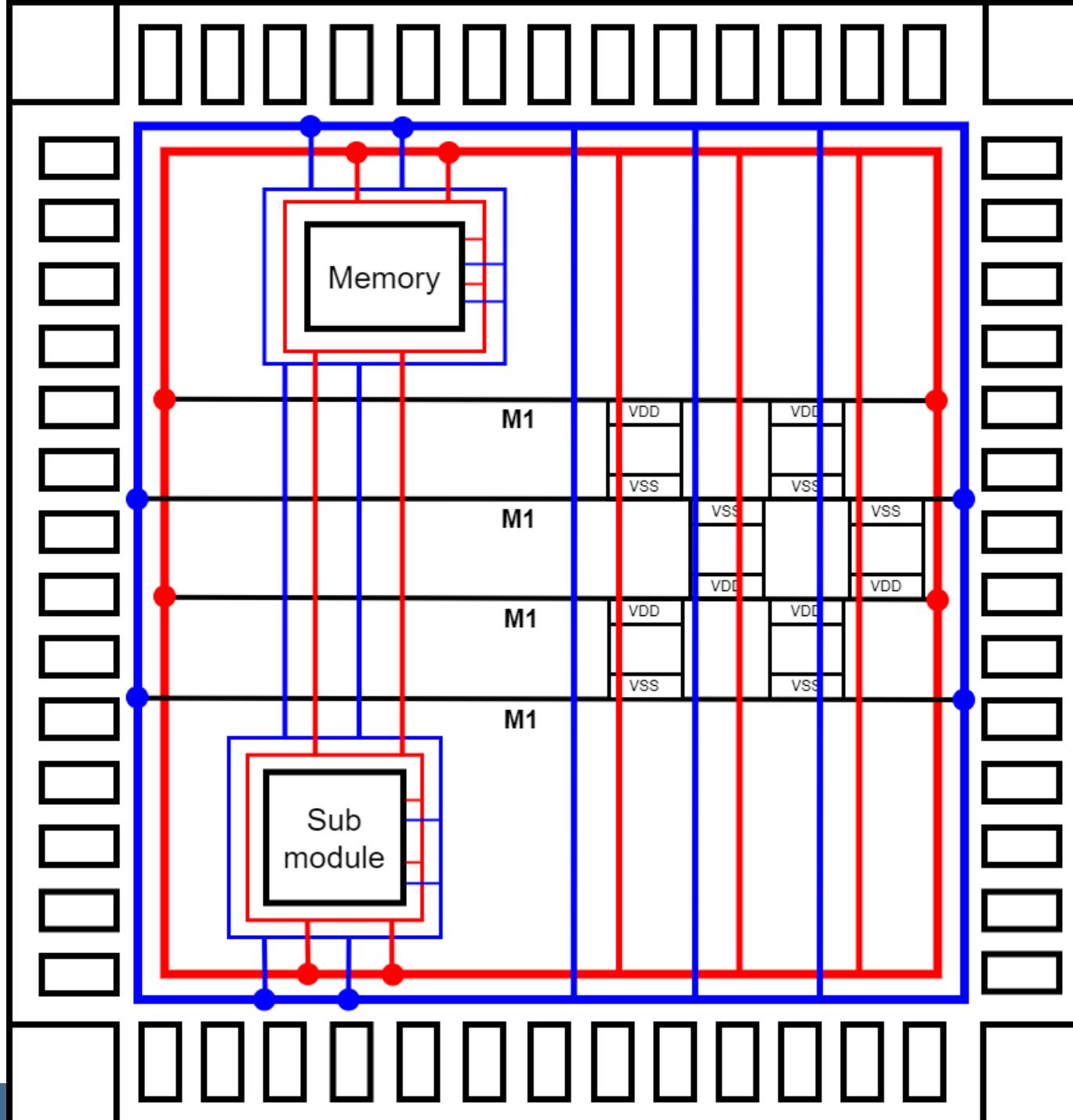
■ VDD
■ VSS



IR Drop을 방지하기
위해 전원 공급을
양방향으로 함

■ VDD
■ VSS

M10 (V)
M11 (H)



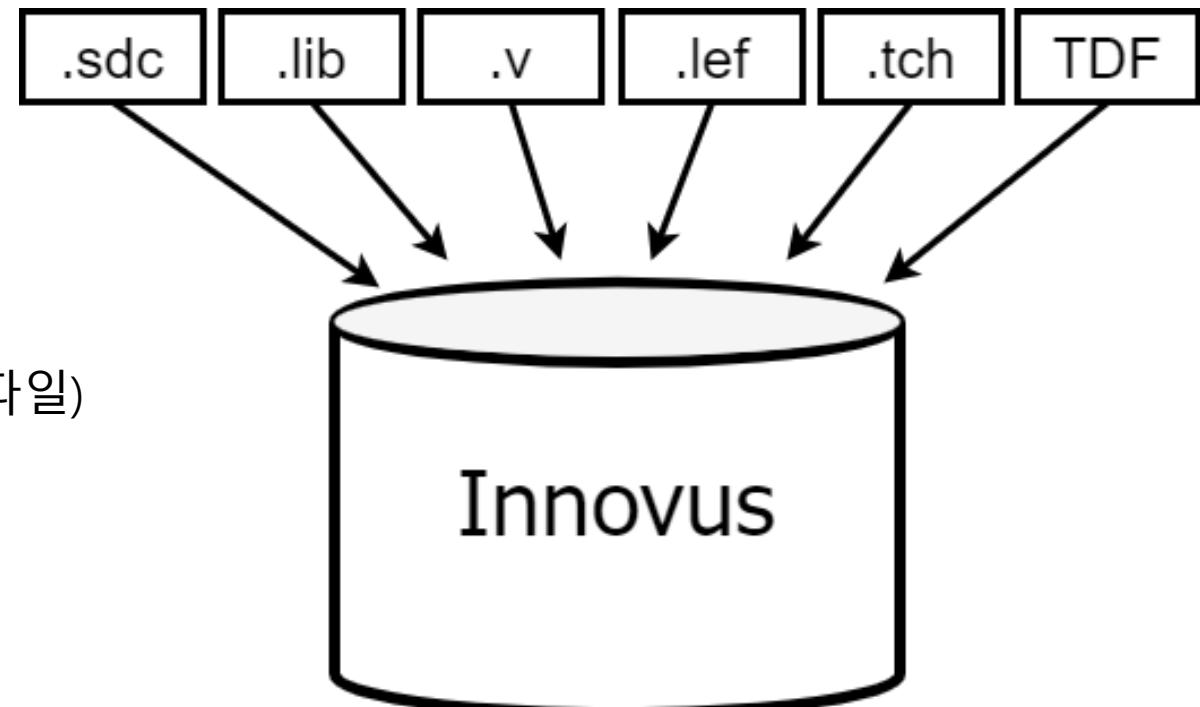
IR Drop과 같은 문제
발생을 방지하기 위해
Stripe(Strap) 연결

Stripe는 수직으로 연결하
며 코어 영역에 다른
metal과 쇼트를 방지하기
위해 M10 사용

Innovus 사용을 위한 파일 설명(예제)

준비 파일

- **디자인:** Gate Level Netlist(.v)
- **Goal:** .sdc 파일, TDF(모듈이나 Io셀의 배치를 수치화한 파일)
- **STD, IO:** .lib 파일, macro.lef 파일
- **공정사:** tech file(.tch), tech.lef 파일



Auto PnR

파일확인

```
$> vi counter.view
```

- 아래의 경로에서 counter.view 파일확인

```
[ex_poly1@npit physical_design]$ pwd  
/home/ex_poly1/SoC2/RAK/RTLtoGDSII/counter_design_database_45nm/physical_design
```

```
[ex_poly1@npit physical_design]$ ls  
counter.scandef counter.view counter_netlist.v counter_sdc.sdc power.tcl readme
```

Counter.view

- Cell delay 관련 설정임
- 2, 5행에서 setup time과 hold time에 대한 라이브러리를 셋업 함
- 8, 10행에서 2행과 5행의 셋업 라이브러리의 컨디션 이름을 설정함
- 위에 설정한 이름을 토대로 delay corner를 생성함

```

2 create_library_set -name max_timing\
3   -timing ../lib/slow_vdd1v0_basicCells.lib
4
5 create_library_set -name min_timing\
6   -timing ../lib/fast_vdd1v0_basicCells.lib
7
8 create_timing_condition -name default_mapping_tc_2\
9   -library_sets min_timing
10 create_timing_condition -name default_mapping_tc_1\
11   -library_sets max_timing
12
13 create_rc_corner -name rccorners\
14   -cap_table ../capttable/cln28hpl_1p10m+alrdl_5x2yu2yz_typical.capTbl\
15   -pre_route_res 1\
16   -post_route_res 1\
17   -pre_route_cap 1\
18   -post_route_cap 1\
19   -post_route_cross_cap 1\
20   -pre_route_clock_res 0\
21   -pre_route_clock_cap 0\
22   -qrc_tech ../QRC_Tech/gpdk045.tch
23
24 create_delay_corner -name max_delay\
25   -timing_condition {default_mapping_tc_1}\n26   -rc_corner rccorners
27 create_delay_corner -name min_delay\
28   -timing_condition {default_mapping_tc_2}\n29   -rc_corner rccorners
30
31 create_constraint_mode -name sdc_cons\
32   -sdc_files\
33   counter_sdc.sdc
34
35 create_analysis_view -name wc -constraint_mode sdc_cons -delay_corner max_delay
36 create_analysis_view -name bc -constraint_mode sdc_cons -delay_corner min_delay
37
38 set_analysis_view -setup wc -hold bc

```

Setup time은 빨간 상자
hold time은 파란 상자

Counter.view

- net delay 관련 설정임
- PnR에서 setup time과 hold time을 모두 해결해야 하므로 net delay 정보가 필요함
- 14행의 cap_table과 22행의 tech파일을 통해 공정사가 제공한 net delay 정보를 준비함

```
2 create_library_set -name max_timing\
3   -timing ../lib/slow_vdd1v0_basicCells.lib
4
5 create_library_set -name min_timing\
6   -timing ../lib/fast_vdd1v0_basicCells.lib
7
8 create_timing_condition -name default_mapping_tc_2\
9   -library_sets min_timing
10 create_timing_condition -name default_mapping_tc_1\
11   -library_sets max_timing
12
13 create_rc_corner -name rccorners\
14   -cap_table ../captable/cln28hpl_1p10m+alrdl_5x2yu2yz_typical.capTbl\
15   -pre_route_res 1\
16   -post_route_res 1\
17   -pre_route_cap 1\
18   -post_route_cap 1\
19   -post_route_cross_cap 1\
20   -pre_route_clock_res 0\
21   -pre_route_clock_cap 0\
22   -qrc_tech ../QRC_Tech/gpdk045.tch
23
24 create_delay_corner -name max_delay\
25   -timing_condition {default_mapping_tc_1}\\
26   -rc_corner rccorners
27 create_delay_corner -name min_delay\
28   -timing_condition {default_mapping_tc_2}\\
29   -rc_corner rccorners
30
31 create_constraint_mode -name sdc_cons\
32   -sdc_files\
33   counter_sdc.sdc
34
35 create_analysis_view -name wc -constraint_mode sdc_cons -delay_corner max_delay
36 create_analysis_view -name bc -constraint_mode sdc_cons -delay_corner min_delay
37
38 set_analysis_view -setup wc -hold bc
```

Counter.view

- 31 ~ 33행은 합성 과정에서 만들어진 .sdc 파일을 사용하여 constraint_mode를 생성함
- 35행과 36행에 각각 setup time, hold time 관련 constraint_mode를 wc와 bc로 나눠서 create_analysis_view를 생성함

```

2 create_library_set -name max_timing\
3   -timing ../lib/slow_vdd1v0_basicCells.lib
4
5 create_library_set -name min_timing\
6   -timing ../lib/fast_vdd1v0_basicCells.lib
7
8 create_timing_condition -name default_mapping_tc_2\
9   -library_sets min_timing
10 create_timing_condition -name default_mapping_tc_1\
11   -library_sets max_timing
12
13 create_rc_corner -name rccorners\
14   -cap_table ../capttable/cln28hpl_1p10m+alrdl_5x2yu2yz_typical.capTbl\
15   -pre_route_res 1\
16   -post_route_res 1\
17   -pre_route_cap 1\
18   -post_route_cap 1\
19   -post_route_cross_cap 1\
20   -pre_route_clock_res 0\
21   -pre_route_clock_cap 0\
22   -qrc_tech ../QRC_Tech/gpdk045.tch
23
24 create_delay_corner -name max_delay\
25   -timing_condition {default_mapping_tc_1}\
26   -rc_corner rccorners
27 create_delay_corner -name min_delay\
28   -timing_condition {default_mapping_tc_2}\
29   -rc_corner rccorners
30
31 create_constraint_mode -name sdc_cons\
32   -sdc_files\
33   counter_sdc.sdc
34
35 create_analysis_view -name wc -constraint_mode sdc_cons -delay_corner max_delay
36 create_analysis_view -name bc -constraint_mode sdc_cons -delay_corner min_delay
37
38 set_analysis_view -setup wc -hold bc

```

bc: best condition
wc: worst condition

Counter.view

- 38행의 set_analysis_view를 생성함
- -setup wc는 worst condition이므로 setup time에 민감함
- -hold bc는 best condition이므로 hold time에 민감함

```
2 create_library_set -name max_timing\
3   -timing ../lib/slow_vdd1v0_basicCells.lib
4
5 create_library_set -name min_timing\
6   -timing ../lib/fast_vdd1v0_basicCells.lib
7
8 create_timing_condition -name default_mapping_tc_2\
9   -library_sets min_timing
10 create_timing_condition -name default_mapping_tc_1\
11   -library_sets max_timing
12
13 create_rc_corner -name rccorners\
14   -cap_table ../capttable/cln28hpl_1p10m+alrdl_5x2yu2yz_typical.capTbl\
15   -pre_route_res 1\
16   -post_route_res 1\
17   -pre_route_cap 1\
18   -post_route_cap 1\
19   -post_route_cross_cap 1\
20   -pre_route_clock_res 0\
21   -pre_route_clock_cap 0\
22   -qrc_tech ../QRC_Tech/gpdk045.tch
23
24 create_delay_corner -name max_delay\
25   -timing_condition {default_mapping_tc_1}\\
26   -rc_corner rccorners
27 create_delay_corner -name min_delay\
28   -timing_condition {default_mapping_tc_2}\\
29   -rc_corner rccorners
30
31 create_constraint_mode -name sdc_cons\
32   -sdc_files\
33   counter_sdc.sdc
34
35 create_analysis_view -name wc -constraint_mode sdc_cons -delay_corner max_delay
36 create_analysis_view -name bc -constraint_mode sdc_cons -delay_corner min_delay
37
38 set_analysis_view -setup wc -hold bc
```

Auto PnR

파일확인

\$> vi power.tcl

- power.tcl 파일확인

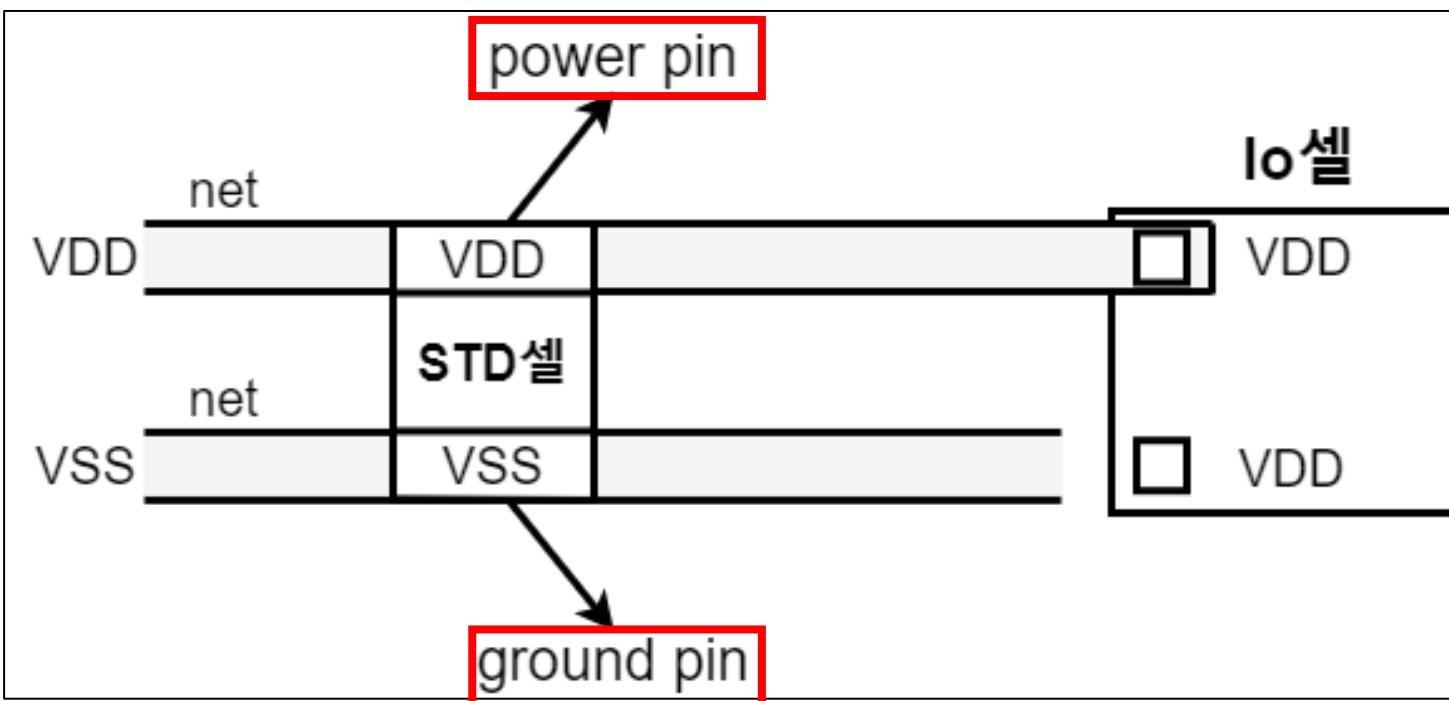
```
[ex_poly1@npit physical_design]$ ls  
counter.scandef  counter.view  counter_netlist.v  counter_sdc.sdc  power.tcl  readme
```

```

1 connect_global_net VDD -type pg_pin -pin VDD -inst *
2 connect_global_net VSS -type pg_pin -pin VSS -inst *
3 connect_global_net VDD -type tie_hi
4 connect_global_net VSS -type tie_lo
5 connect_global_net VDD -type tie_hi -pin VDD -inst *
6 connect_global_net VSS -type tie_lo -pin VSS -inst *

```

- 글로벌한 power net를 연결하는 명령이며
툴 사용시 source_power.tcl 함
- 1, 2행은 작은 셀들의 power pin을 VDD, VSS
의 net와 연결시켜 줌
- Io셀의 VDD, VSS power pin과 VDD, VSS net
와 연결시켜 줌

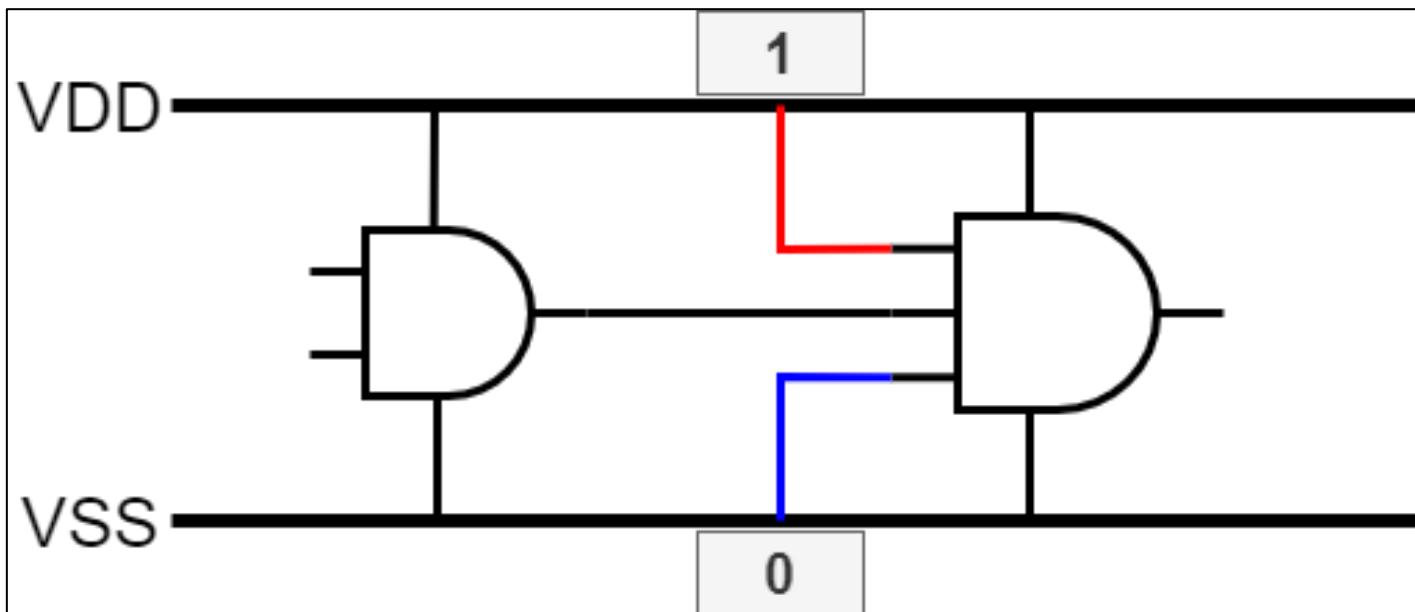


```

1 connect_global_net VDD -type pg_pin -pin VDD -inst *
2 connect_global_net VSS -type pg_pin -pin VSS -inst *
3 connect_global_net VDD -type tie_hi
4 connect_global_net VSS -type tie_lo
5 connect_global_net VDD -type tie_hi -pin VDD -inst *
6 connect_global_net VSS -type tie_lo -pin VSS -inst *

```

- 글로벌한 power net를 연결하는 명령이며 툴 사용시 source_power.tcl 함
- 3행은 cell에 1(high)가 입력되어야 할 때 **빨간색** net와 같이 VDD에 연결시키는 명령임
- 4행은 cell에 0(low)가 입력되어야 할 때 **파란색** net와 같이 VSS에 연결시키는 명령임



Pins.io

- RAK을 사용하여 실습을 진행하므로 pins.io는 없이 일단 진행함
- pins.io는 각종 pin과 io셀에 대한 위치 또는 각종 정보가 들어있음

Innovus (예제)

Auto PnR

Innovus 툴 사용 준비

- 두개의 터미널 사용 (아래의 경로에서 진행)
- 하나는 innovus 툴 실행, 나머지는 파일 확인을 위해 대기

```
ex.poly1@npit:physical_design
File Edit View Search Terminal Help
Cadence Innovus(TM) Implementation System.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved worldwide.

Version: v22.16-s082_1, built Fri Jun 7 09:42:52 PDT 2024
Options: -stylus
Date: Wed Feb 19 13:48:11 2025
Host: npit.ic.rnd1 (x86_64 w/Linux 3.10.0-1160.119.1.el7.x86_64) (20cores*80cpus*Intel(R) Xeon(R) Silver 4316 CPU @ 2.30 GHz 30720KB)
OS: Red Hat Enterprise Linux Server 7.9 (Maipo)

License:
[13:48:11.440209] Configured Lic search path (22.01-s003): 35266@npit-service1.iptime.org

      invs  Innovus Implementation System 22.1      ch
eckout succeeded
      8 CPU jobs allowed with the current license(s). U
se set_multi_cpu_usage to set your required CPU count.

Create and set the environment variable TMPDIR to /home/ex_poly1/
SoC2/RAK/RTLtoGDSII/counter_design_database_45nm/physical_design/
innovus_temp_71034_5f85f843-0c94-4c00-af10-9ddbeaaba754_npit.ic.r
nd1_ex_poly1_4tsHgP.

Change the soft stacksize limit to 0.2%RAM (771 mbytes). Set glob
al soft_stack_size_limit to change the value.

**INFO: MMC transition support version v31-84

@innovus 1> 
```

```
ex_poly1@npit physical_design]$ pwd
/home/ex_poly1/SoC2/RAK/RTLtoGDSII/counter_design_database_45nm/physical_design
[ex_poly1@npit physical_design]$ 
```

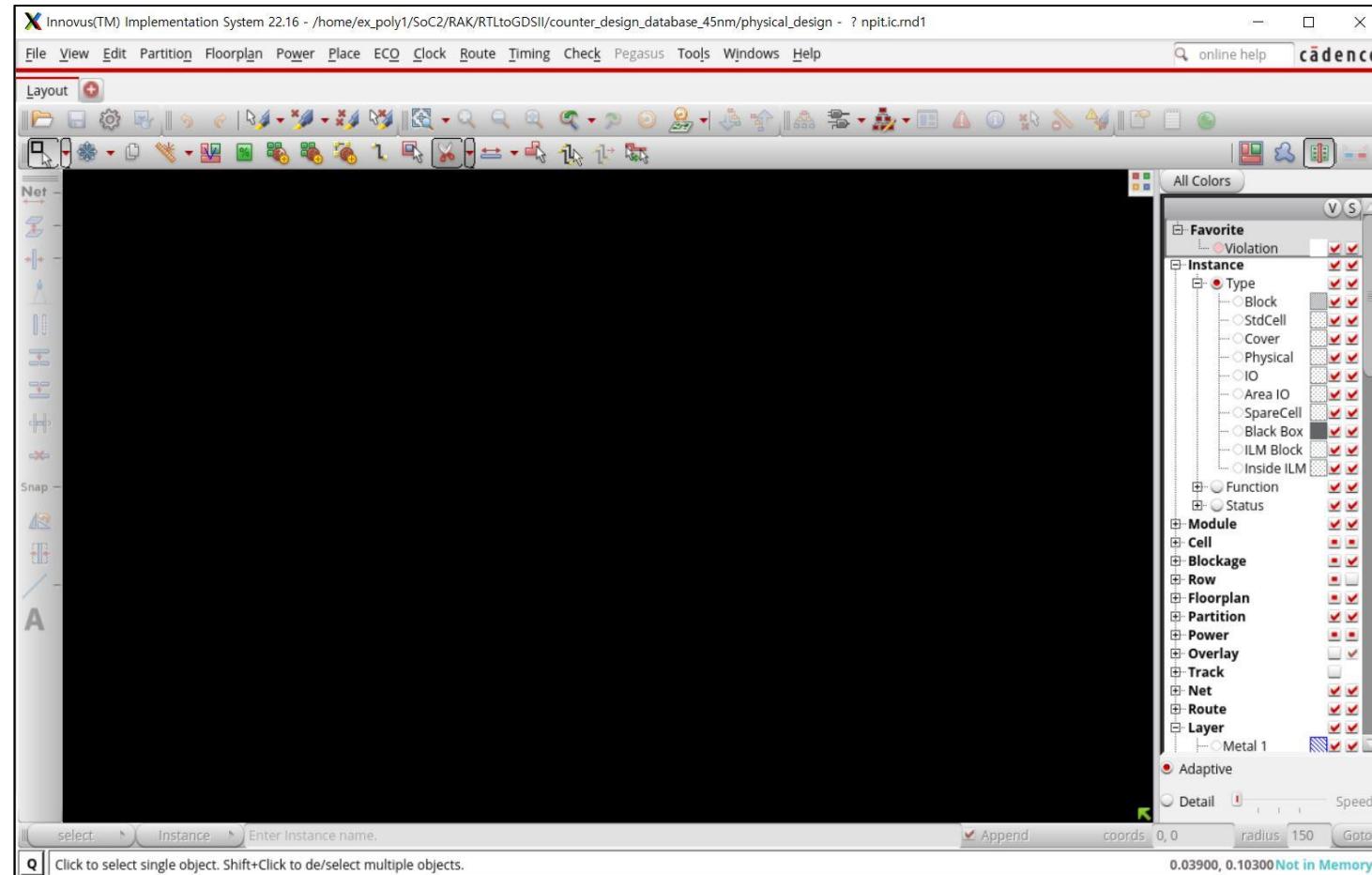
Auto PnR

Innovus 툴 사용 준비

\$> innovus -stylus

- Innovus의 gui가 자동으로 실행됨

```
[ex_poly1@npit physical_design]$ innovus -stylus
```



Auto PnR

Innovus 툴 사용 준비

- physical_design 폴더 파일확인

```
[ex_poly1@npit physical_design]$ ls  
counter.scandef  counter.view  counter_netlist.v  counter_sdc.sdc  power.tcl  readme
```

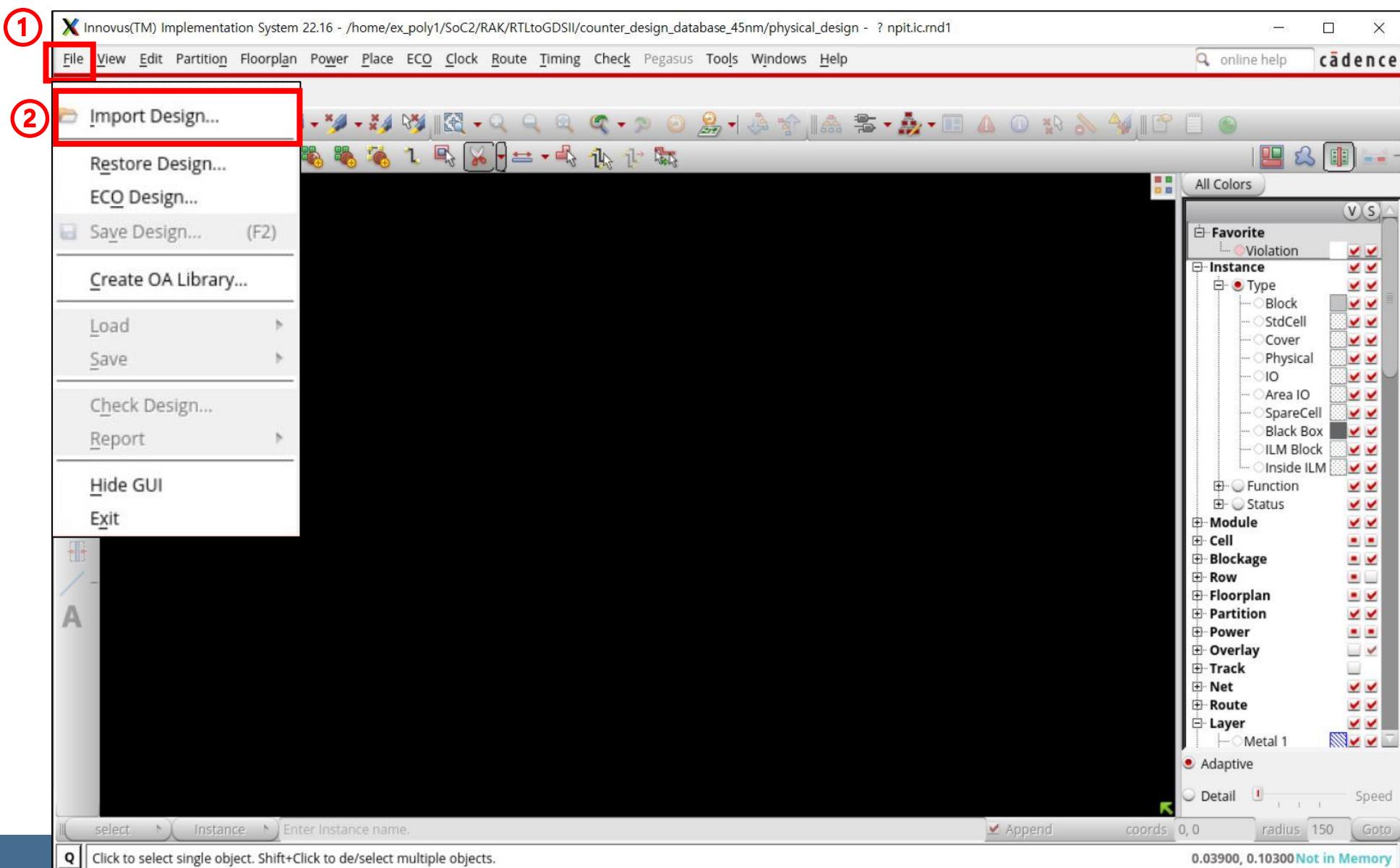
LAB (예제)

Auto PnR

Innovus

\$> innovus -stylus

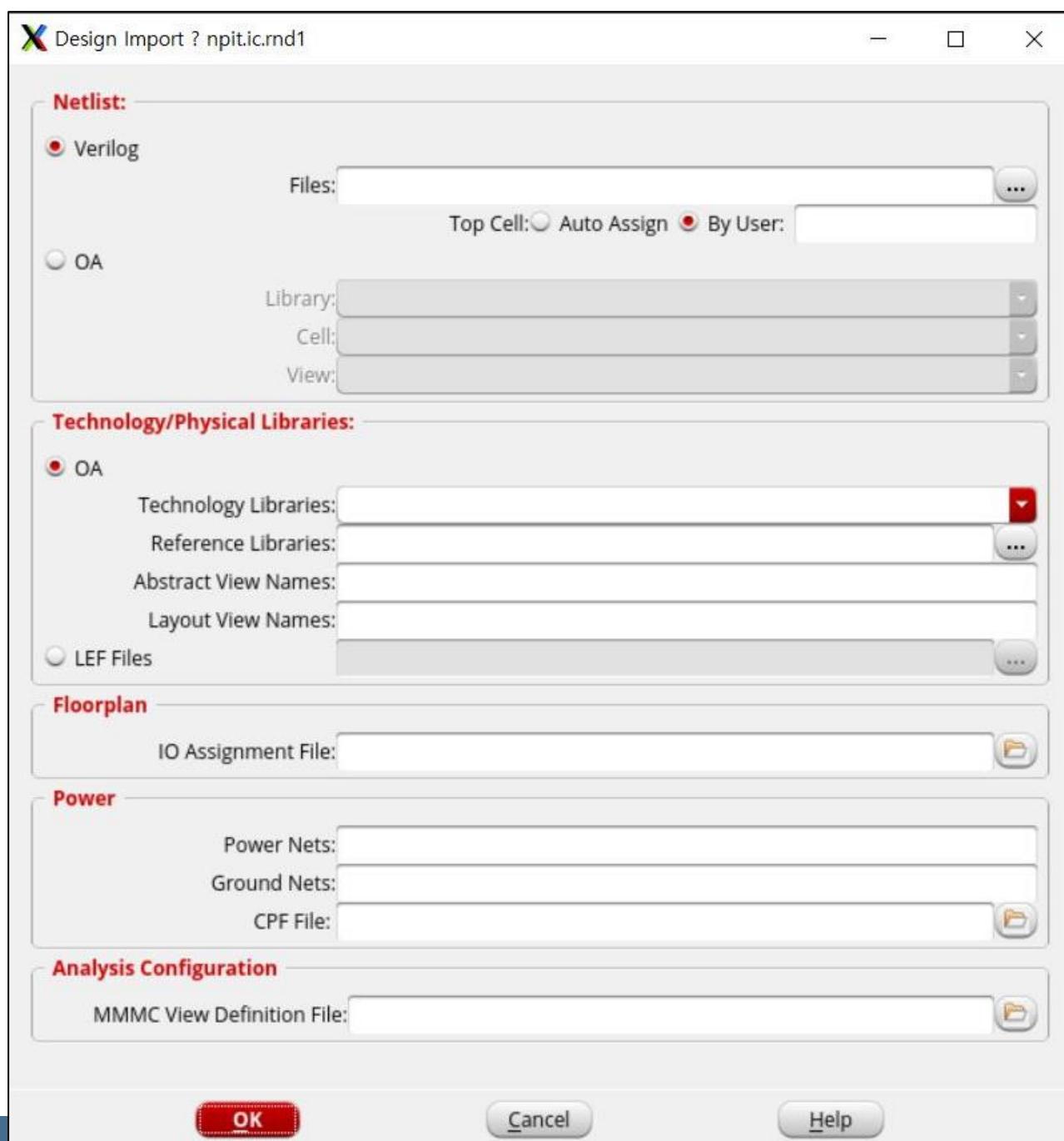
- Import Design에서 미리 준비된 파일을 불러들임



Auto PnR

Innovus

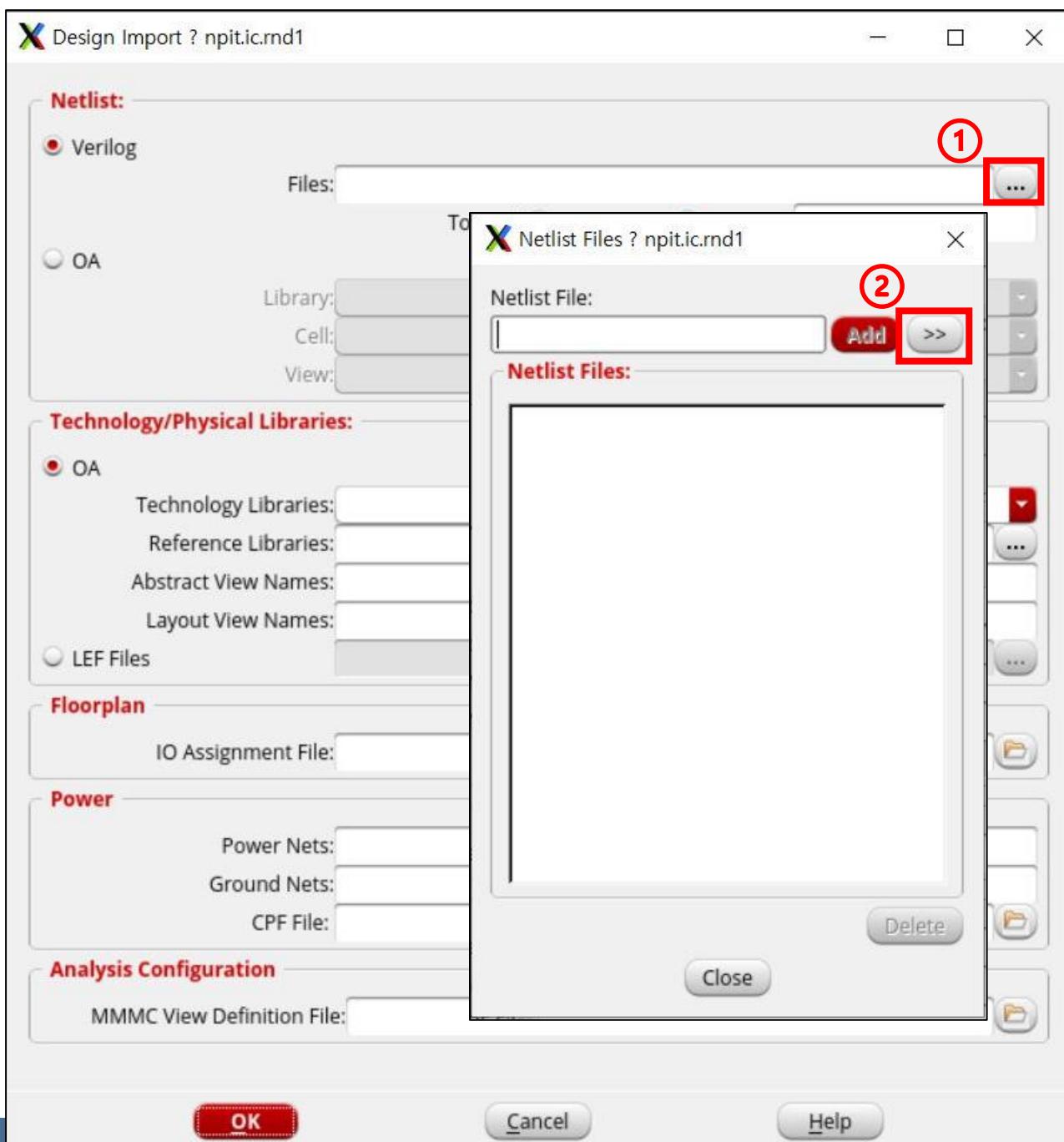
- Import Design



Auto PnR

Innovus

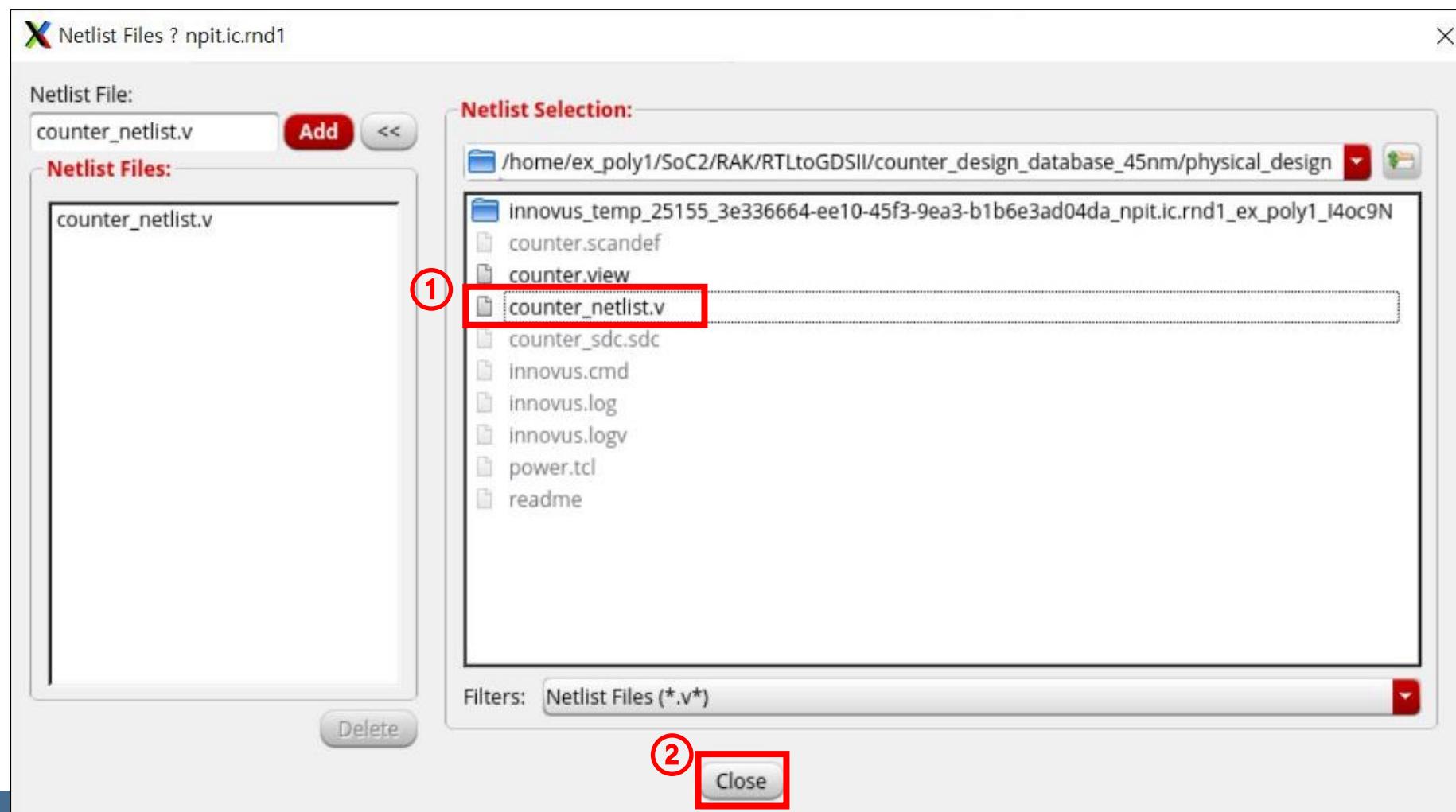
- Import Design
- Verilog(.v) 파일을 불러들임



Auto PnR

Innovus

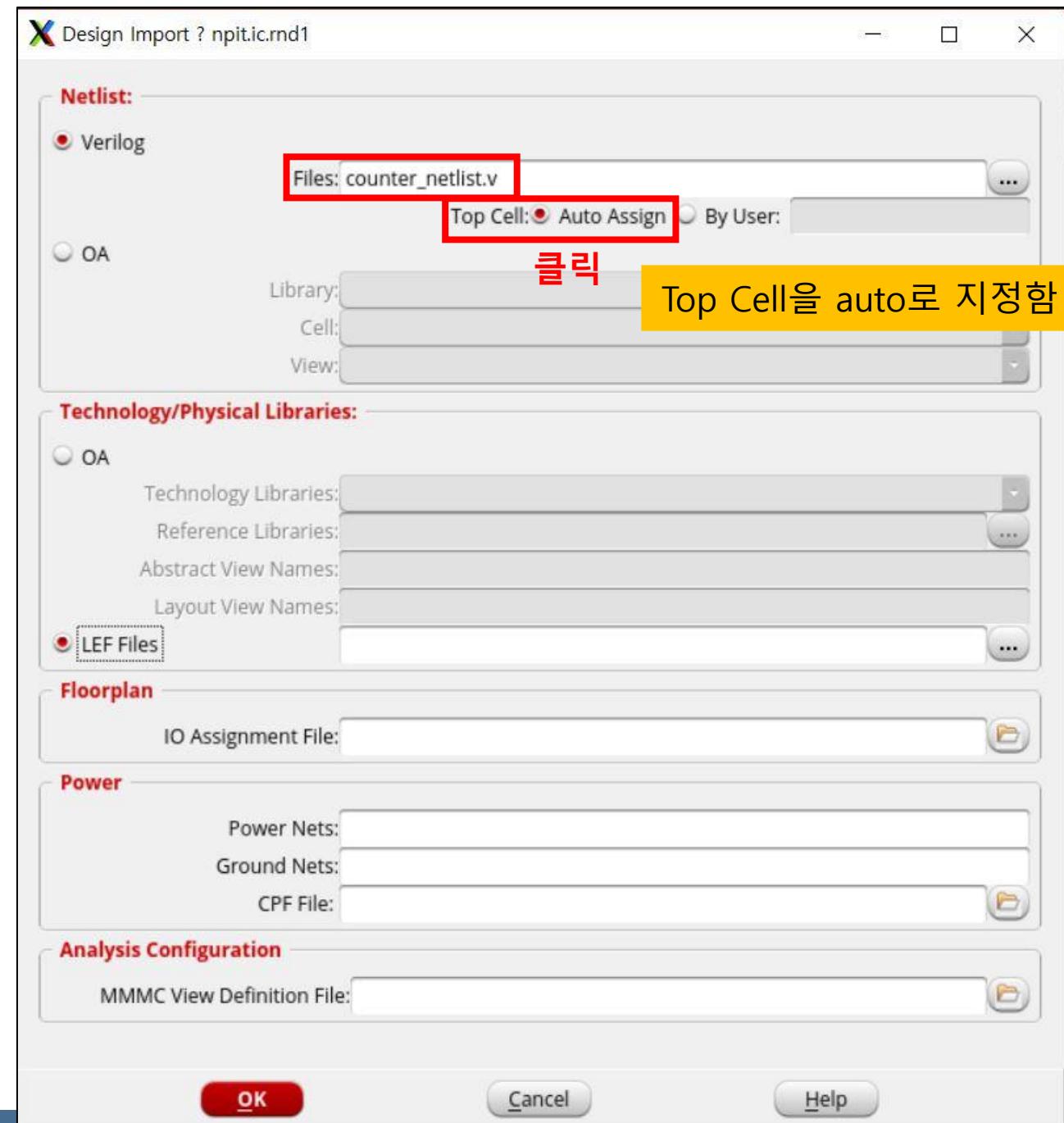
- Import Design
- Verilog(.v) 파일을 불러들임



Auto PnR

Innovus

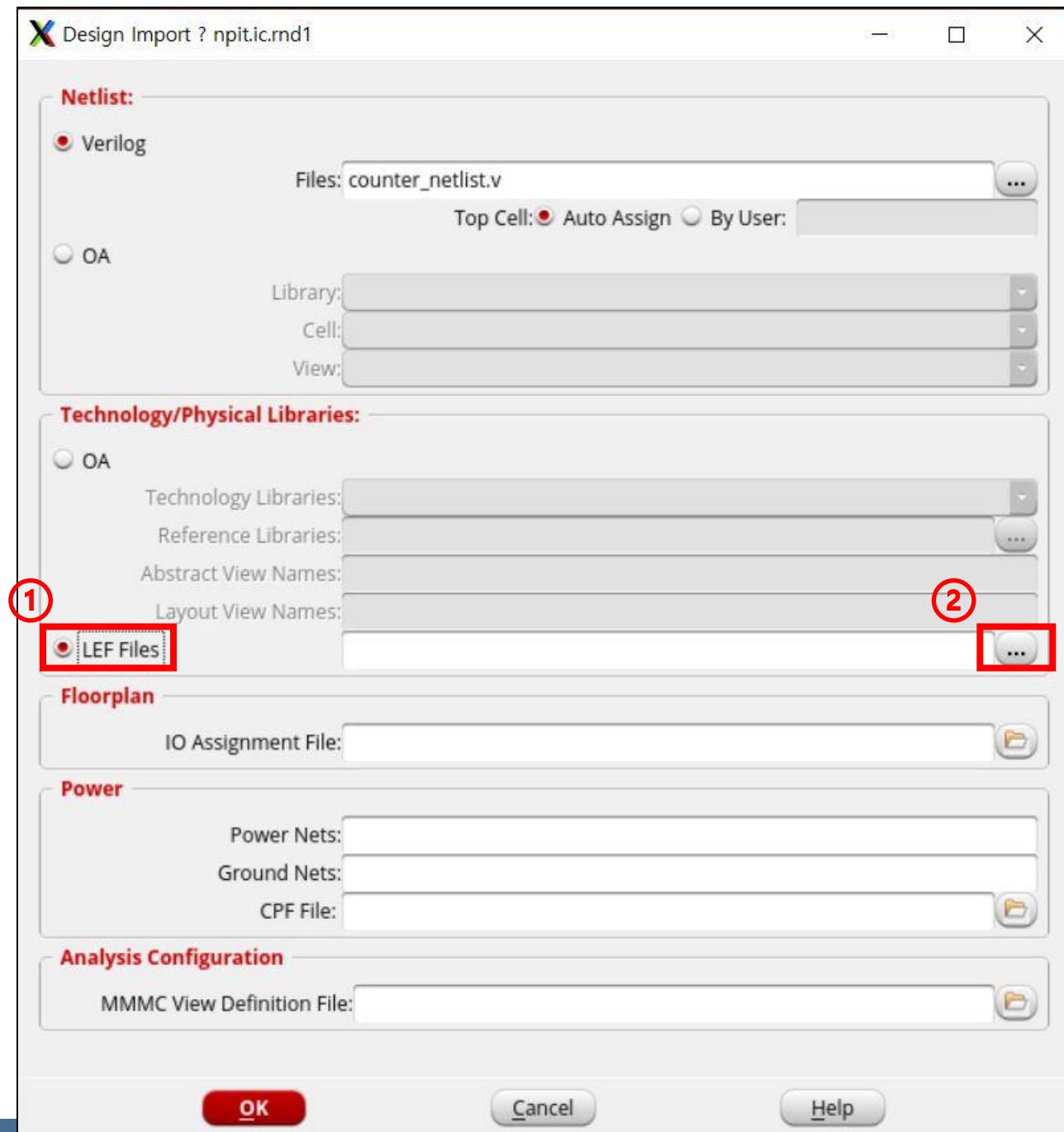
- Import Design
- Verilog(.v) 파일을 불러들임



Auto PnR

Innovus

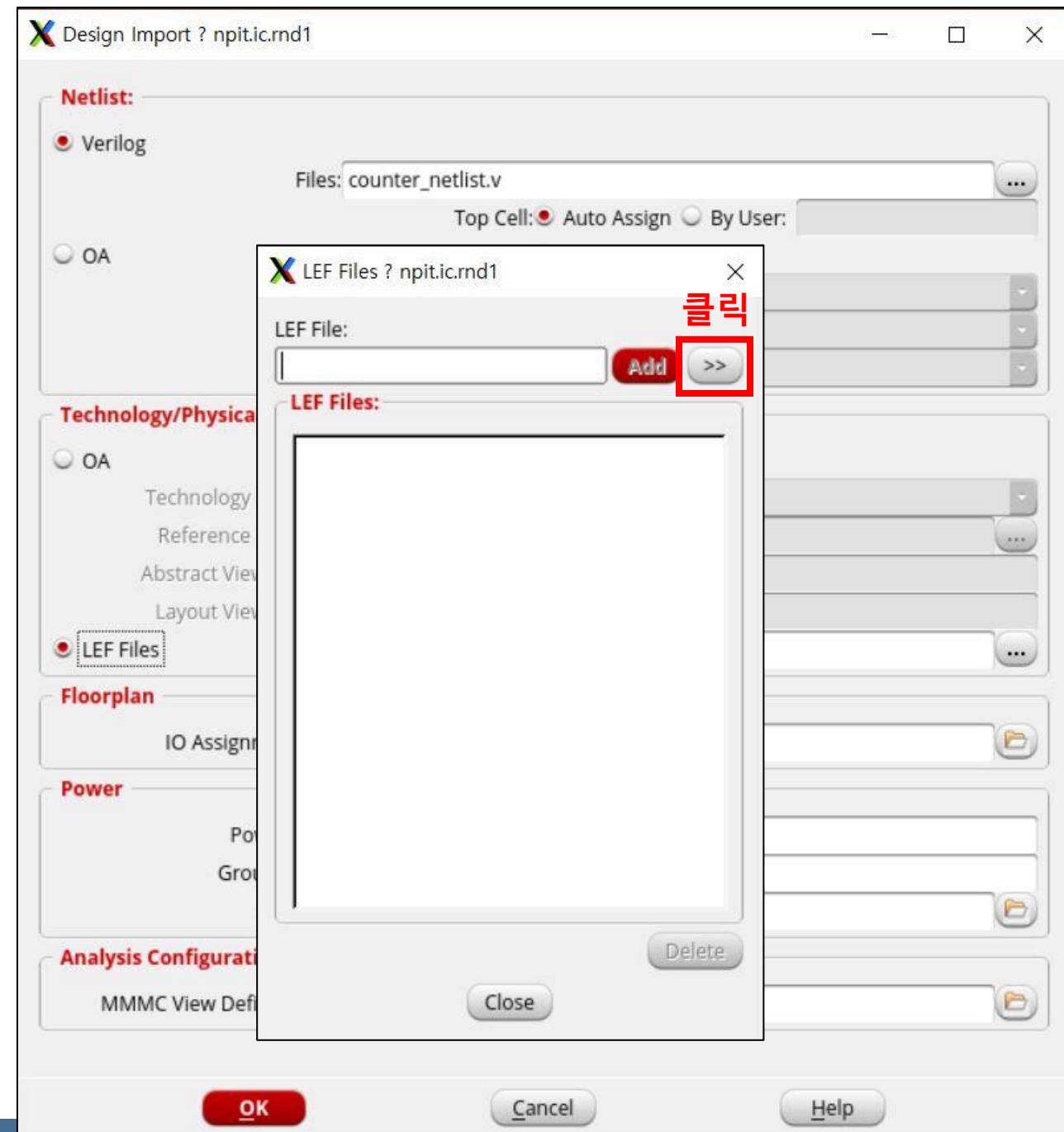
- Import Design
- LEF Files을 불러들임



Auto PnR

Innovus

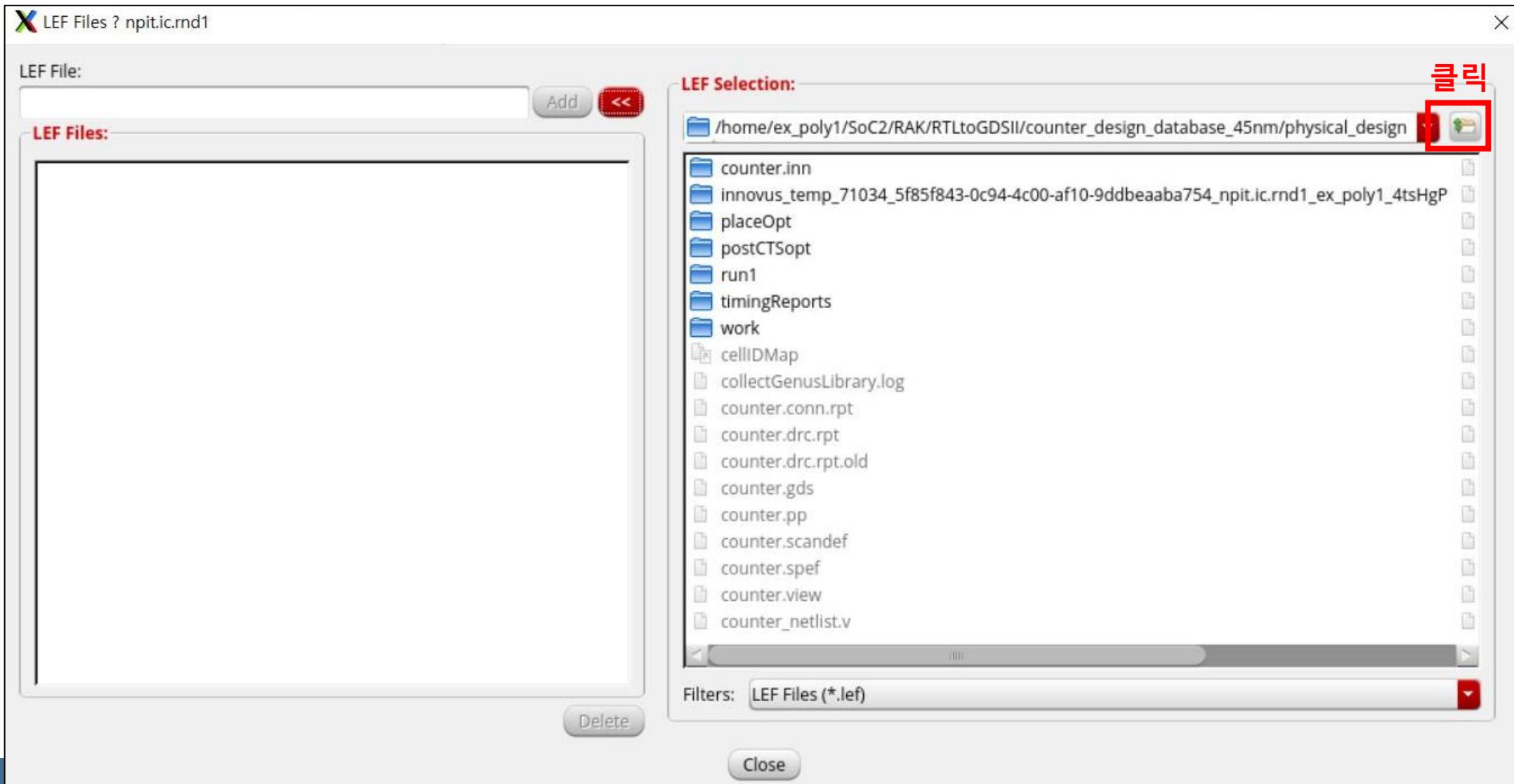
- Import Design
- LEF Files을 불러들임



Auto PnR

- LEF Files을 불러들임

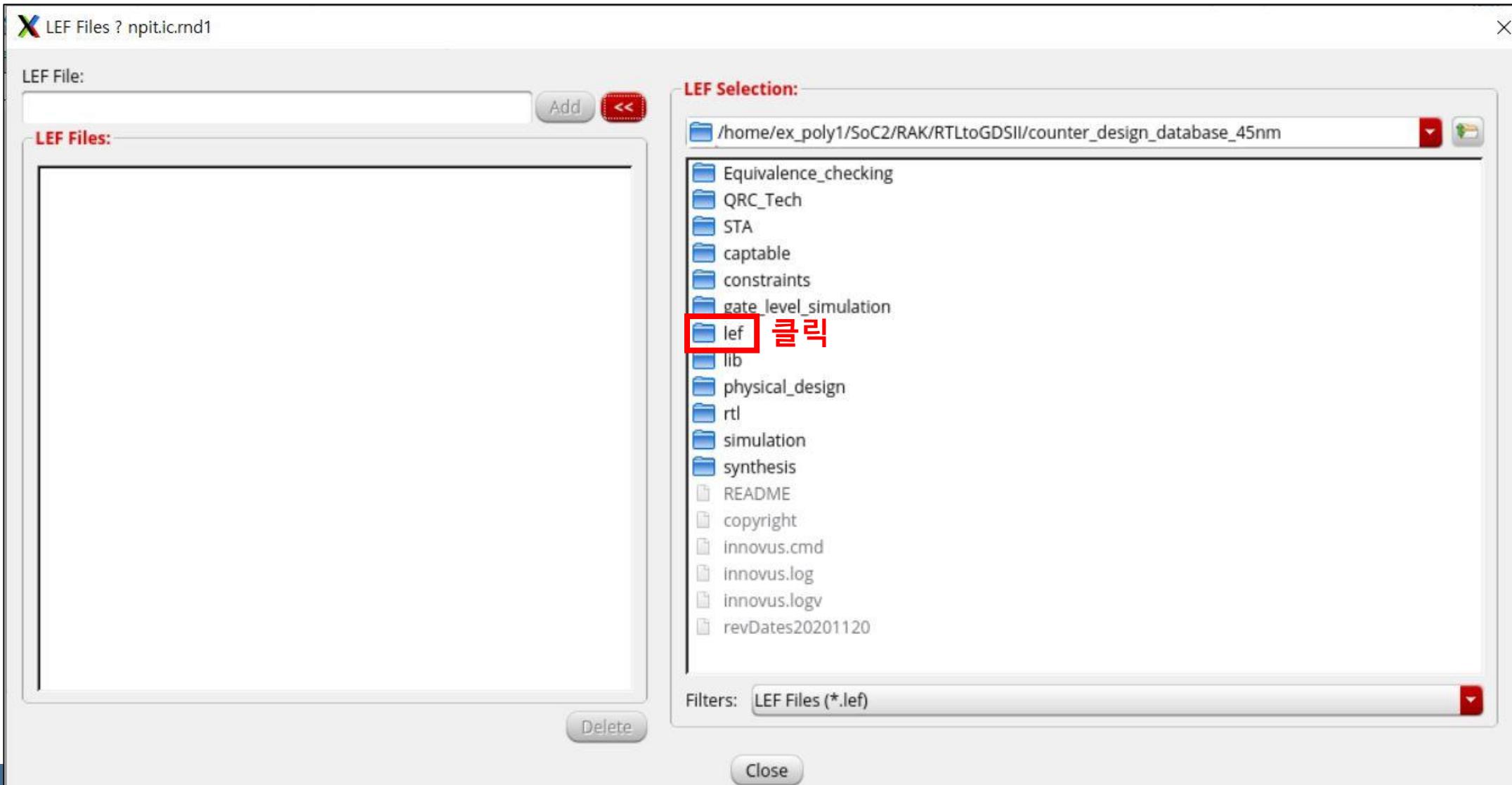
Innovus



Auto PnR

- LEF Files을 불러들임

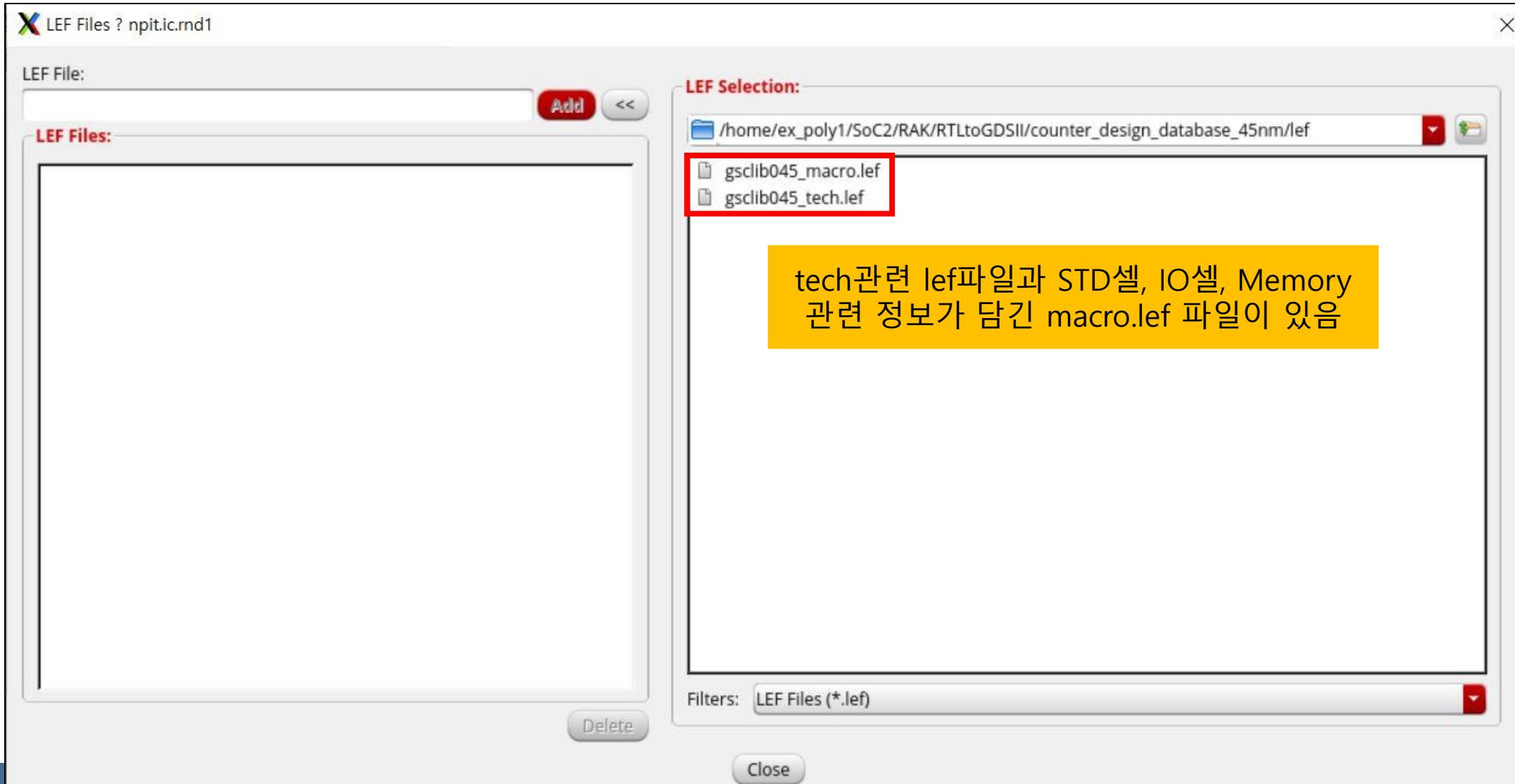
Innovus



Auto PnR

- LEF Files을 불러들임

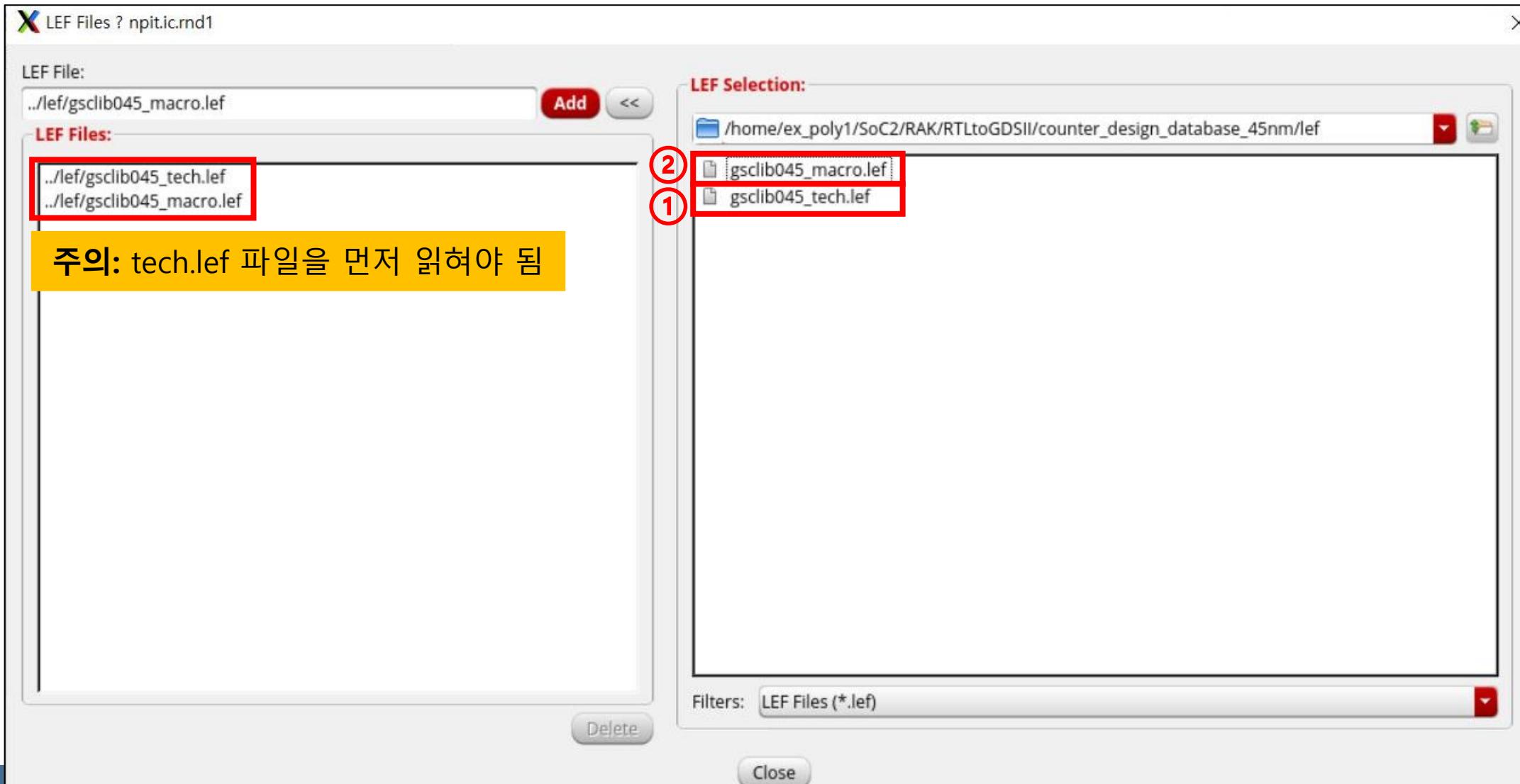
Innovus



Auto PnR

- LEF Files을 불러들임

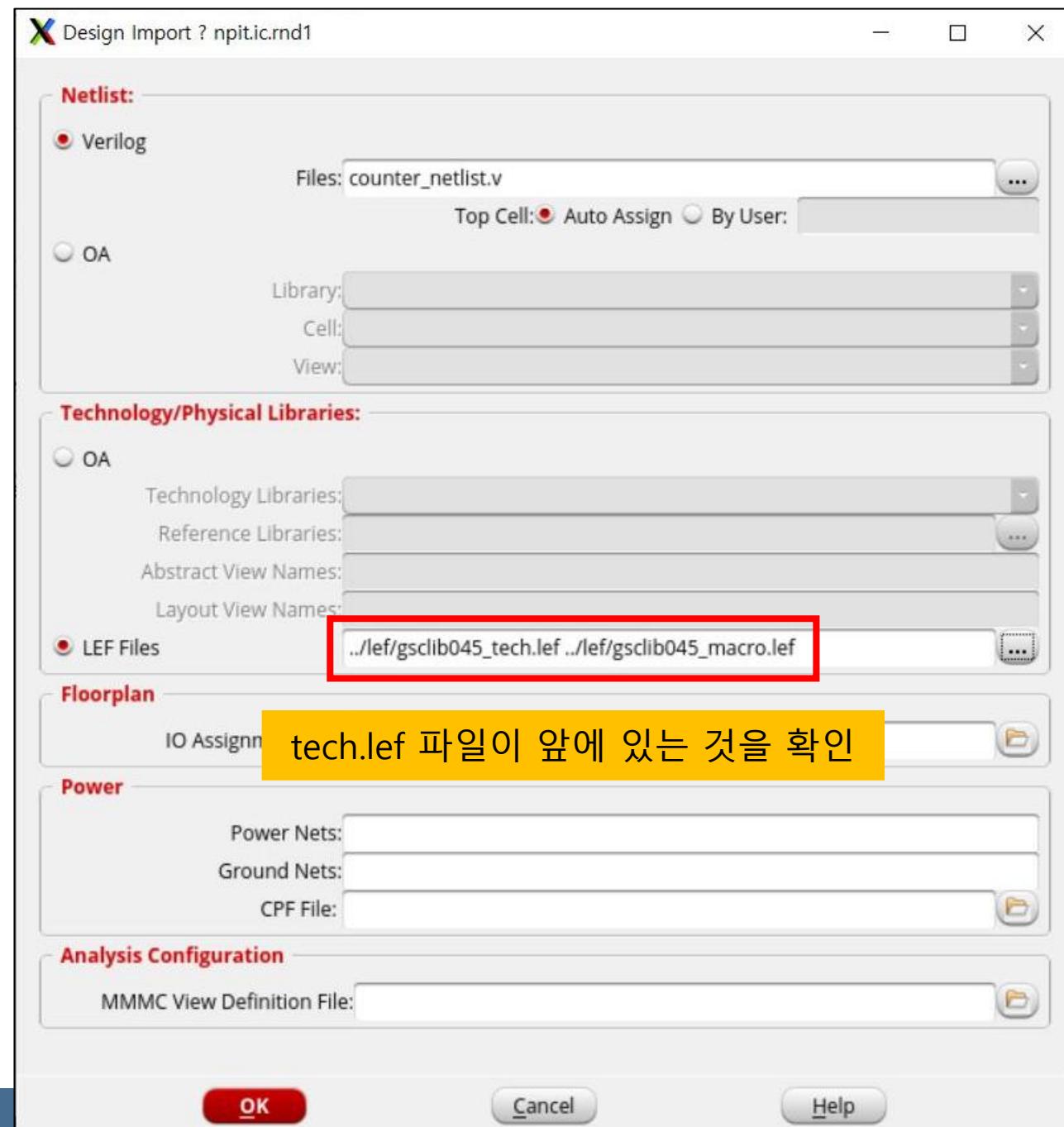
Innovus



Auto PnR

Innovus

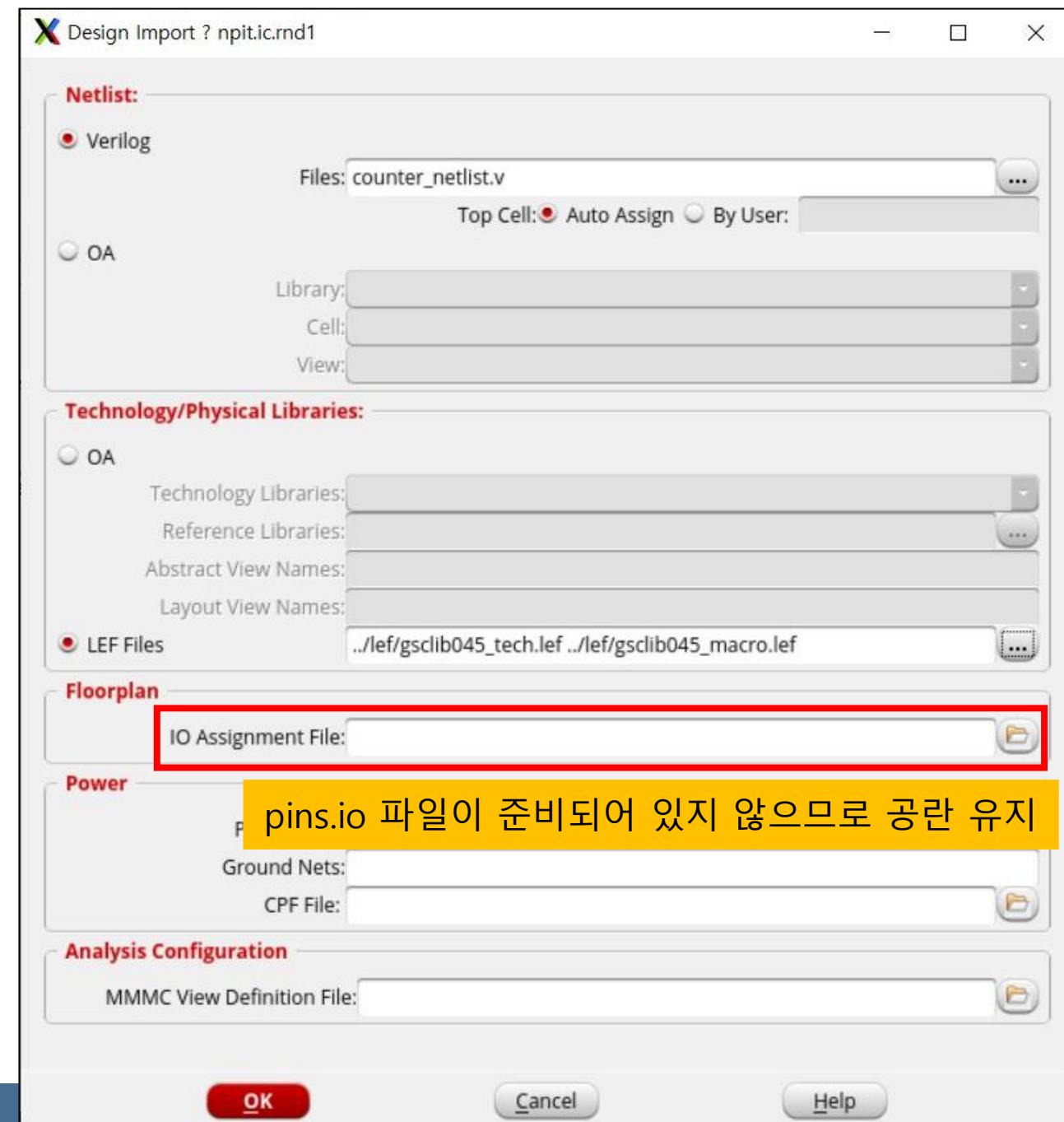
- Import Design
- LEF Files을 불러들임



Auto PnR

Innovus

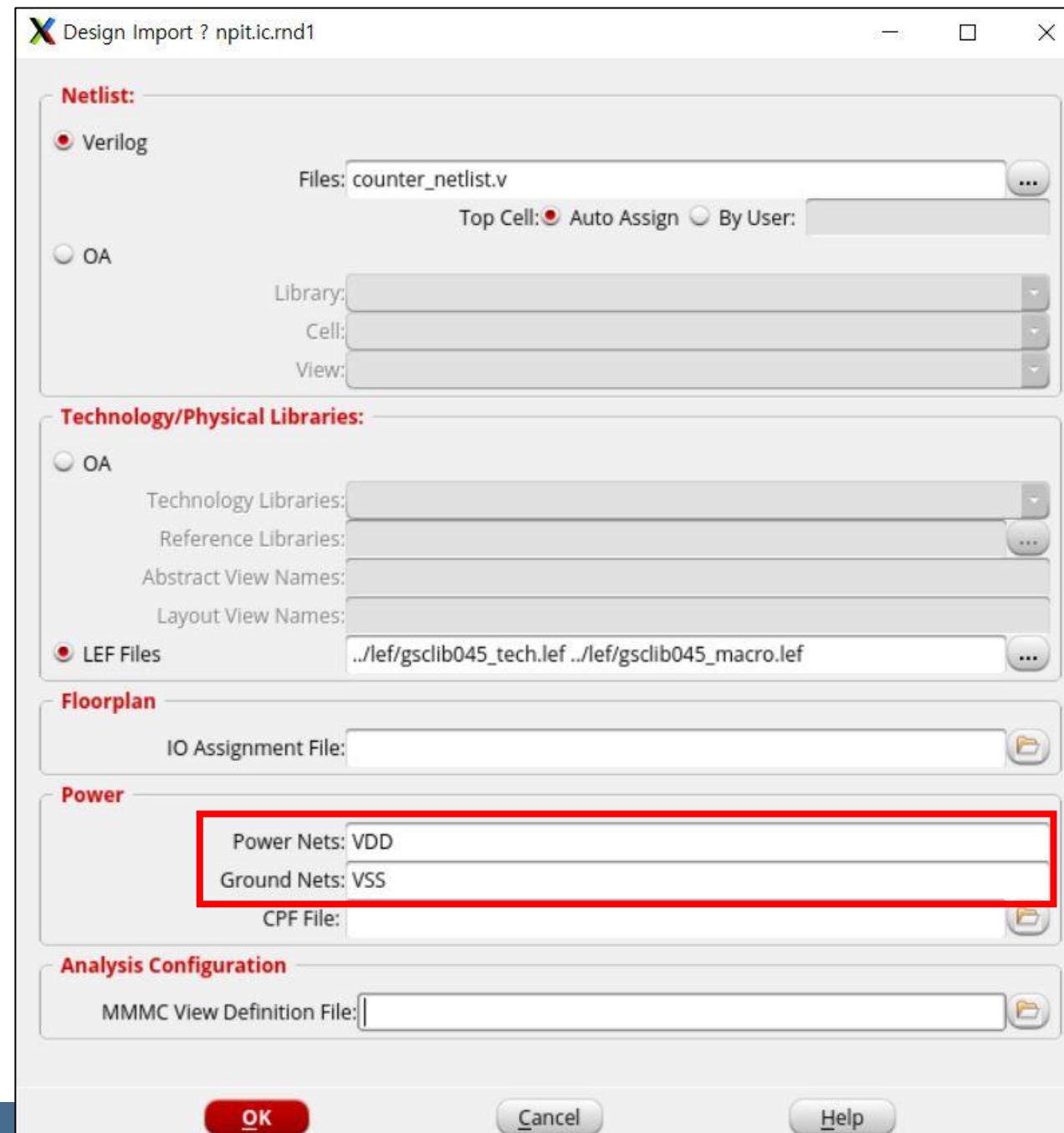
- Import Design



Auto PnR

Innovus

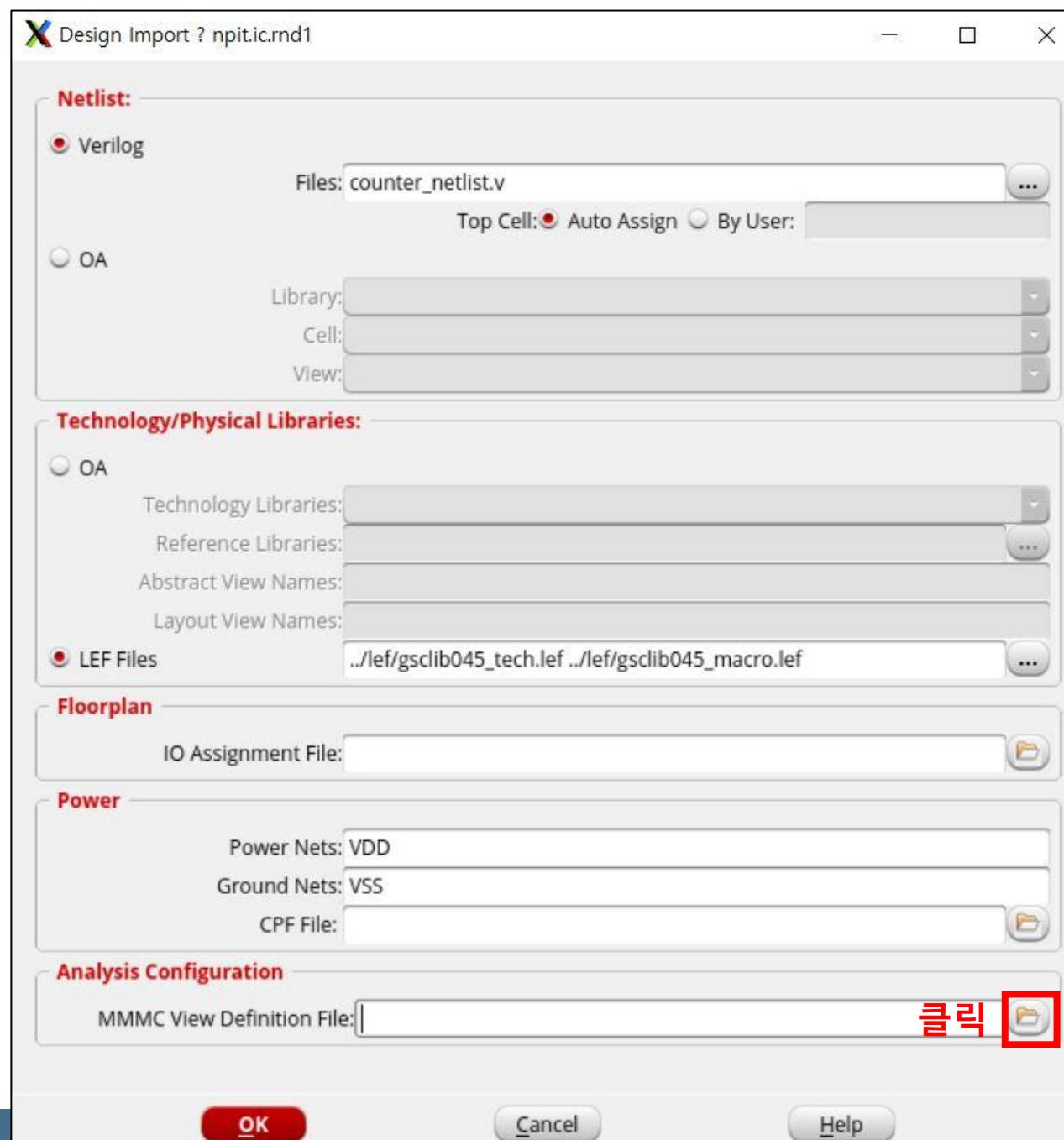
- Import Design
- Power Nets, Ground Nets에 각각 VDD, VSS 입력



Auto PnR

Innovus

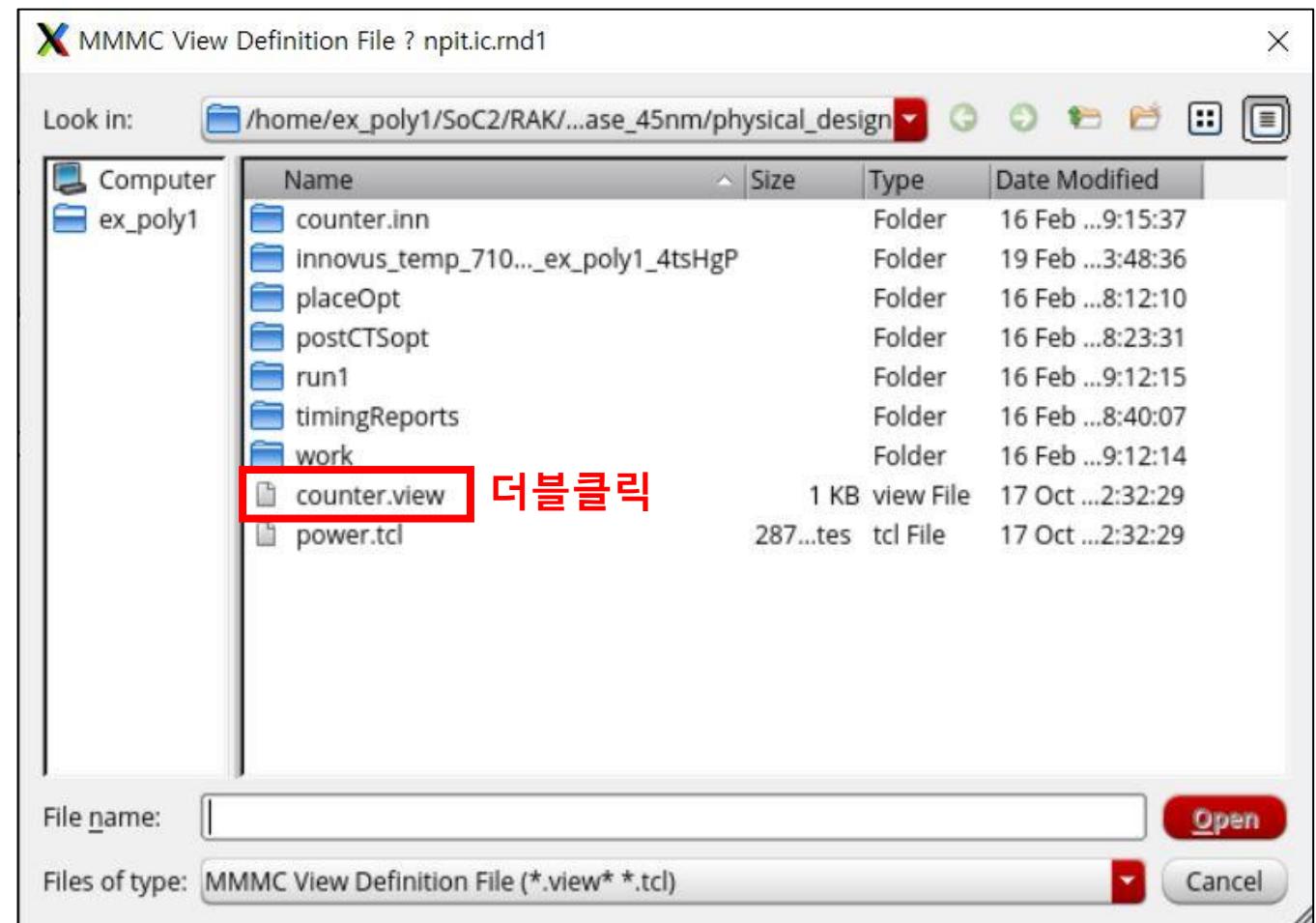
- Import Design
- Analysis Configuration



Auto PnR

Innovus

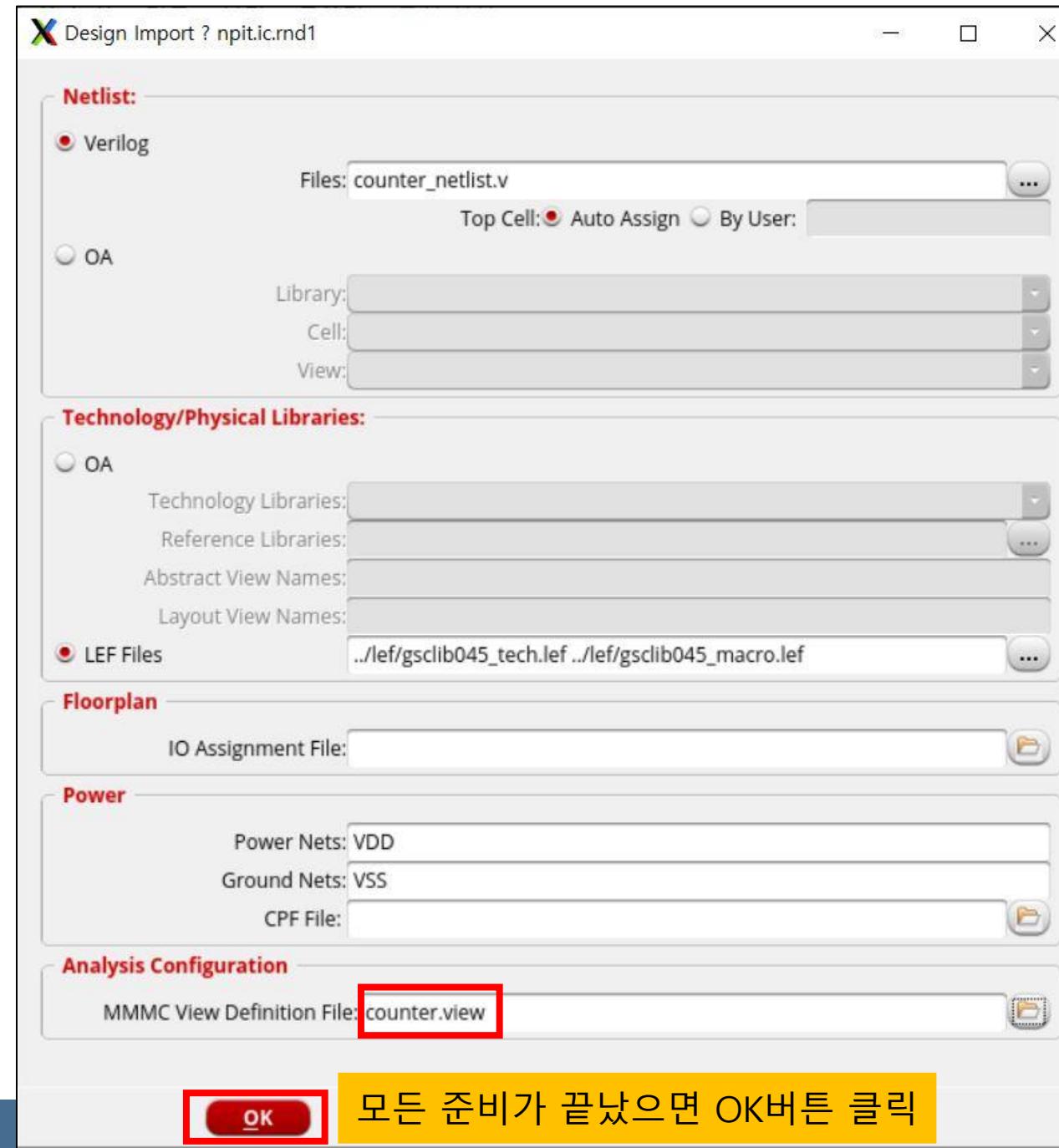
- Import Design
- Analysis Configuration



Auto PnR

Innovus

- Analysis Configuration
- 실습 진행하기 전에 확인했던 Cell delay, Net delay 관련 파일인 counter.view를 읽어 들임

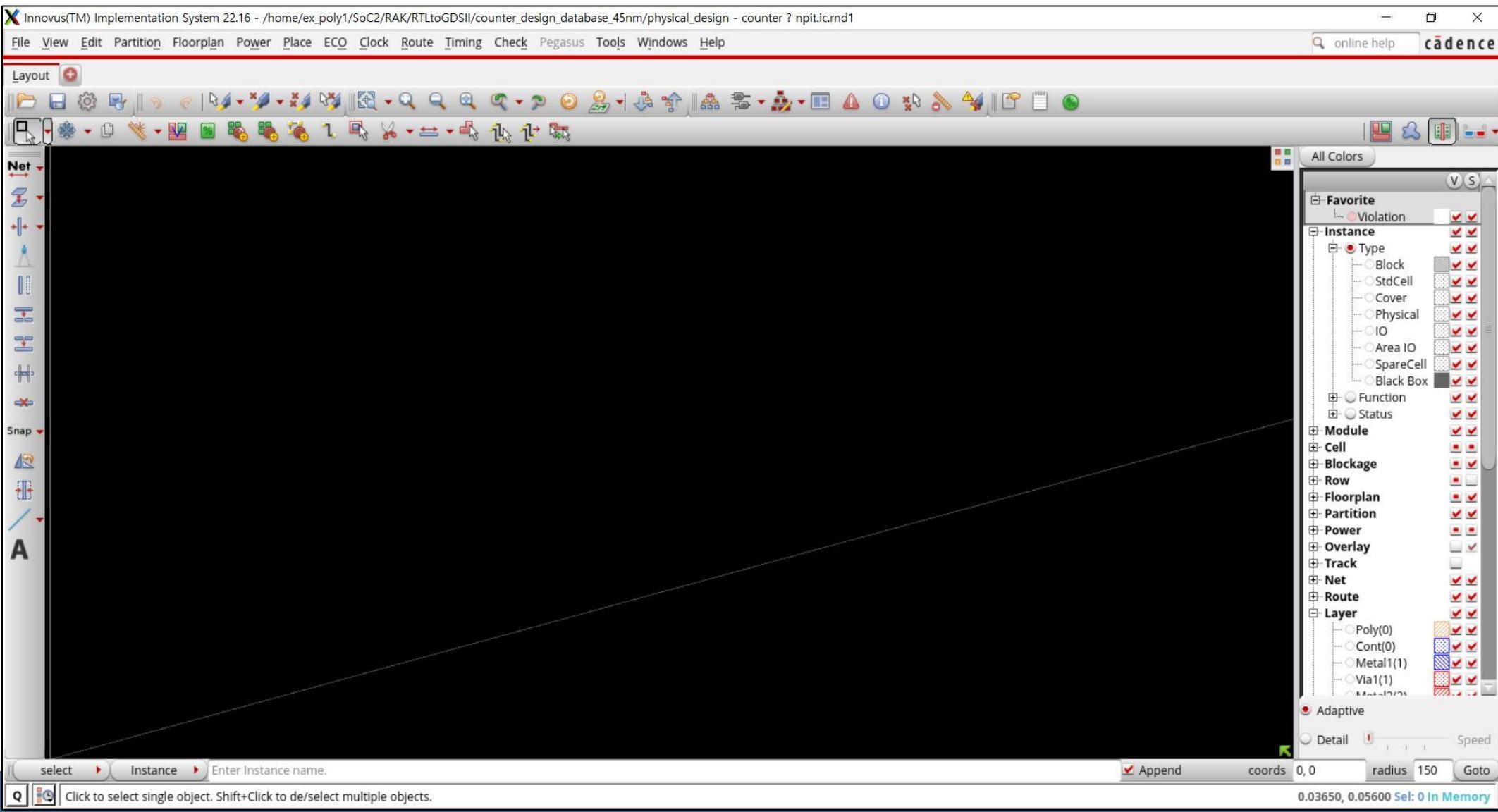


Auto PnR

Innovus

- Import Design에서 미리 준비된 파일을 불러온 상태임

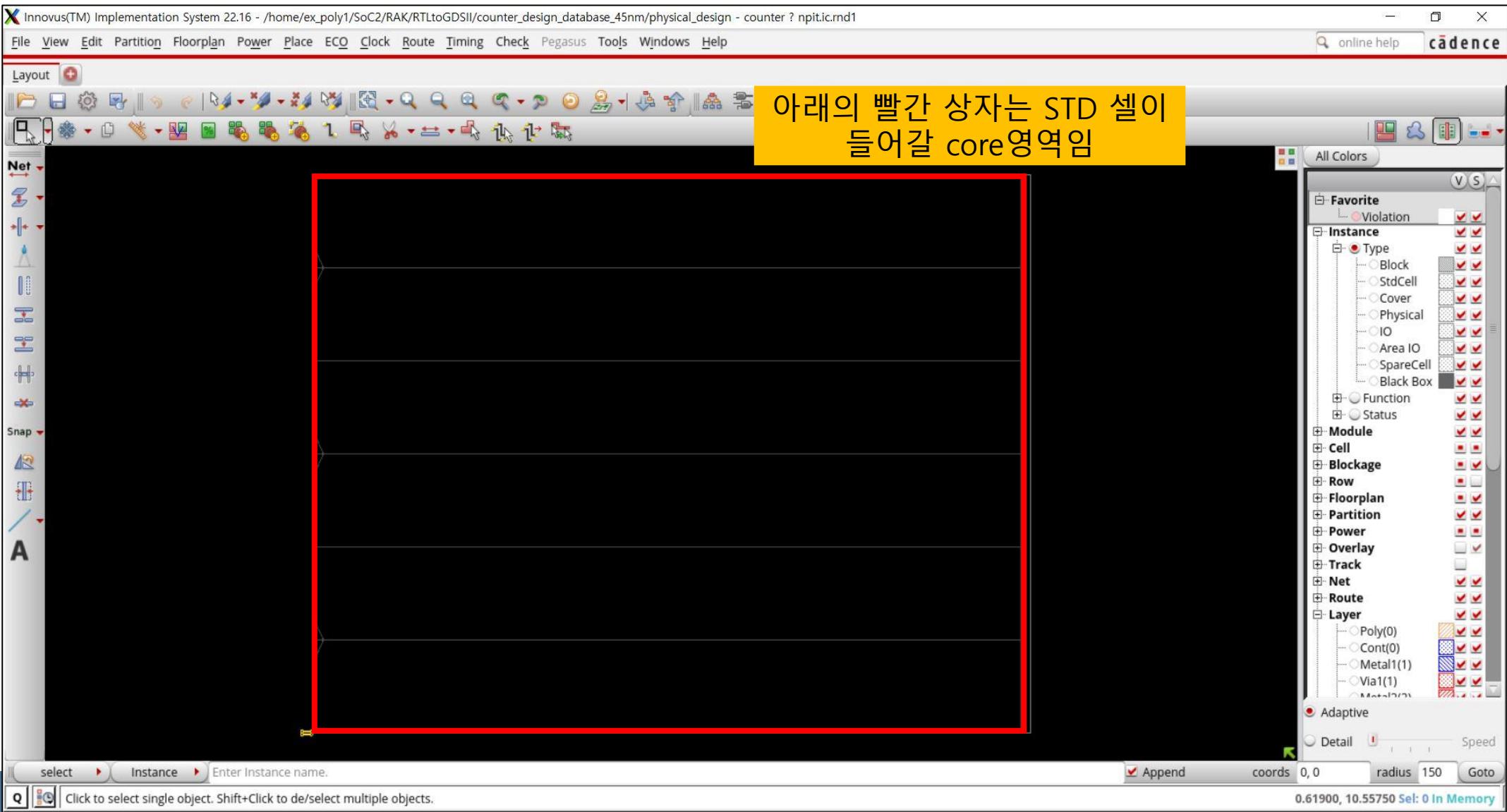
- 단축기 f



Auto PnR

Innovus

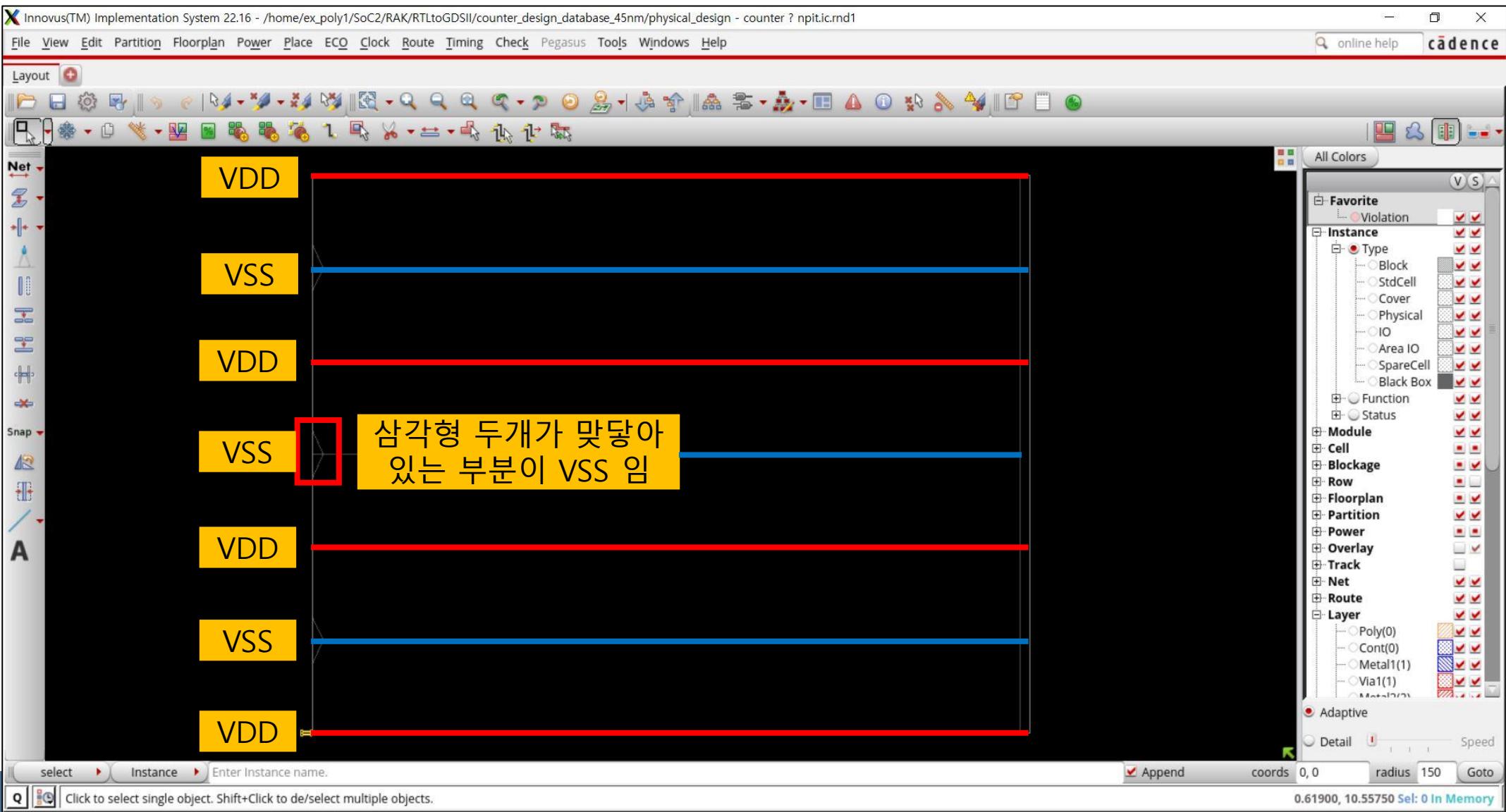
- Double Back을 확인함



Auto PnR

Innovus

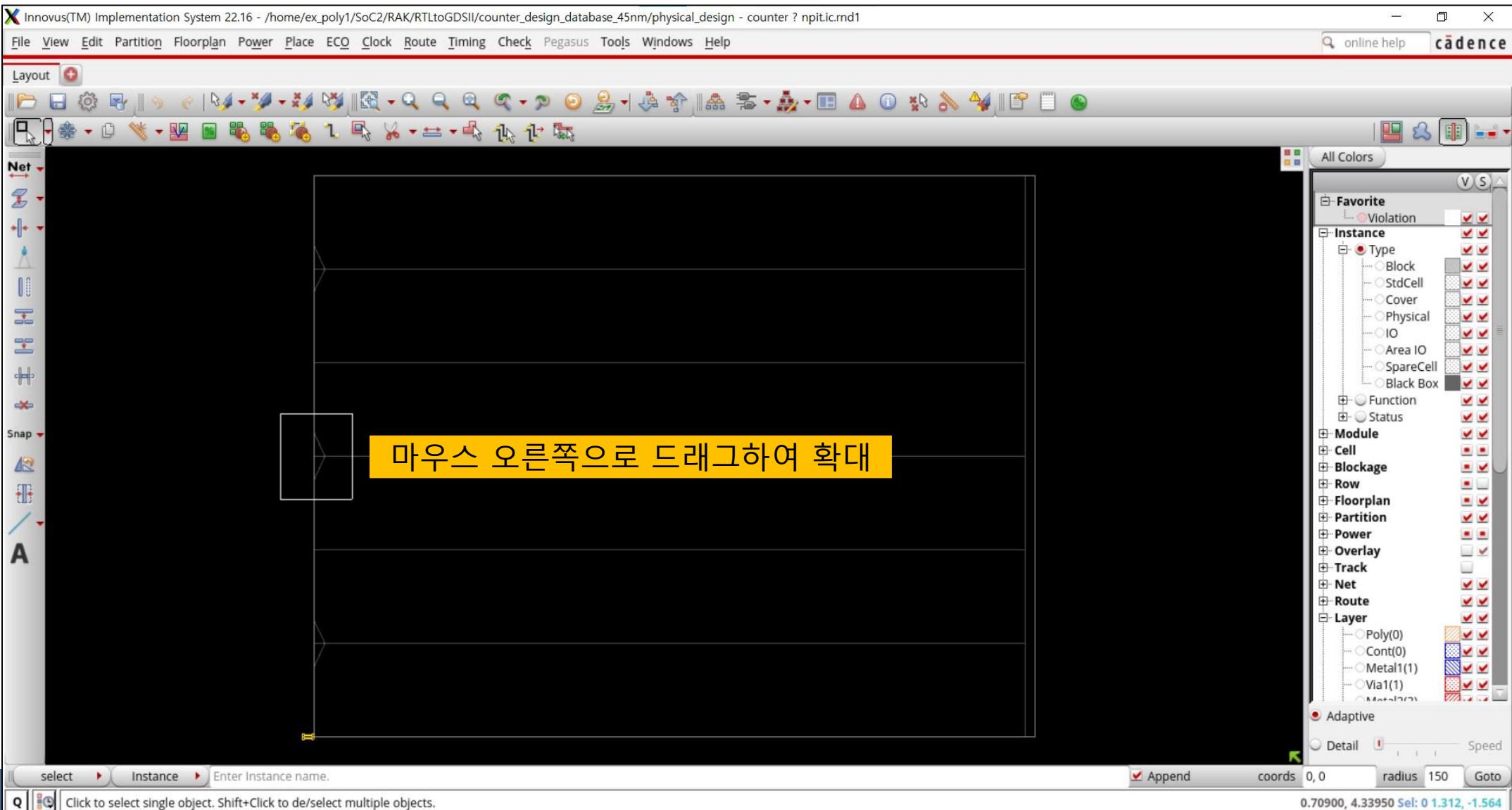
- Double Back을 확인함



Auto PnR

Innovus

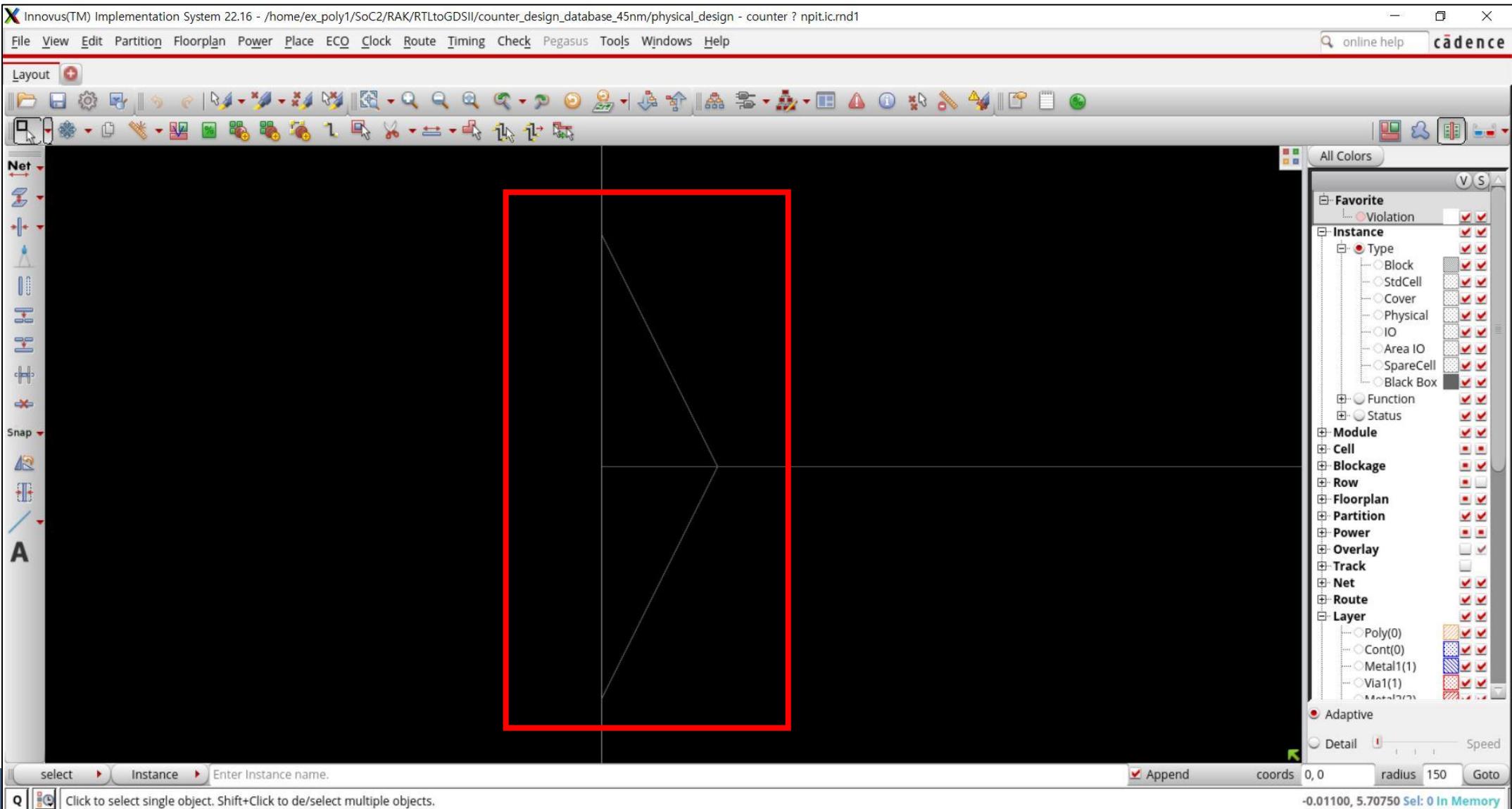
- Double Back을 확인함



Auto PnR

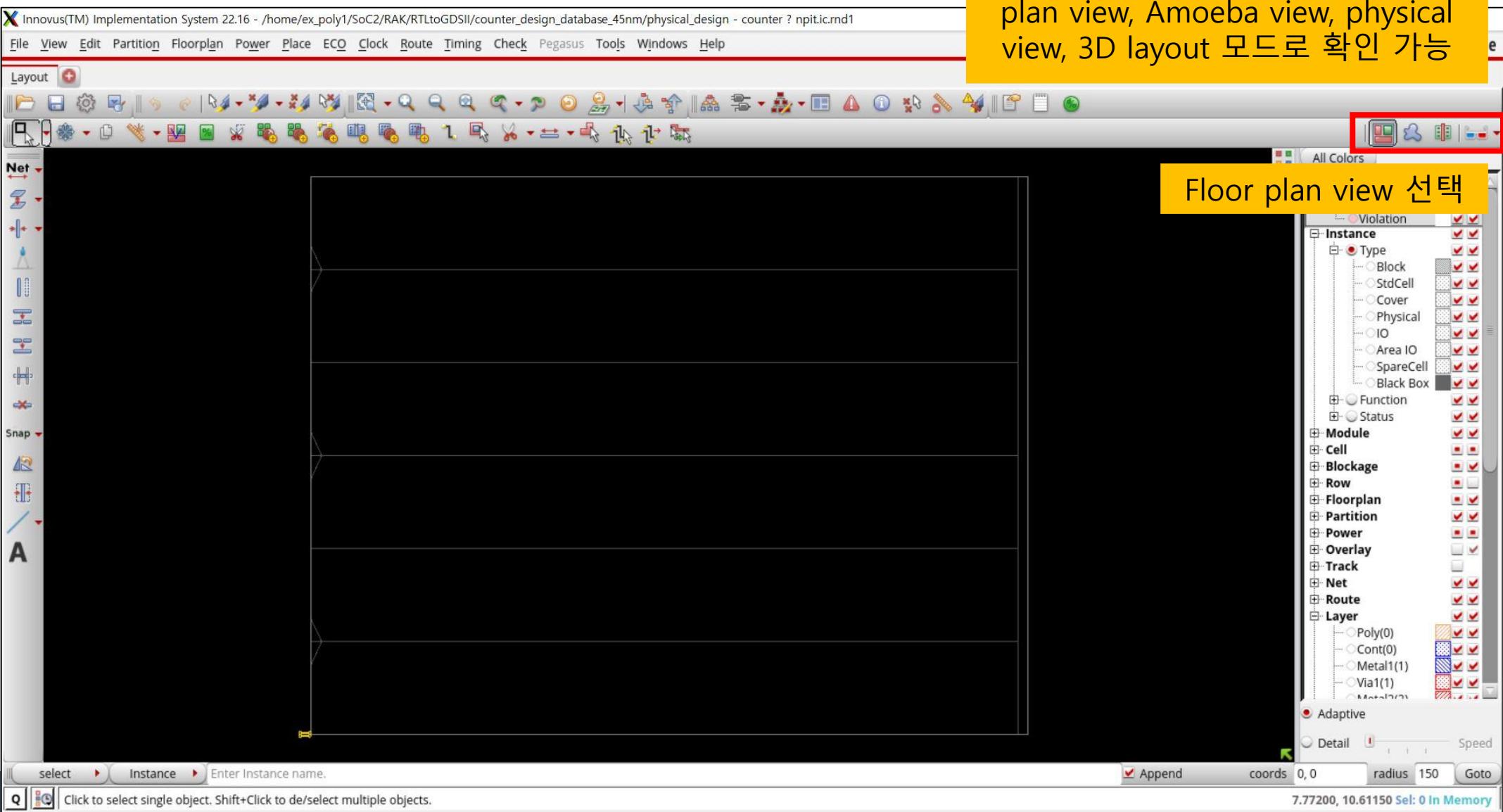
Innovus

- Double Back0I 잘 형성된 것을 확인함



Auto PnR

Innovus



Auto PnR

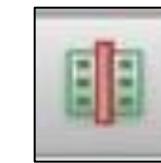
Innovus



Floor plan view



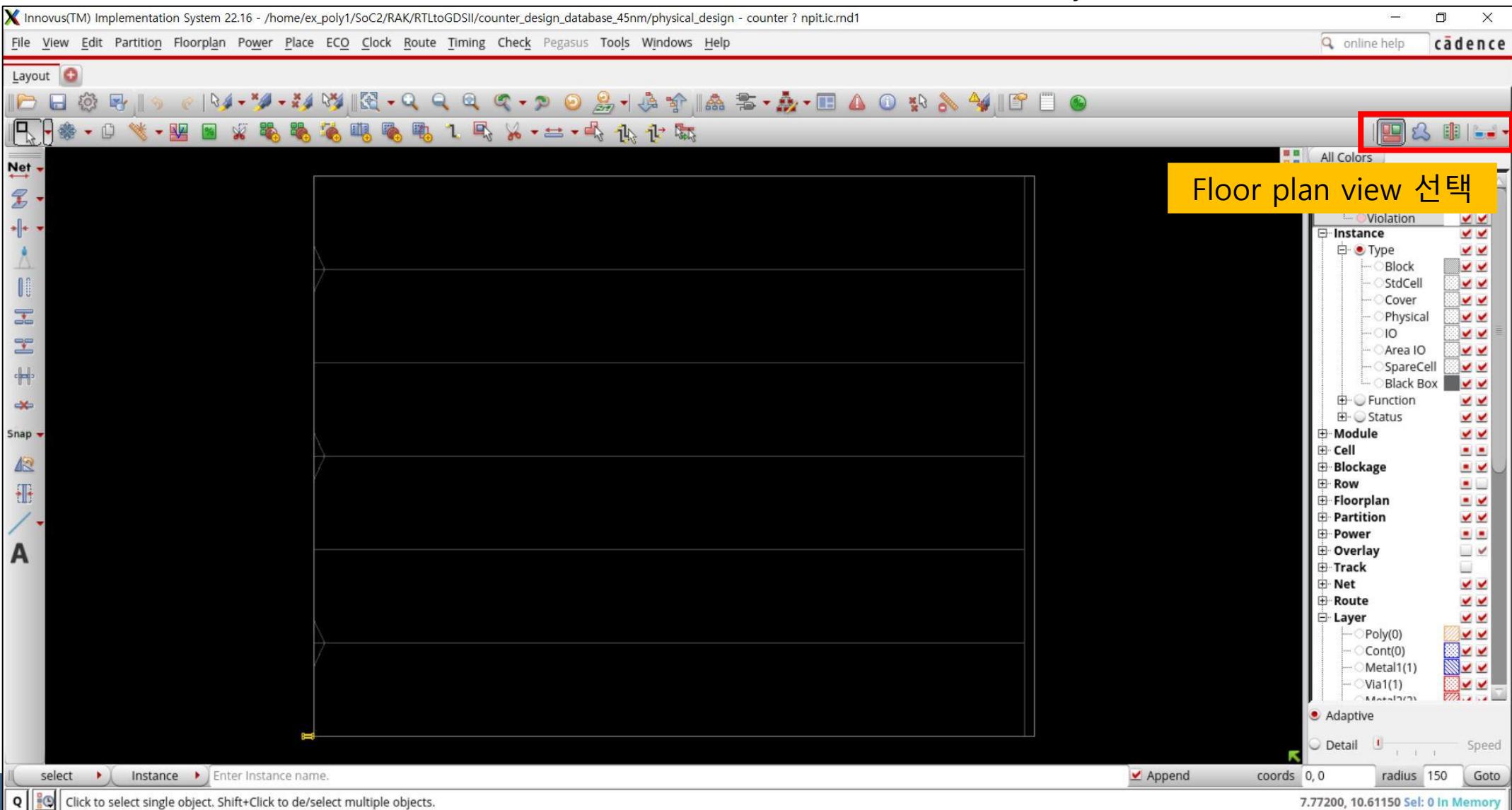
Amoeba view



physical view



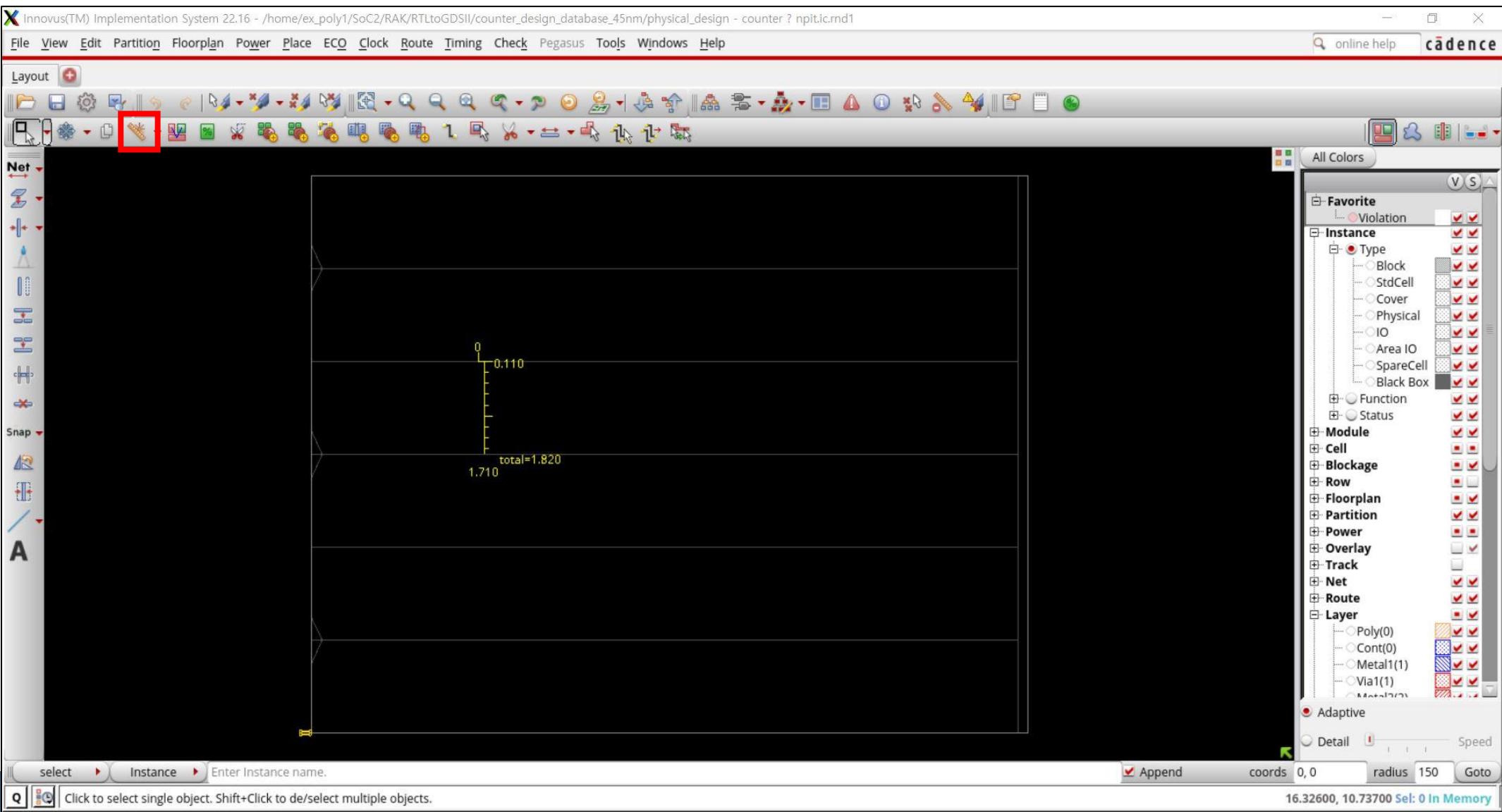
3D layout



Auto PnR

Innovus

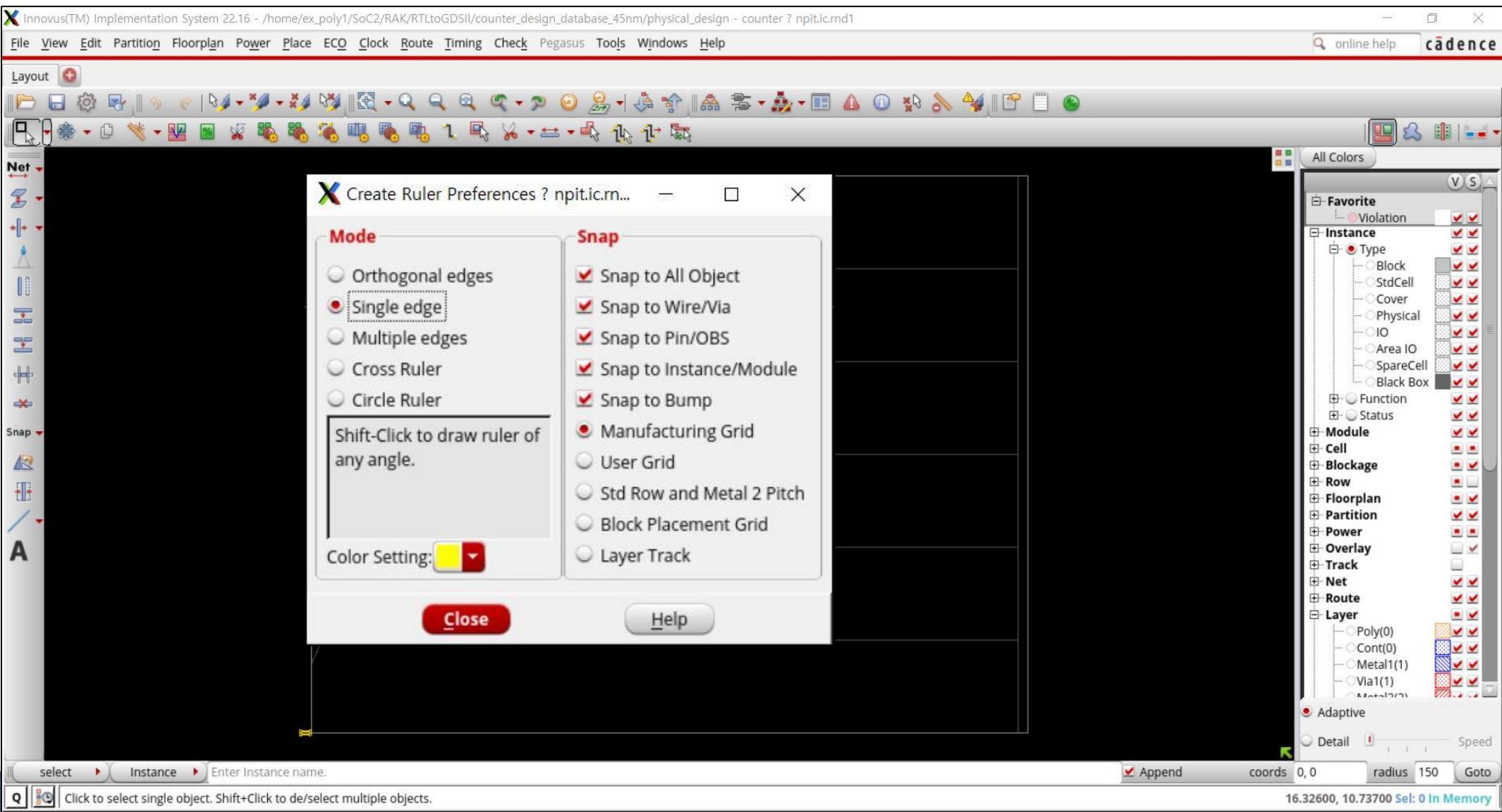
- Ruler 기능 확인
- 단축기 k 사용 또는 빨간 상자 클릭



Auto PnR

Innovus

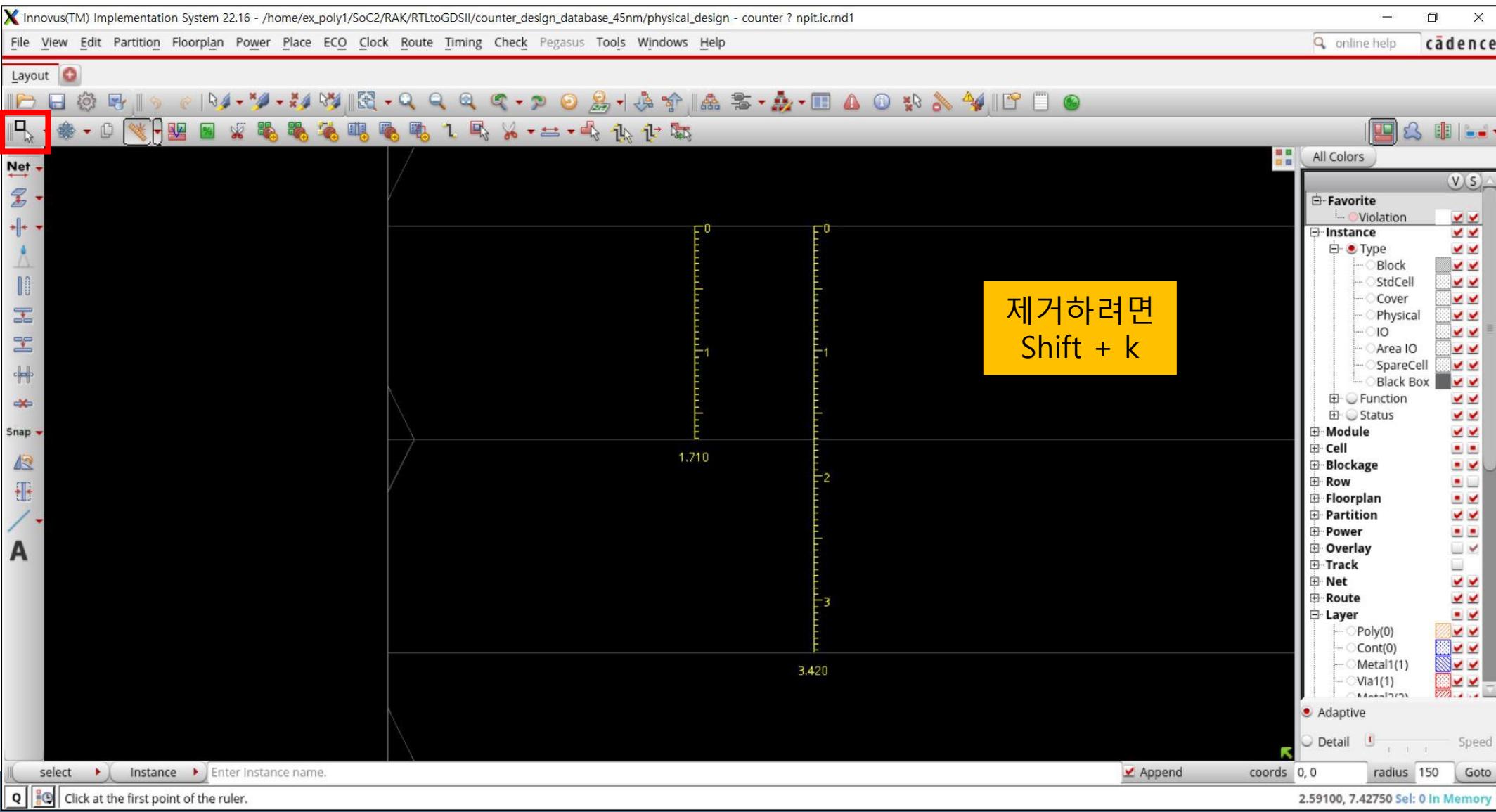
- Ruler 기능 확인
- F3을 눌러 Single edge 클릭하면 길이를 더 직관적으로 볼 수 있음



Auto PnR

Innovus

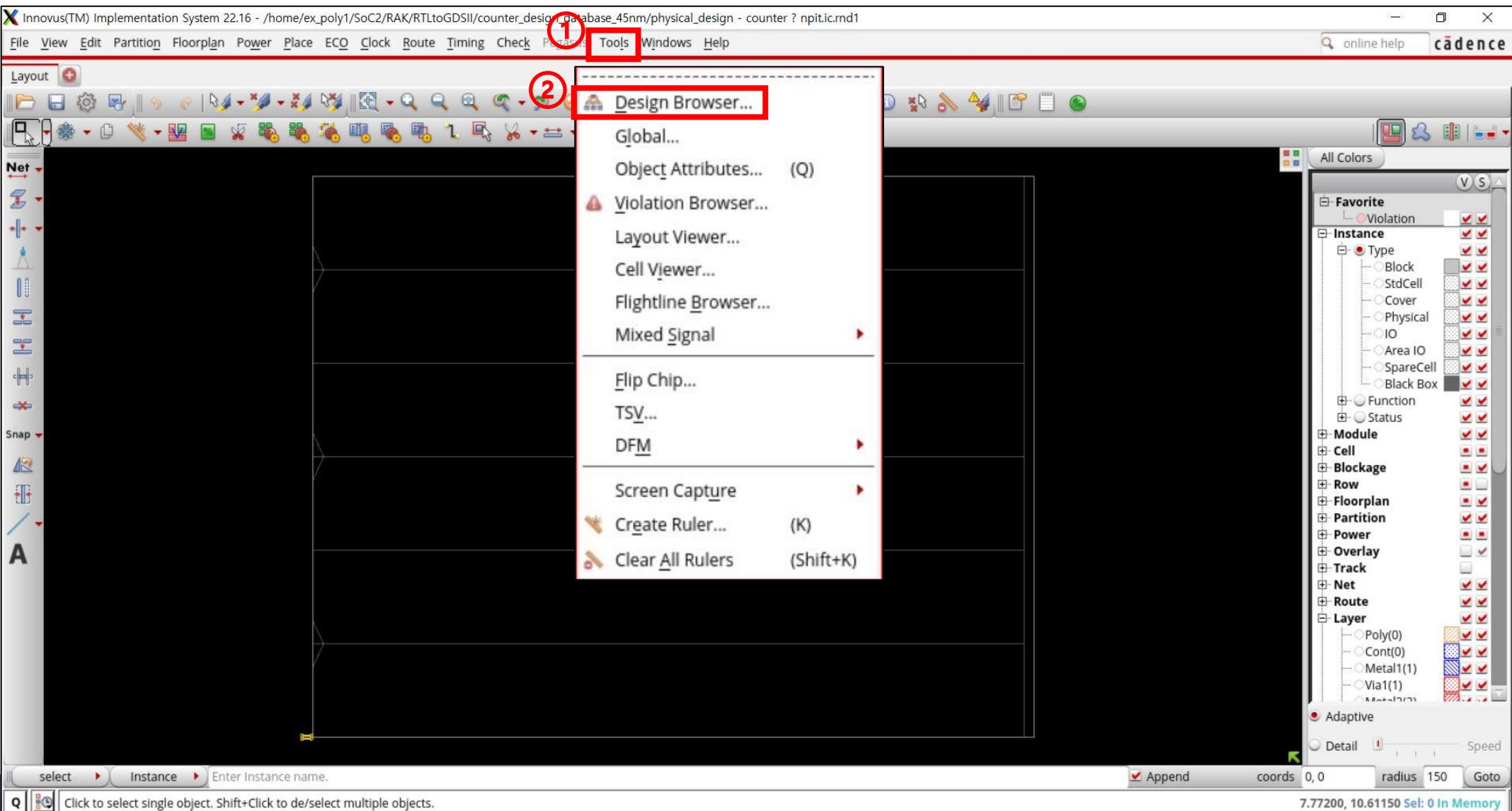
- Ruler 기능 확인
- 원하는 길이 측정 후 빨간 상자를 클릭하여 자 해제



Auto PnR

Innovus

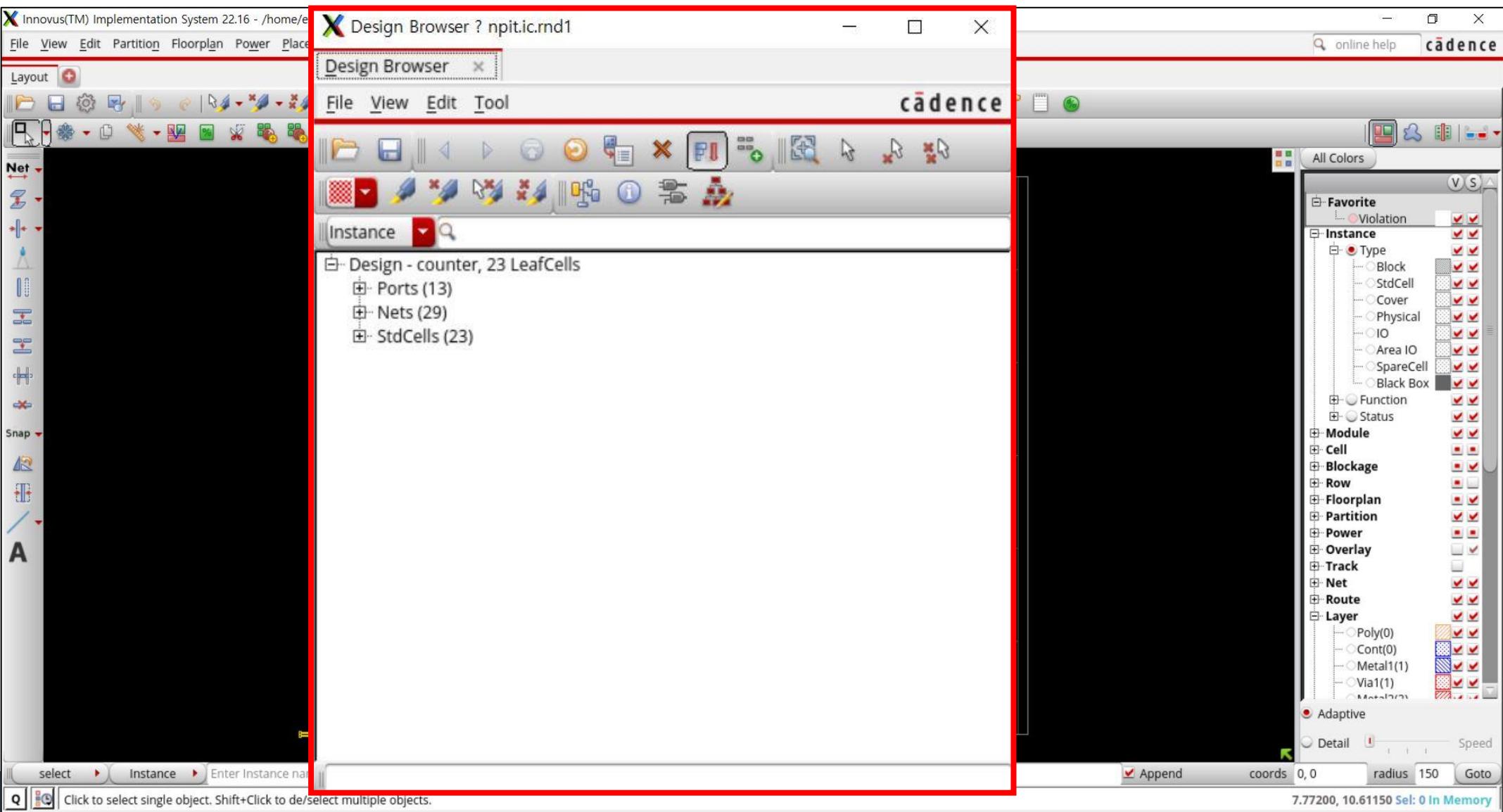
- Design Browser... 확인



Auto PnR

Innovus

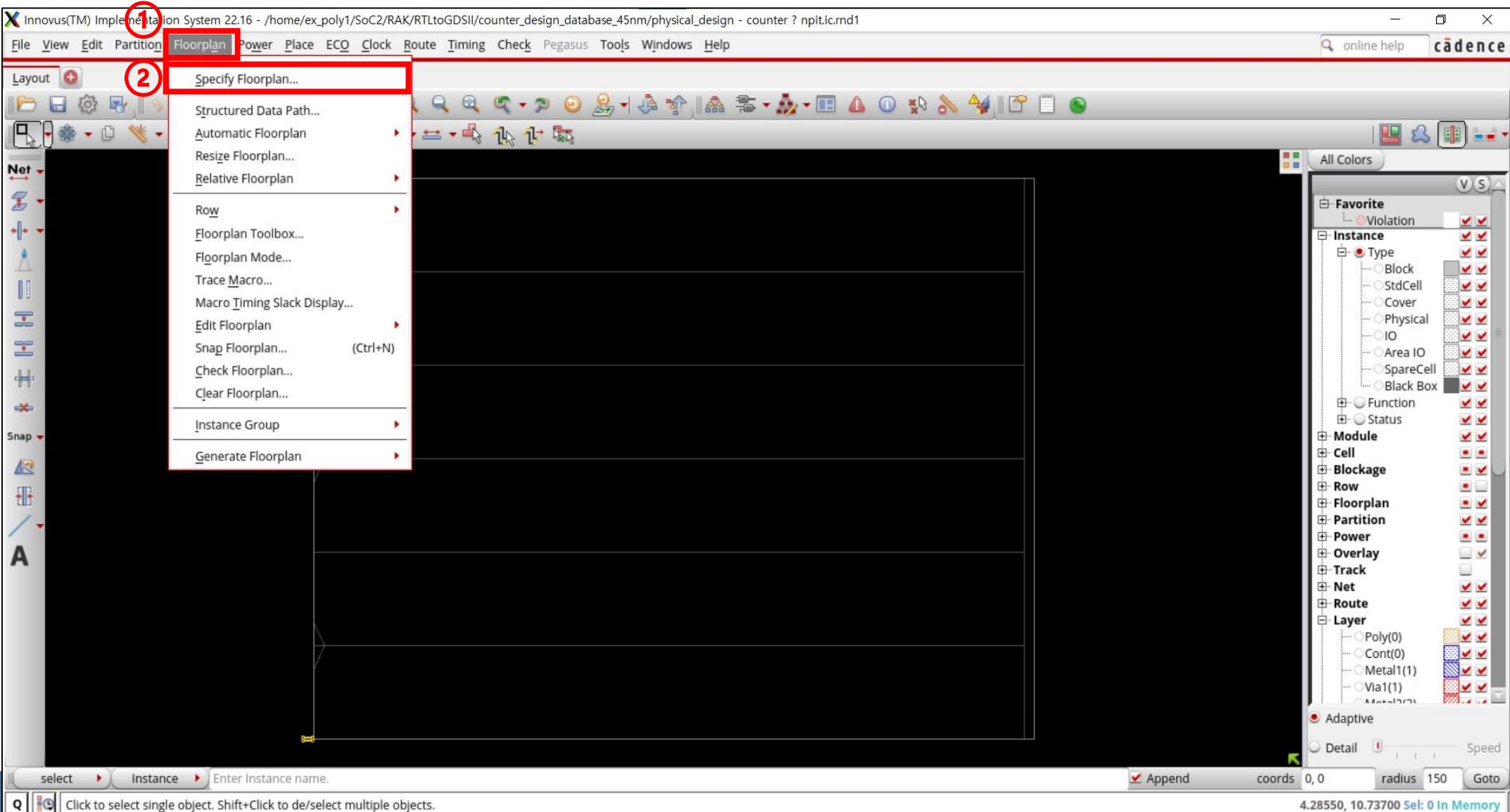
- Design Browser... 확인



Auto PnR

Innovus

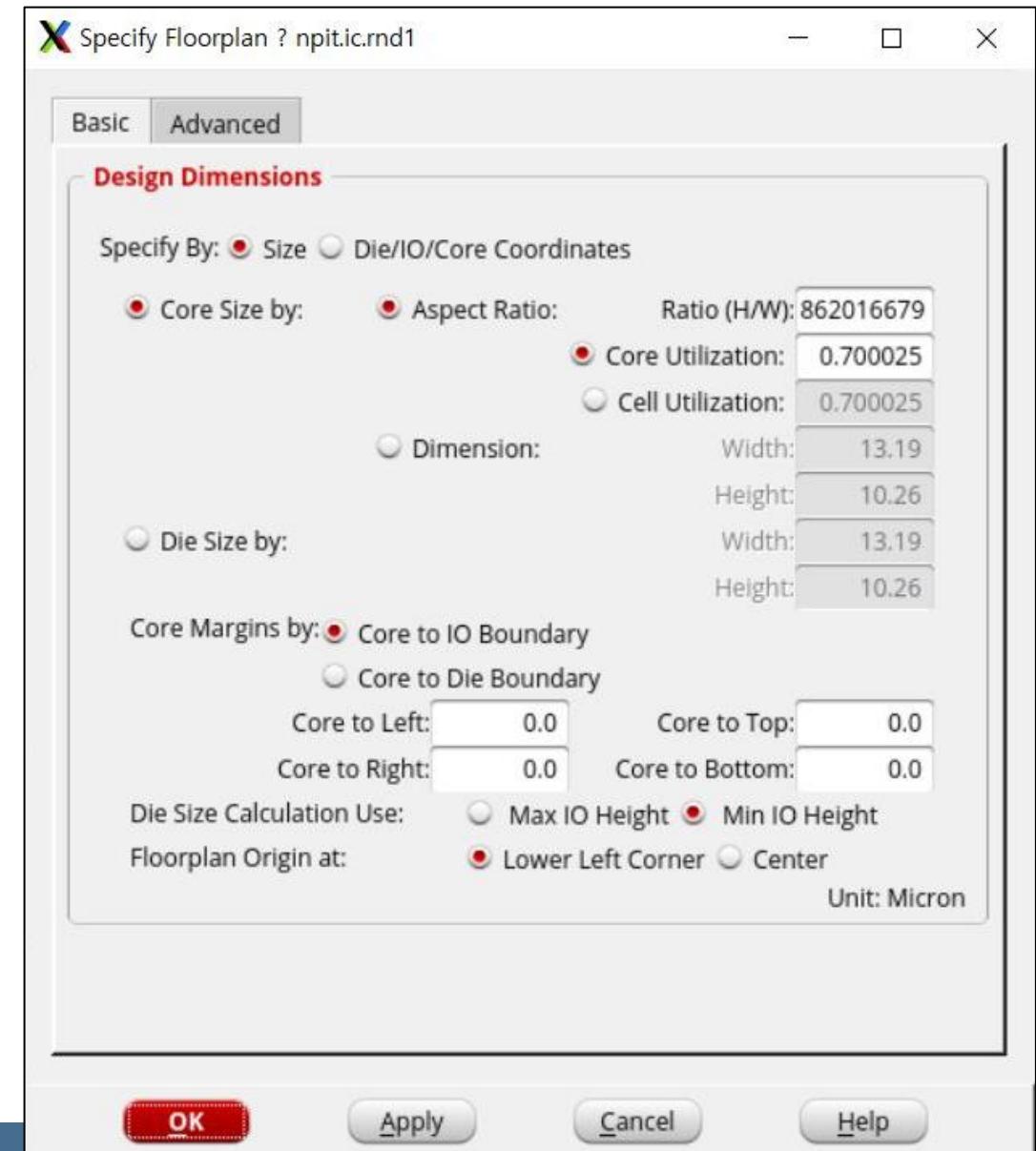
- Floor planning the Design



Auto PnR

Innovus

- Floor planning the Design



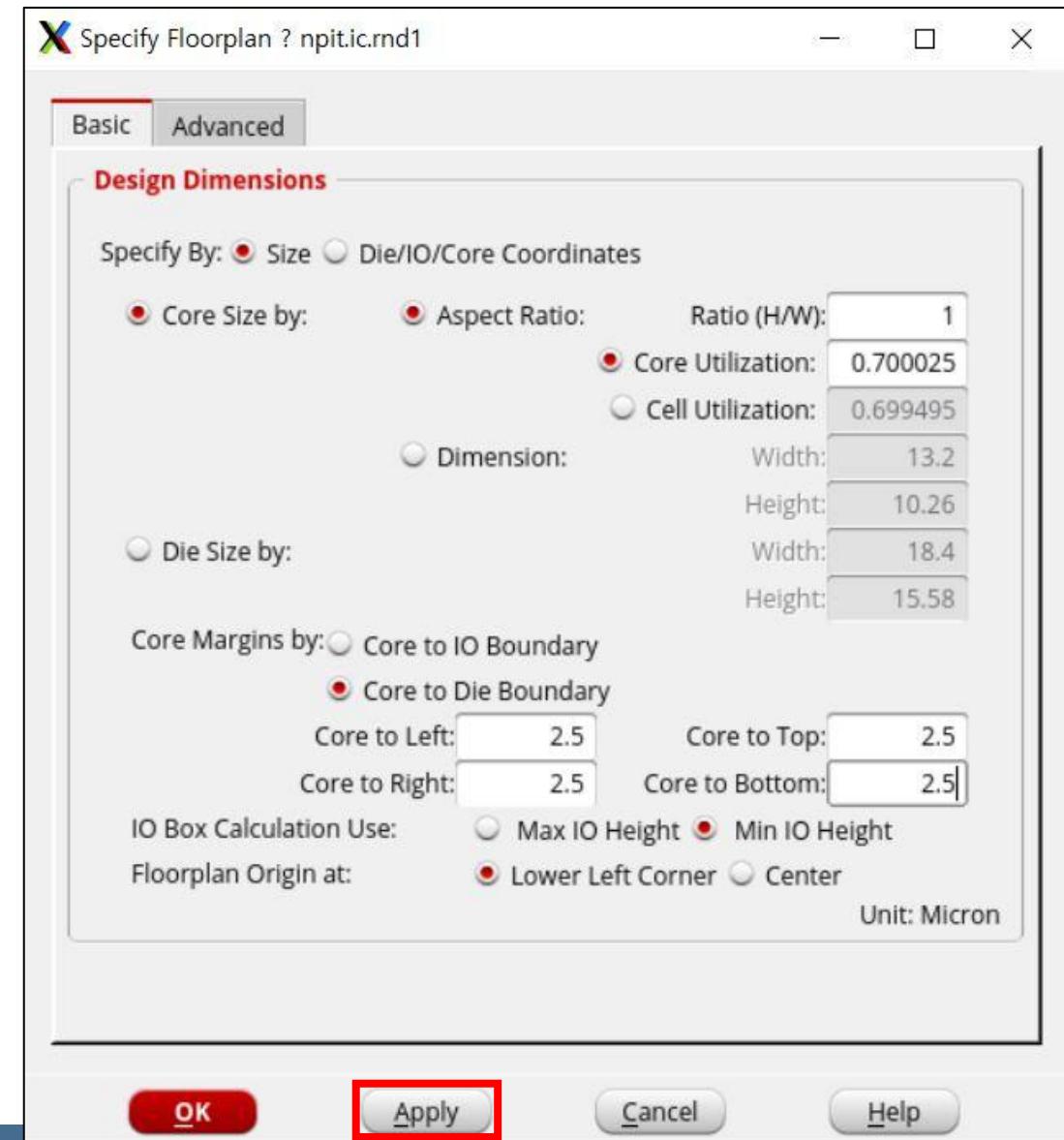
- Floorplan을 위한 설정
- Specify Floorplan 창 확인

Auto PnR

Innovus

- Floor planning the Design

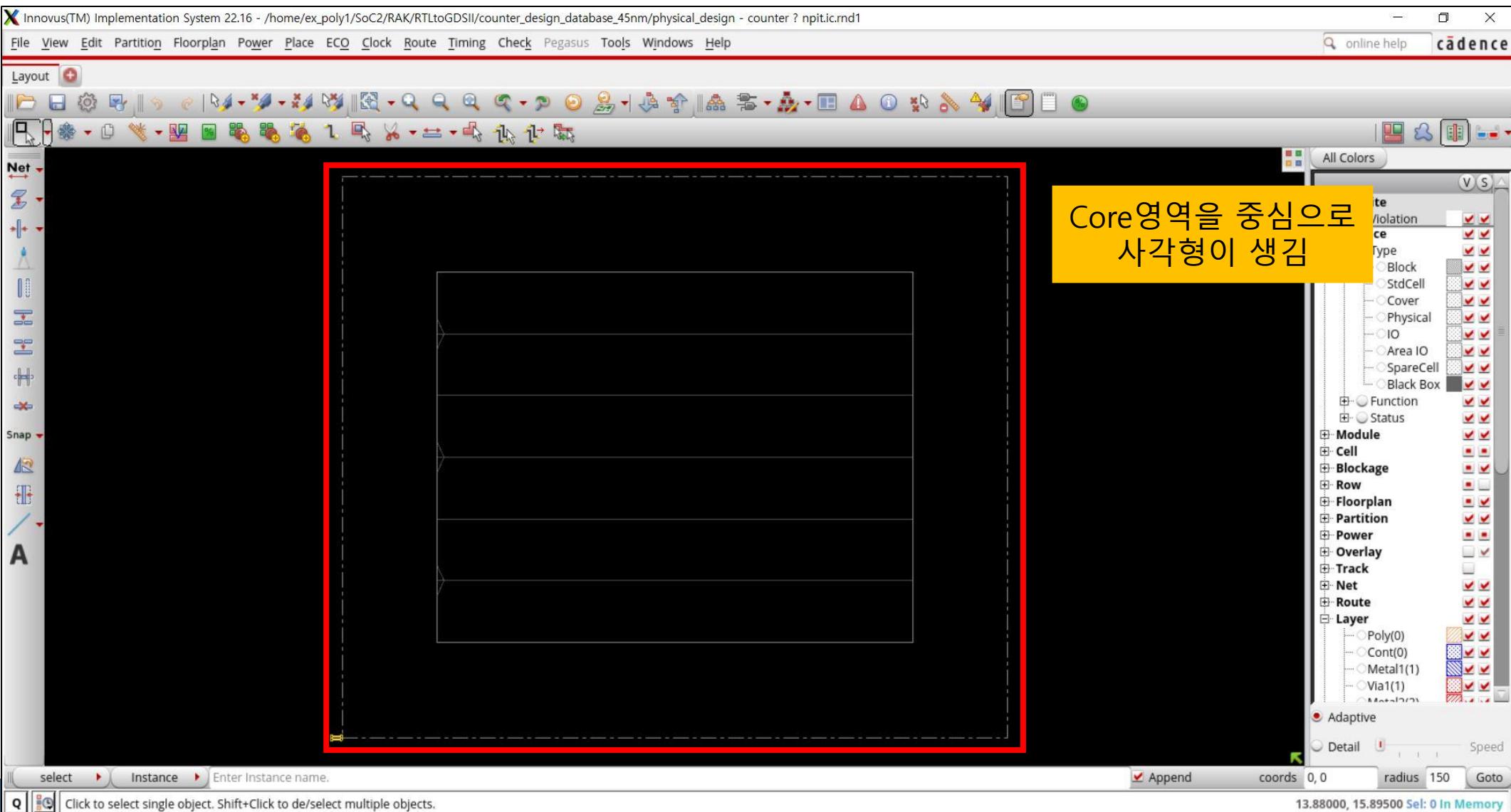
- 오른쪽 그림과 같이 설정한 후 Apply 클릭



Auto PnR

Innovus

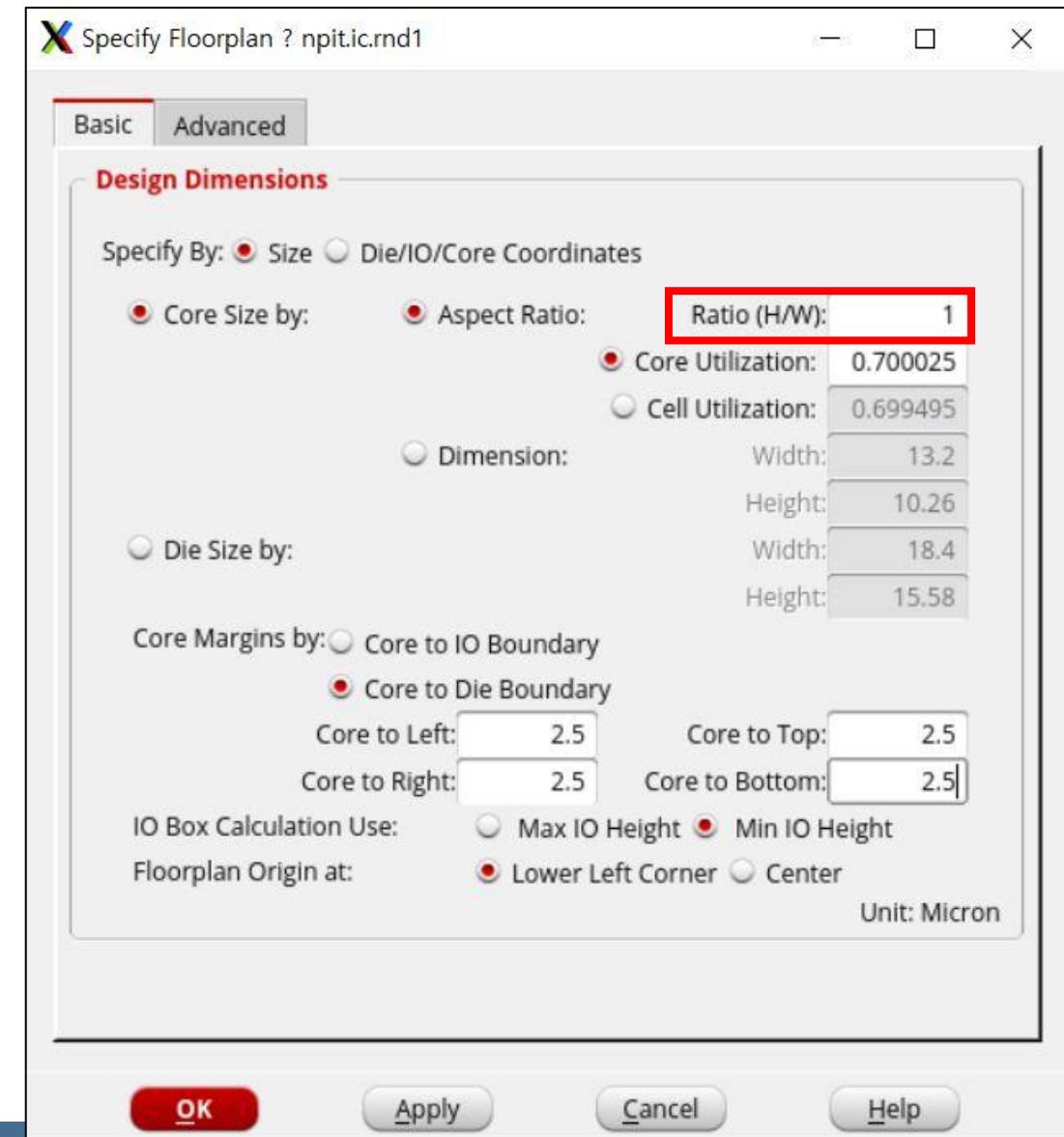
- Floor planning the Design



Auto PnR

Innovus

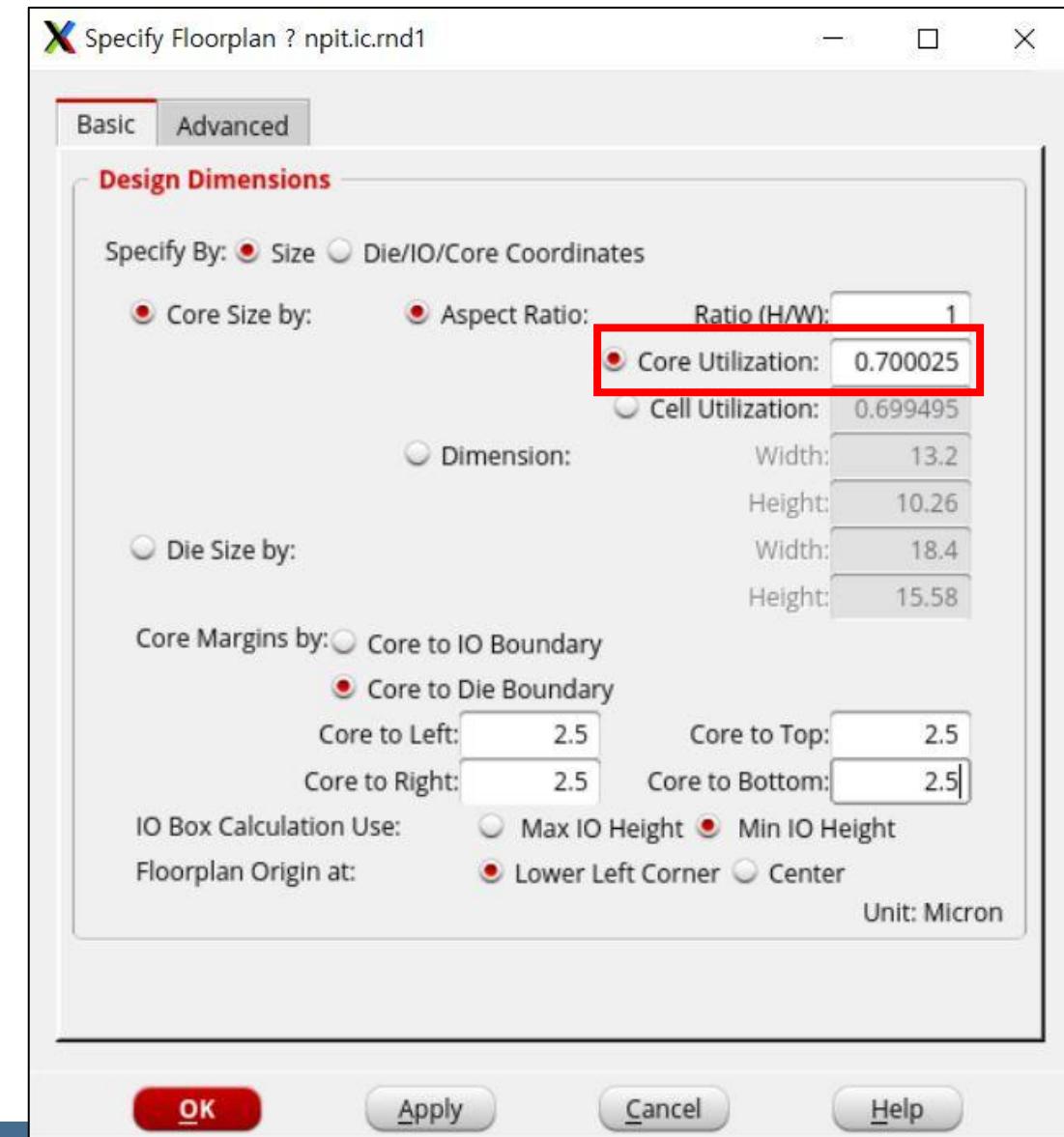
- Ratio(Height/Width)가 1이므로 정사각형으로 만든다는 의미임



Auto PnR

Innovus

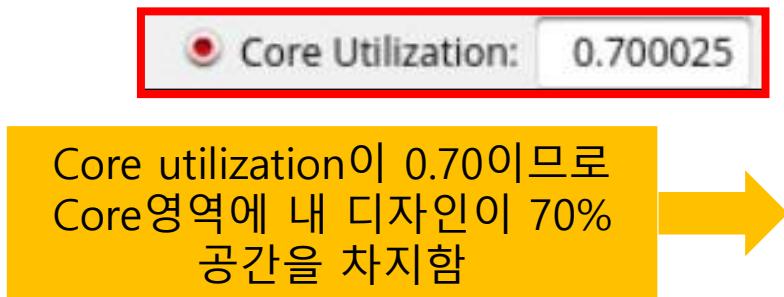
- Core Utilization이 0.70임



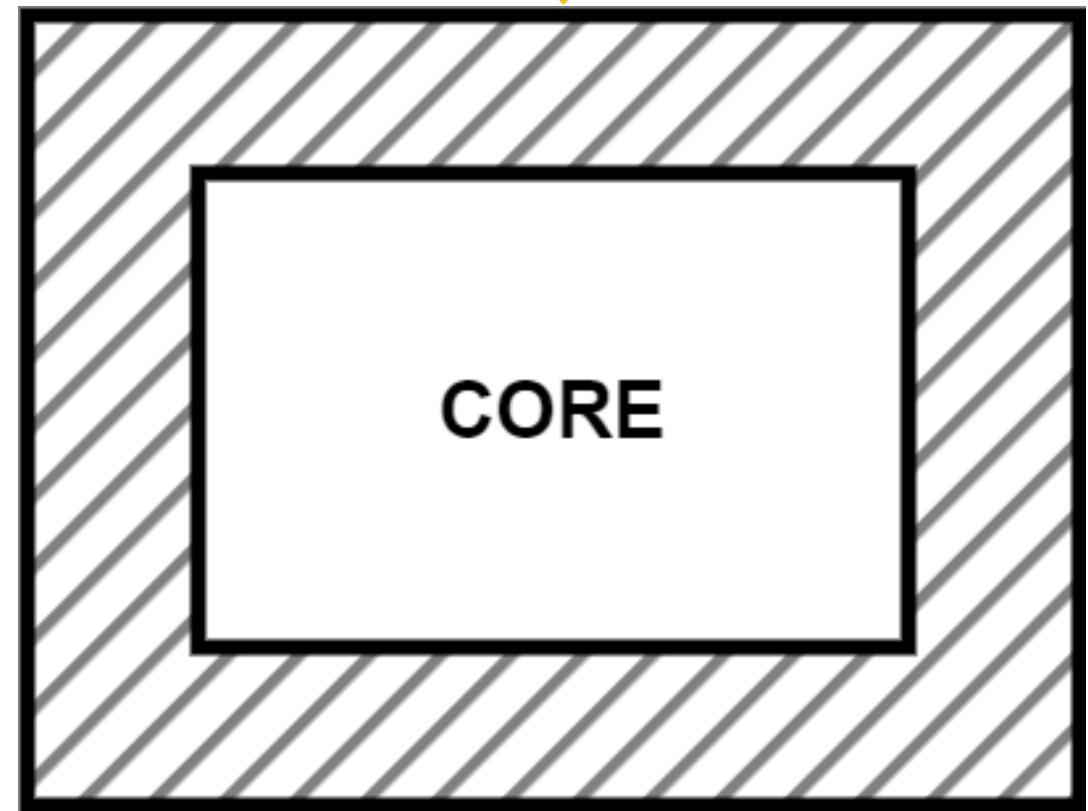
Auto PnR

Innovus

- Utilization이란?
- 총 크기에서 내 디자인을 위해 땅을 얼마나 설정해줄 것인가



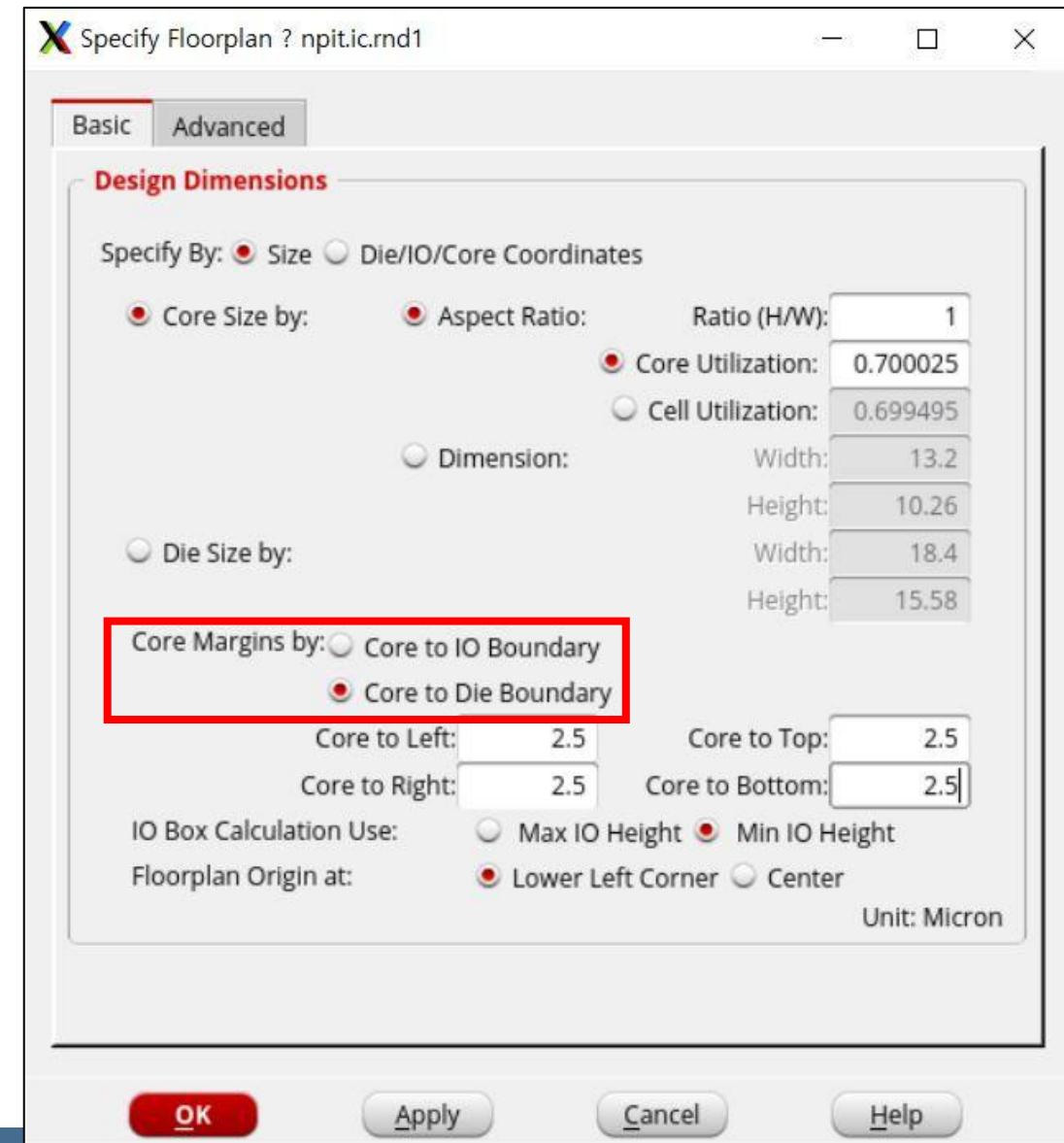
30%는 Rectangular ring 배치와 hold time violation 을 대비한 잉여공간임



Auto PnR

Innovus

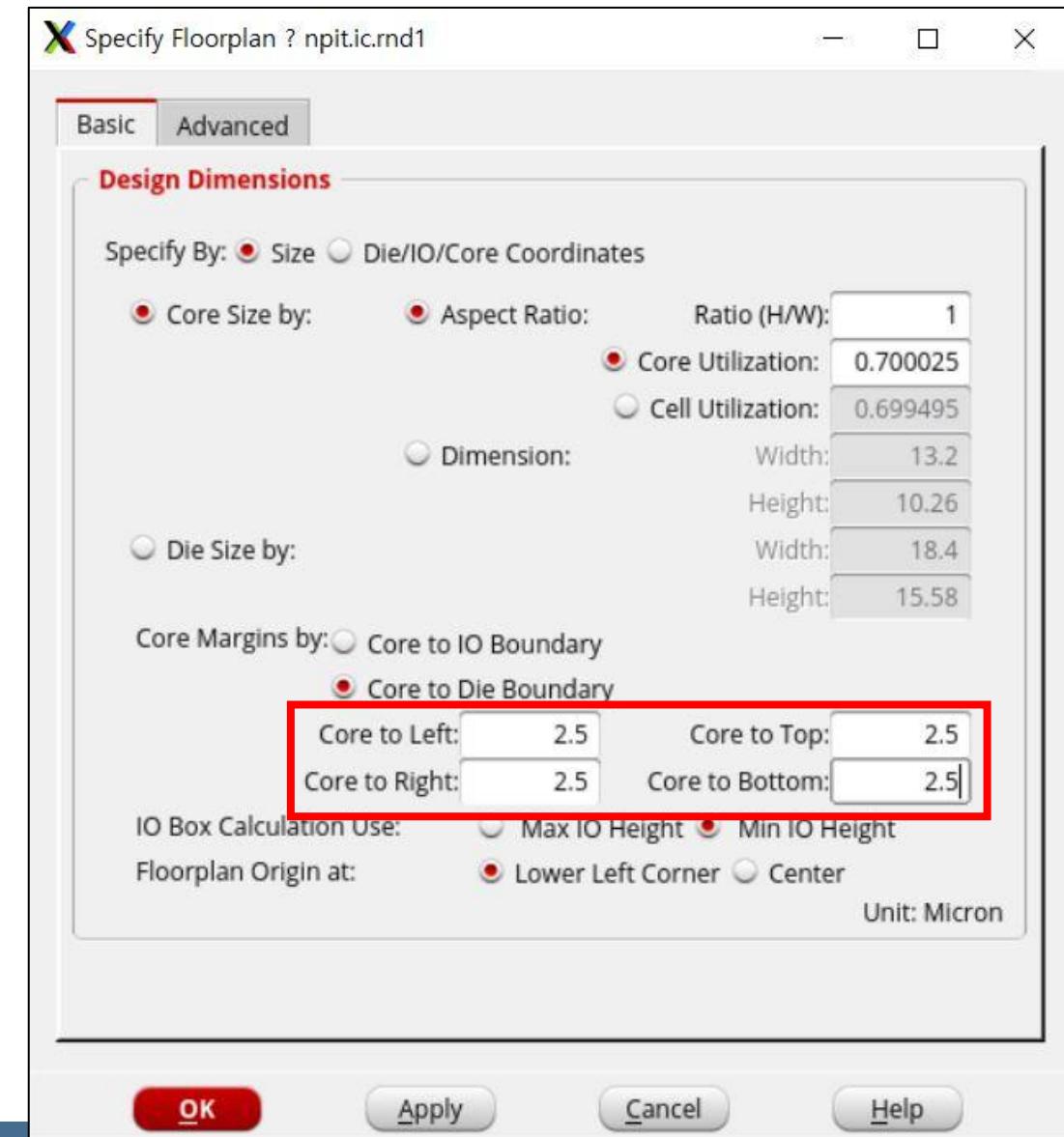
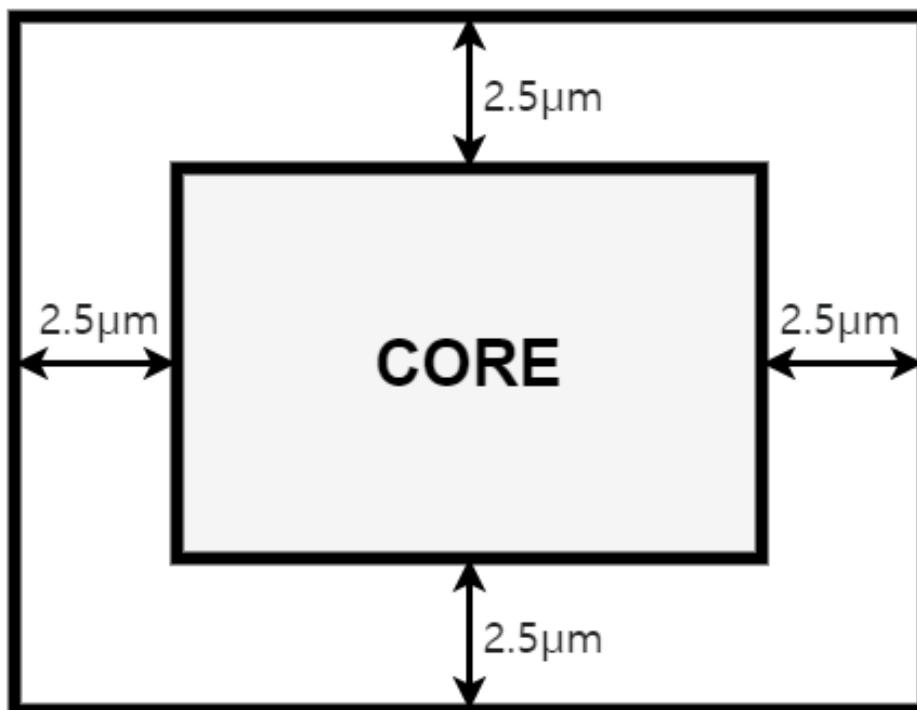
- Core to IO Boundary는 IO셀을 사용하는 TOP 디자인을 할 때 사용함
- Core to Die Boundary는 pin을 사용하는 작은 디자인을 할 때 사용함
- 지금은 TOP모듈이 아니므로 Core to Die Boundary를 선택



Auto PnR

Innovus

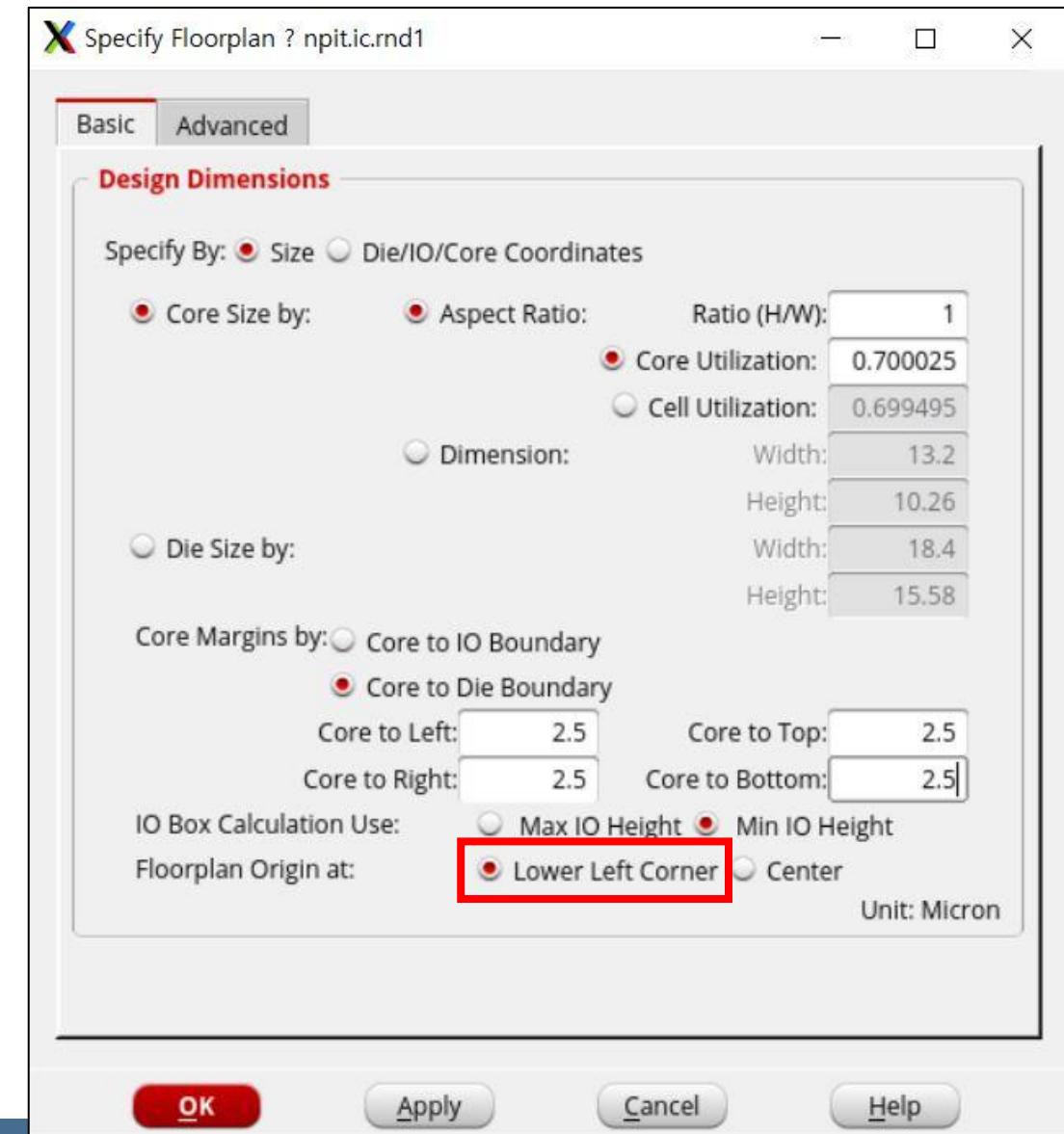
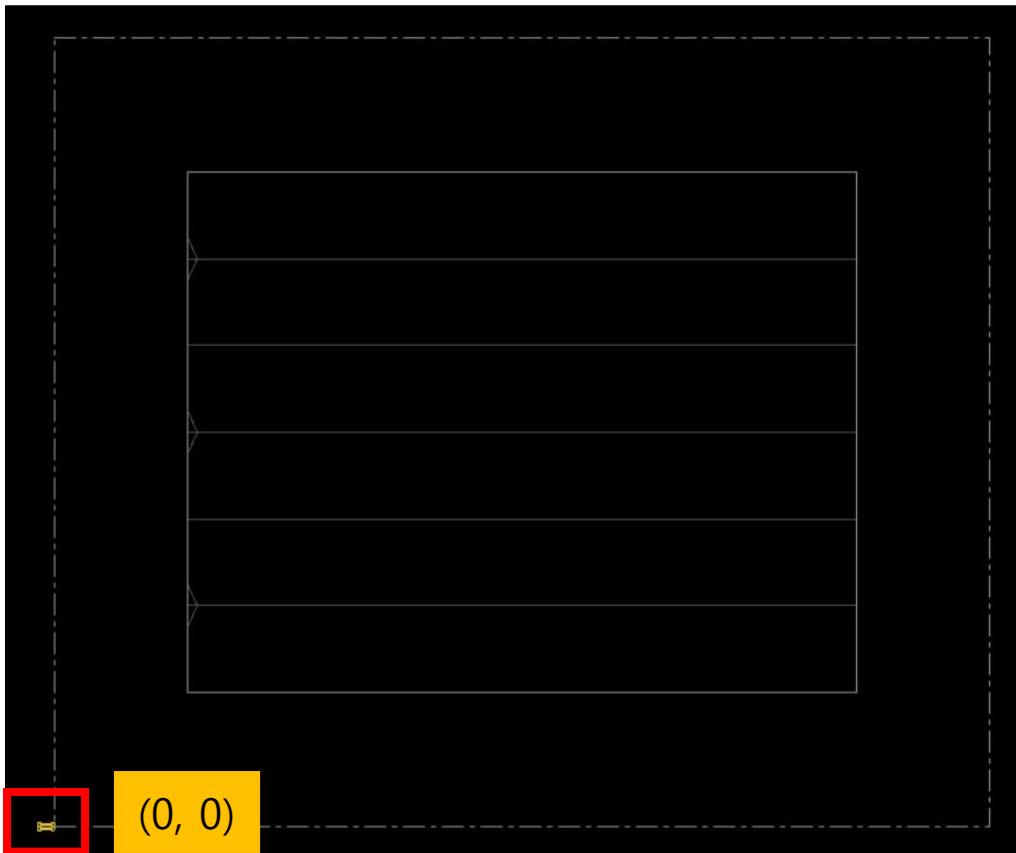
- Core과의 거리를 나타냄



Auto PnR

Innovus

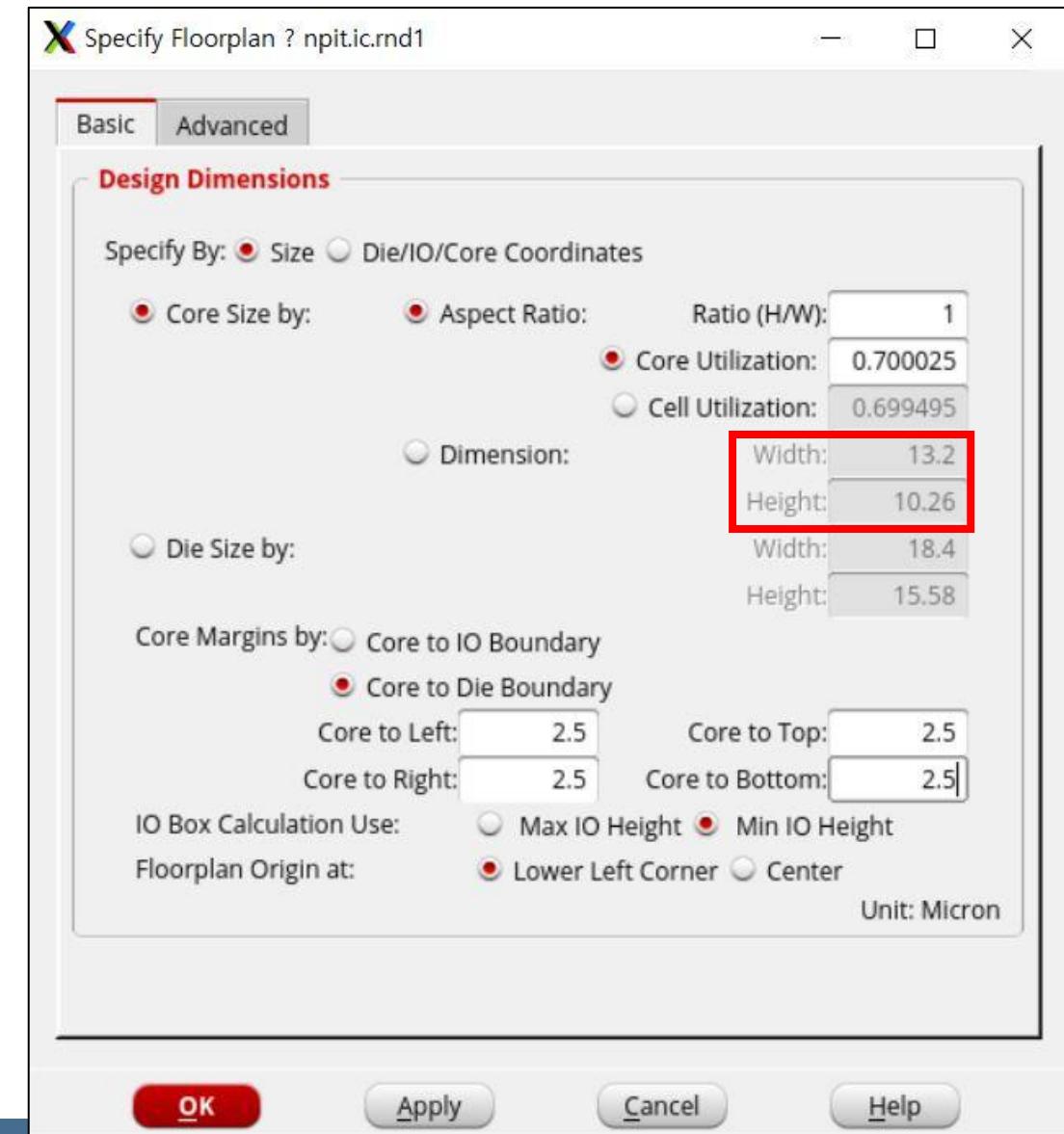
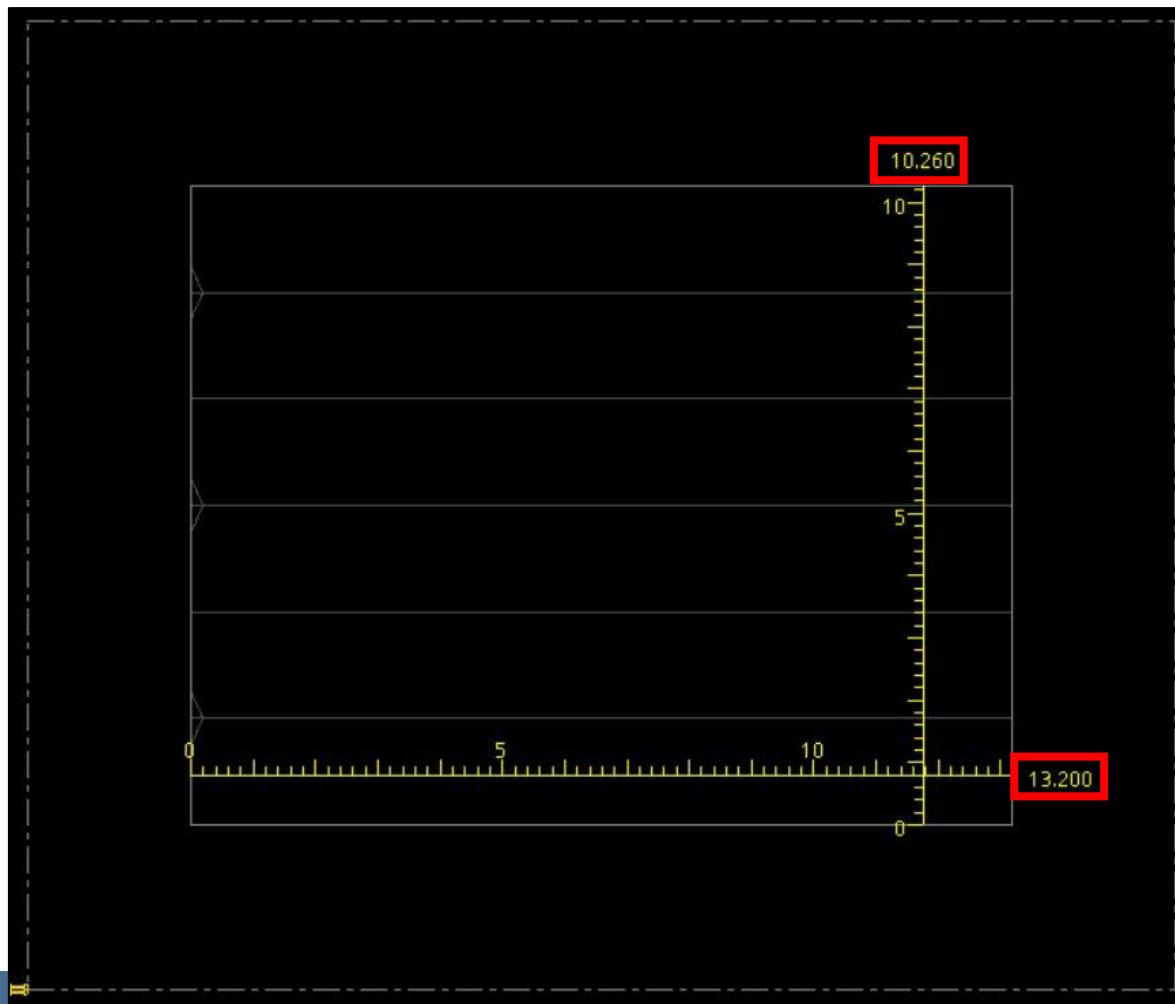
- Origin의 위치를 왼쪽 아래로 설정함



Auto PnR

Innovus

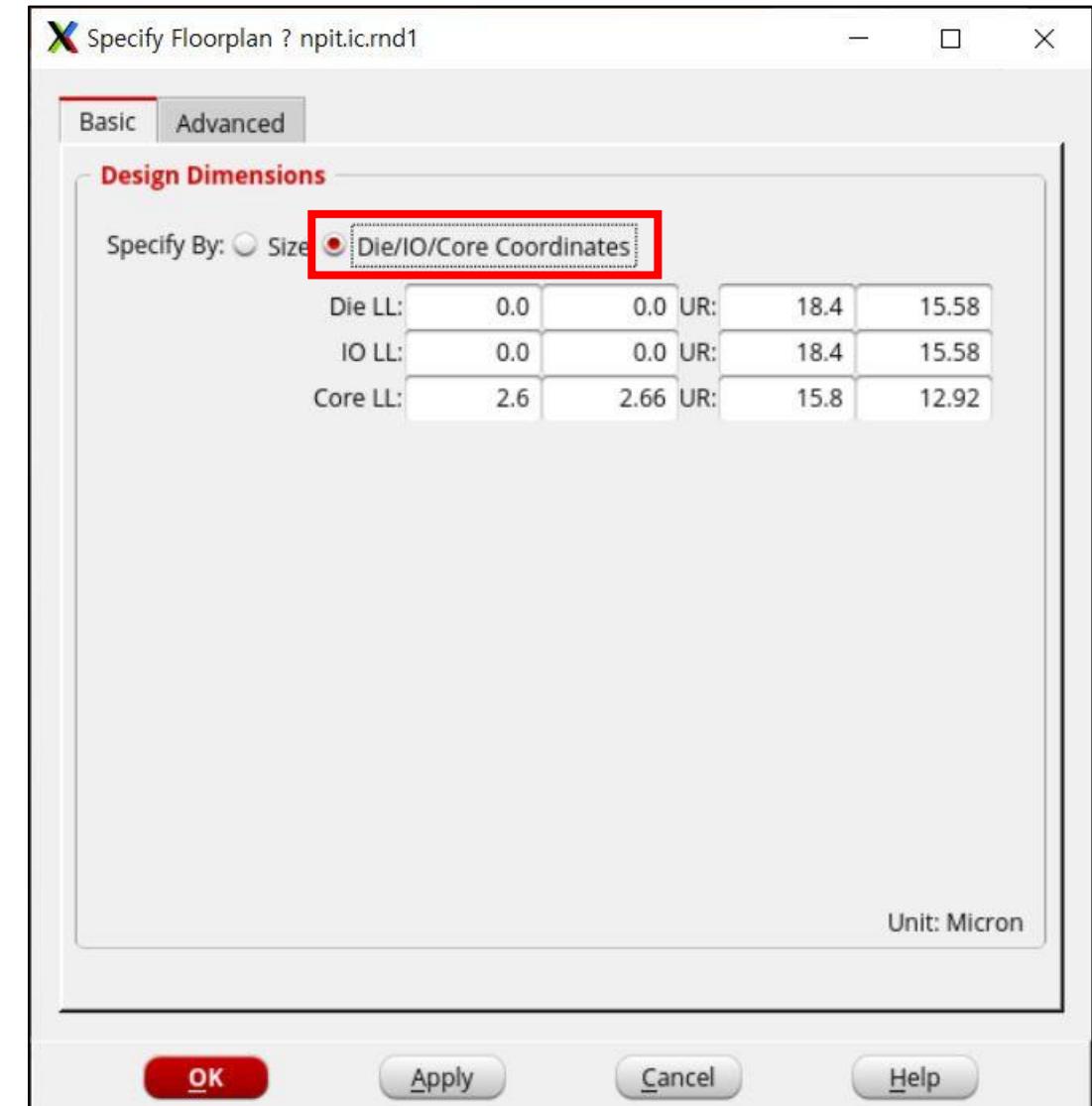
- Core 영역의 크기 확인



Auto PnR

Innovus

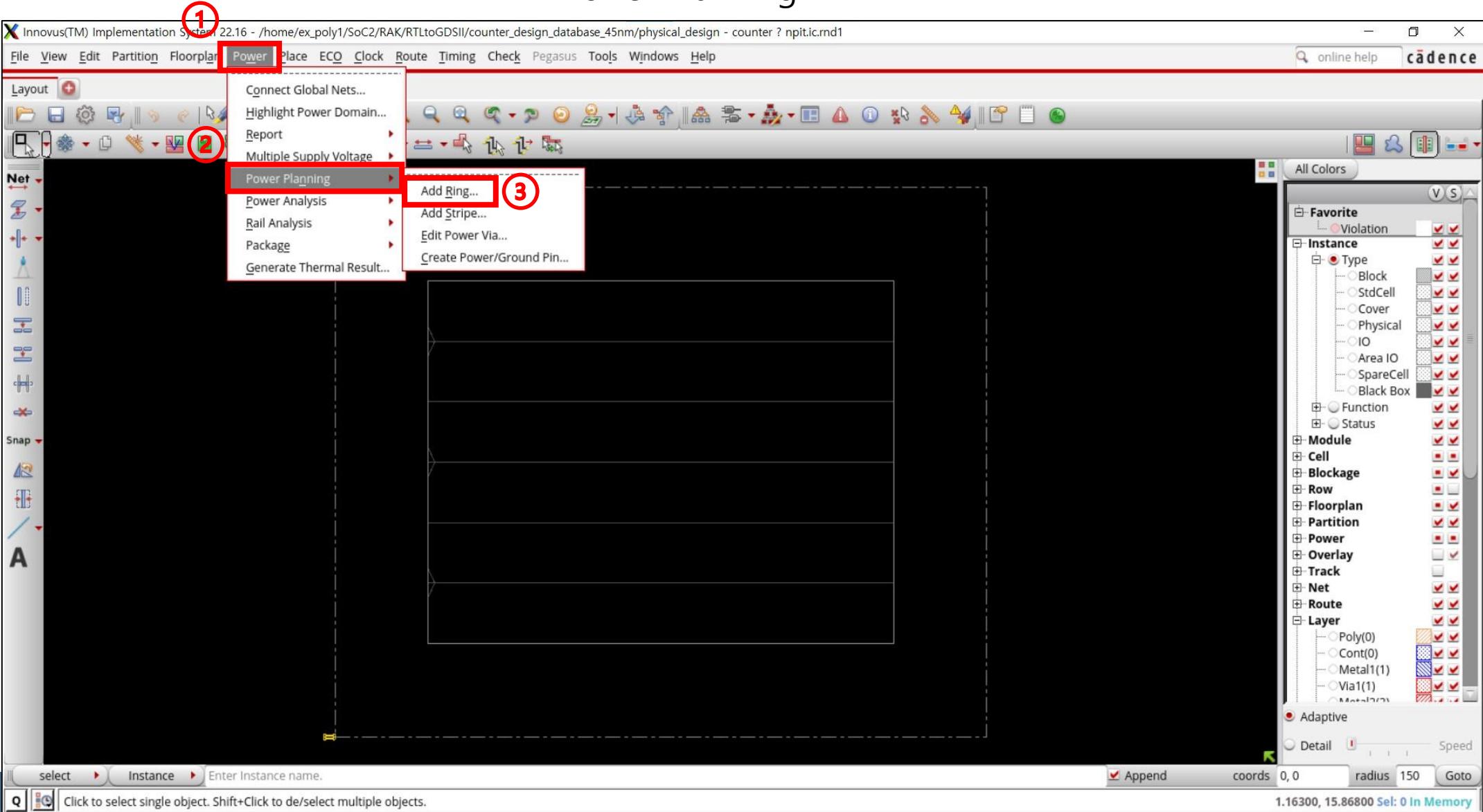
- Specify Floorplan 설정 시 Die/IO/Core Coordinates에서 Die 사이즈와 Utilization 설정 가능



Auto PnR

Innovus

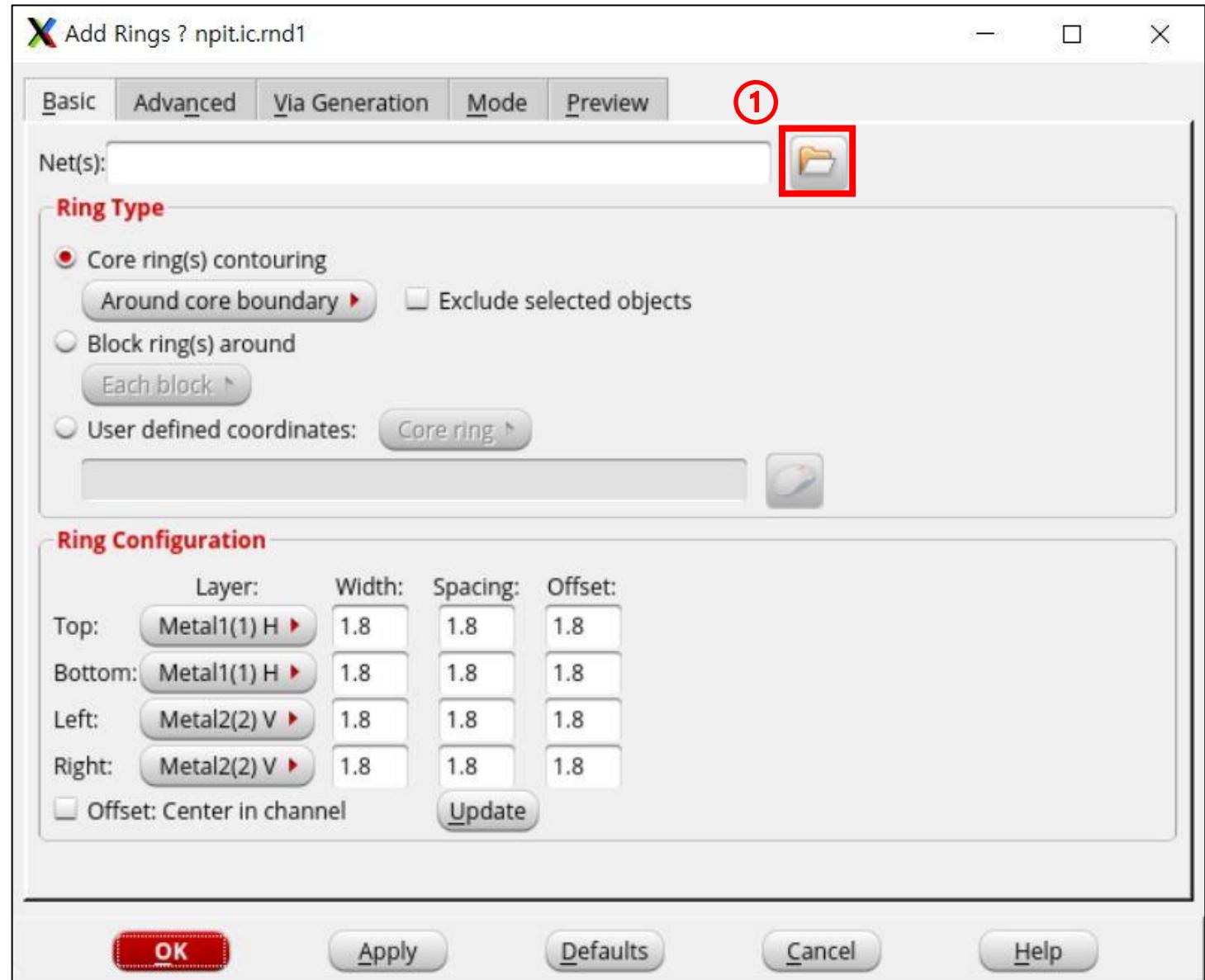
- Power Planning



Auto PnR

Innovus

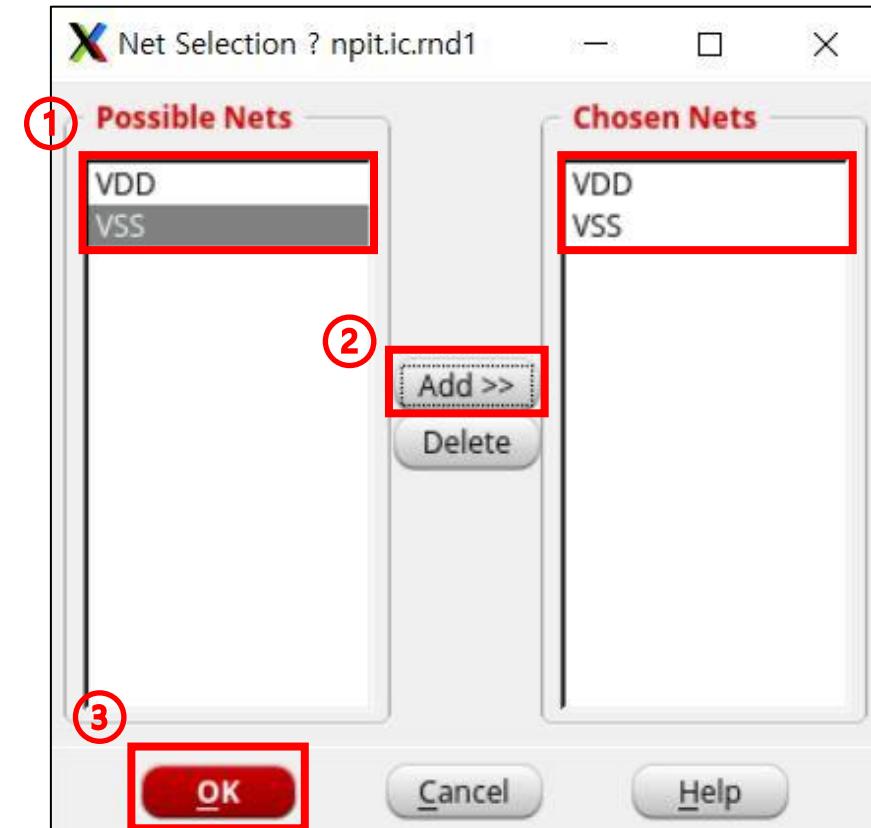
- Power Planning – add ring



Auto PnR

Innovus

- Power Planning – add ring

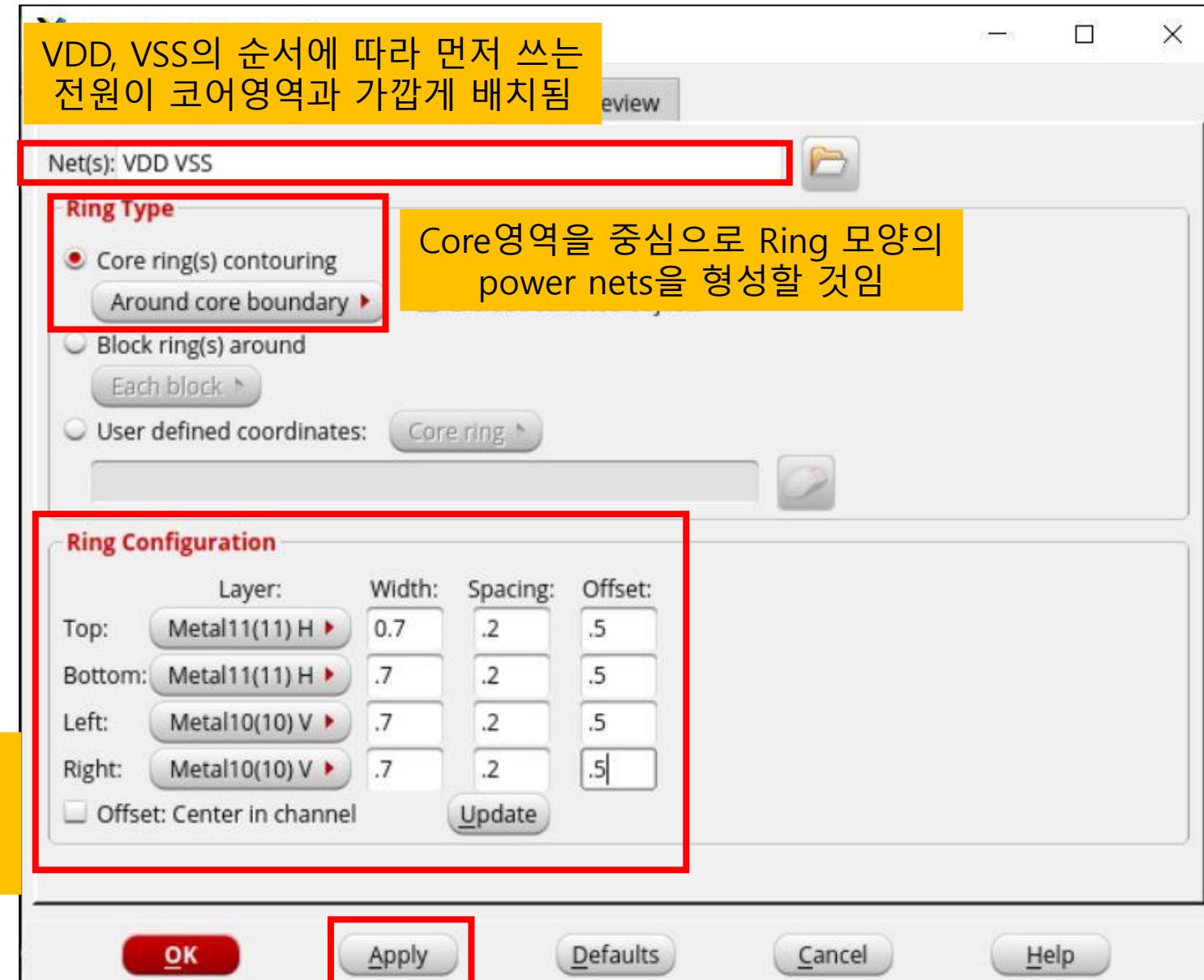


Auto PnR

Innovus

- Power Planning – add ring
- 오른쪽 창의 설정 값과 똑같이 설정 후 Apply 클릭

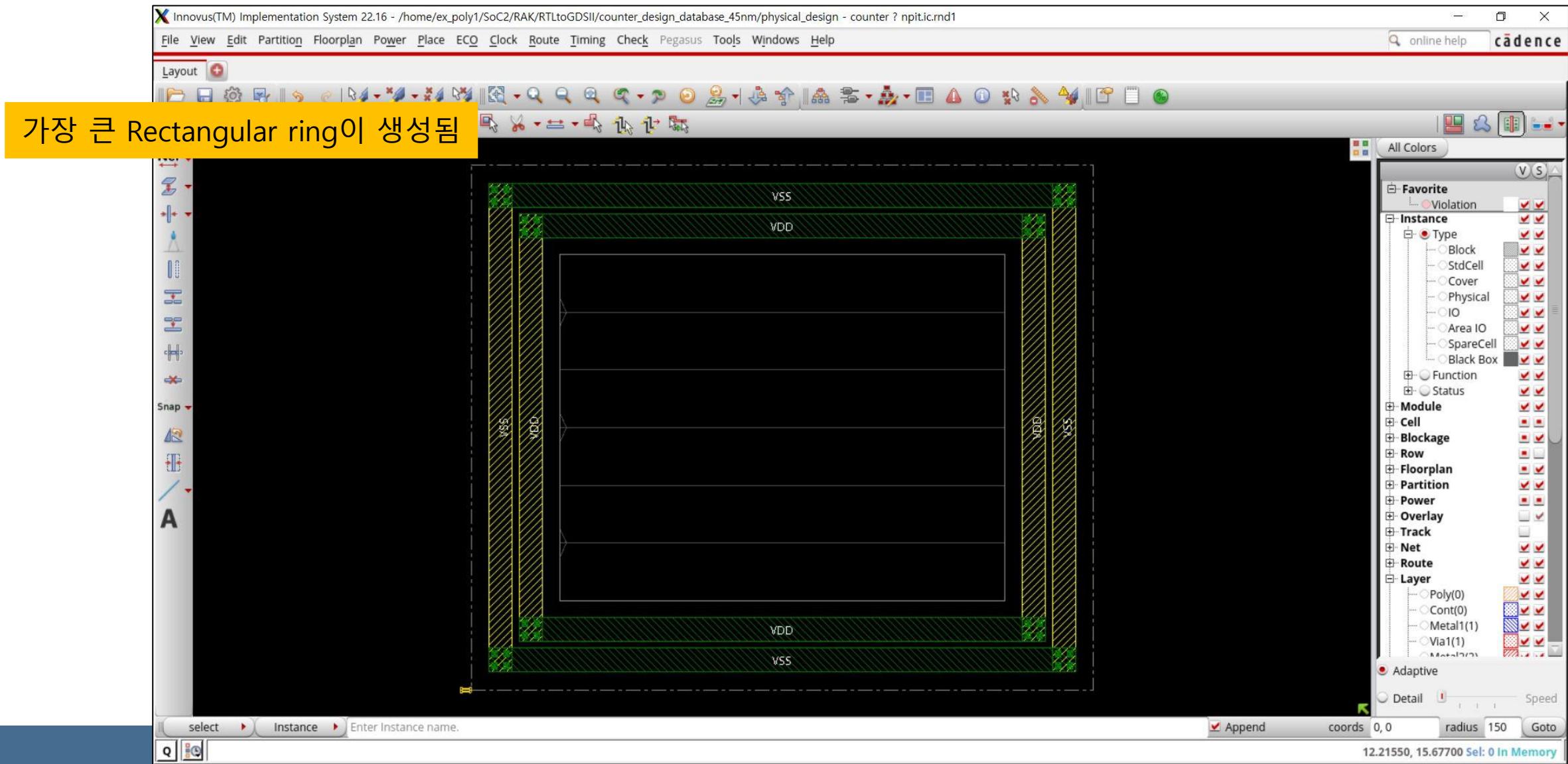
Rectangular ring는 power nets이므로 Max Width가 가장 큰 M10, M11 사용함
Spacing과 Offset도 공정사문서를 참고하여 설정



Auto PnR

Innovus

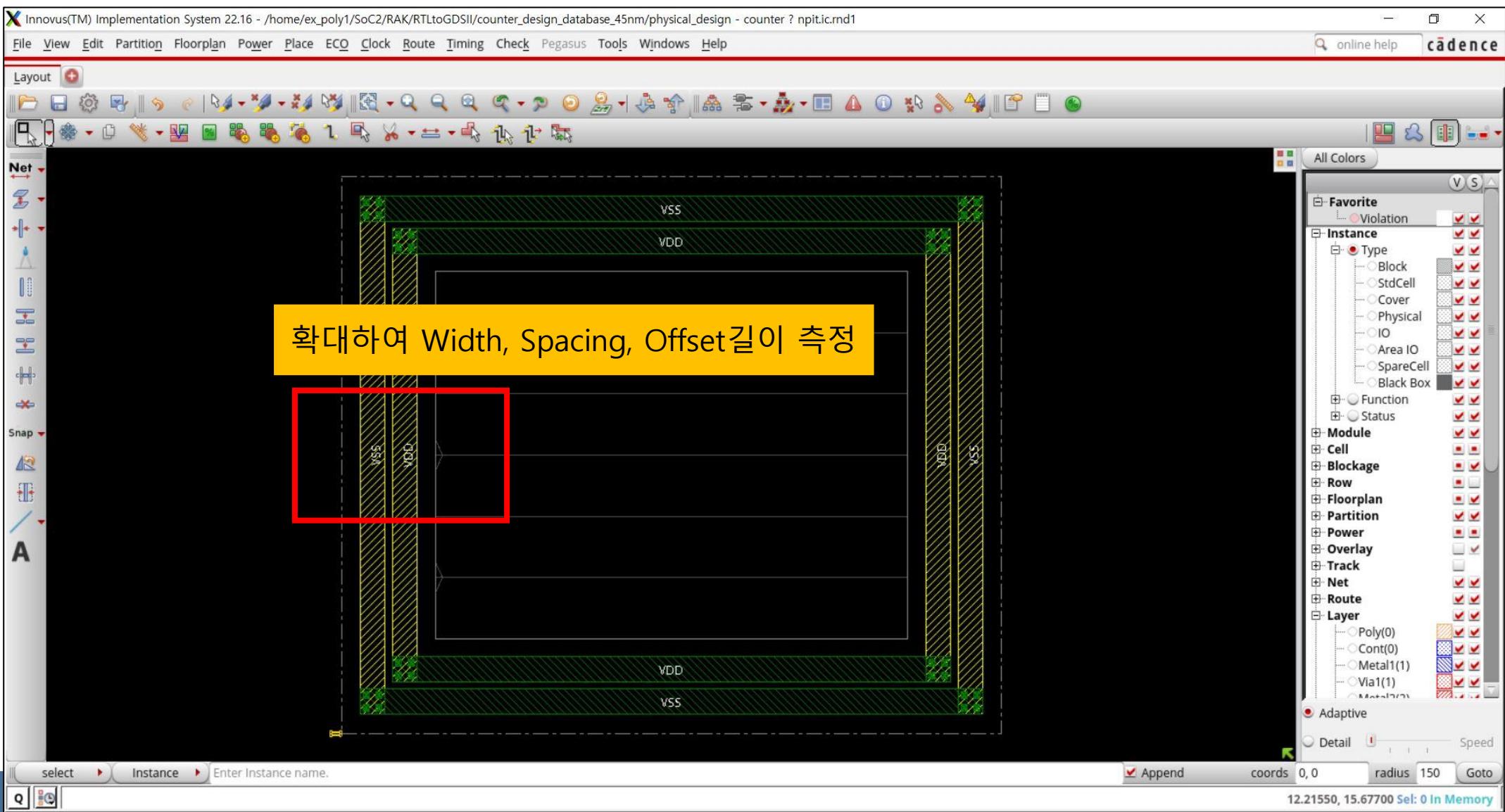
- Power Planning – add ring



Auto PnR

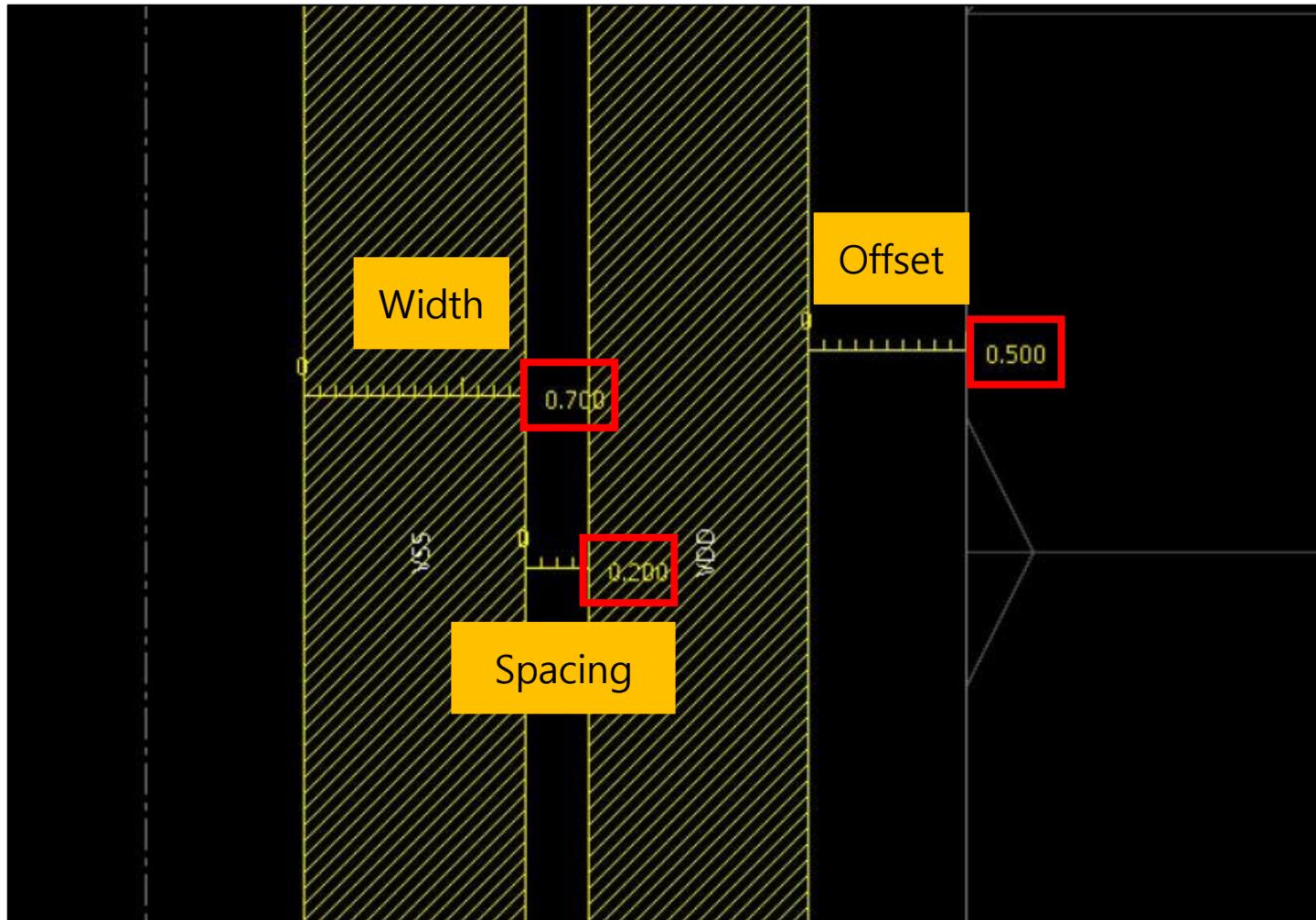
Innovus

- Power Planning – add ring



Auto PnR

Innovus



- Ring Configuration 길이 비교

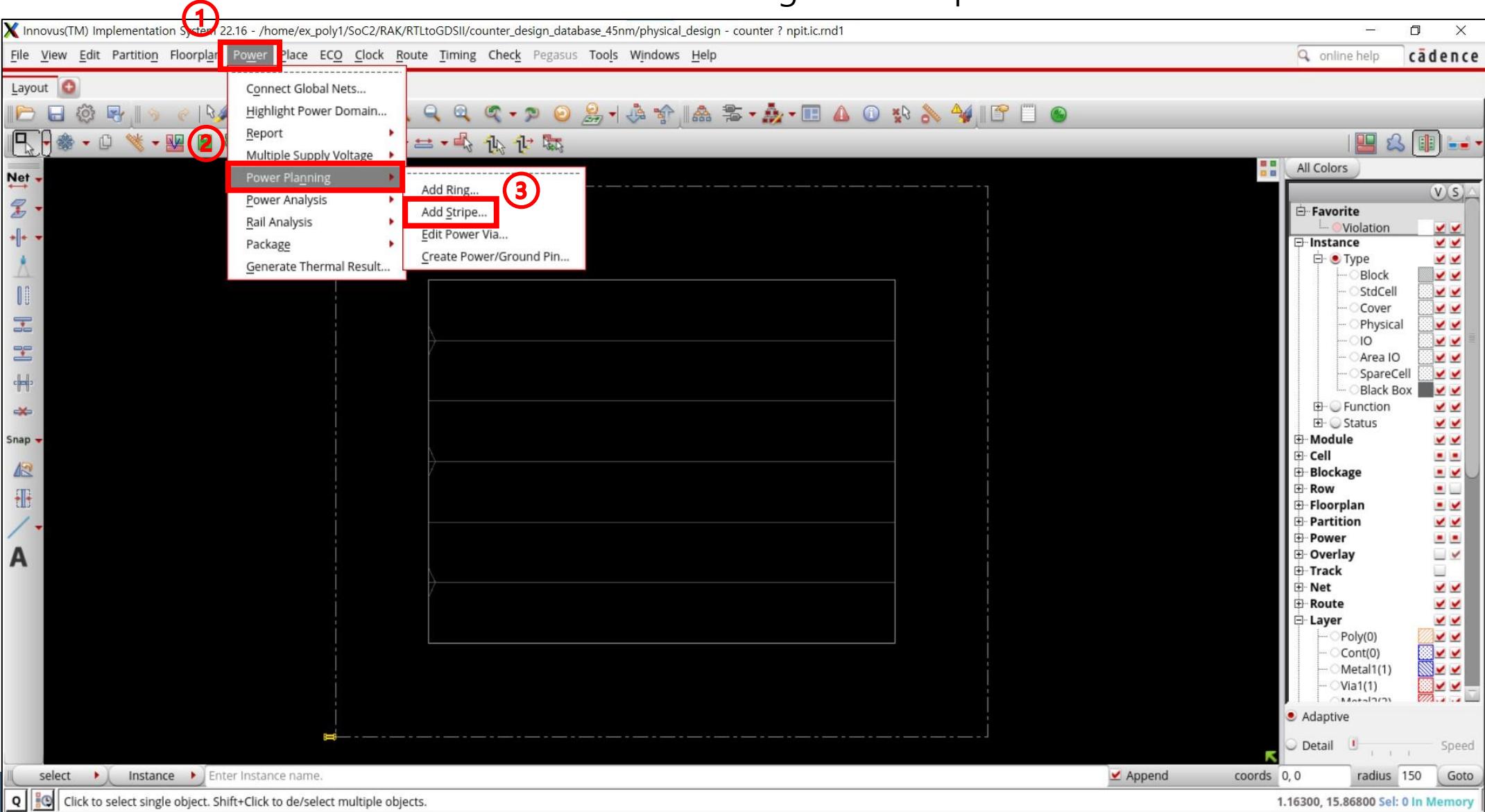
Ring Configuration				
	Layer:	Width:	Spacing:	Offset:
Top:	Metal11(11) H ▶	0.7	.2	.5
Bottom:	Metal11(11) H ▶	.7	.2	.5
Left:	Metal10(10) V ▶	.7	.2	.5
Right:	Metal10(10) V ▶	.7	.2	.5

Offset: Center in channel Update

Auto PnR

Innovus

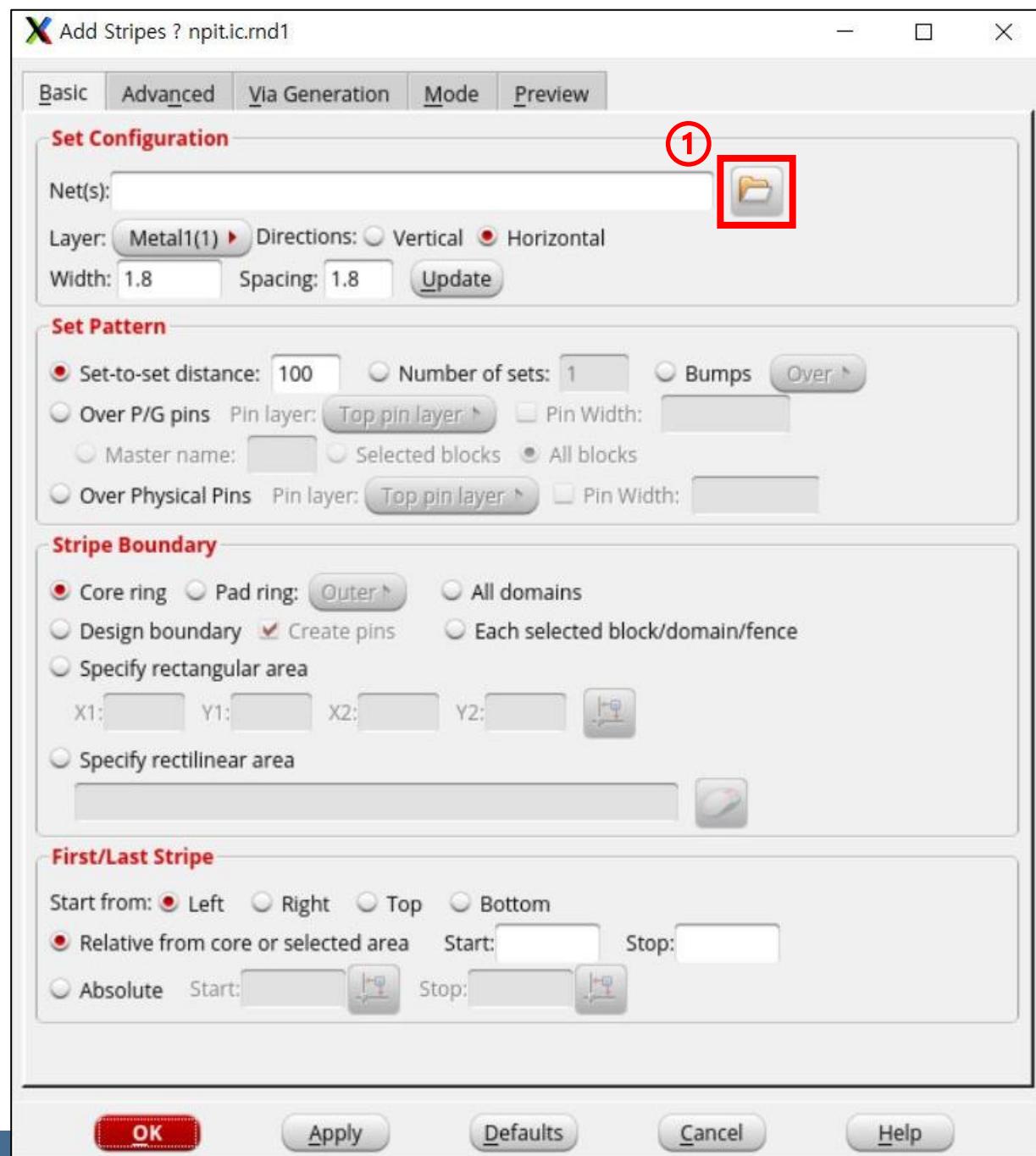
- Power Planning – add stripe



Auto PnR

Innovus

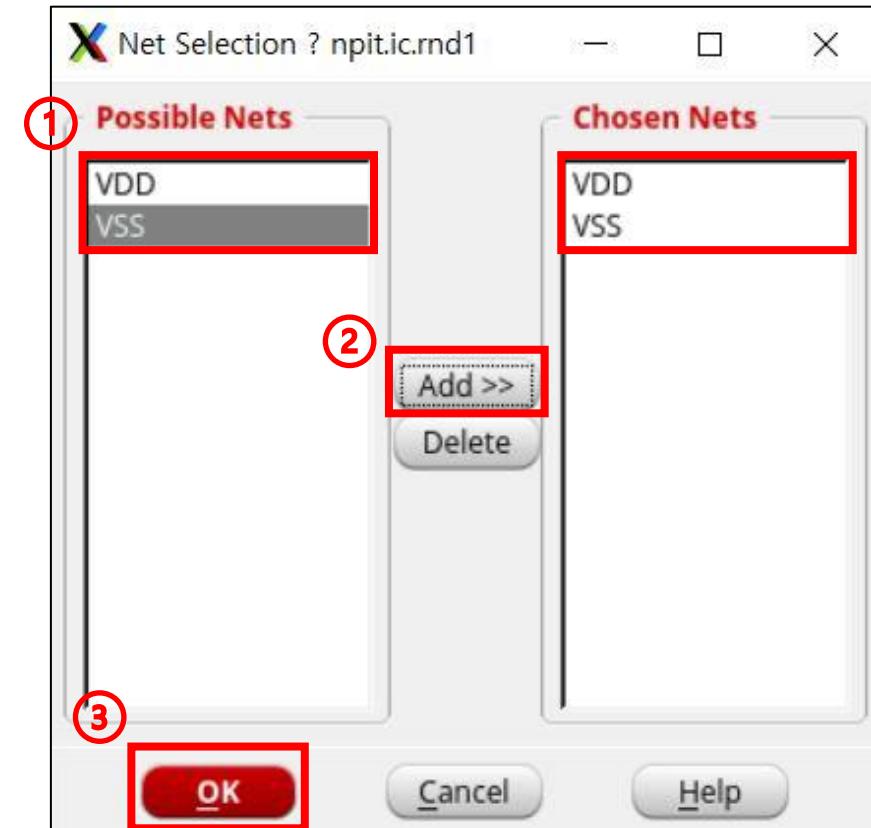
- Power Planning – add stripe



Auto PnR

Innovus

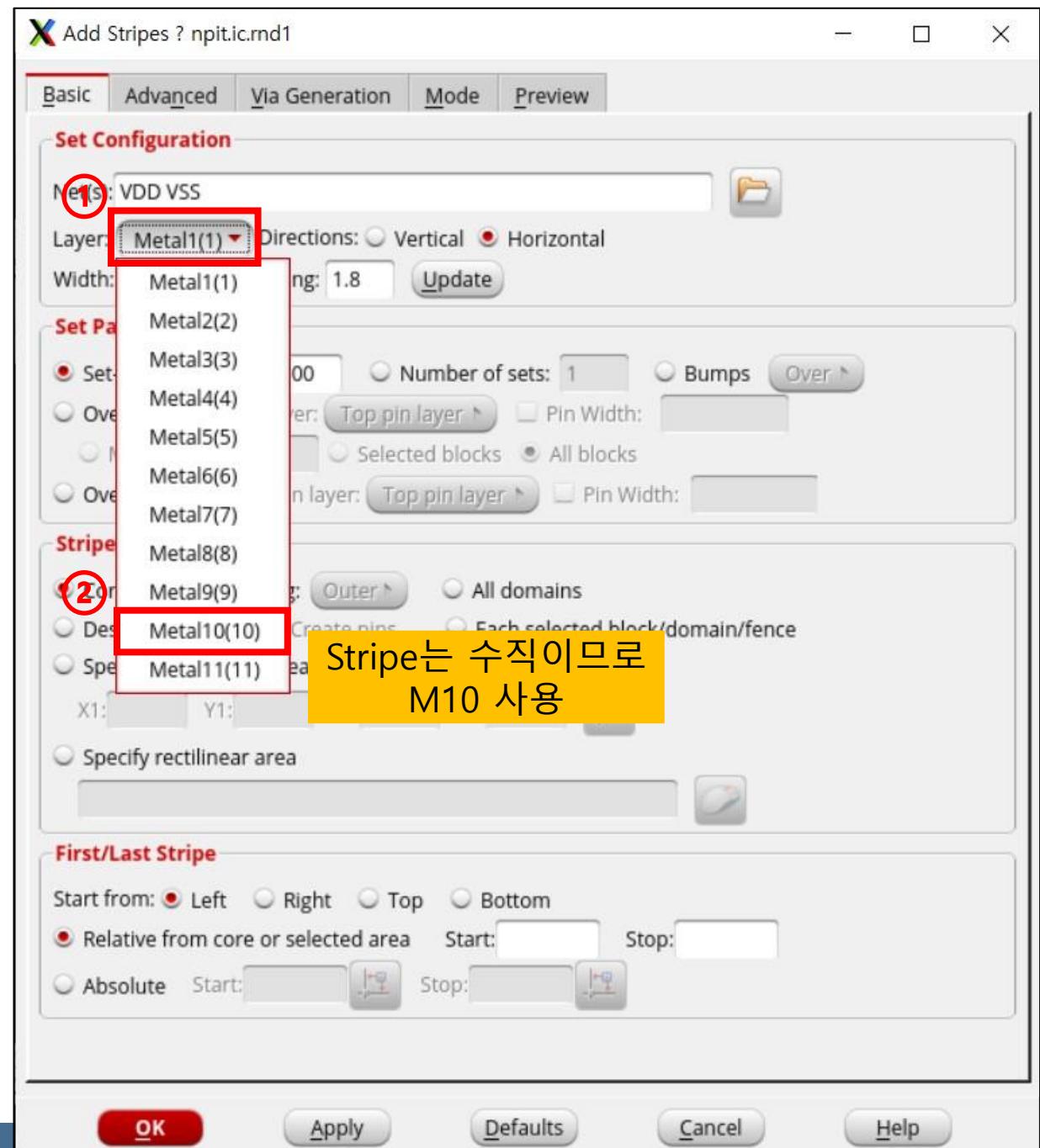
- Power Planning – add stripe



Auto PnR

Innovus

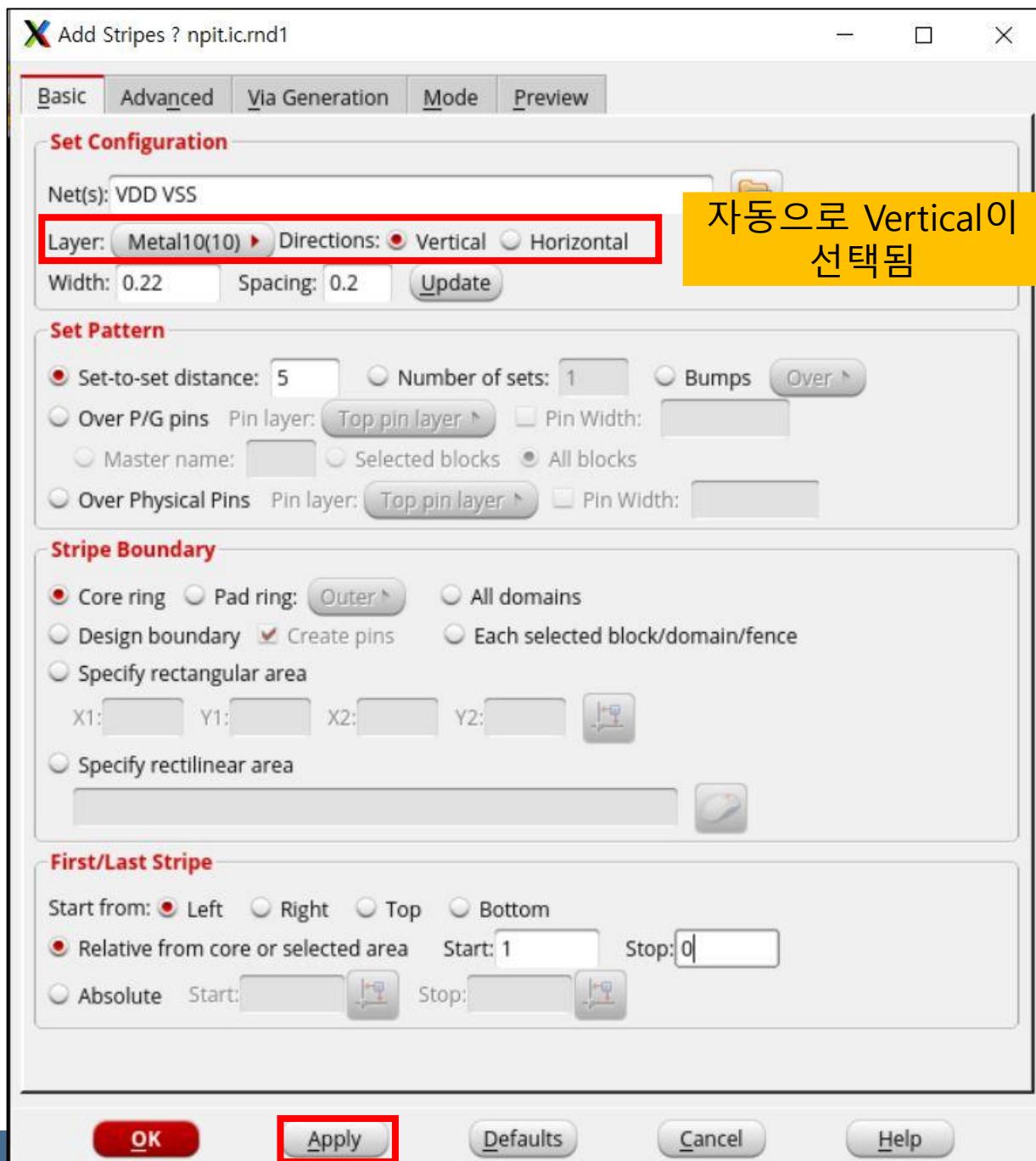
- Power Planning – add stripe



Auto PnR

Innovus

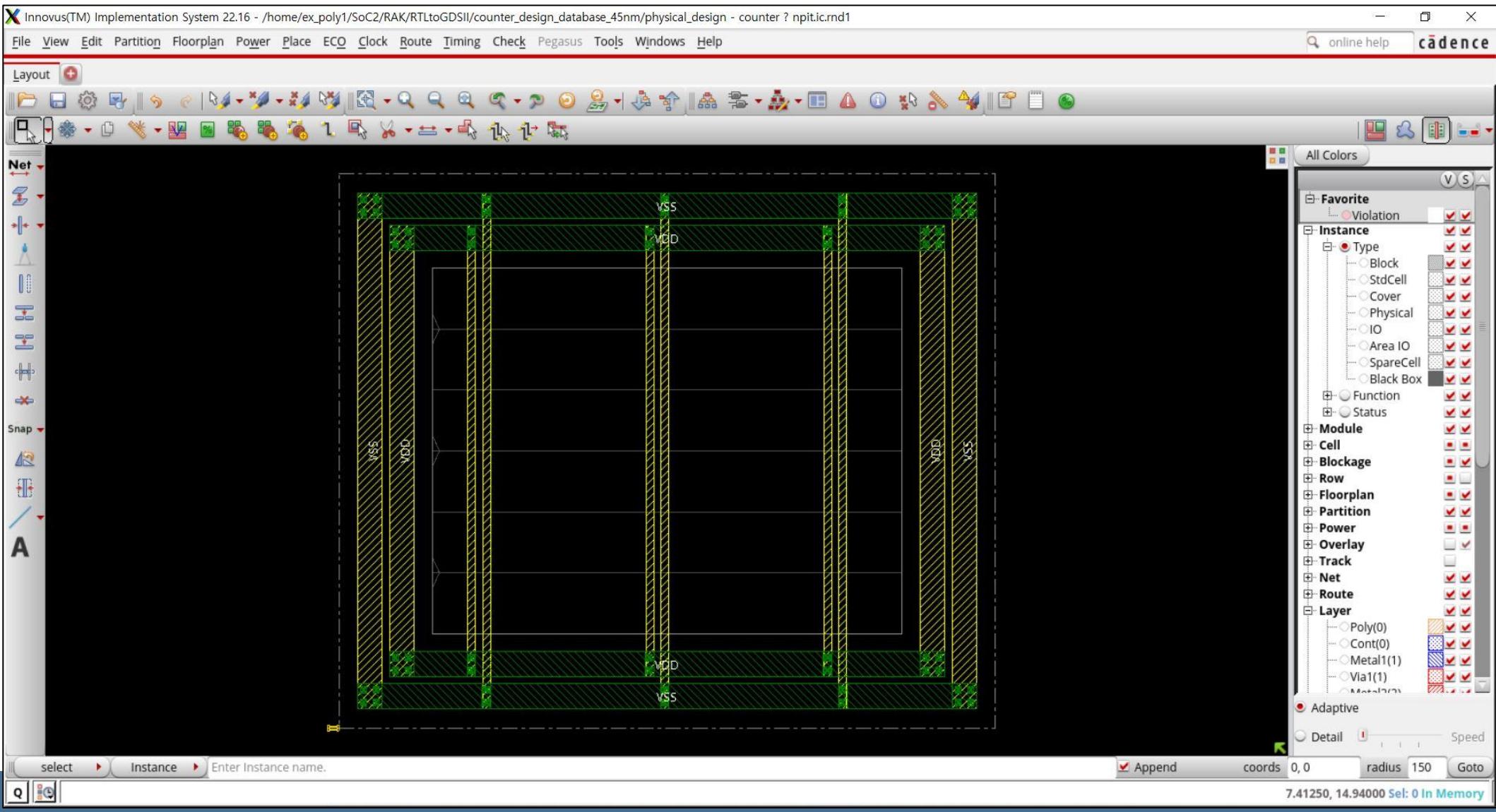
- Power Planning – add stripe
- 오른쪽 창의 설정 값과 똑같이 설정 후 Apply 클릭



Auto PnR

Innovus

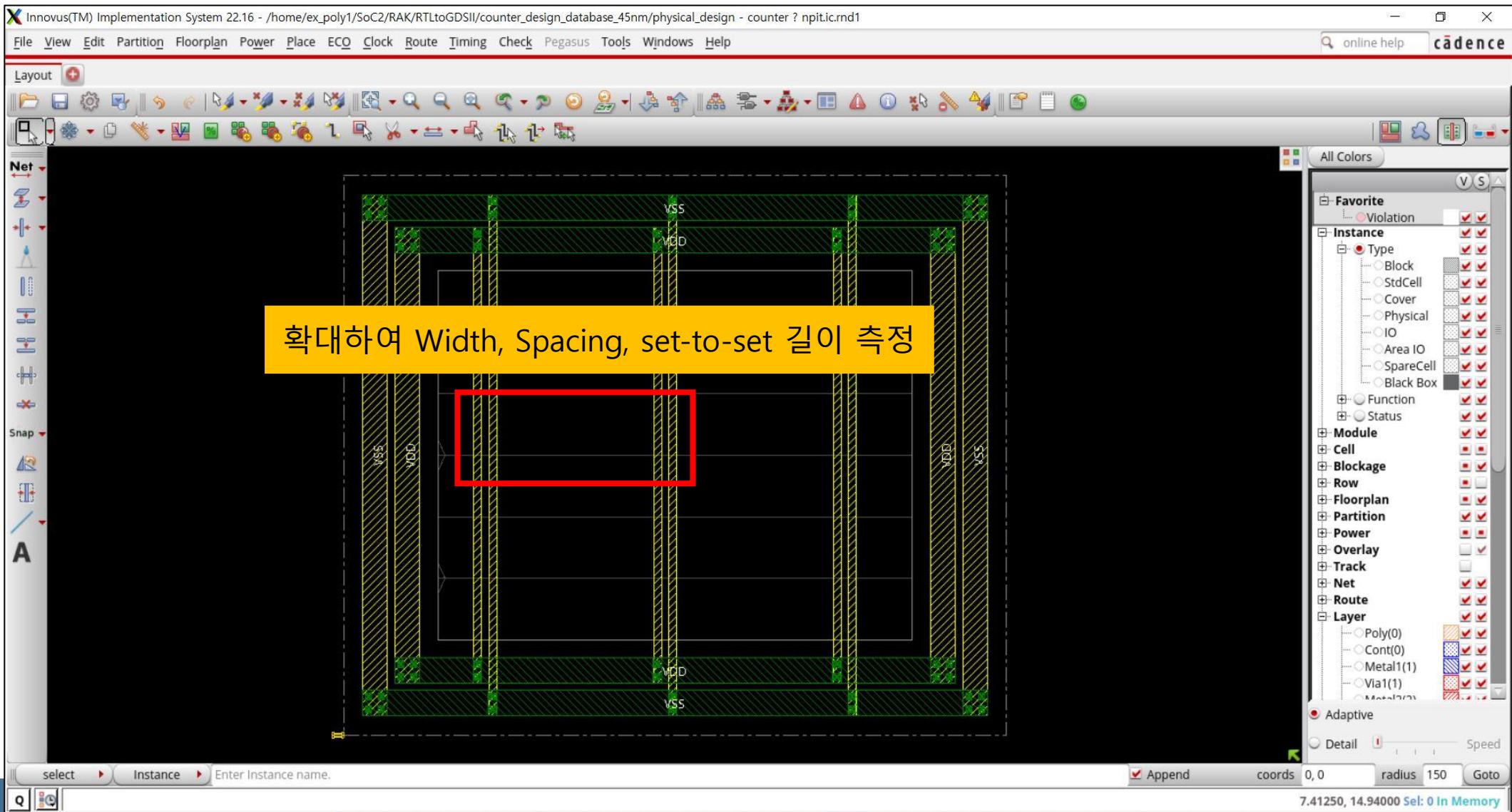
- Power Planning – add stripe



Auto PnR

Innovus

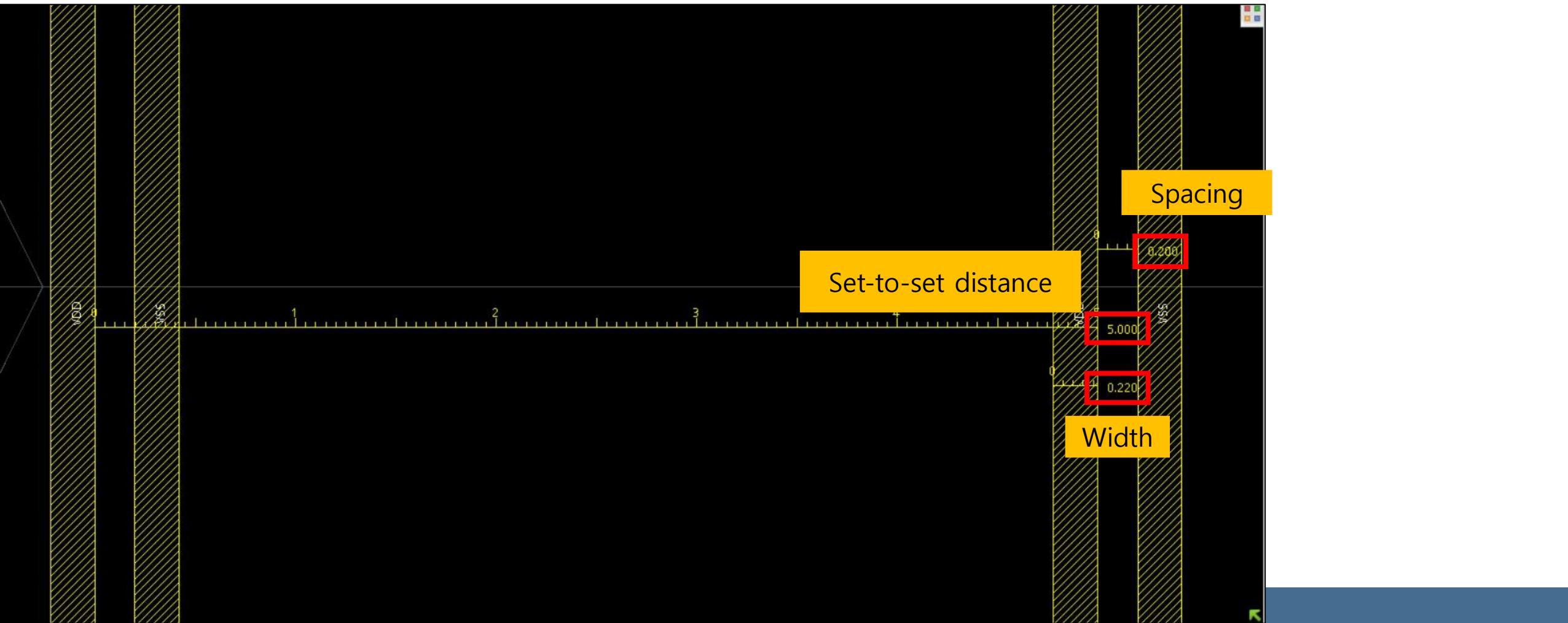
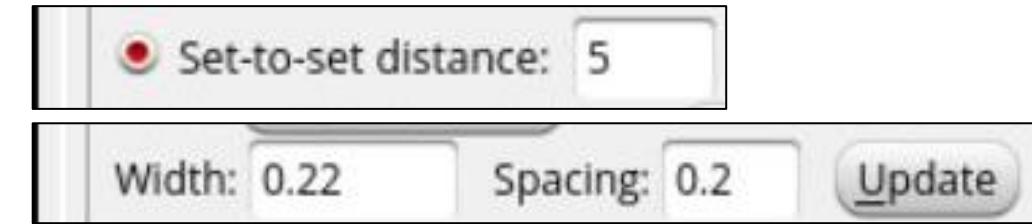
- Power Planning – add stripe



Auto PnR

Innovus

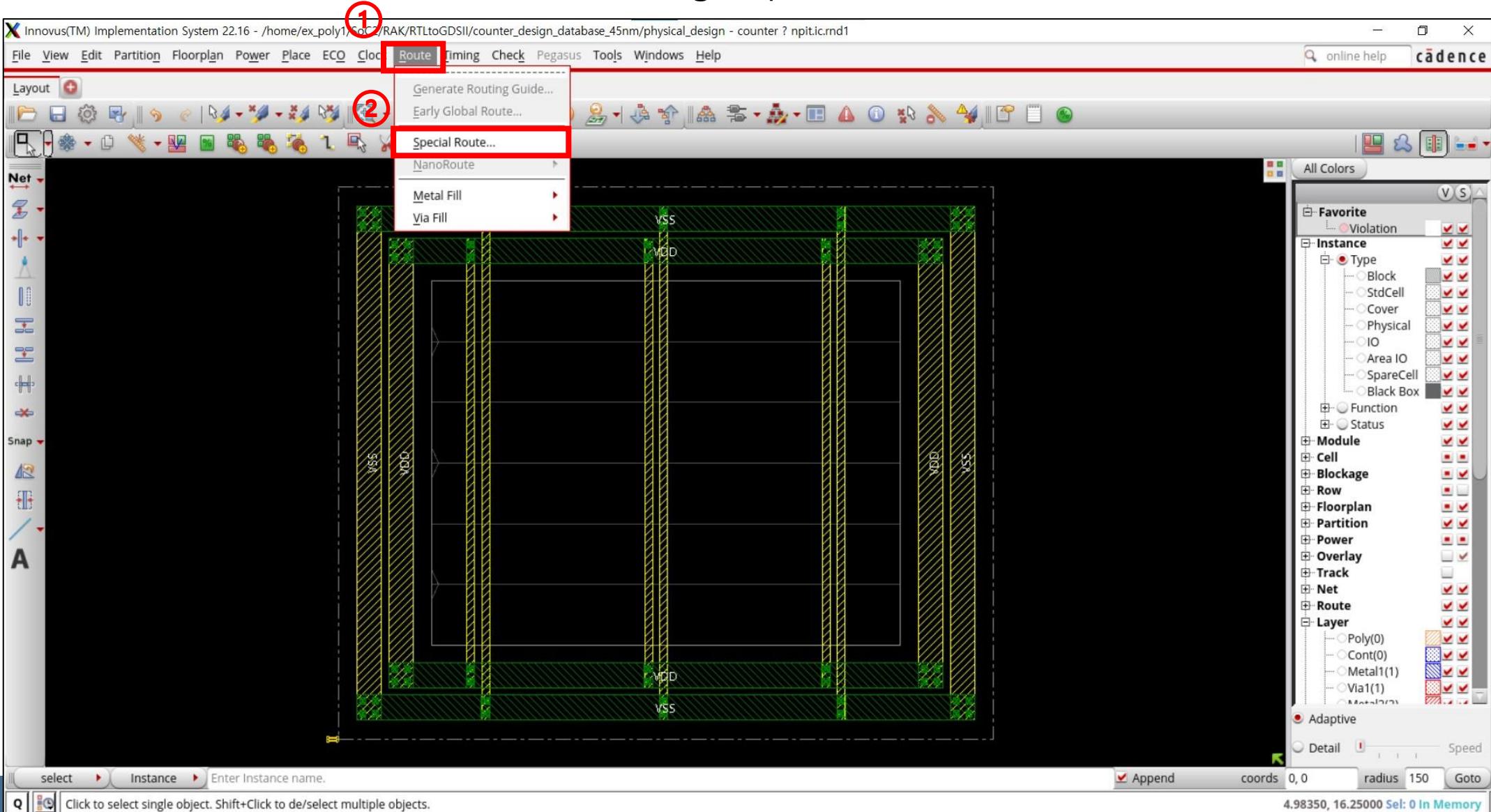
- 설정 길이측정



Auto PnR

Innovus

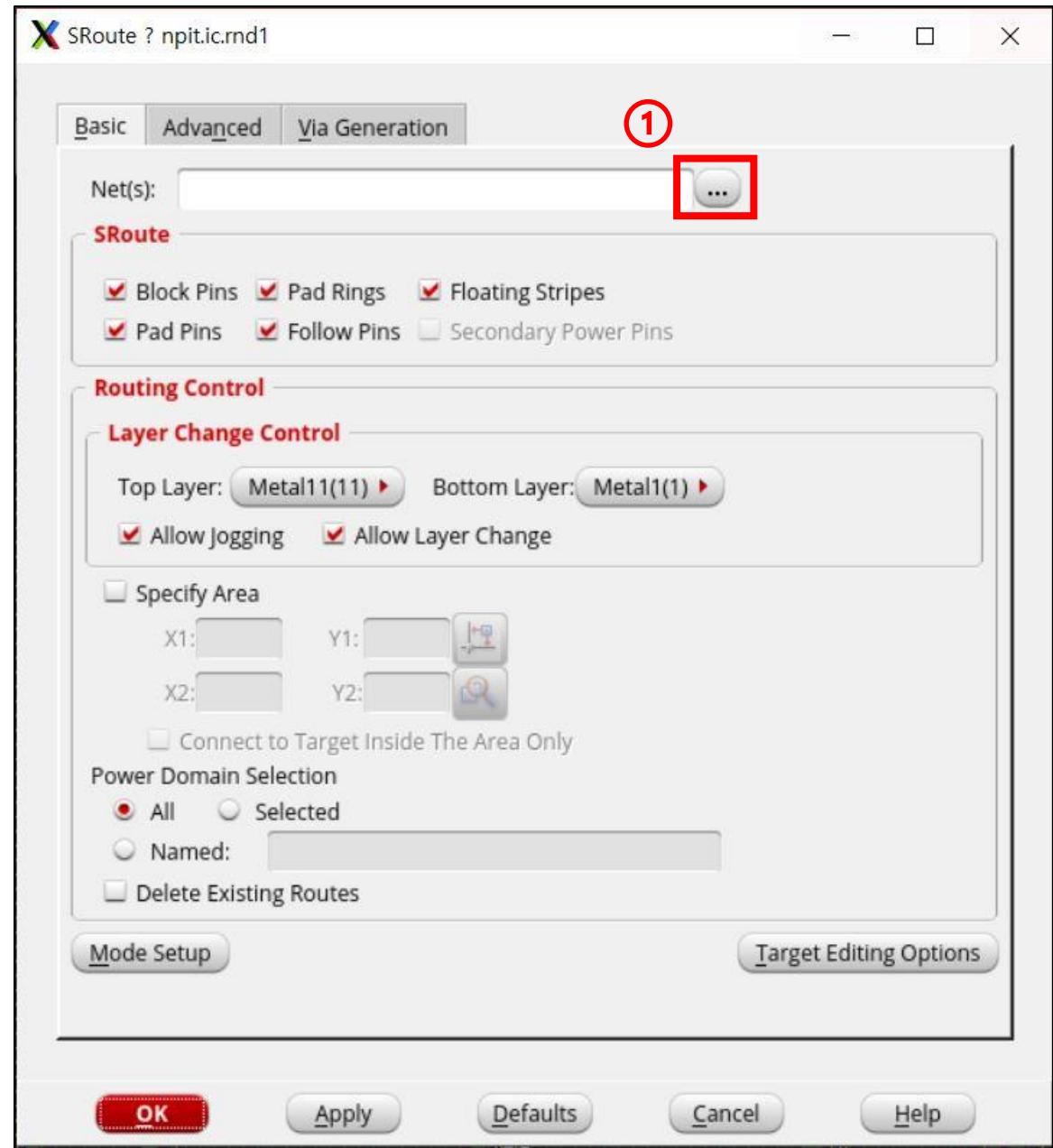
- Power Planning - Special Route (Rail)



Auto PnR

Innovus

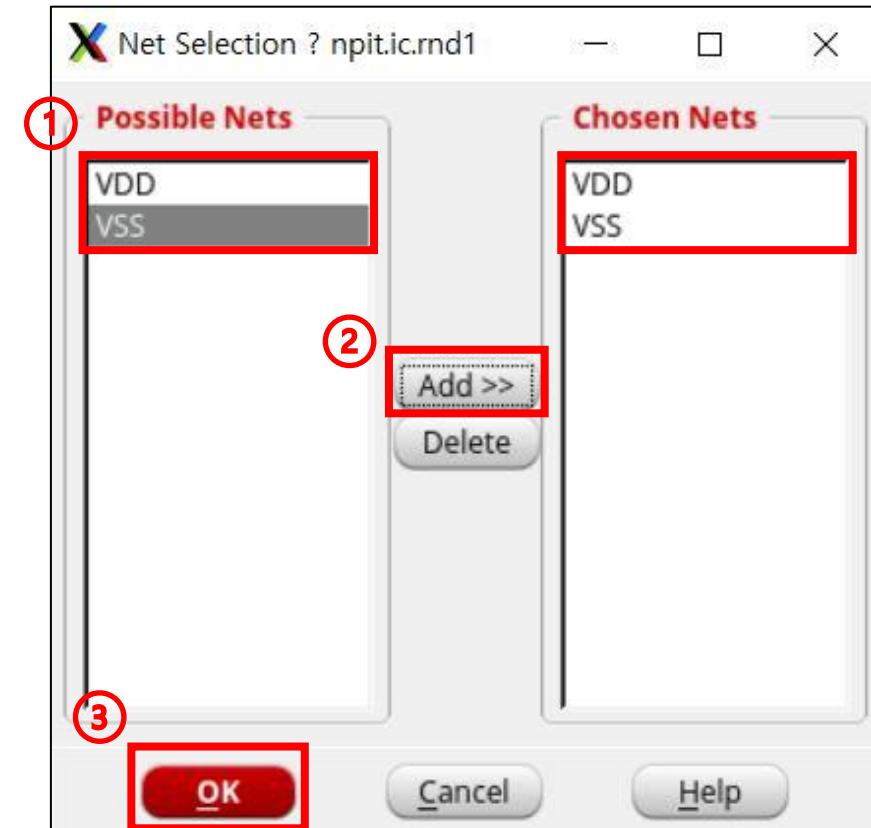
- Power Planning - Special Route (Rail)



Auto PnR

Innovus

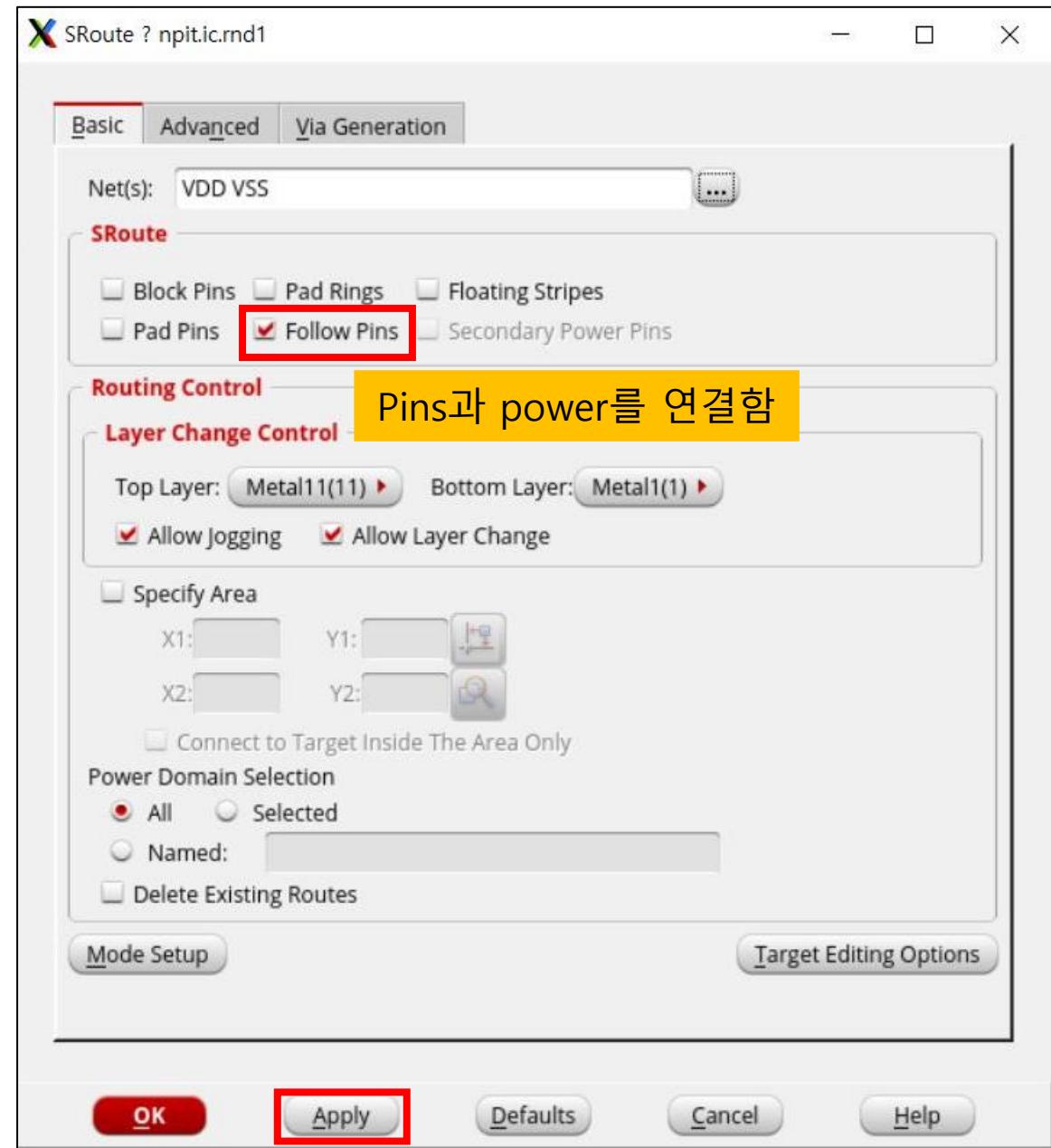
- Power Planning - Special Route (Rail)



Auto PnR

Innovus

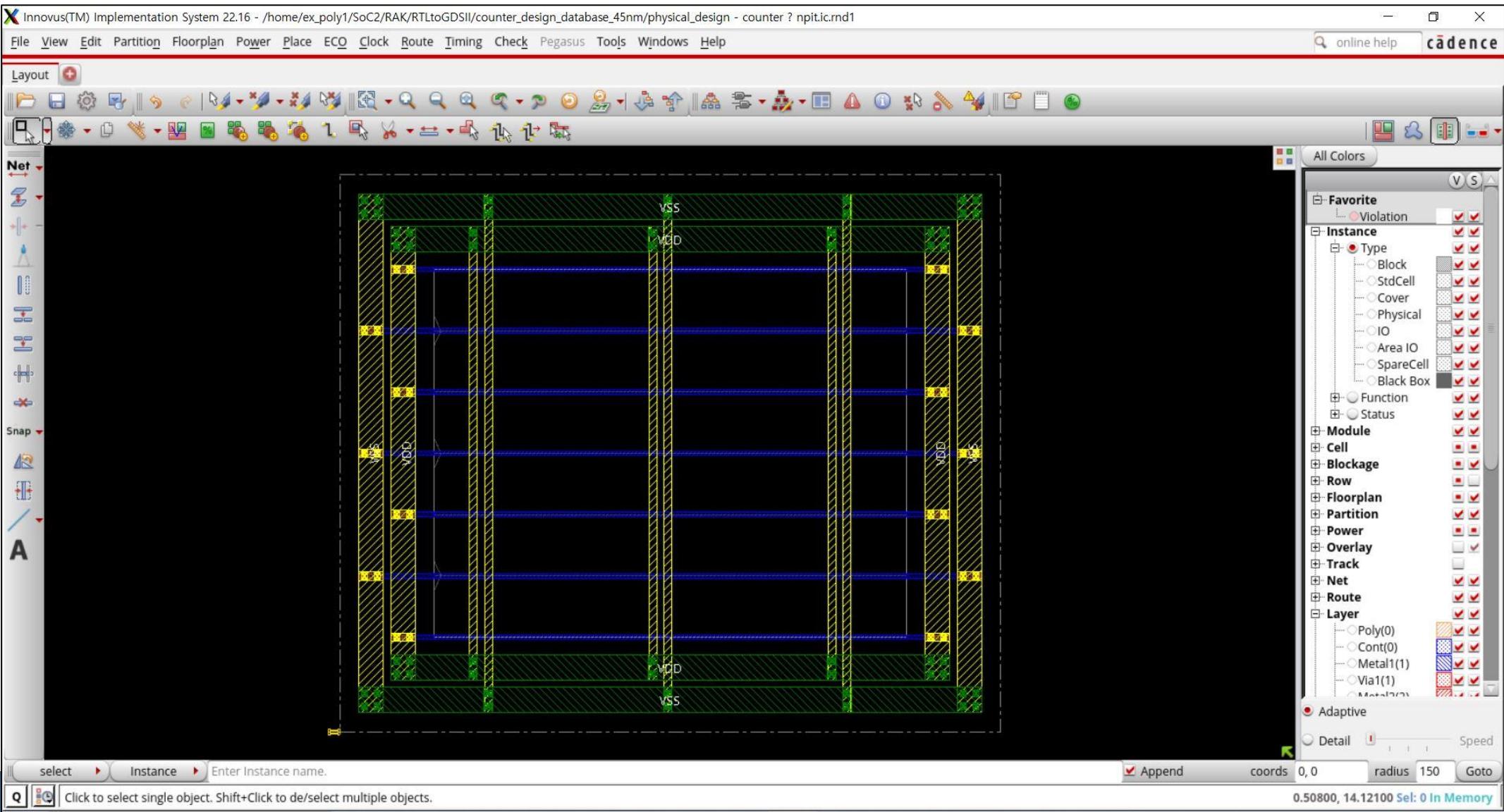
- Power Planning - Special Route (Rail)
- 오른쪽 창의 설정 값과 똑같이 설정 후 Apply 클릭



Auto PnR

Innovus

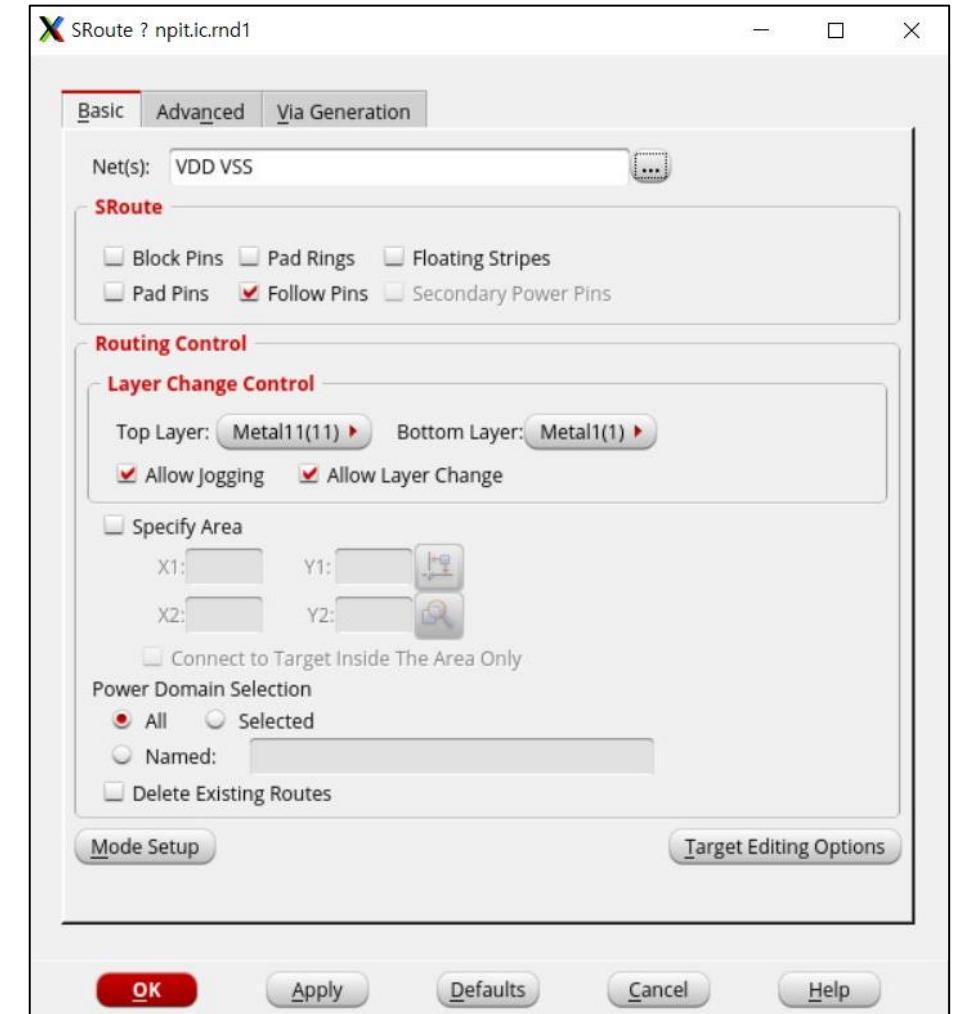
- Power Planning - Special Route (Rail)



Auto PnR

Innovus

- Power Planning - Special Route (Rail)
- Gui로 Rail을 설정하는 대신 아래의 명령으로도 설정 가능함
- 명령어를 매번 작성하기 힘드므로 power.tcl을 사용하여 필요할 때 소스함



Net과 pin을 연결

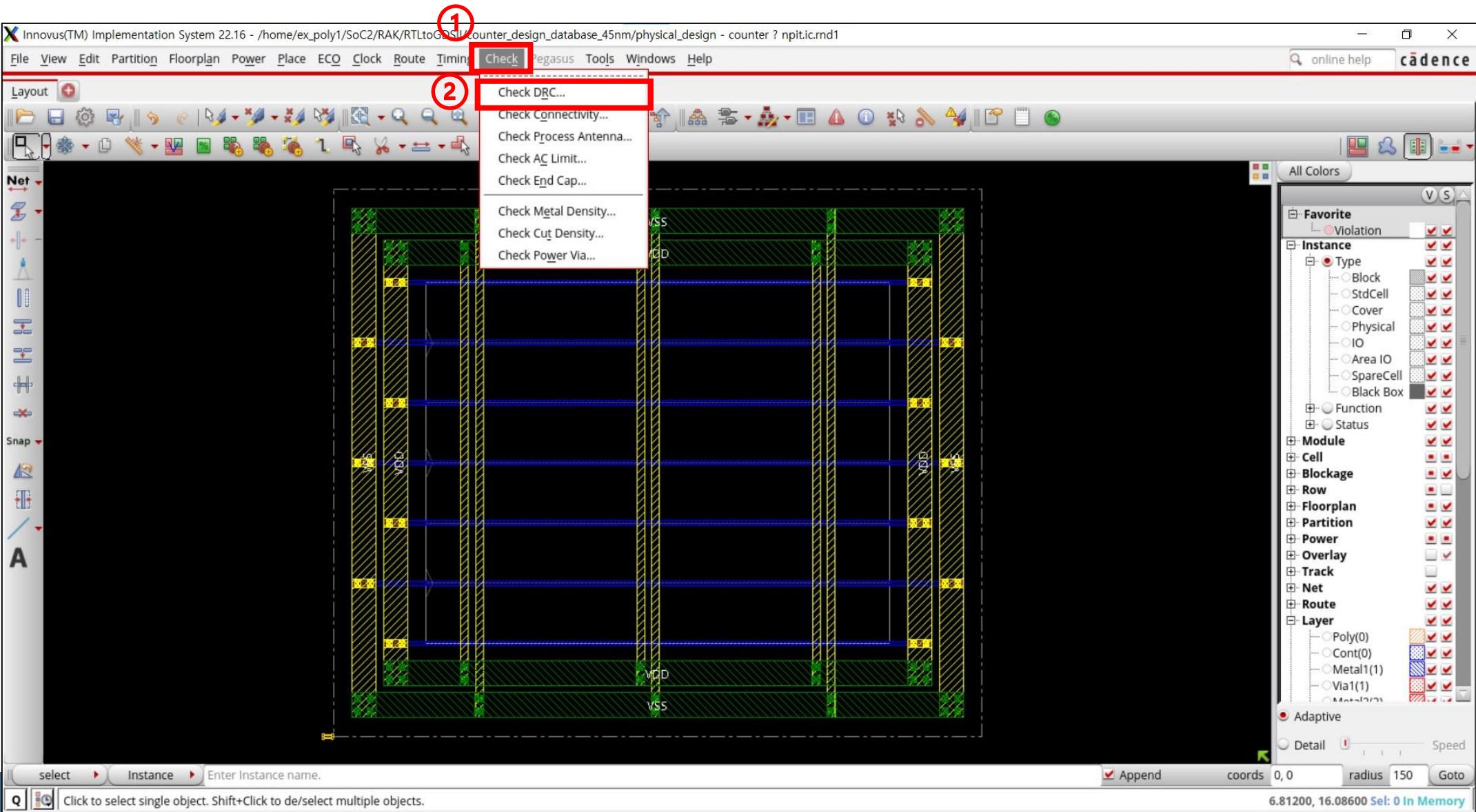
```
connect_global_net VDD -type pg_pin -pin VDD -inst_base_name *
connect_global_net VSS -type pg_pin -pin VSS -inst_base_name *
```

pg_pin → power ground pin

Auto PnR

Innovus

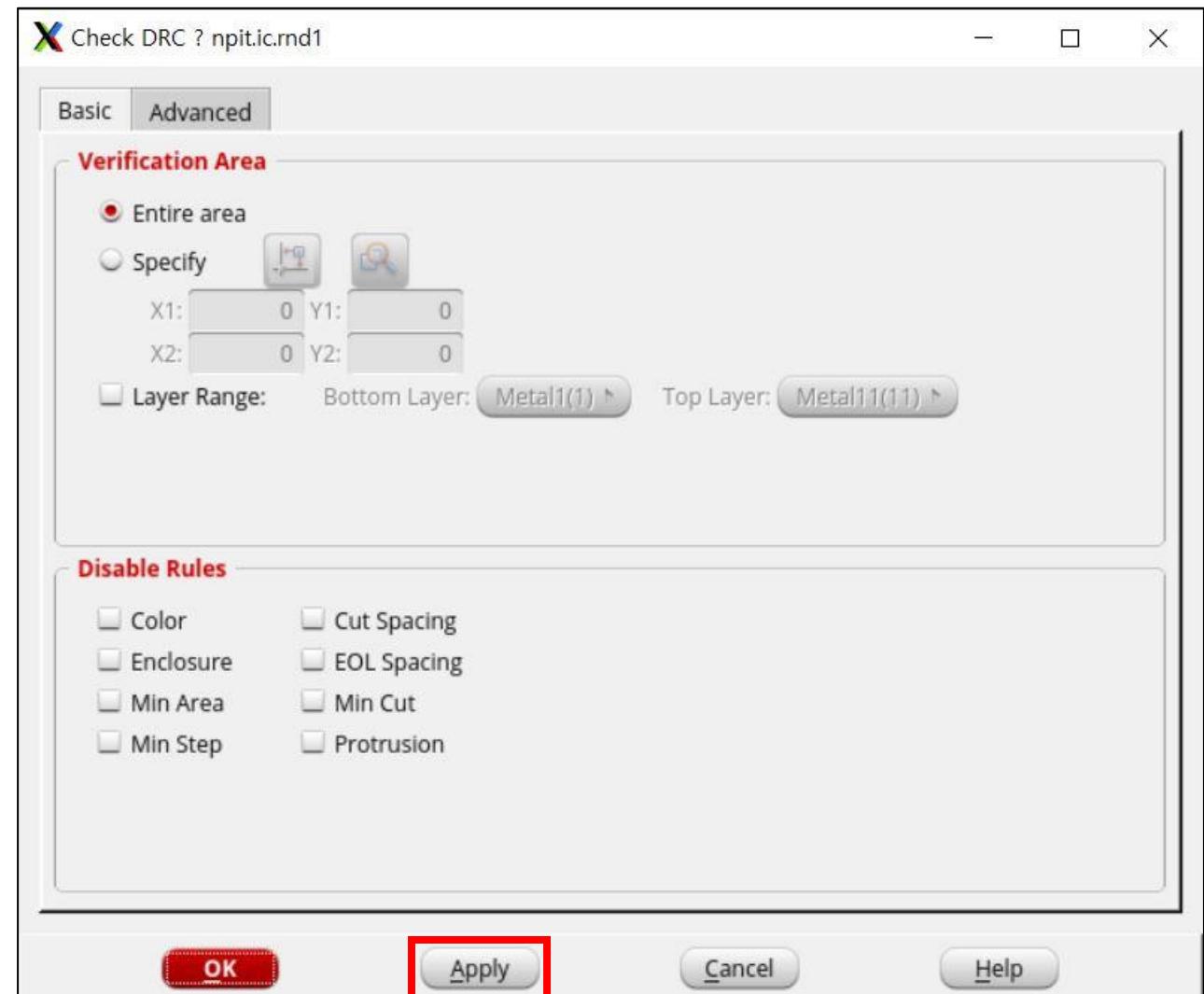
- Check - DRC



Auto PnR

Innovus

- Check – DRC
- 오른쪽 창과 똑같이 설정 후 Apply 클릭



Auto PnR

Innovus

- Check – DRC
- 터미널 창에서 결과 확인 가능

```
ex_poly1@npit:physical_design
File Edit View Search Terminal Help

route_special created 21 wires.
ViaGen created 126 vias, deleted 0 via to avoid violation.
+-----+-----+
| Layer |     Created    |     Deleted   |
+-----+-----+
| Metal1 |         21        |       NA      |
| Via1  |         14        |       0       |
| Via2  |         14        |       0       |
| Via3  |         14        |       0       |
| Via4  |         14        |       0       |
| Via5  |         14        |       0       |
| Via6  |         14        |       0       |
| Via7  |         14        |       0       |
| Via8  |         14        |       0       |
| Via9  |         14        |       0       |
+-----+-----+
#-check_ndr_spacing auto          # enums={true false auto}, default=auto, user setting
#-check_same_via_cell true        # bool, default=false, user setting
#-report counter.drc.rpt         # string, default="", user setting
*** Starting Verify DRC (MEM: 2087.5) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 18.400 15.580} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

Verification Complete : 0 Viols.          DRC 위반 없음
*** End Verify DRC (CPU TIME: 0:00:00.0  ELAPSED TIME: 0:00:00.0  MEM: 256.1M) ***
```

Auto PnR

Innovus

- Running Placement Optimization - 명령과 결과 확인

①

read_def counter.scandef

Front-End 단계에서 스캔했던 플립플롭의
순서정보를 툴에 입력

```
@innovus 3> read_def counter.scandef
Reading DEF file 'counter.scandef', current time is Mon Feb 24 03:03:58 2025 ...
--- CASESENSITIVE ON
--- DIVIDERCHAR '/'
DEF file 'counter.scandef' is parsed, current time is Mon Feb 24 03:03:59 2025.
```

②

set_db reorder_scan_comp_logic true

셀의 위치 조정을 가능하게 함

```
ruenovus 4> set_db reorder_scan_comp_logic true
1 true
```

Auto PnR

Innovus

- Running Placement Optimization - 명령과 결과 확인

③

place_opt_design

디자인을 최적화하는 단계임

- 버퍼 생성
- 게이트 크기 조정
- 회로 재구성
- 회로 remapping
- 핀 스와핑
- 버퍼 삭제
- 인스턴스 이동

```
Info: Summary of CRR changes:  
      - Timing transform commits:          0  
Disable CTE adjustment.  
Disable Layer aware incrSKP.  
#optDebug: fT-D <X 1 0 0 0>  
**place_opt_design ... cpu = 0:00:09, real = 0:00:32, mem = 2523.9M **  
*** Finished GigaPlace ***
```

```
*** Summary of all messages that are not suppressed in this session:
```

Severity	ID	Count	Summary
WARNING	IMPEXT-3530	3	The process node is not set. Use the com...
WARNING	IMPSP-5140	2	Global net connect rules have not been c...
WARNING	IMPSP-315	2	Found %d instances insts with no PG Term...
WARNING	IMPOPT-576	1	%d nets have unplaced terms.
WARNING	IMPOPT-3195	2	Analysis mode has changed.
WARNING	IMPOPT-665	13	%s : Net has unplaced terms or is connec...
WARNING	TCLCMD-513	94	The software could not find a matching o...
ERROR	TCLCMD-917	2	Cannot find '%s'

*** Message Summary: 117 warning(s), 2 error(s)

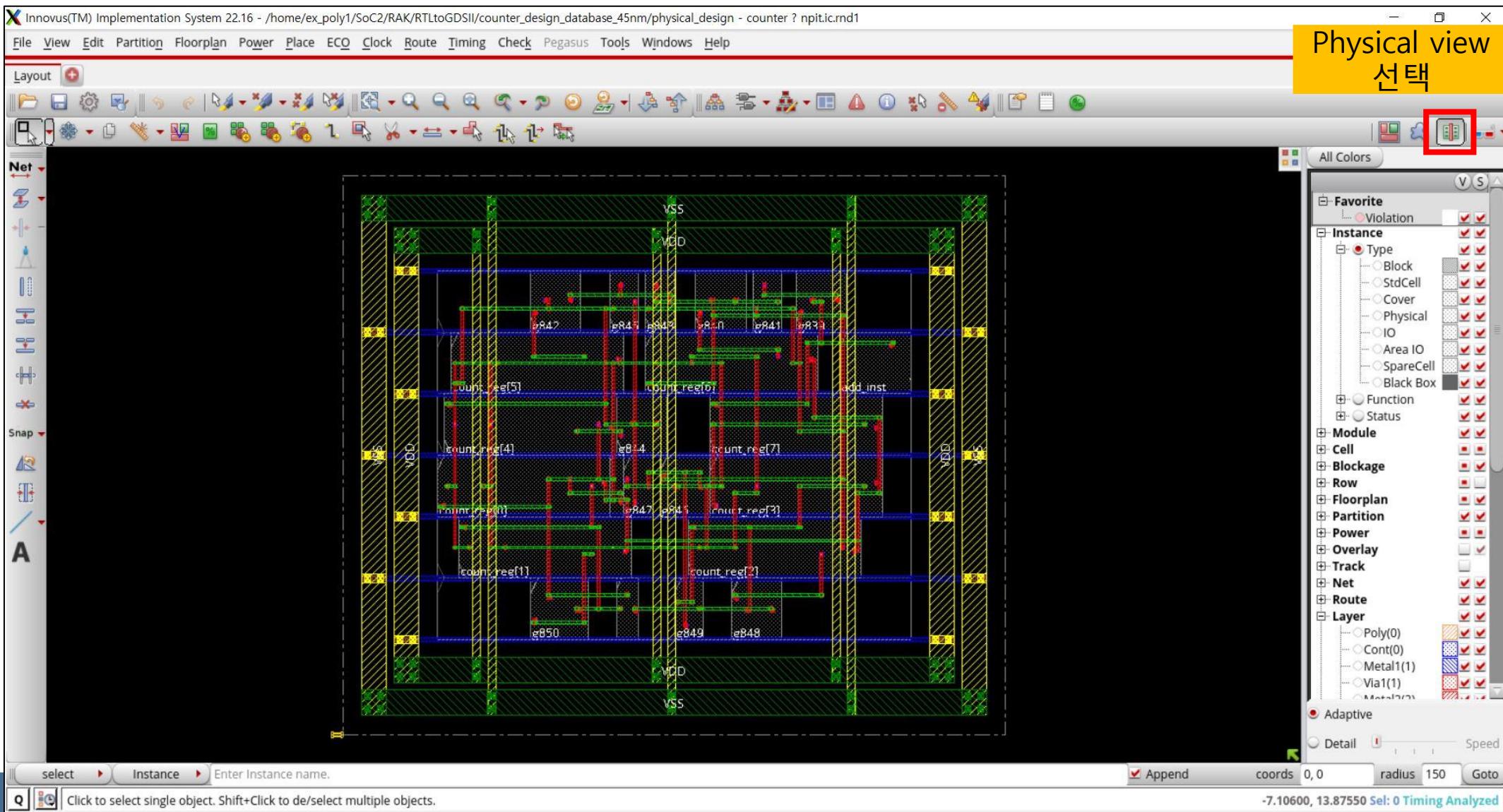
2개의 에러가 발생하지만 나중에
해결되므로 스킵

```
*** place_opt_design #1 [finish] () : cpu/real = 0:00:09.3/0:00:31.8 (0.3), totSession cpu/real = 0:0  
3:15.5/1:12:35.3 (0.0), mem = 2523.9M
```

Auto PnR

Innovus

- Running Placement Optimization



Auto PnR

Innovus

- Running Placement Optimization - 명령과 결과 확인

④

write_db placeOpt

Place 결과를 저장함

```
[ex_poly1@npit physical_design]$ ls
collectGenusLibrary.log    innovus.log1
counter.drc.rpt            innovus.log2
counter.scandef          innovus.logv
counter.view             innovus.logv1
counter_netlist.v        innovus.logv2
counter_sdc.sdc
1_8JtZ8a
innovus.cmd
innovus.cmd1
innovus.cmd2
innovus.log
```

placeOpt 폴더가 생성됨

placeOpt
power.tcl
readme
timingReports

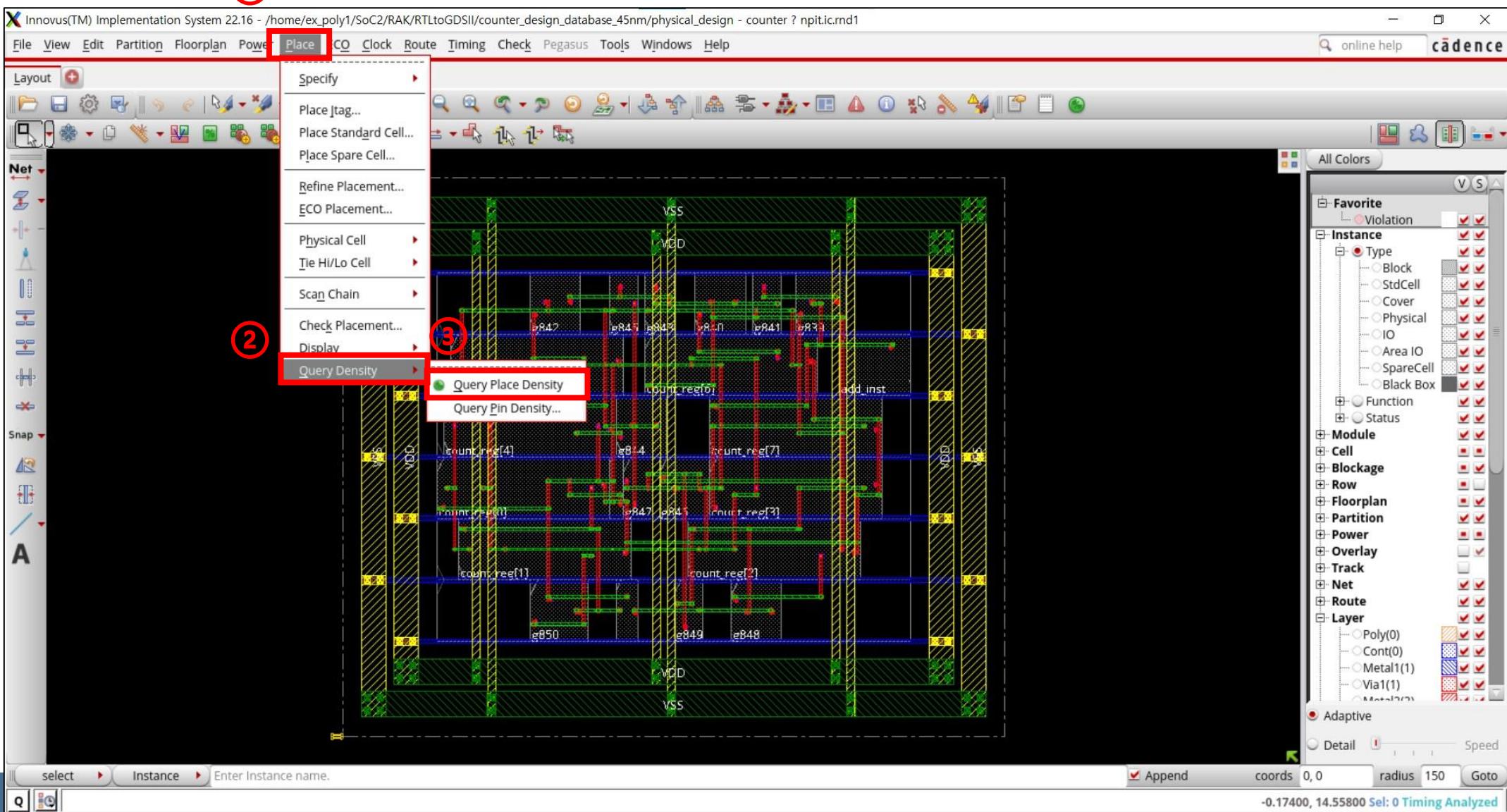
```
*** 1 scan chain passed sanity check.
Saving property file placeOpt/counter.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=2722.6M) ***
Saving rc congestion map placeOpt/counter.congmap.gz ...
% Begin Save power constraints data ... (date=02/24 03:43:10, mem=2069.0M)
% End Save power constraints data ... (date=02/24 03:43:10, total cpu=0:00:00.0, real=0:00:00.0, peak
res=2069.1M, current mem=2069.1M)
Generated self-contained design placeOpt
#% End save design ... (date=02/24 03:43:11, total cpu=0:00:01.7, real=0:00:02.0, peak res=2072.4M,
current mem=2072.4M)
*** Message Summary: 0 warning(s), 0 error(s)
```

에러가 사라진 것을 확인함

Auto PnR

Innovus

- Running Placement Optimization – Query Place Density



Auto PnR

Innovus

- Running Placement Optimization – Query Place Density

```
Checking Preroutes.....
No. of regular pre-routes not on tracks : 0

Reporting Utilizations.....
Core utilization = 69.949495 Core utilization 약 70%임을 확인함
Effective Utilizations
Average macro density = 0.000.
Average module density = 0.699.
Pure std cell Density 0.699495
Density for the design = 0.699.
= stdcell_area 277 sites (95 um2) / alloc_area 396 sites (135 um2).
Pin Density = 0.2626.
= total # of pins 104 / total area 396.
*** Message Summary: 0 warning(s), 0 error(s) Warning, error 없음
```

Auto PnR

Innovus

- Running Clock Tree Synthesis - 명령과 결과 확인

①

create_clock_tree_spec

입력에 넣었던 sdc 파일을 이용해 spec by constraint 생성함

```
@innovus 7> create_clock_tree_spec
Creating clock tree spec for modes (timing configs): sdc_cons
cts_spec_config_create_generator_skew_groups=true: create_clock_tree_spec will generate skew groups w
ith a name prefix of "_clock_gen" to balance clock generator connected flops with the clock generator
they drive.
Reset timing graph...
Ignoring AAE DB Resetting ...
Reset timing graph done.
Ignoring AAE DB Resetting ...
Analyzing clock structure...
Analyzing clock structure done.
Reset timing graph...
Ignoring AAE DB Resetting ...
Reset timing graph done.
Extracting original clock gating for clk...
    clock_tree clk contains 8 sinks and 0 clock gates.
Extracting original clock gating for clk done.
The skew group clk/sdc_cons was created. It contains 8 sinks and 1 sources.
Checking clock tree convergence...
Checking clock tree convergence done.
```

Auto PnR

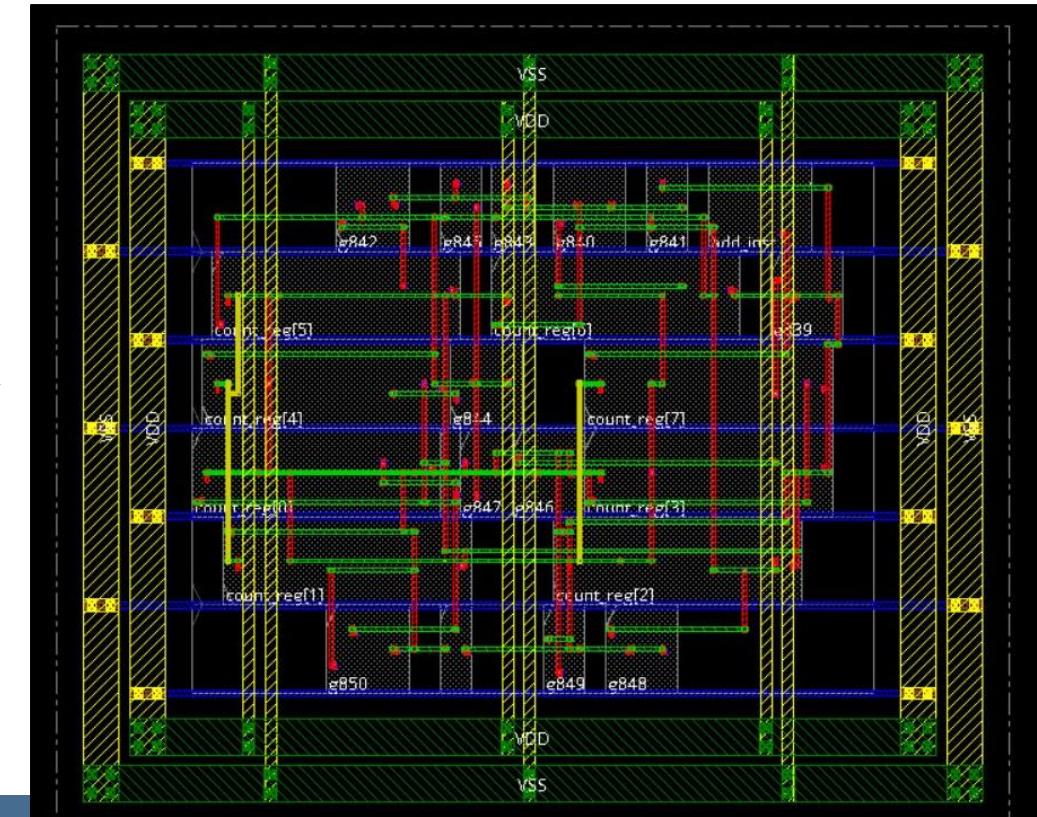
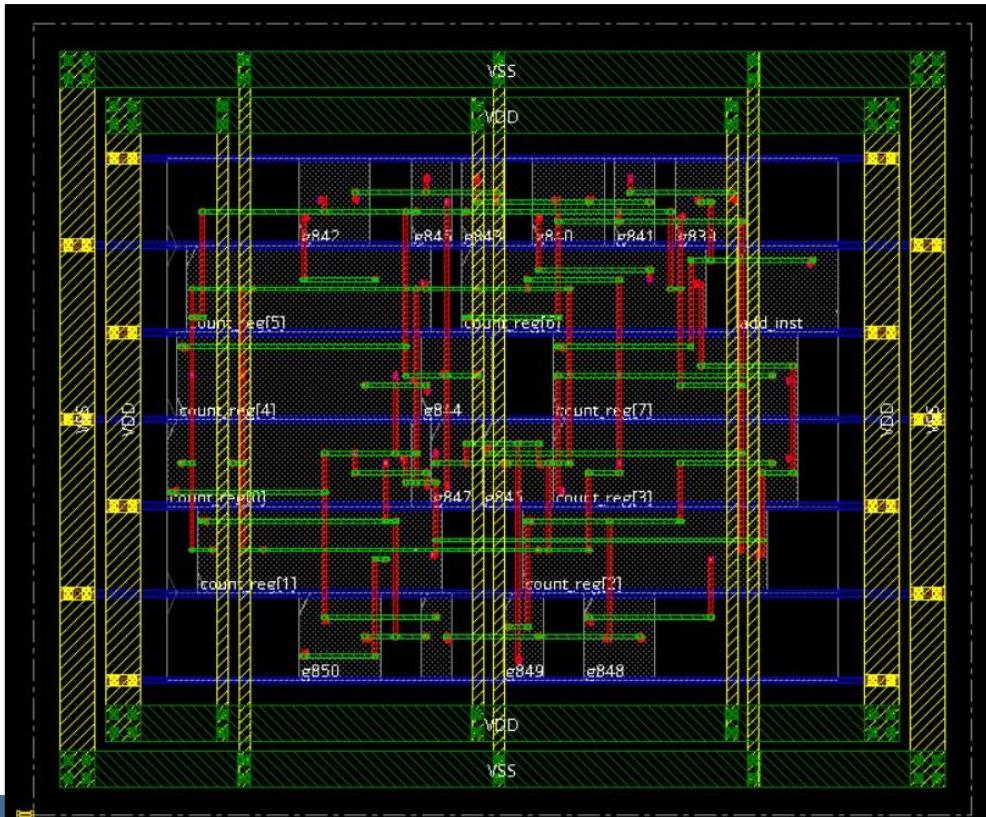
Innovus

- Running Clock Tree Synthesis - CTS를 통해 Uncertainty, Transition, Latency가 확실해짐

②

ccopt_design

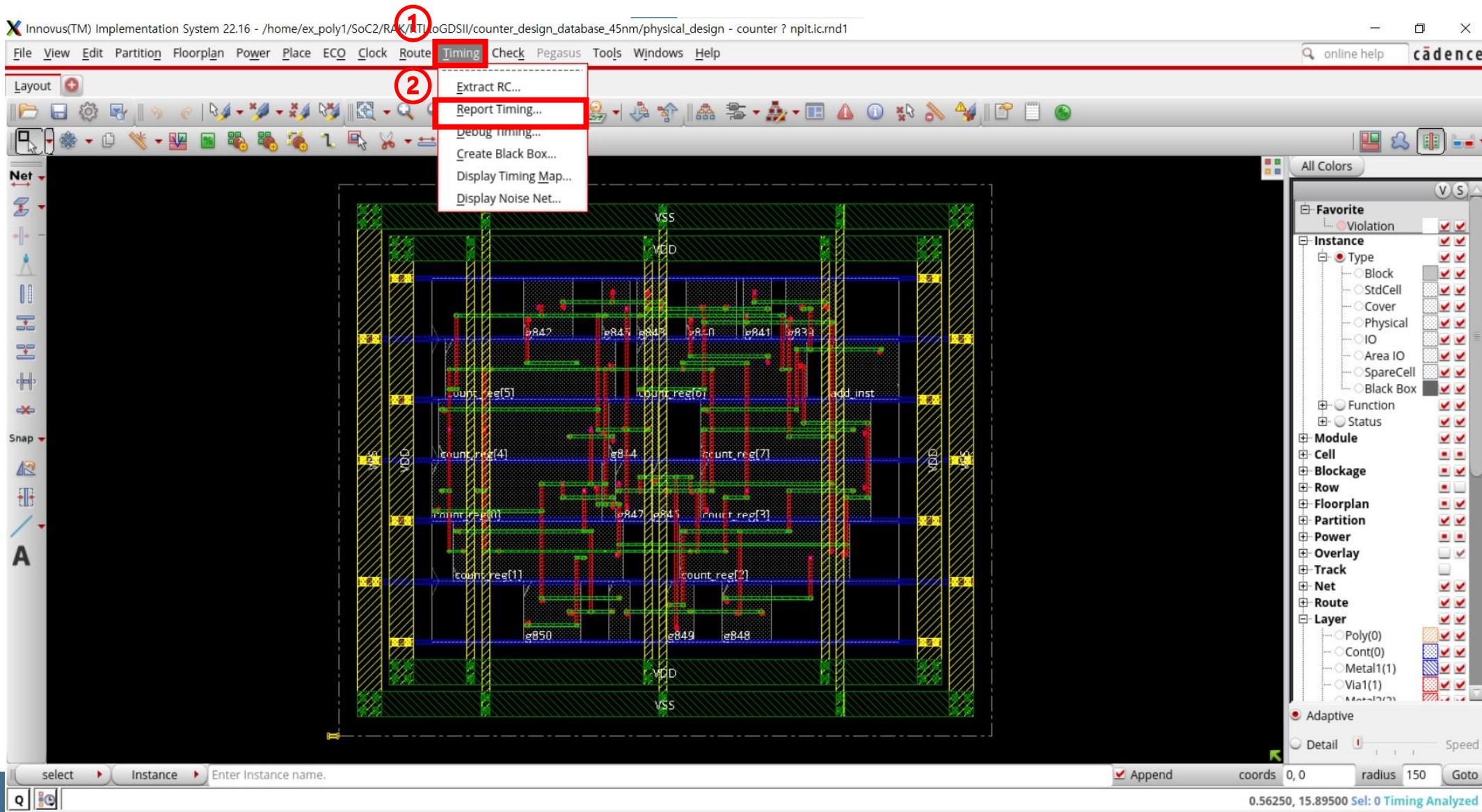
실제로 클럭을 생성함 (gui에 변화가 일어 남)



Auto PnR

Innovus

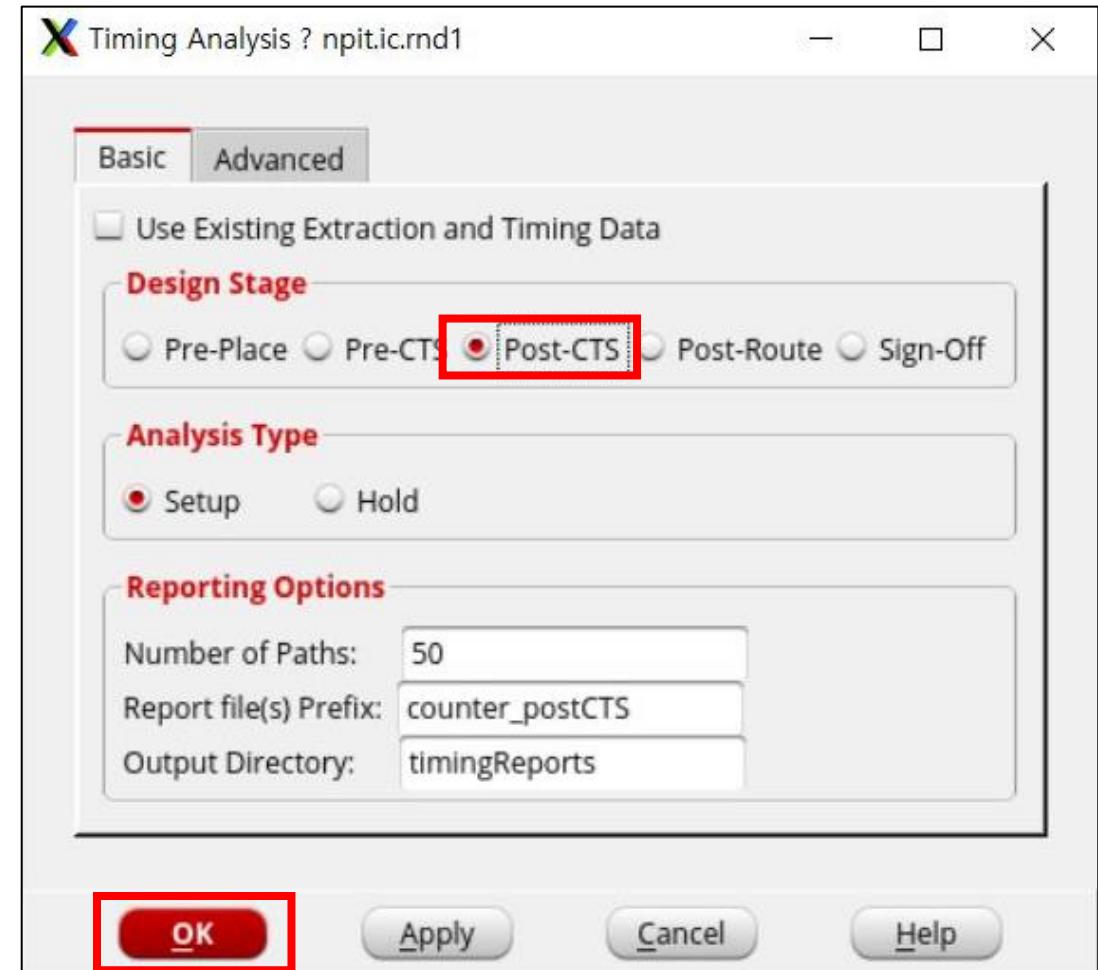
- Running Clock Tree Synthesis – report timing



Auto PnR

Innovus

- Running Clock Tree Synthesis – report timing
- 오른쪽 창과 똑같이 설정 후 Apply 클릭



Auto PnR

Innovus

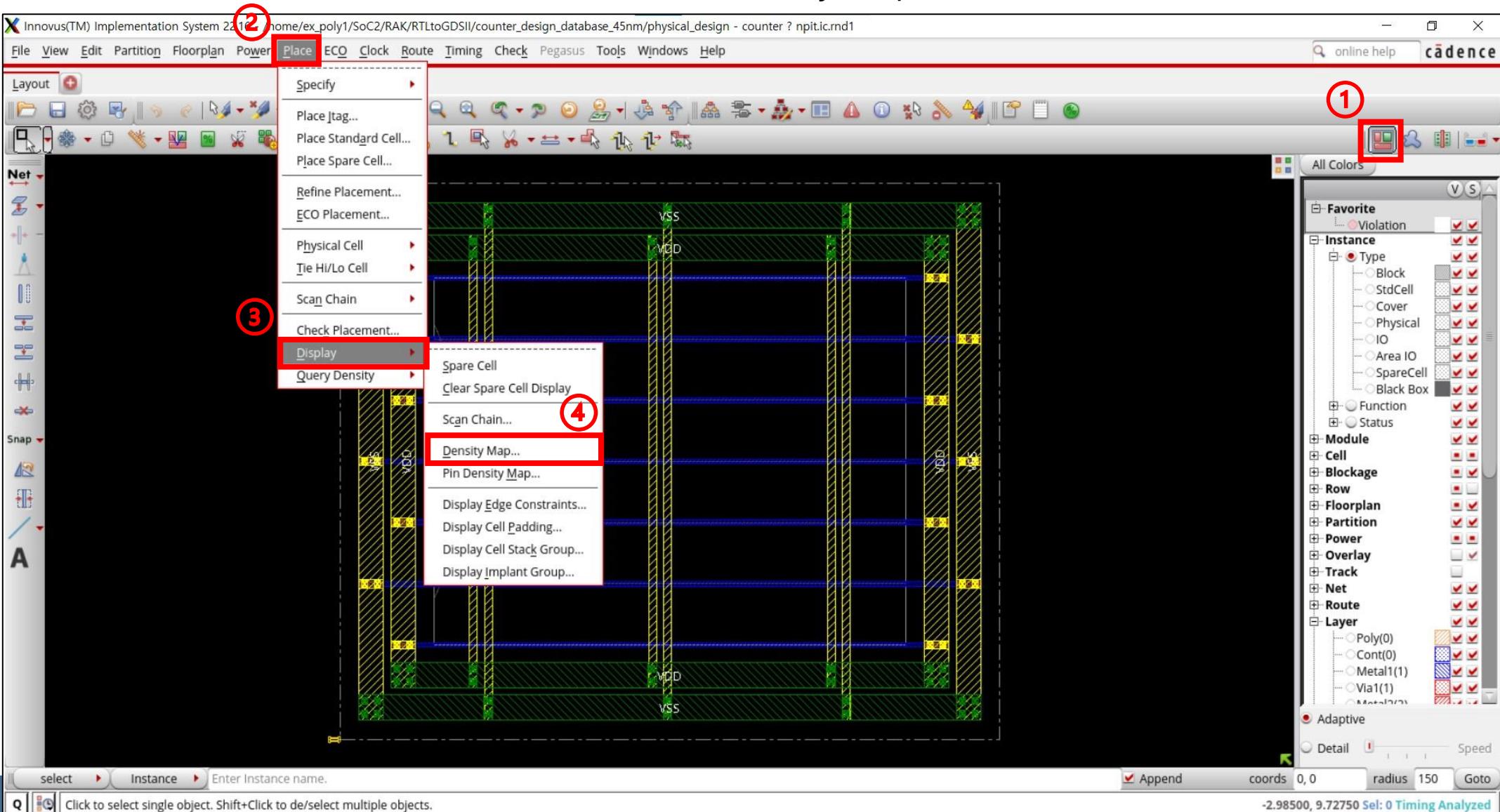
- Running Clock Tree Synthesis – report timing 결과

Setup views included:				Route 전이므로 setup time만 확인 가능
WC				
Setup mode	all	reg2reg	default	
WNS (ns):	8.430	8.430	8.691	
TNS (ns):	0.000	0.000	0.000	
Violating Paths:	0	0	0	
All Paths:	40	15	25	
DRVs	Real		Total	
	Nr nets(terms)	Worst Vio	Nr nets(terms)	
max_cap	0 (0)	0.000	0 (0)	
max_tran	0 (0)	0.000	0 (0)	
max_fanout	0 (0)	0	0 (0)	
max_length	0 (0)	0	0 (0)	
Density: 69.949%	Density가 대략 70%임을 확인			
Routing Overflow: 0.00% H and 0.00% V				
Reported timing to dir timingReports				
Total CPU time: 0.43 sec				
Total Real time: 1.0 sec				
Total Memory Usage: 2564.652344 Mbytes				
*** time_design #1 [finish] () : cpu/real = 0:00:00.4/0:00:00.9 (0.5),				

Auto PnR

Innovus

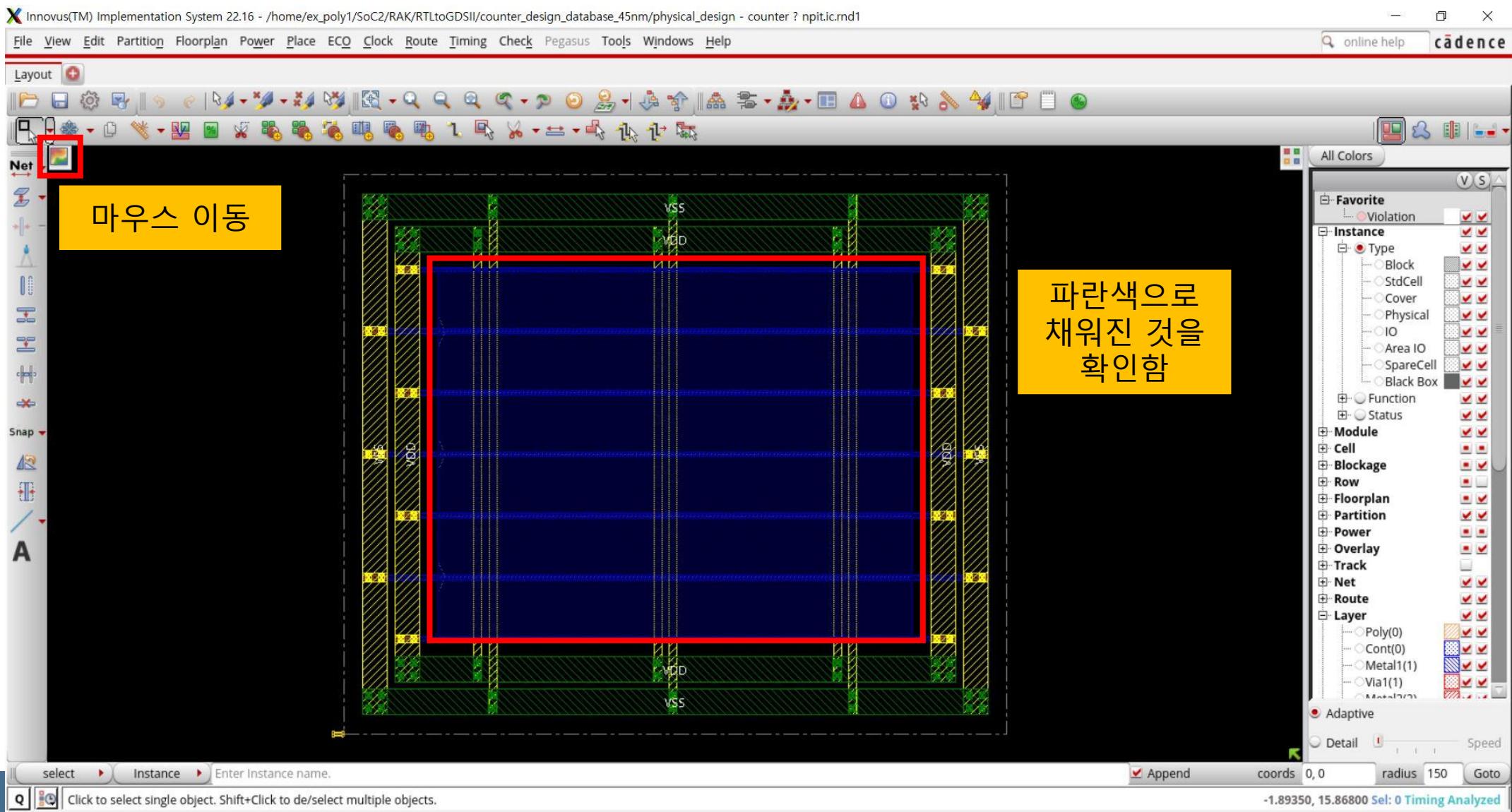
- Place - Density Map



Auto PnR

Innovus

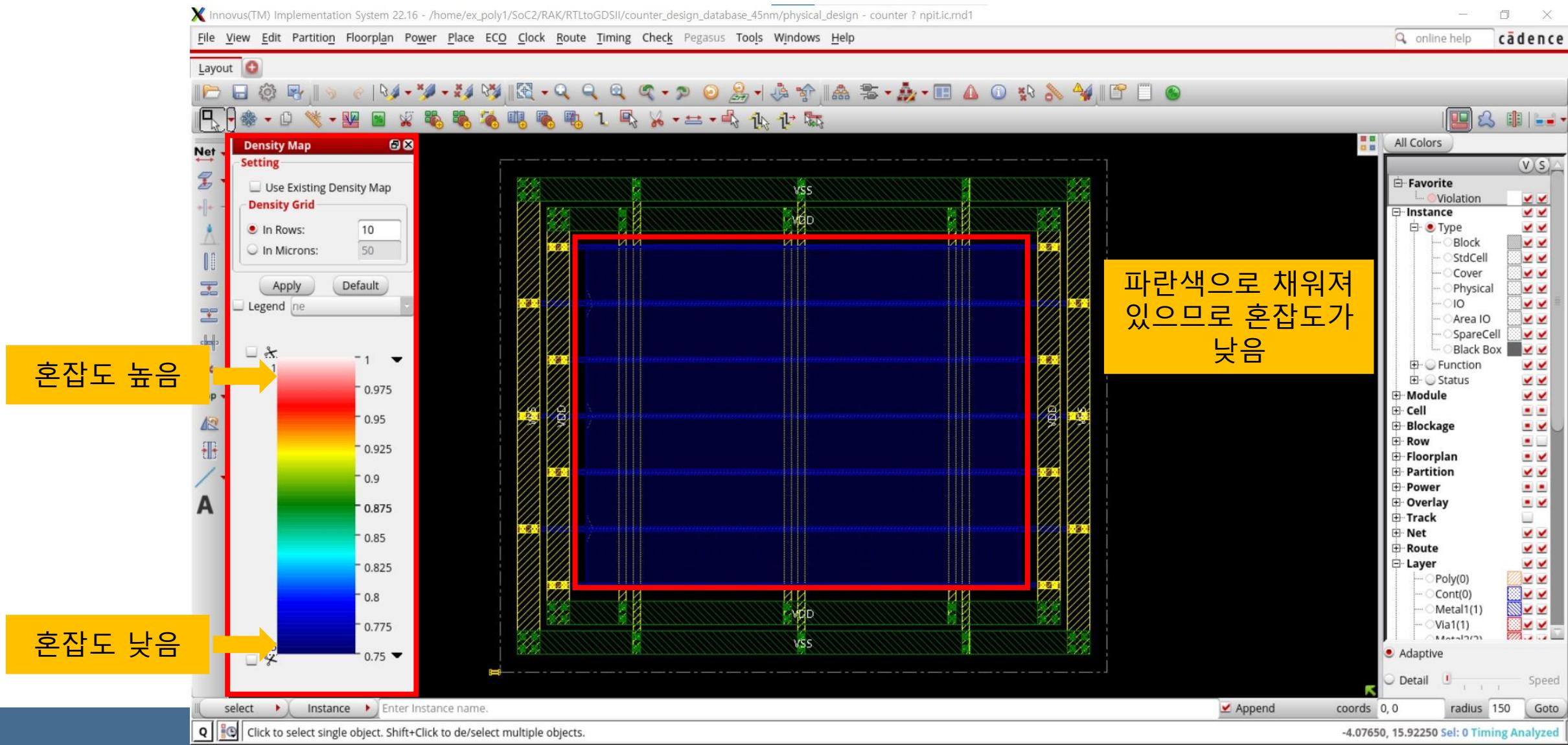
- Place - Density Map



Auto PnR

Innovus

- Place - Density Map



Auto PnR

Innovus

- Running Clock Tree Synthesis - 명령과 결과 확인

③

write_db postCTSoft

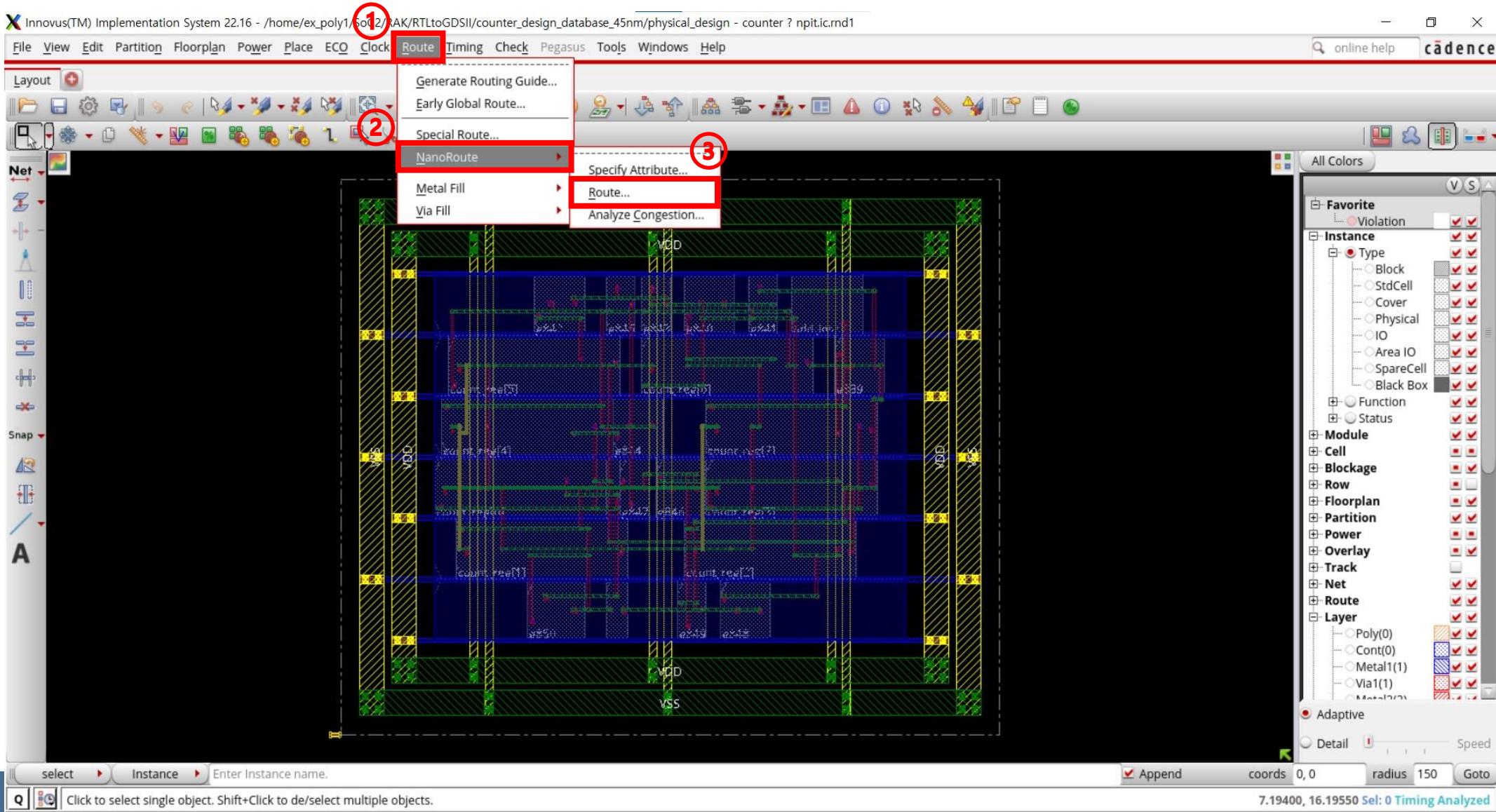
CTS(Clock Tree Synthesis) 결과를
postCTSoft 폴더에 저장함

```
2M, current mem=2062.2M)
Saving SCANDEF file ...
*** Scan Trace Summary (runtime: cpu: 0:00:00.0 , real: 0:00:00.0):
Successfully traced 1 scan chain (total 8 scan bits).
Start applying DEF ordered sections ...
Successfully applied all DEF ordered sections.
*** Scan Sanity Check Summary:
*** 1 scan chain passed sanity check.
Saving property file postCTSoft/counter.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=2769.2M) ***
Saving rc congestion map postCTSoft/counter.congmap.gz ...
% Begin Save power constraints data ... (date=02/24 14:23:25, mem=2062.2M)
% End Save power constraints data ... (date=02/24 14:23:25, total cpu=0:00:00.0, real=0:00:00.0, peak
res=2062.2M, current mem=2062.2M)
Generated self-contained design postCTSoft
#% End save design ... (date=02/24 14:23:26, total cpu=0:00:01.7, real=0:00:02.0, peak res=2063.0M, c
urrent mem=2063.0M)
*** Message Summary: 0 warning(s), 0 error(s)
```

Auto PnR

Innovus

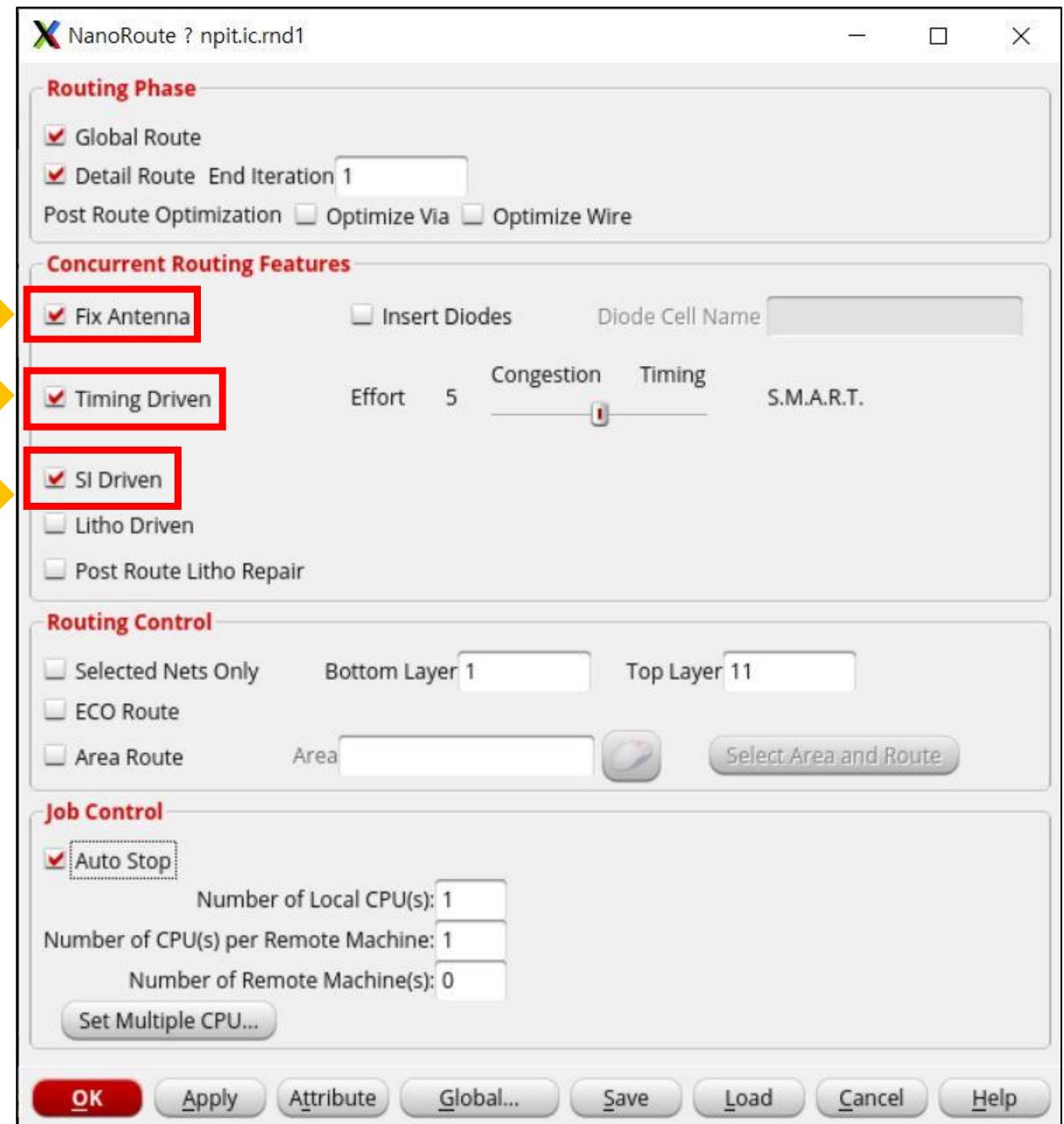
- Routing the Nets



Auto PnR

Innovus

- 안테나 효과 발생시 제거함
- 타이밍을 고려함
- 서로 근접한 Net의 신호를 고려함

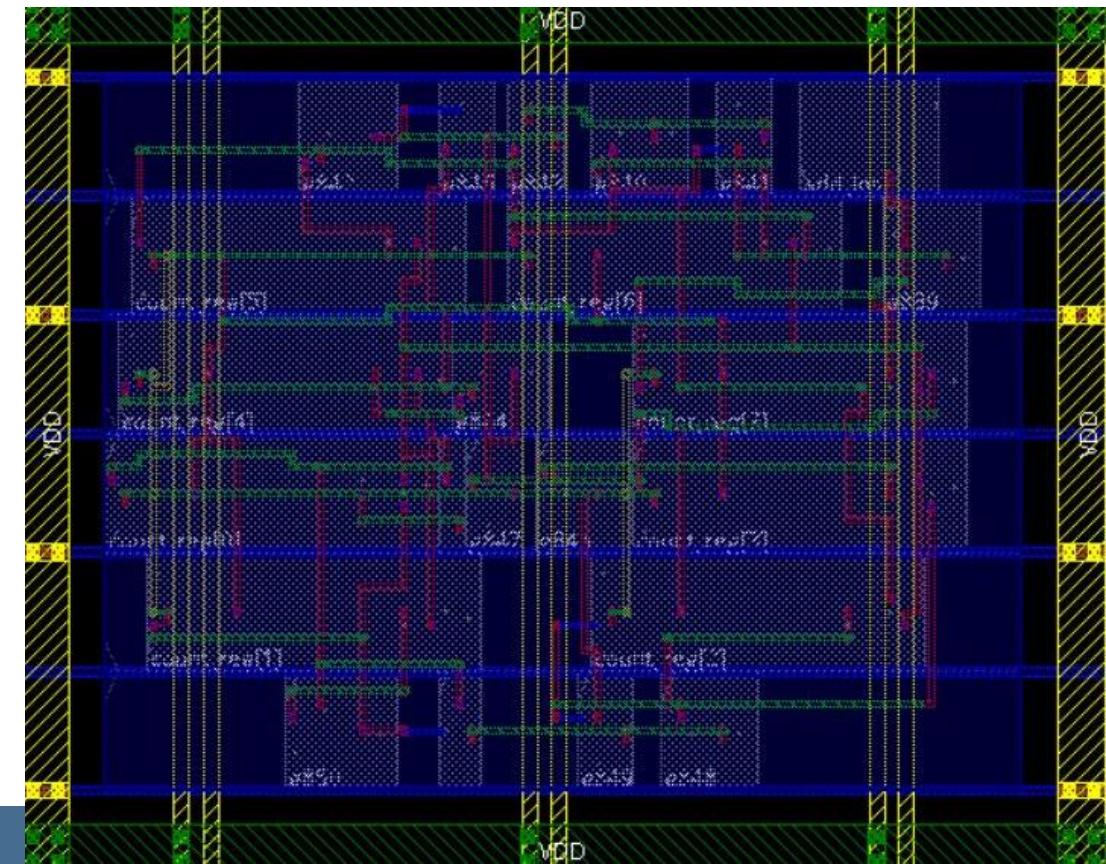
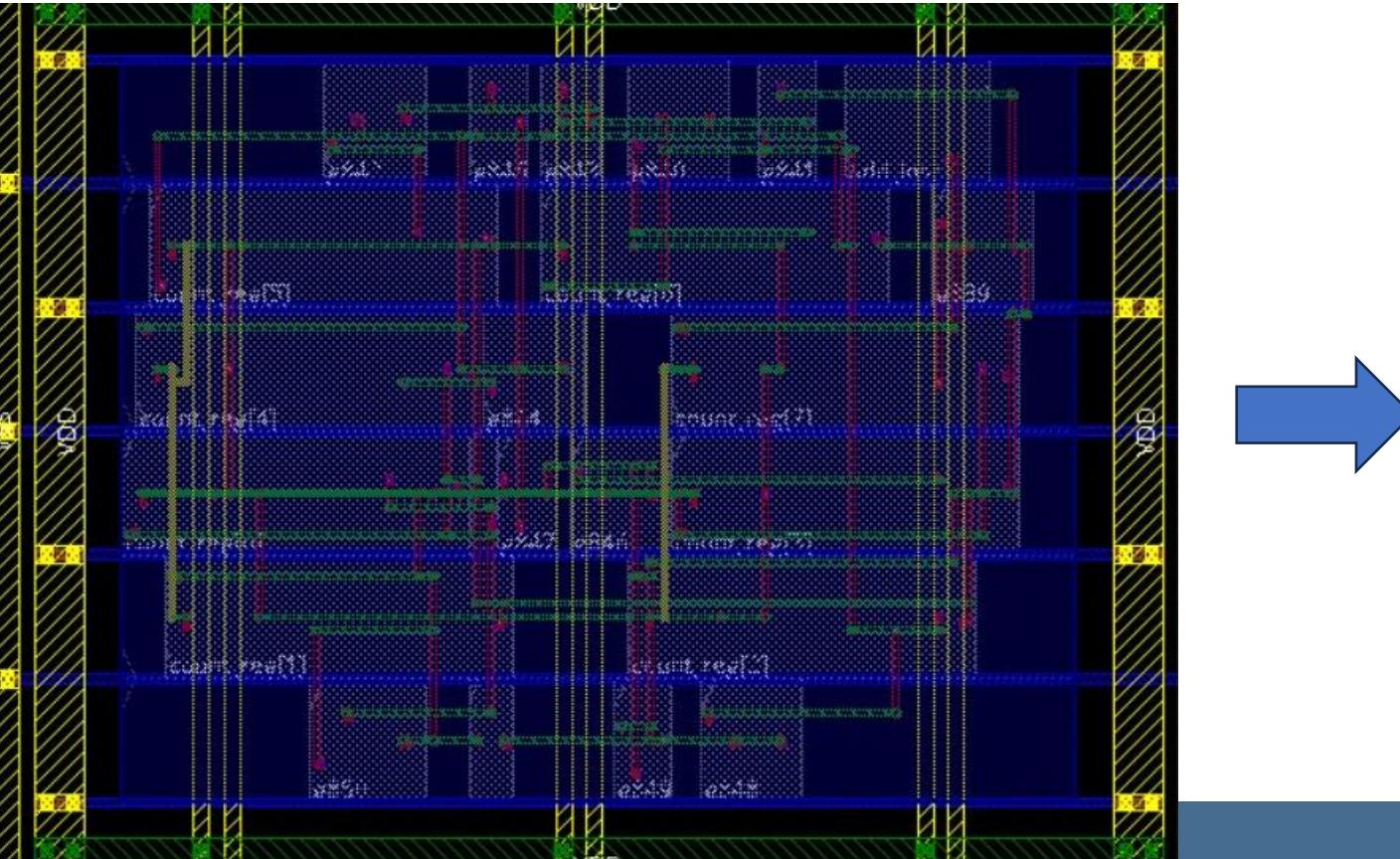


- Routing the Nets
- 오른쪽 창과 똑같이 설정 후 Apply 클릭

Auto PnR

Innovus

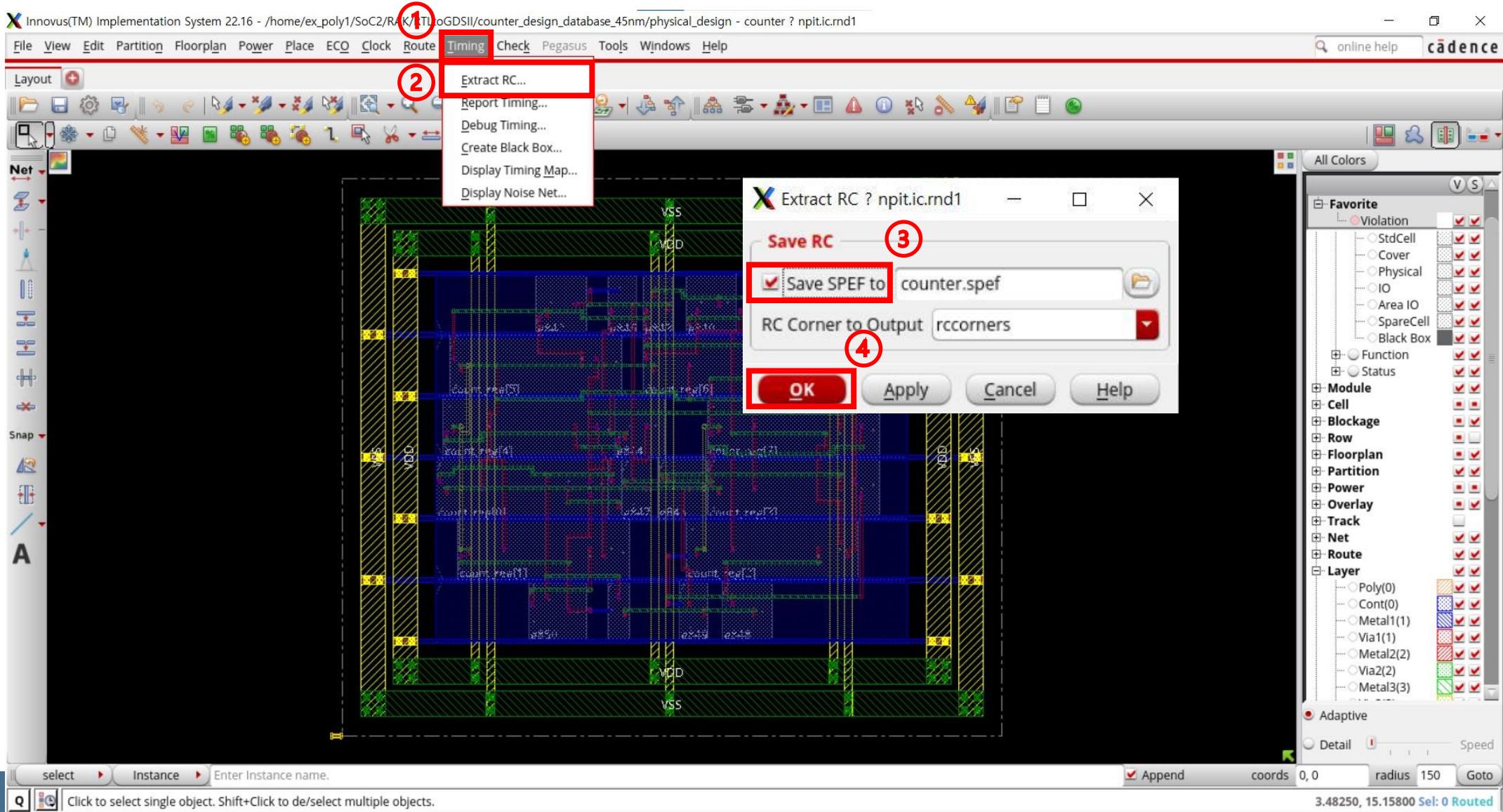
- Routing the Nets
- 설정 값을 고려하여 배선이 바뀜



Auto PnR

Innovus

- Extraction and Timing Analysis



Auto PnR

Innovus

- Extraction and Timing Analysis
- 기생 RC의 정보를 알 수 있는 spef 파일을 생성함
- 타이밍에 대한 정확한 정보를 얻을 수 있음

```
RCMode: PreRoute
    RC Corner Indexes          0
    Capacitance Scaling Factor : 1.000000
    Resistance Scaling Factor : 1.000000
    Clock Cap. Scaling Factor : 1.000000
    Clock Res. Scaling Factor : 1.000000
    Shrink Factor              : 0.900000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC Grid density data for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
Creating RPSQ from WeeR and WRes ...
```

```
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Read: 0.000000 M)
@innovus 40> write_parasitics -spef_file counter.spef ...
**ERROR: (IMPEXT-7102): There are net(s) in the design with open terms. Air fixing, which involves adding estimated RC elements to connect or complete the broken RC graph, will not be done while writing the SPEF.
```

```
Type 'man IMPEXT-7102' for more detail.
```

툴을 사용하는 연습 과정이므로
에러는 무시하고 진행함 M)

Auto PnR

Innovus

- Extraction and Timing Analysis

타이밍에 대한 Analysis 타입을
ocv(on chip variation)로 할 것임

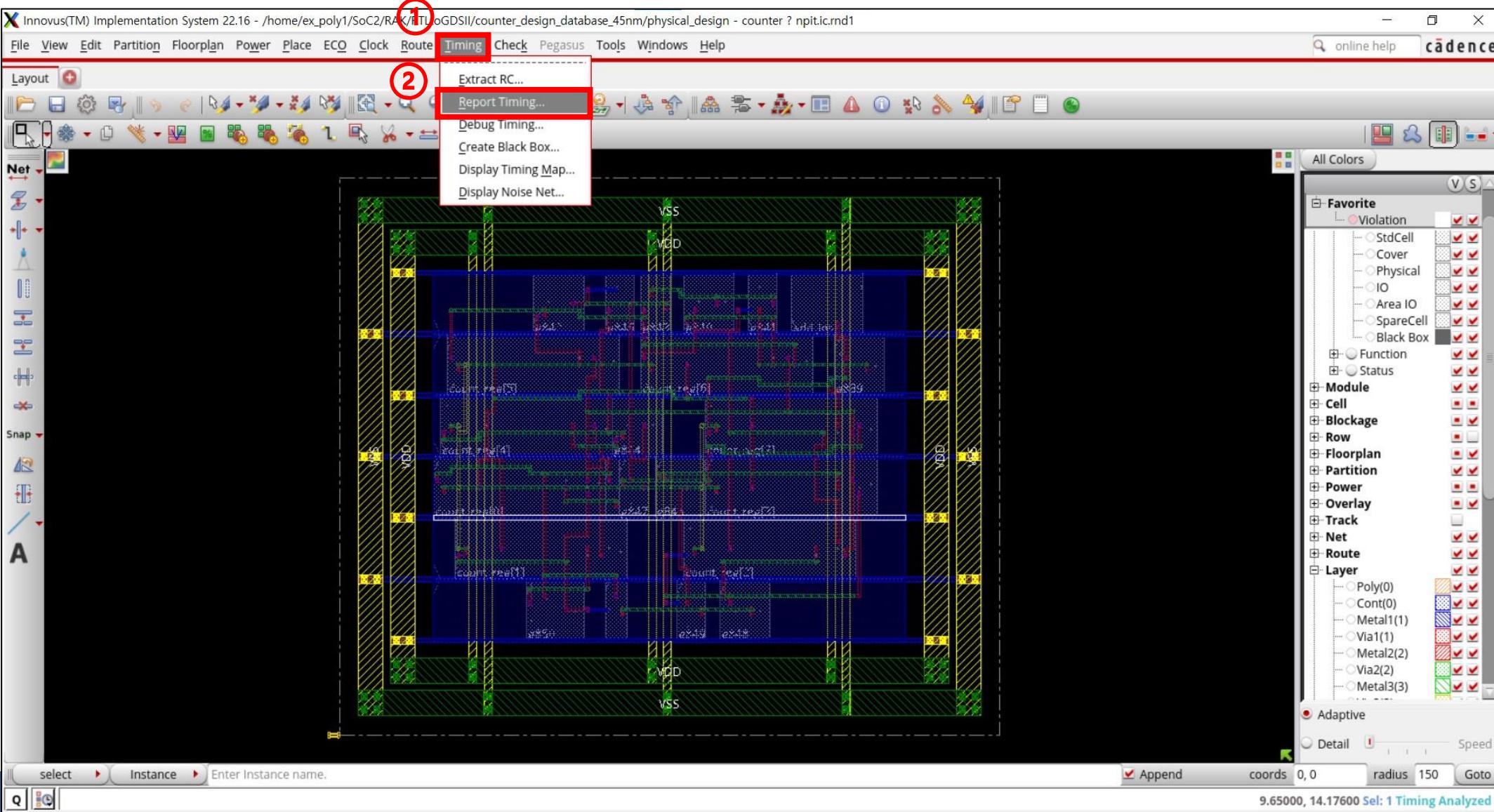
① set_db timing_analysis_type ocv

```
@innovus 42> set_db timing_analysis_type ocv
1 ocv
```

Auto PnR

Innovus

- Extraction and Timing Analysis – Report Timing

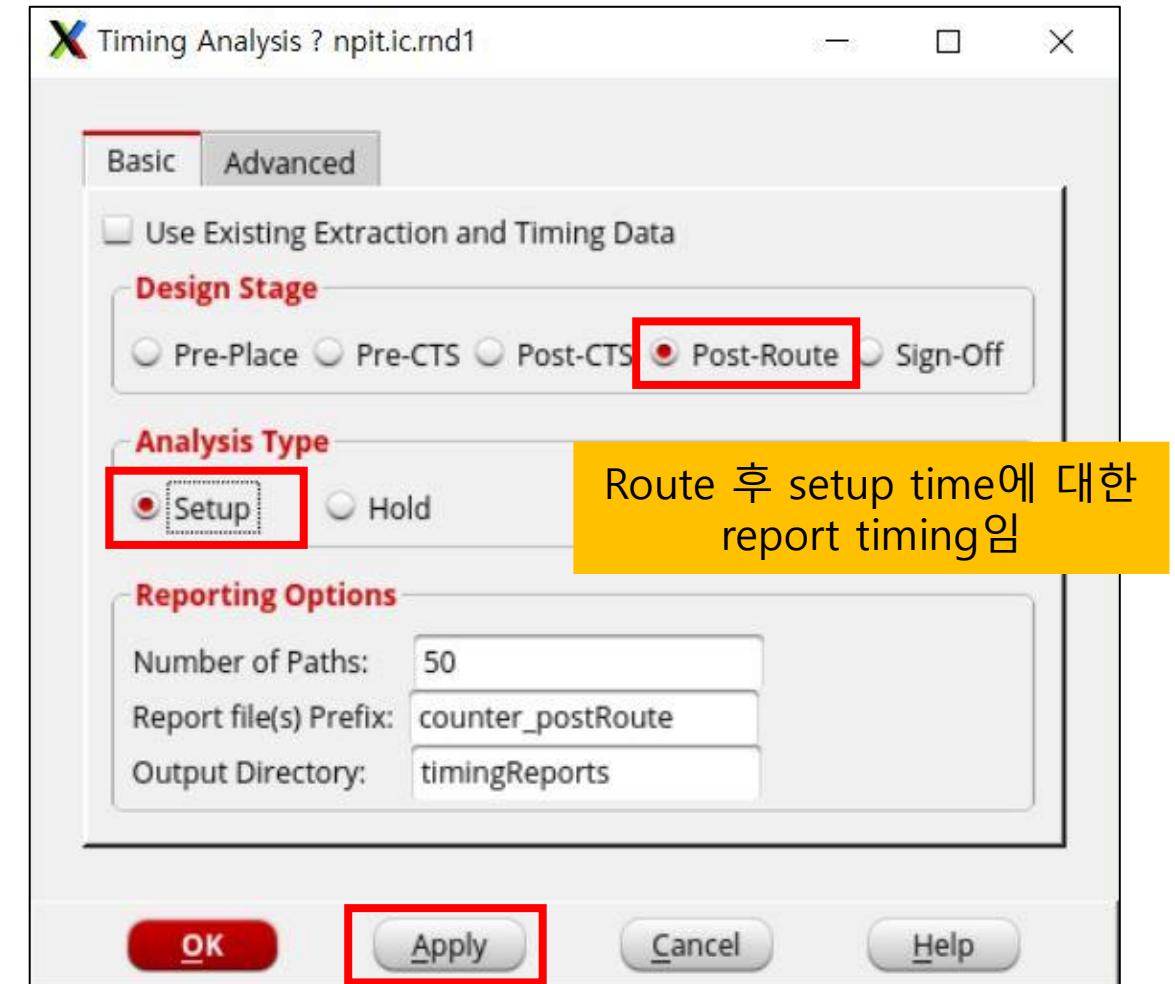


Auto PnR

Innovus

- Extraction and Timing Analysis – Report Timing
- 오른쪽 창과 똑같이 설정 후 Apply 클릭
- 아래의 명령으로도 확인 가능

```
time_design -post_route
```



Auto PnR

Innovus

- Extraction and Timing Analysis – Report Timing
- Setup time 결과

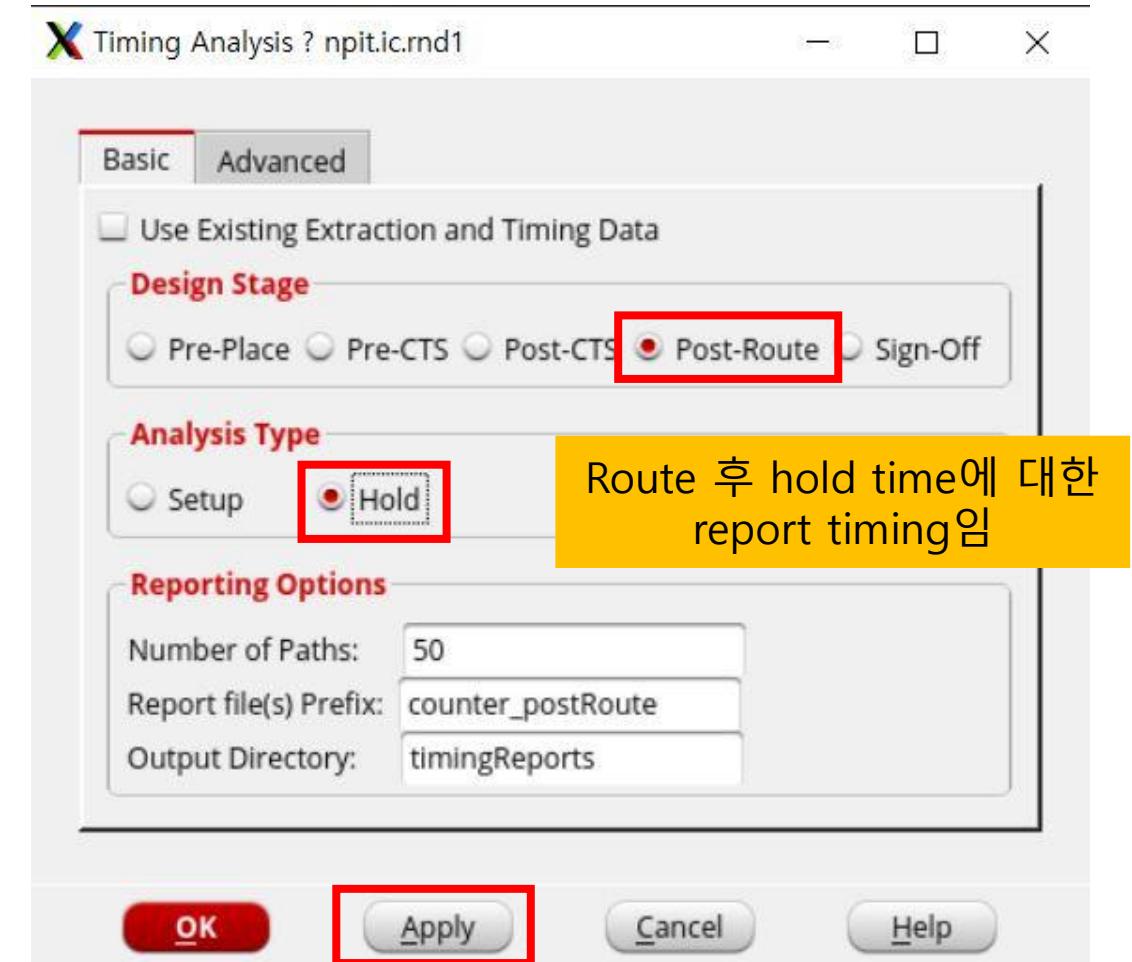
```
Setup views included:  
wc  
  
+-----+-----+-----+  
| Setup mode | all | reg2reg | default |  
+-----+-----+-----+  
| WNS (ns): | 8.443 | 8.443 | 8.737 |  
| TNS (ns): | 0.000 | 0.000 | 0.000 |  
| Violating Paths: | 0 | 0 | 0 |  
| All Paths: | 40 | 15 | 25 |  
+-----+-----+-----+  
  
+-----+-----+-----+  
| DRVs | Real | Total |  
| | Nr nets(terms) | Worst Vio | Nr nets(terms)  
+-----+-----+-----+  
| max_cap | 0 (0) | 0.000 | 0 (0) |  
| max_tran | 0 (0) | 0.000 | 0 (0) |  
| max_fanout | 0 (0) | 0 | 0 (0) |  
| max_length | 0 (0) | 0 | 0 (0) |  
+-----+-----+-----+  
Density: 69.949% Density 약 70%  
  
Reported timing to dir timingReports  
Total CPU time: 0.96 sec  
Total Real time: 1.0 sec  
Total Memory Usage: 2782.390625 Mbytes  
Reset AAE Options  
*** time_design #2 [finish] () : cpu/real = 0:00:01.0/0:00:01.1 (0.9), totSession cpu/real = 0:03:00.4/0:49:09.3 (0.1), mem = 2782.4M
```

Auto PnR

Innovus

- Extraction and Timing Analysis – Report Timing
- 오른쪽 창과 똑같이 설정 후 Apply 클릭
- 아래의 명령으로도 확인 가능

```
time_design -post_route -hold
```



Auto PnR

Innovus

- Extraction and Timing Analysis – Report Timing
- hold time 결과

```
Hold views included:  
bc  
  
+-----+-----+-----+  
| Hold mode | all | reg2reg | default |  
+-----+-----+-----+  
| WNS (ns):| -0.093 | -0.025 | -0.093 |  
| TNS (ns):| -1.005 | -0.176 | -0.828 |  
| Violating Paths:| 17 | 8 | 9 |  
| All Paths:| 24 | 15 | 9 |  
+-----+-----+-----+
```

음수 값 발생

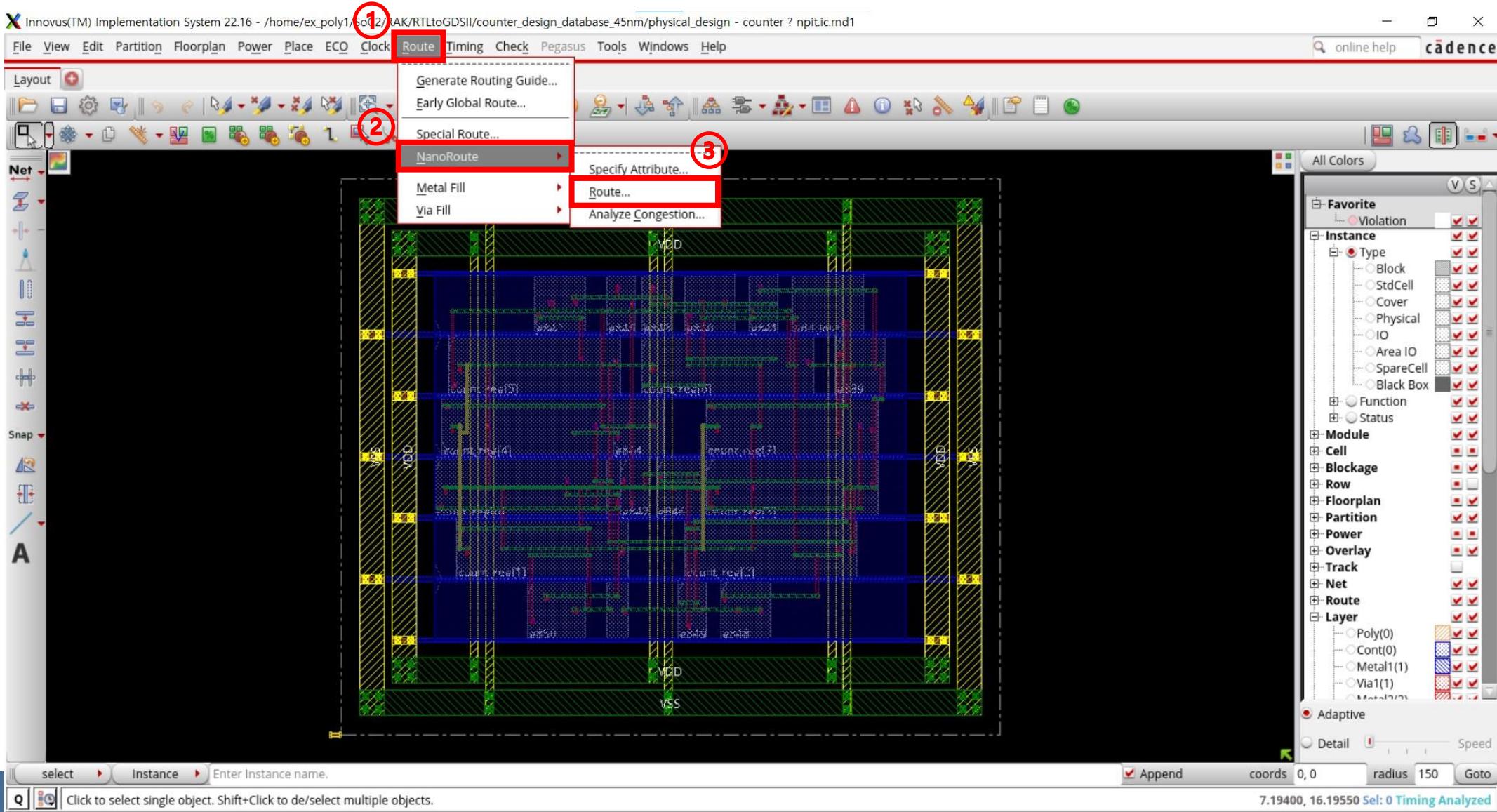
Density: 69.949% Density 약 70%

```
Reported timing to dir timingReports  
Total CPU time: 0.92 sec  
Total Real time: 1.0 sec  
Total Memory Usage: 2732.230469 Mbytes  
Reset AAE Options  
*** time_design #3 [finish] () : cpu/real = 0:00:00.9/0:00:01.1 (0.8), totSession cpu/real = 0:03:15.6/0:56:43.8 (0.1), mem = 2732.2M
```

Auto PnR

Innovus

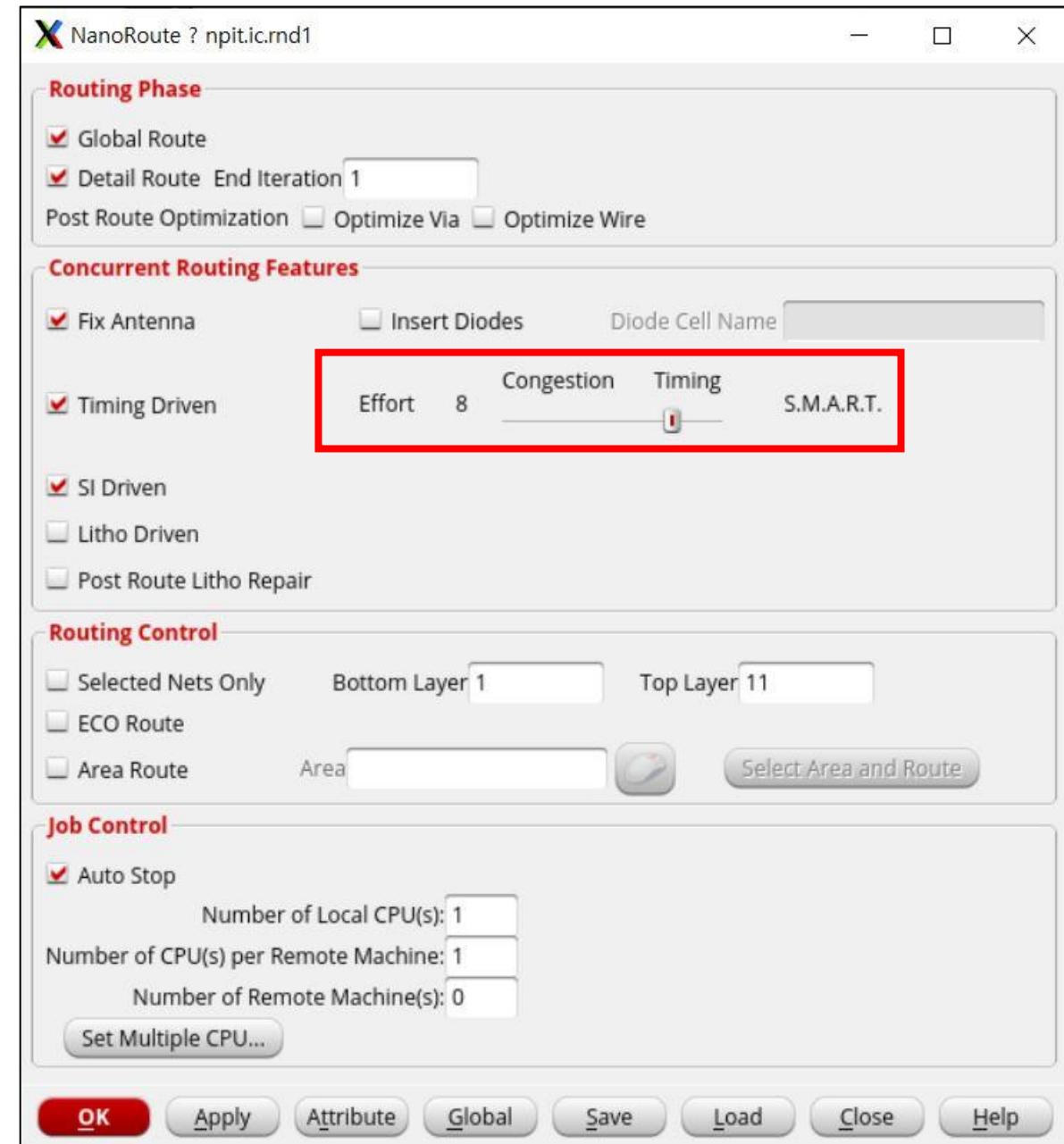
- hold time 음수 값 수정



Auto PnR

Innovus

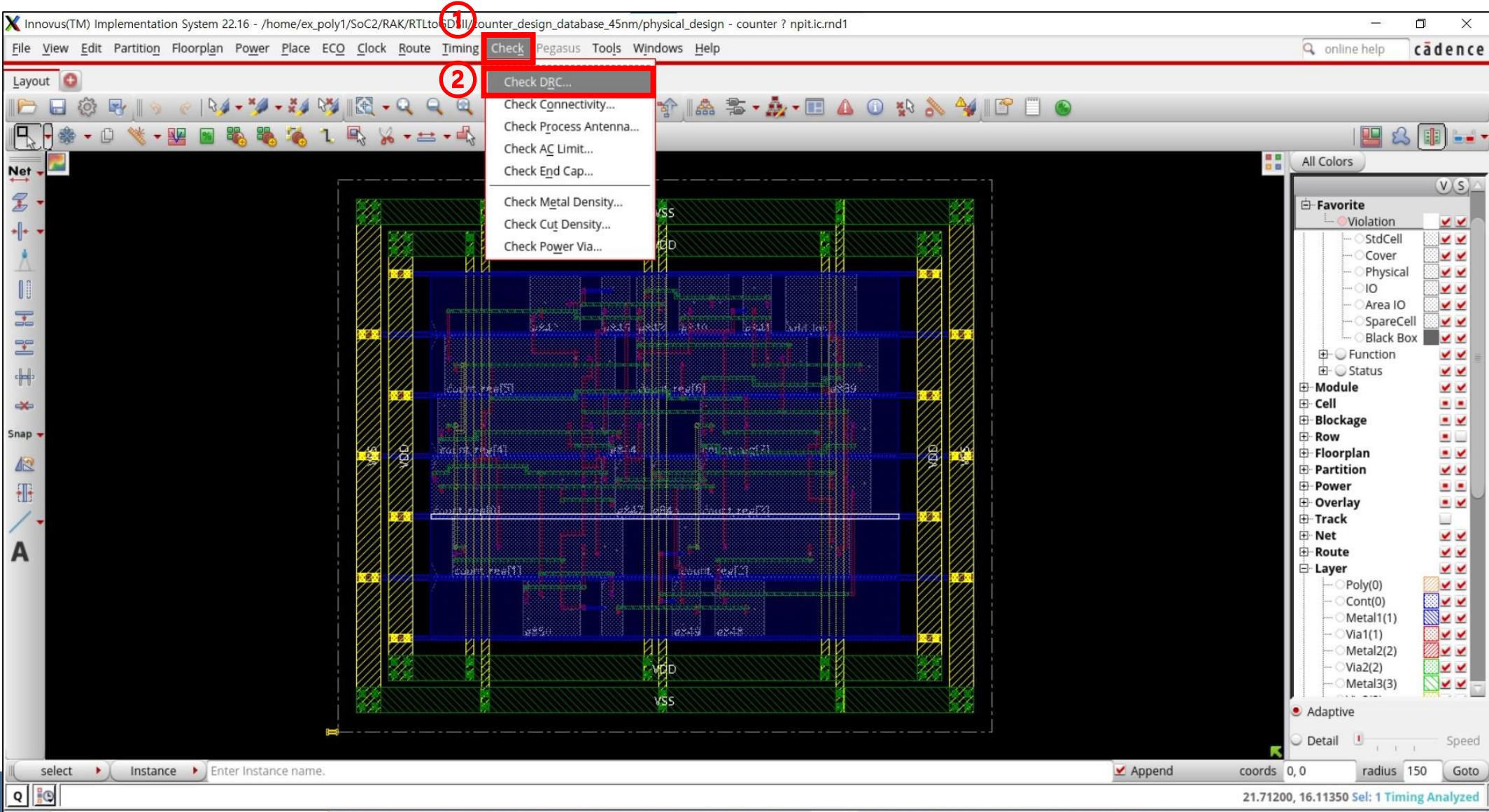
- hold time에 음수 값이 나오지 않도록 하기 위해 Effort를 Timing 쪽으로 설정 후 route



Auto PnR

Innovus

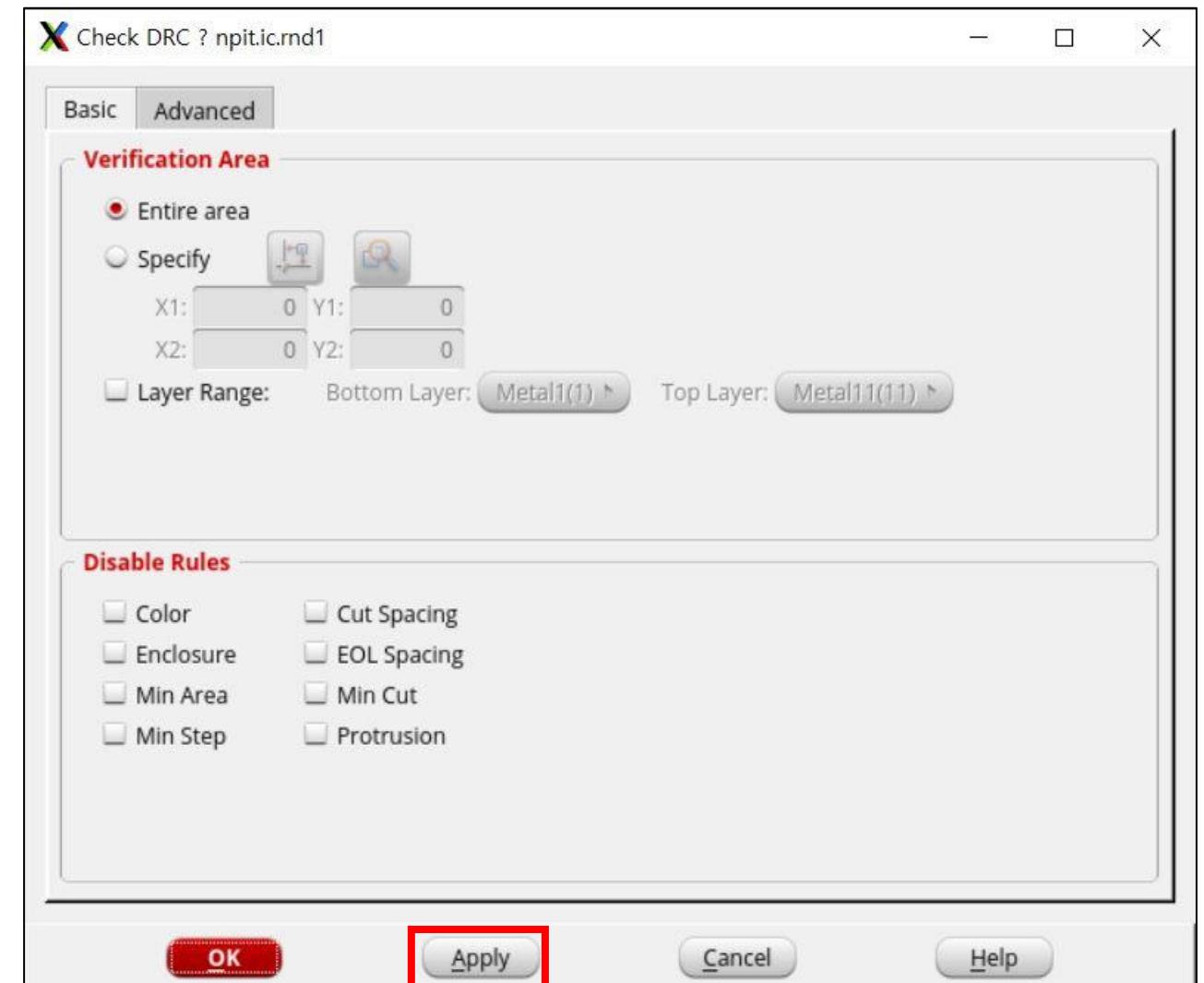
- Running Physical Verification – Check DRC



Auto PnR

Innovus

- Running Physical Verification – Check DRC
- 오른쪽 창과 똑같이 설정 후 Apply 클릭



Auto PnR

Innovus

- Running Physical Verification – Check DRC

```
VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 18.400 15.580} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 18 Viols.
```

Verification Complete : 18 Viols.

Violation Summary By Layer and Type:

	Short	Totals
Metal1	18	18
Totals	18	18

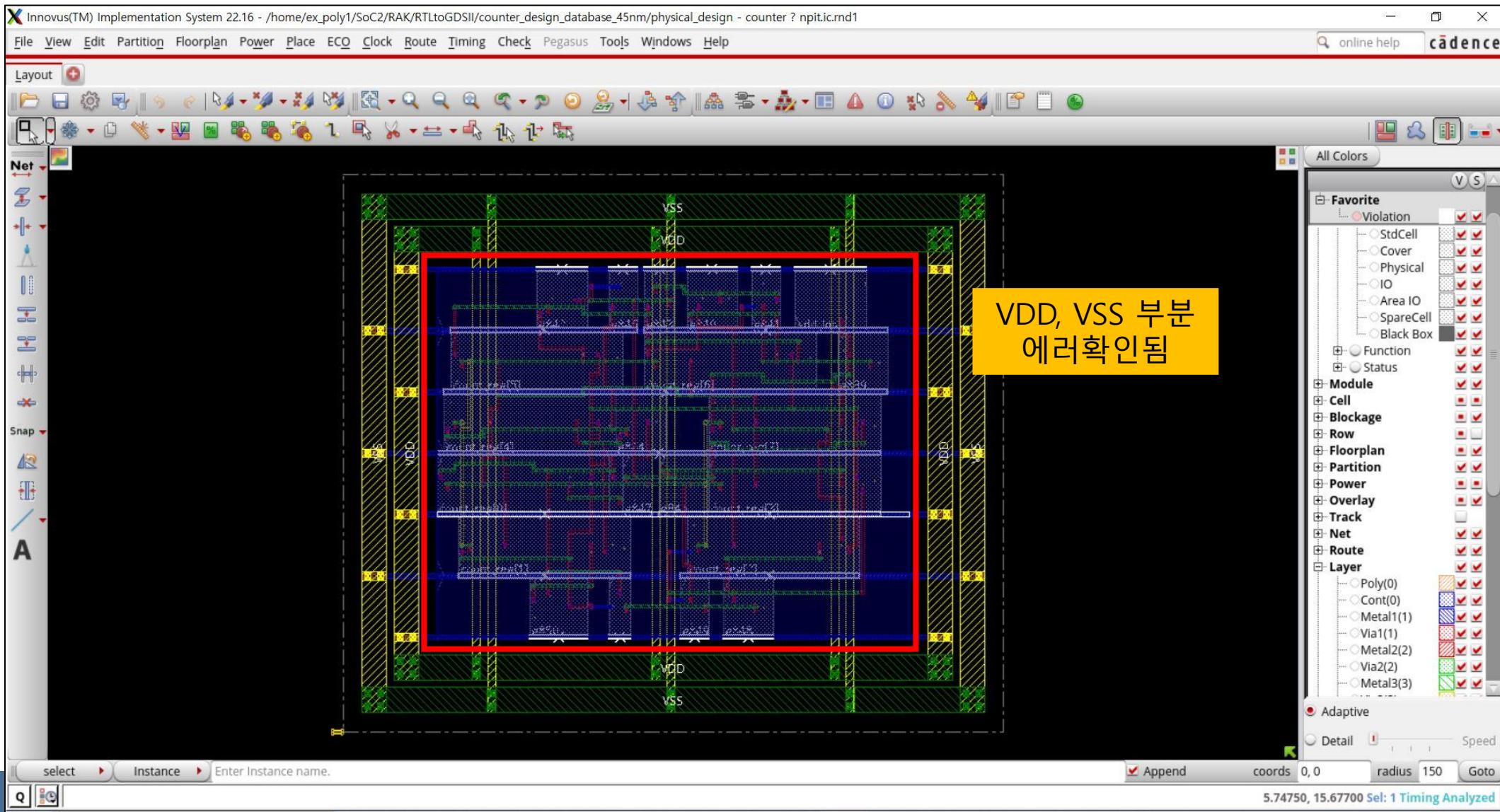
에러 18개 확인

*** End Verify DRC (CPU TIME: 0:00:00.0 ELAPSED TIME: 0:00:00.0 MEM: 264.1M) ***

Auto PnR

Innovus

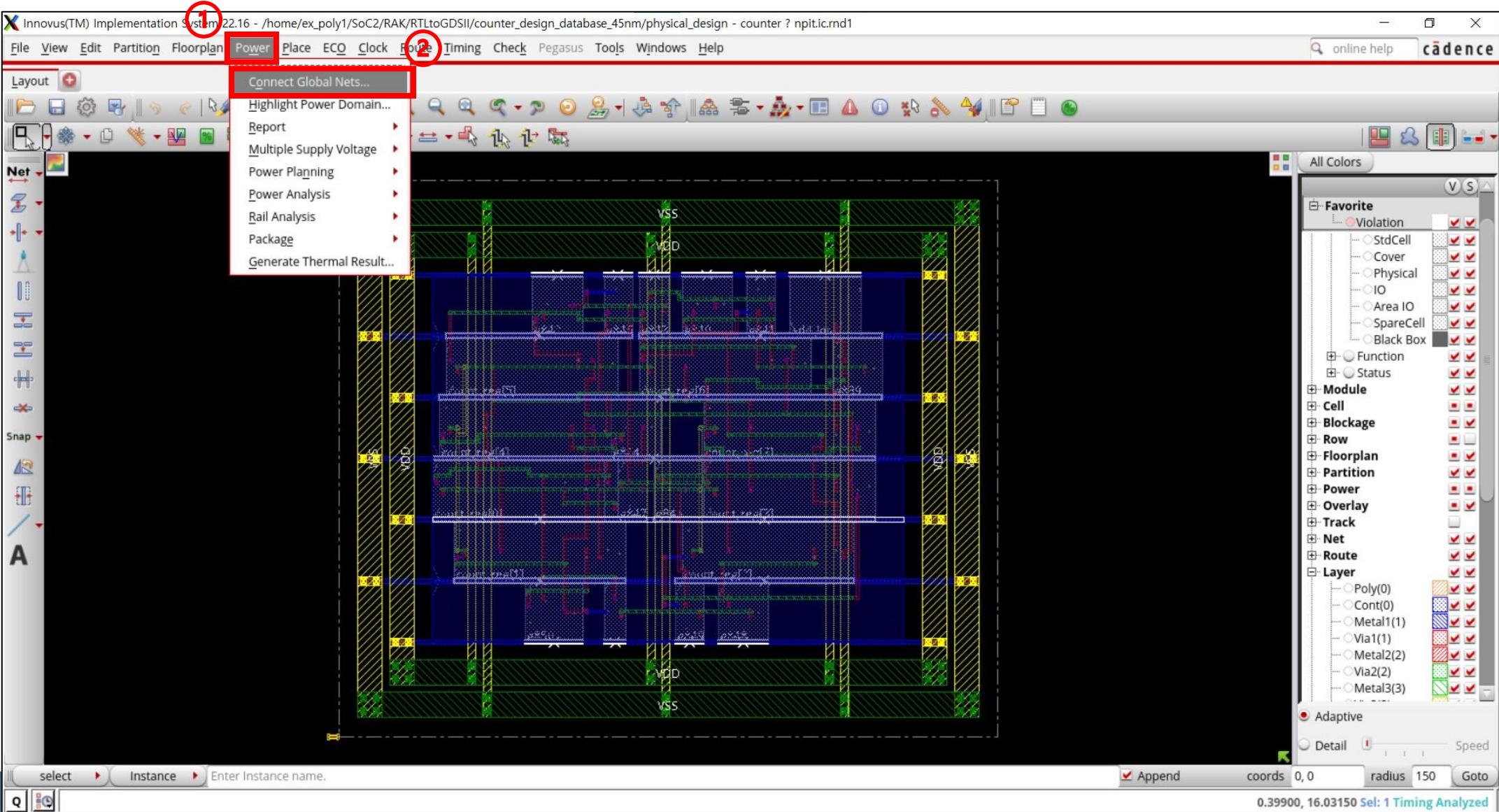
- Running Physical Verification – Check DRC



Auto PnR

Innovus

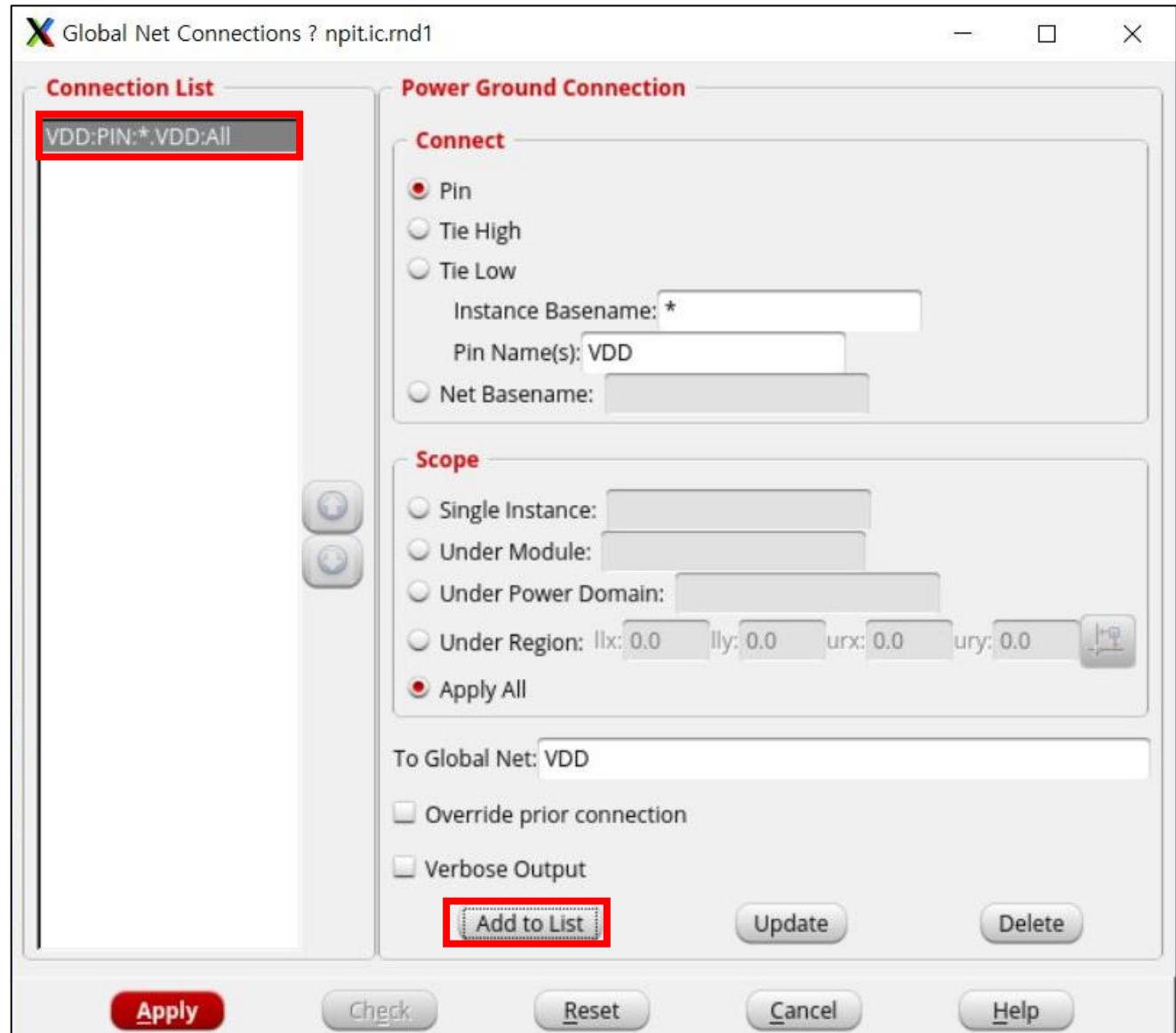
- Running Physical Verification – 에러 수정



Auto PnR

Innovus

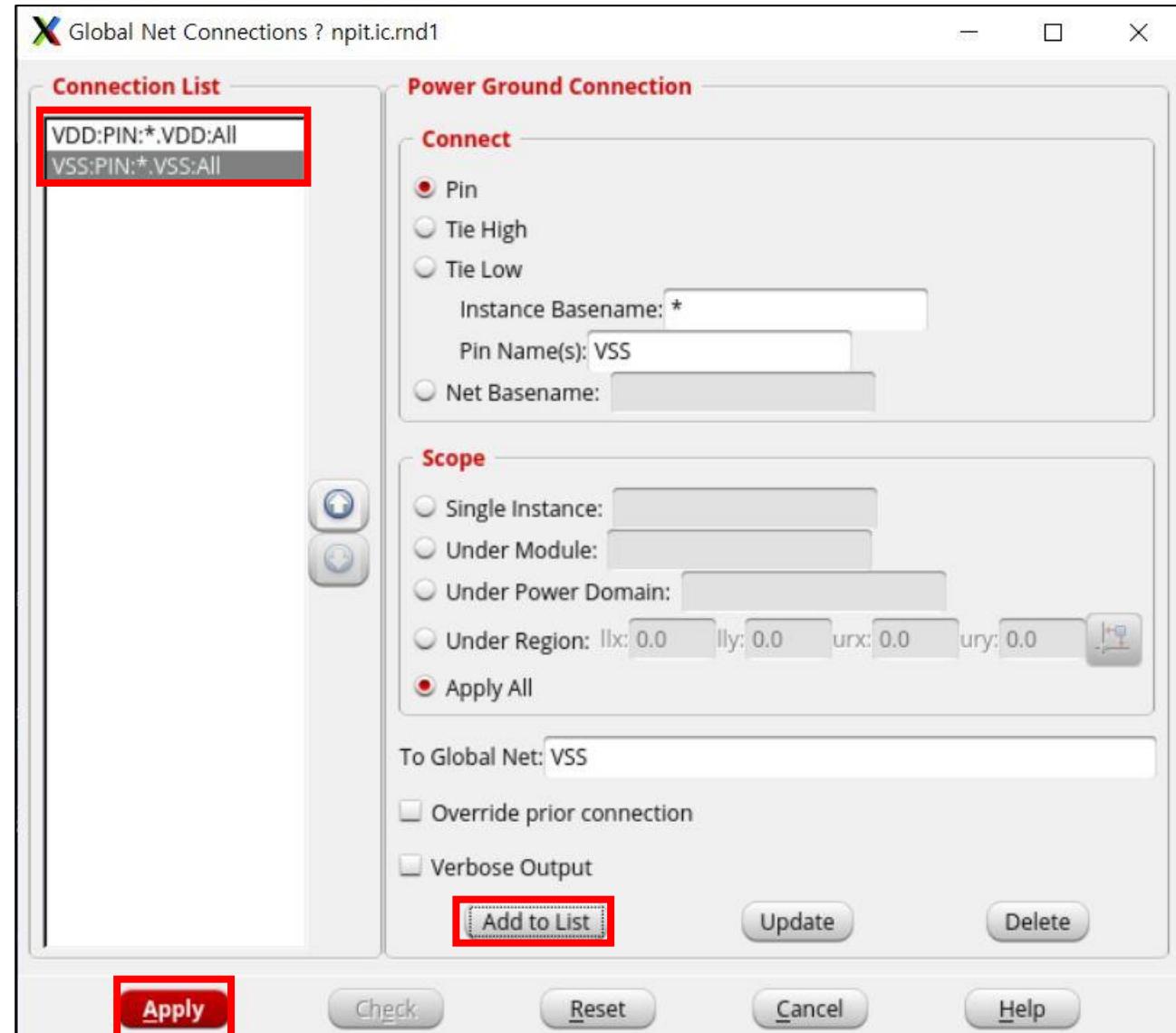
- Connect Global Nets
- 오른쪽 창과 똑같이 설정 후 Add to List 클릭
- Connection List에 VDD가 입력됨



Auto PnR

Innovus

- Connect Global Nets
- 오른쪽 창과 똑같이 설정 후 Add to List 클릭
- Connection List 확인 후 Apply 클릭



Auto PnR

Innovus

- Connect Global Nets 결과
- 이전에 설명했던 Power.tcl에 있는 명령과 같은 것임

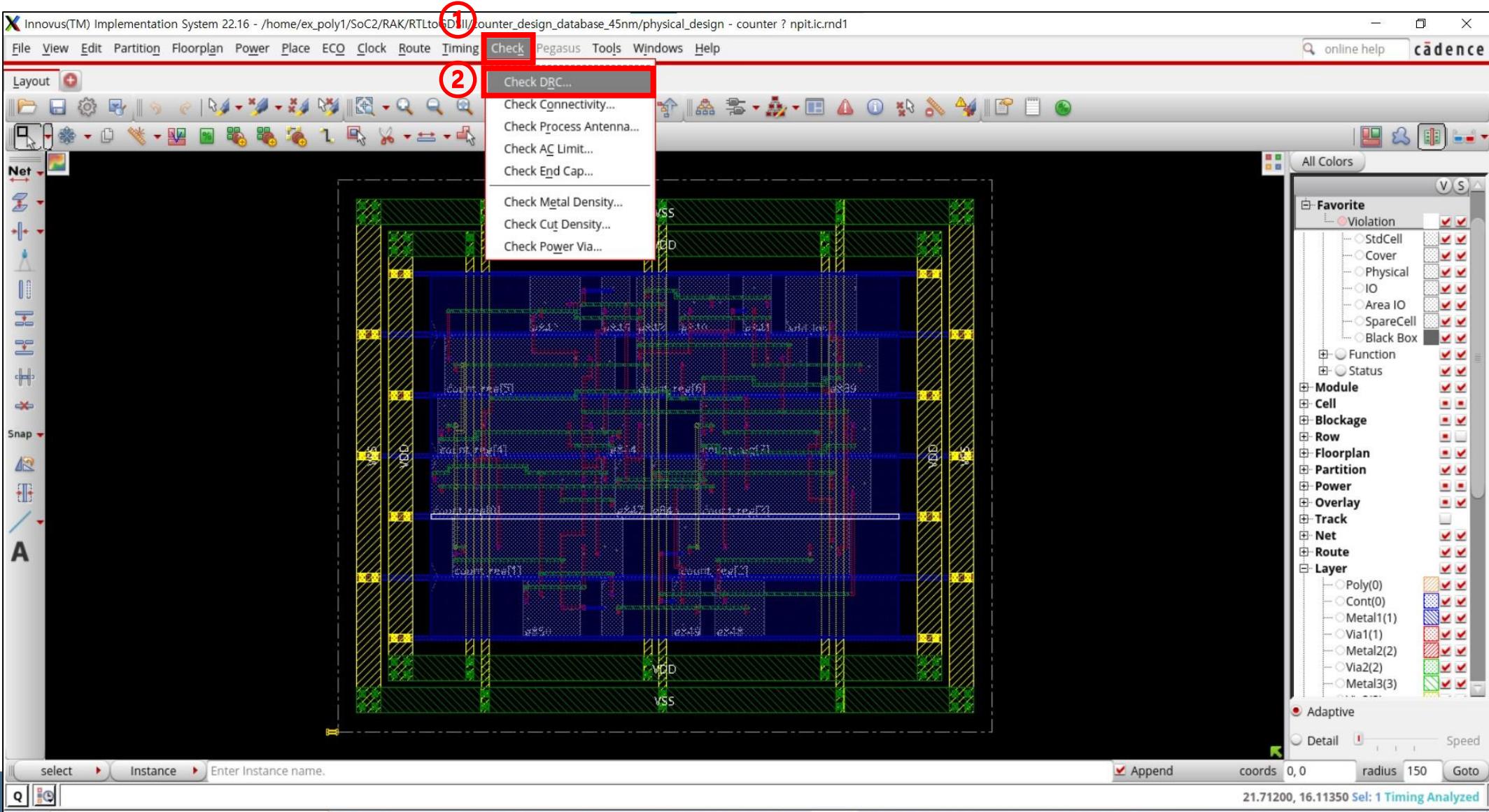
Pin과 Power Net을
연결해주는 명령임

```
@innovus 49> delete global net connections
@innovus 50> connect_global_net VDD -type pg_pin -pin_base_name VDD -inst_base_name *
@innovus 51> connect_global_net VSS -type pg_pin -pin_base_name VSS -inst_base_name *
```

Auto PnR

Innovus

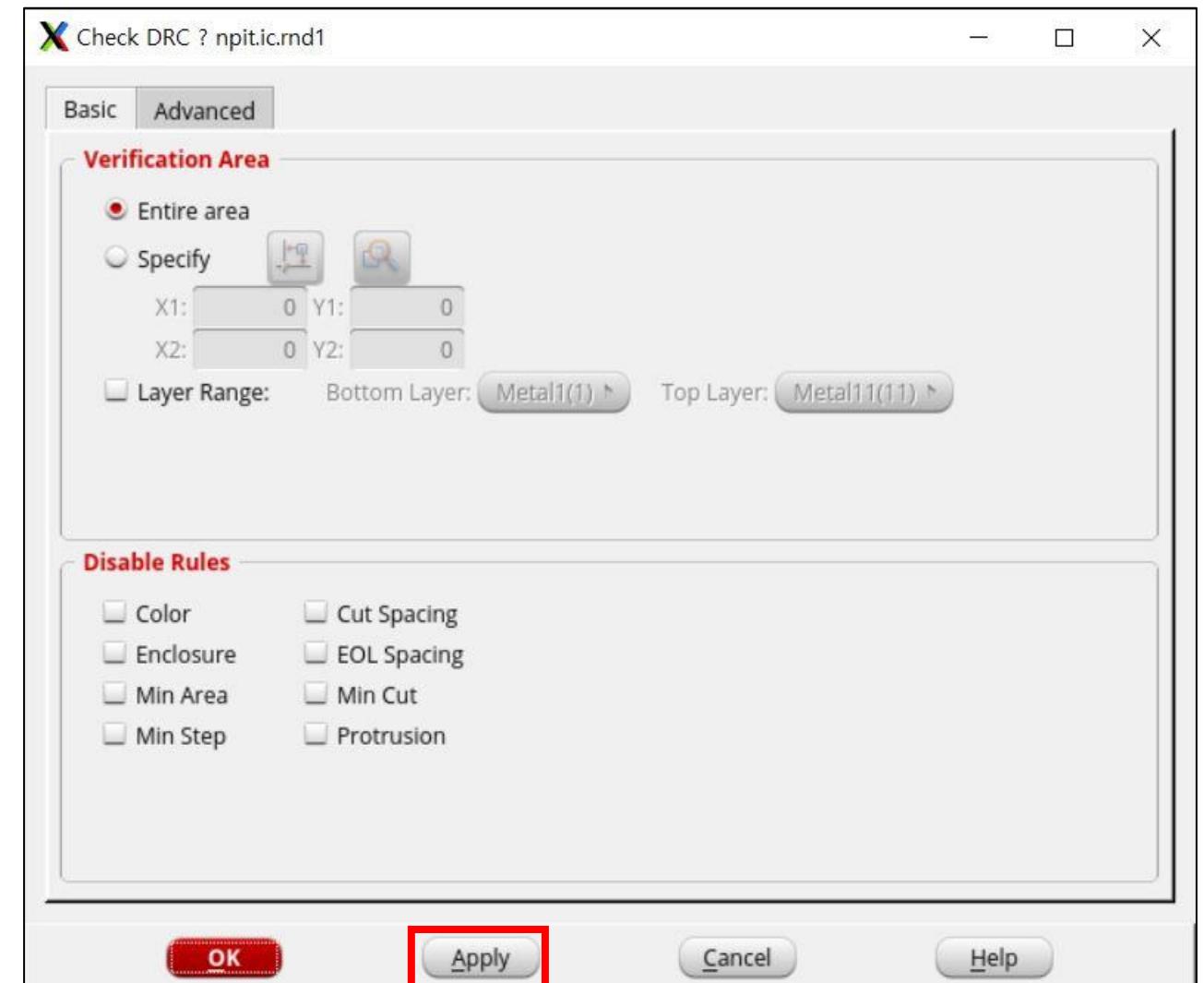
- Running Physical Verification – Check DRC



Auto PnR

Innovus

- Running Physical Verification – Check DRC
- 오른쪽 창과 똑같이 설정 후 Apply 클릭



Auto PnR

Innovus

- Running Physical Verification – Check DRC

```
@innovus 53> check_drc
#-check_ndr_spacing auto                      # enums={true false auto}, default=auto, user setting
#-check_same_via_cell true                     # bool, default=false, user setting
#-report counter.drc.rpt                      # string, default="", user setting
*** Starting Verify DRC (MEM: 3010.4) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 18.400 15.580} 1 of 1
VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

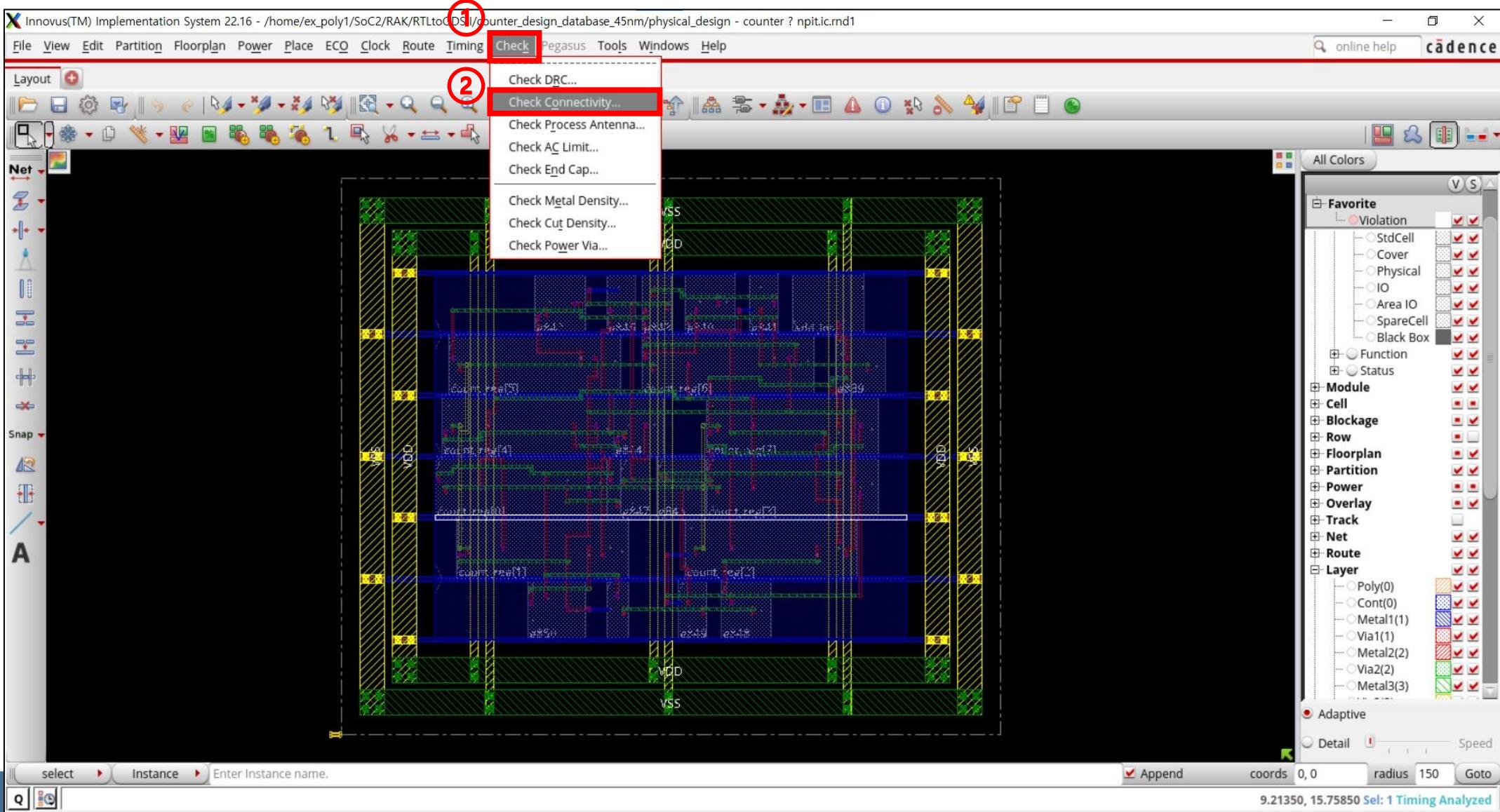
Verification Complete : 0 Viols. 예러 없음

*** End Verify DRC (CPU TIME: 0:00:00.0 ELAPSED TIME: 0:00:00.0 MEM: 8.0M) ***
```

Auto PnR

Innovus

- Check Connectivity (LVS)



Auto PnR

Innovus

- Check Connectivity (LVS)
- 오른쪽 창과 똑같이 설정 후 OK 클릭



Auto PnR

Innovus

- Check Connectivity (LVS)
- Warning, Error 없음

```
Begin Summary
    Found no problems or warnings.
End Summary

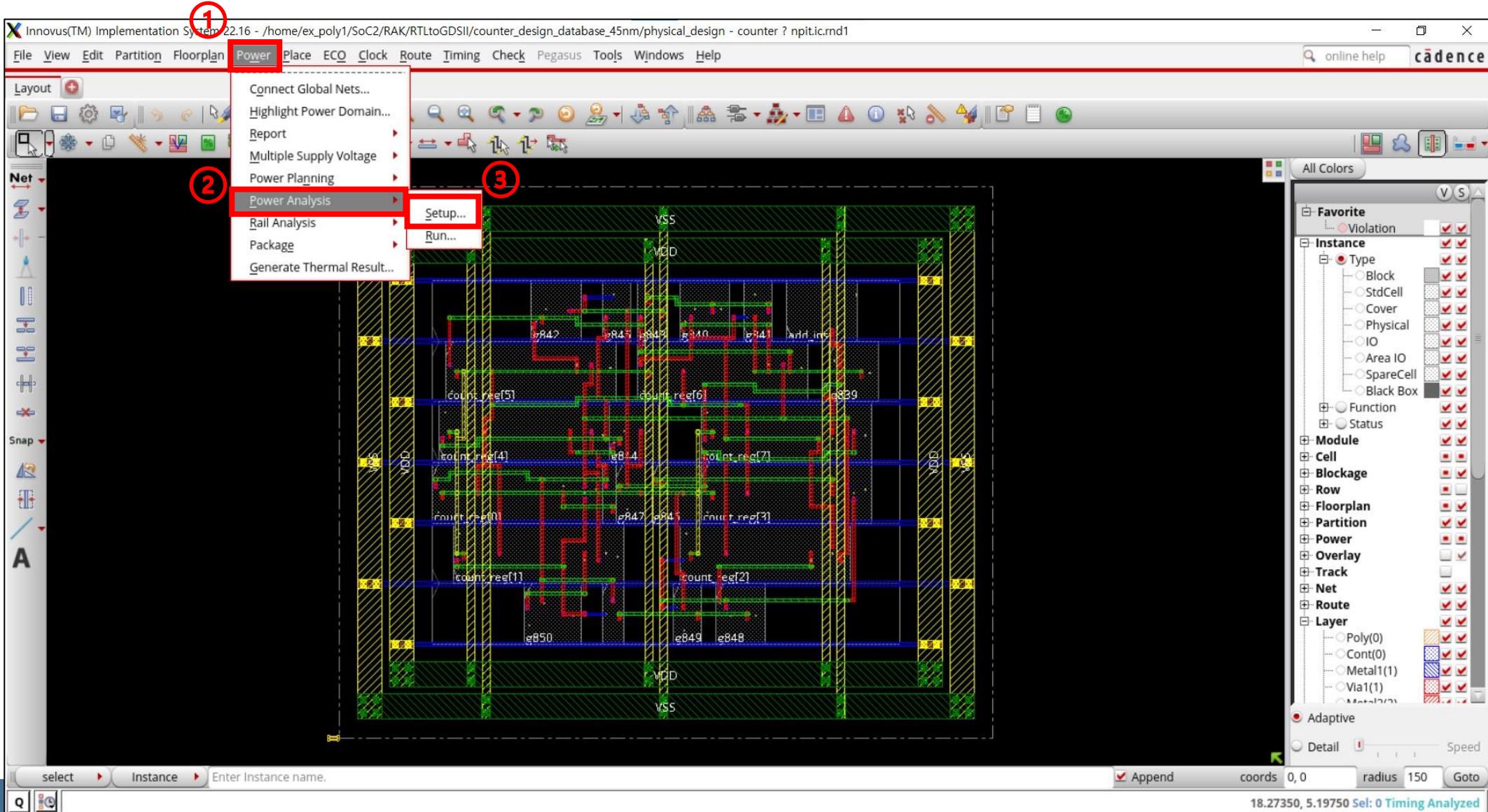
End Time: Mon Feb 24 22:02:11 2025
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.0  MEM: 0.000M)
```

Auto PnR

Innovus

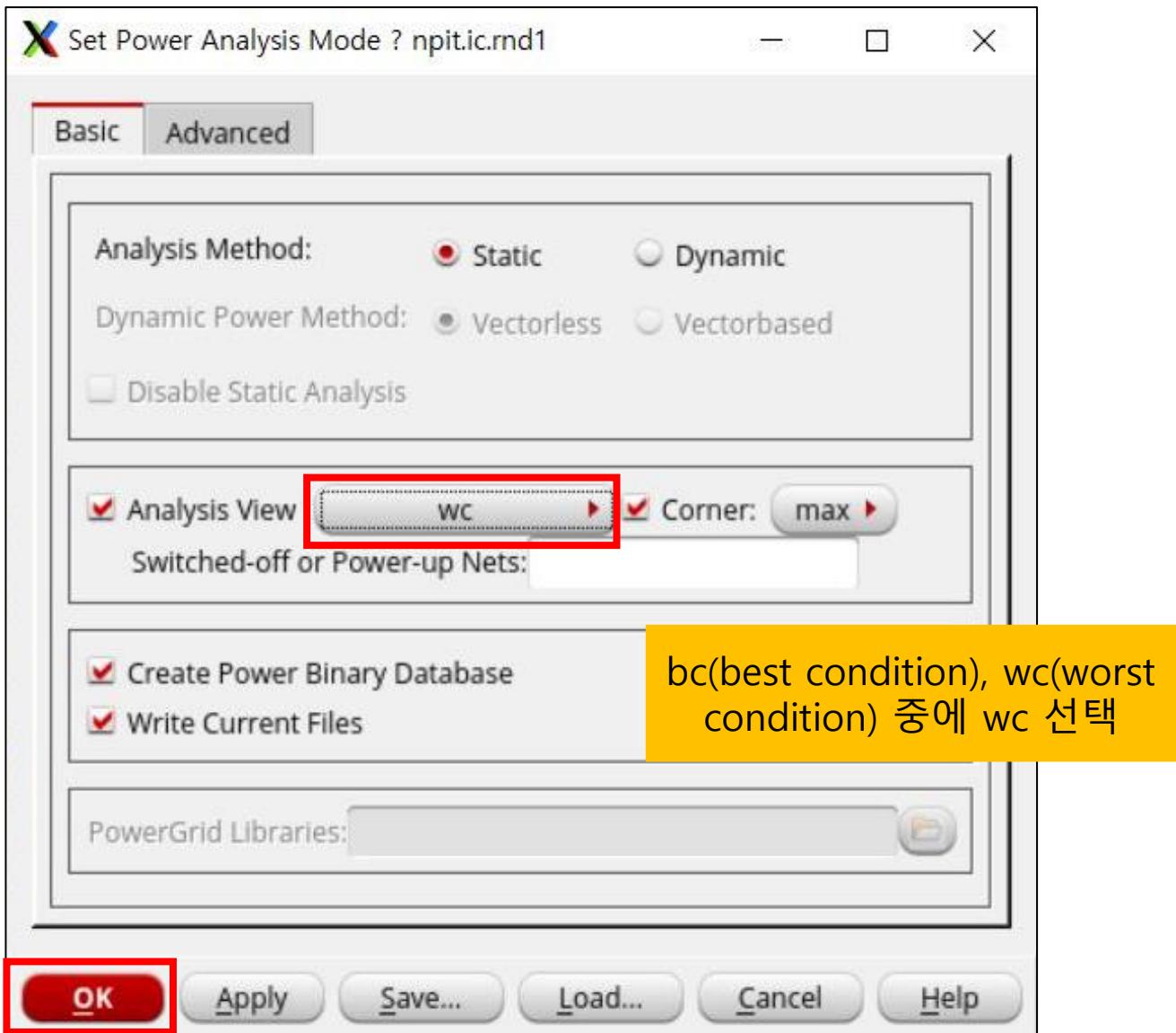
- Running Power Analysis - Setup



Auto PnR

Innovus

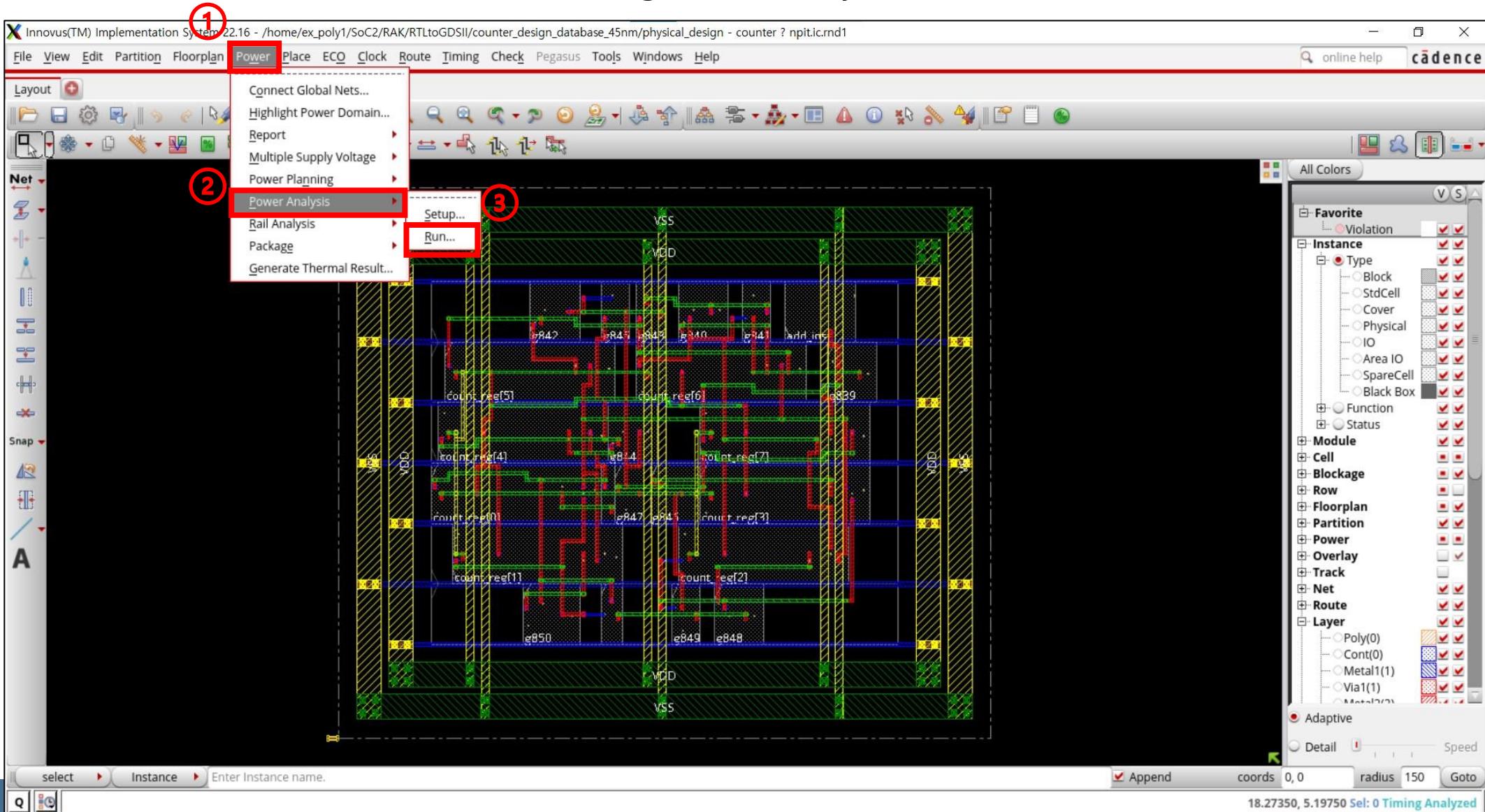
- Running Power Analysis - Setup
- 오른쪽 창과 똑같이 설정 후 OK 클릭



Auto PnR

Innovus

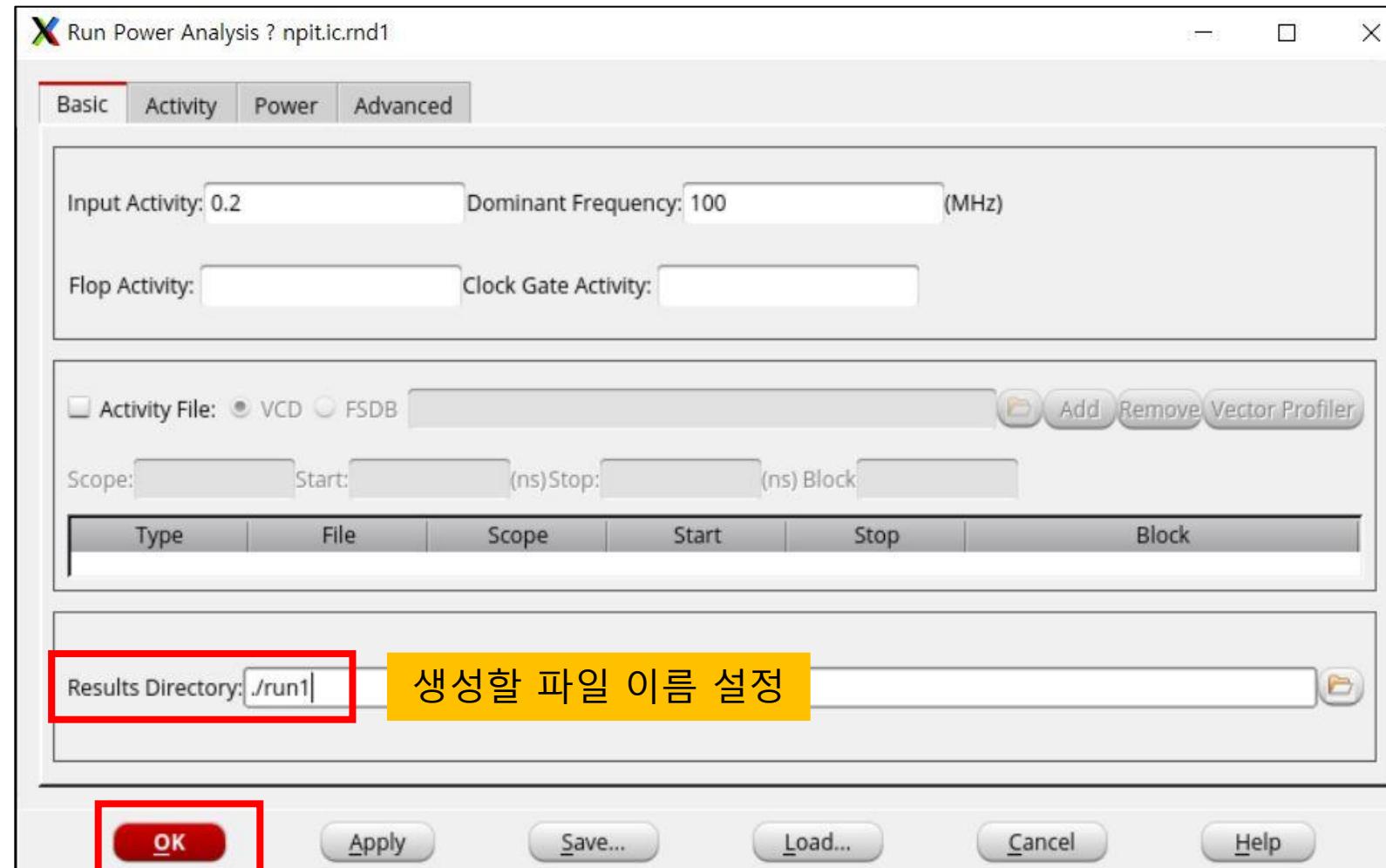
- Running Power Analysis - Run



Auto PnR

Innovus

- Running Power Analysis - Run
- 오른쪽 창과 똑같이 설정 후 OK 클릭



Auto PnR

Innovus

Total Power 소모량에
대한 정보가 나옴

- Running Power Analysis – Run

```
Total Power
-----
Total Internal Power:      0.00448175      87.4003%
Total Switching Power:    0.00064405      12.5598%
Total Leakage Power:      0.00000205      0.0399%
Total Power:               0.00512785

** WARN:  (VOLTUS_POWR-3424): Cell INVX1 has no power pin defined in LEF/PGV.
** WARN:  (VOLTUS_POWR-3424): Cell TBUFX1 has no power pin defined in LEF/PGV.
** WARN:  (VOLTUS_POWR-3424): Cell NAND2X1 has no power pin defined in LEF/PGV.
** WARN:  (VOLTUS_POWR-3424): Cell SDFFRHQX1 has no power pin defined in LEF/PGV.
** WARN:  (VOLTUS_POWR-3424): Cell XOR2XL has no power pin defined in LEF/PGV.
** WARN:  (VOLTUS_POWR-3424): Cell NAND2BX1 has no power pin defined in LEF/PGV.
** WARN:  (VOLTUS_POWR-3424): Cell XNOR2X1 has no power pin defined in LEF/PGV.

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=2174.72MB/4492.46MB/2221.19MB)

Begin Creating Binary Database
Ended Creating Binary Database: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=2694.94MB/6038.89MB/2694.95MB)

Output file is ./run1/counter.rpt
```

Auto PnR

Innovus

- Running Power Analysis – Run → 다른 터미널에서 폴더 확인
- Power Analysis 결과가 들어간 run1 폴더가 생성됨

```
[ex_poly1@npit physical_design]$ ls
collectGenusLibrary.log  counter_sdc.sdc  innovus.log1  innovus.logv3
                           rc_model.bin
counter.conn.rpt          innovus.cmd     innovus.log2  innovus.logv4
                           readme
counter.conn.rpt.old      innovus.cmd1    innovus.log3  innovus.logv5
                           run1
counter.drc.rpt           innovus.cmd2    innovus.log4  innovus.logv6
```

Auto PnR

Innovus

- Running Power Analysis – Run
- counter.rpt 파일 확인

\$> cd run1

\$> vi counter.rpt

```
[ex_poly1@npit run1]$ ls  
cellIDMap  counter.rpt  power.db  power.db.cnstr.tcl  static_VDD.ptiavg  static_VSS.ptiavg  voltus_power.ptifiles
```

Auto PnR

Innovus

- Running Power Analysis – Run
- counter.rpt 파일 확인

\$> vi counter.rpt

```
9 *      Design: counter
10 *
11 *      Liberty Libraries used:
12 *          wc: ../../lib/slow_vdd1v0_basicCells.lib
13 *
14 *      Power Domain used:
15 *          Rail:          VDD          Voltage:        0.9
16 *
17 *      Power View : wc    Operating condition → wc (worst condition)
18 *
19 *      User-Defined Activity : N.A.
20 *
21 *      Activity File: N.A.
22 *
23 *      Hierarchical Global Activity: N.A.
24 *
25 *      Global Activity: N.A.
26 *
27 *      Sequential Element Activity: N.A.
28 *
29 *      Primary Input Activity: 0.200000
30 *
31 *      Default icg ratio: N.A.
32 *
33 *      Global Comb ClockGate Ratio: N.A.
34 *
35 *      Power Units = 1mW
36 *
37 *      Time Units = 1e-09 secs
38 *
39 *      Temperature = 125    wc (worst condition)
40 *                          이므로 온도가 높음
41 *      report_power -outfile ./run1/counter.rpt -rail_analysis_format VS
```

Auto PnR

각 셀에 대한 전력
소모량 확인함

Innovus

- Running Power Analysis – Run
- counter.rpt 파일 확인

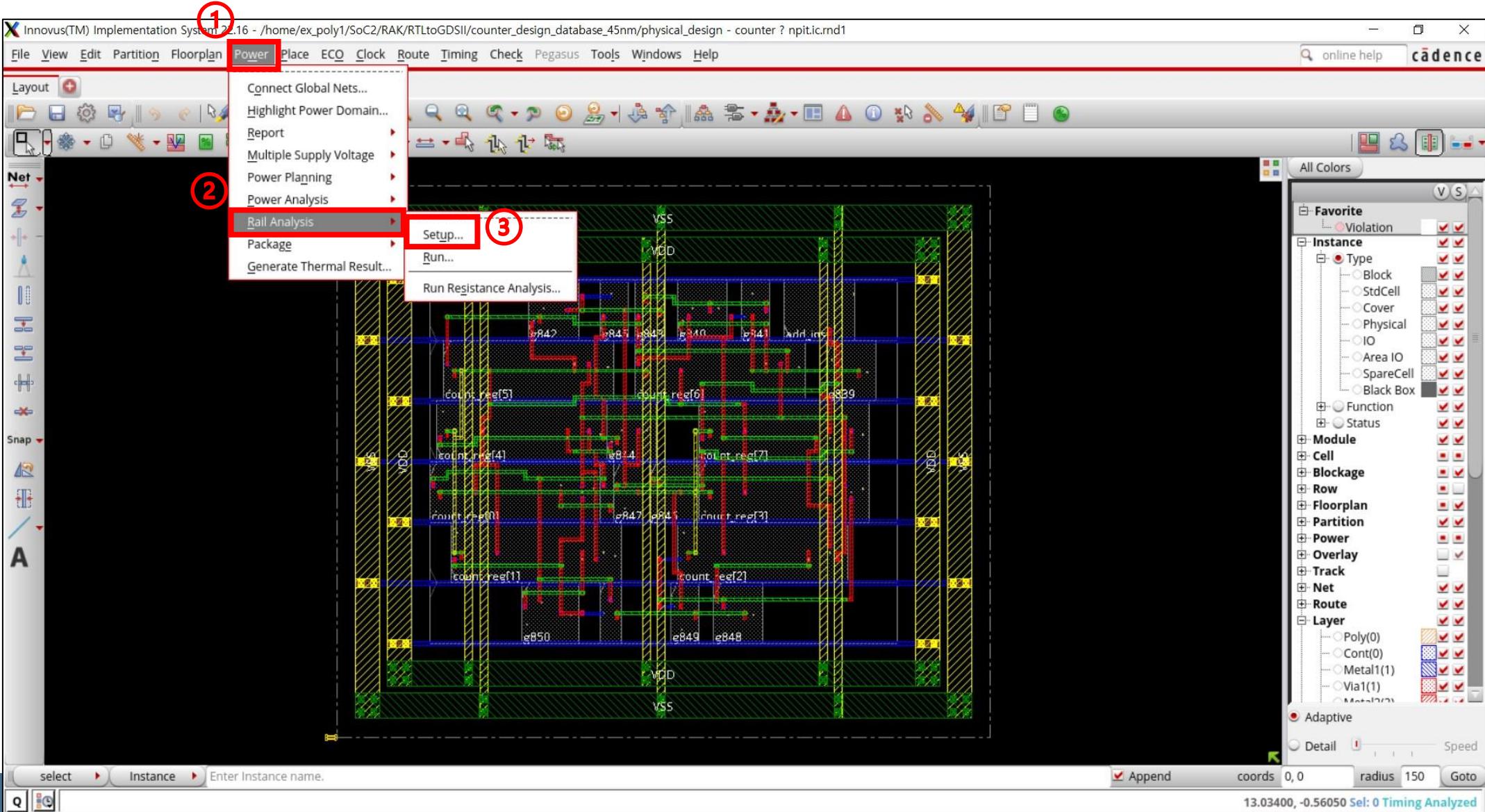
\$> vi counter.rpt

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
count_reg[3]	0.0005457	5.808e-05	0.000604	1.74e-07	SDFFRHQX1
count_reg[2]	0.000532	5.69e-05	0.0005891	1.74e-07	SDFFRHQX1
count_reg[7]	0.0005348	4.17e-05	0.0005767	1.74e-07	SDFFRHQX1
count_reg[6]	0.000499	5.796e-05	0.0005572	1.74e-07	SDFFRHQX1
count_reg[4]	0.0004963	3.86e-05	0.0005351	1.74e-07	SDFFRHQX1
count_reg[5]	0.0004824	5.096e-05	0.0005335	1.74e-07	SDFFRHQX1
count_reg[0]	0.0004693	4.212e-05	0.0005116	1.74e-07	SDFFRHQX1
count_reg[1]	0.0004488	3.874e-05	0.0004877	1.74e-07	SDFFRHQX1
add_inst	6.857e-05	8.924e-05	0.0001579	5.276e-08	TBUFX1
g846	4.825e-05	2.089e-05	6.919e-05	5.763e-08	XNOR2X1
g844	5.253e-05	1.625e-05	6.883e-05	5.67e-08	XNOR2X1
g848	4.912e-05	1.899e-05	6.817e-05	5.947e-08	XNOR2X1
g839	4.105e-05	1.05e-05	5.161e-05	5.59e-08	XNOR2X1
g840	3.865e-05	1.24e-05	5.111e-05	5.601e-08	XNOR2X1
g850	3.362e-05	1.409e-05	4.776e-05	5.293e-08	XOR2XL
g842	3.611e-05	1.156e-05	4.773e-05	5.624e-08	XNOR2X1
g849	2.925e-05	1.567e-05	4.495e-05	3.382e-08	NAND2BX1
g851	1.609e-05	1.734e-05	3.346e-05	2.606e-08	NAND2X1
g847	2.148e-05	1.028e-05	3.179e-05	3.24e-08	NAND2BX1
g845	1.477e-05	5.716e-06	2.052e-05	3.169e-08	NAND2BX1
g769	8.714e-06	1.031e-05	1.905e-05	2.082e-08	INVX1
g843	9.381e-06	3.954e-06	1.337e-05	3.133e-08	NAND2BX1
g841	5.815e-06	1.778e-06	7.625e-06	3.115e-08	NAND2BX1
Total (23 of 23)	0.004482	0.000644	0.005128	2.047e-06	
Total Capacitance		3.358e-14 F			
Power Density		*** No Die Area ***			

Auto PnR

Innovus

- Running Rail Analysis - Setup

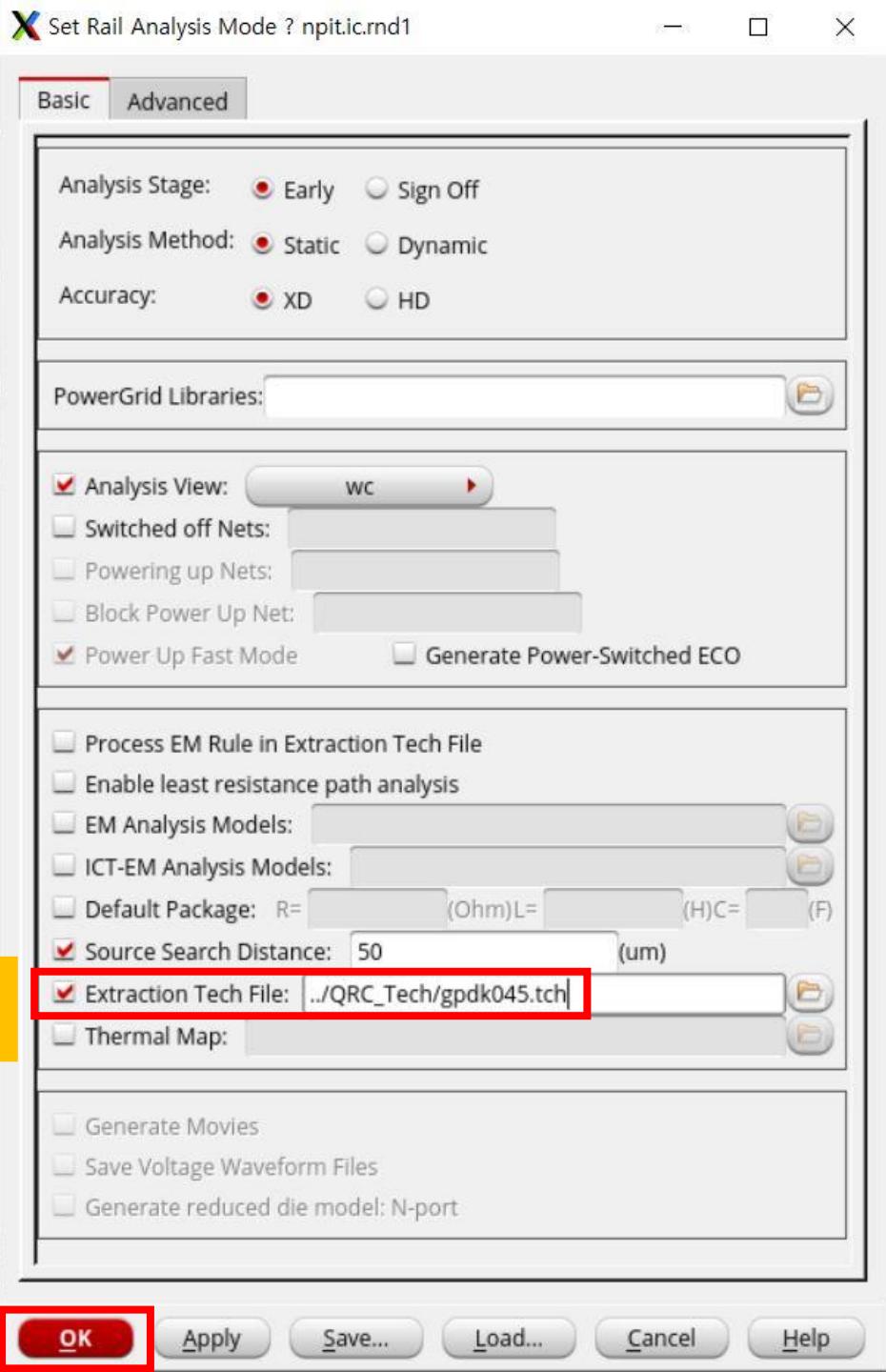


Auto PnR

Innovus

- Running Rail Analysis - Setup
- 오른쪽 창과 똑같이 설정 후 OK 클릭

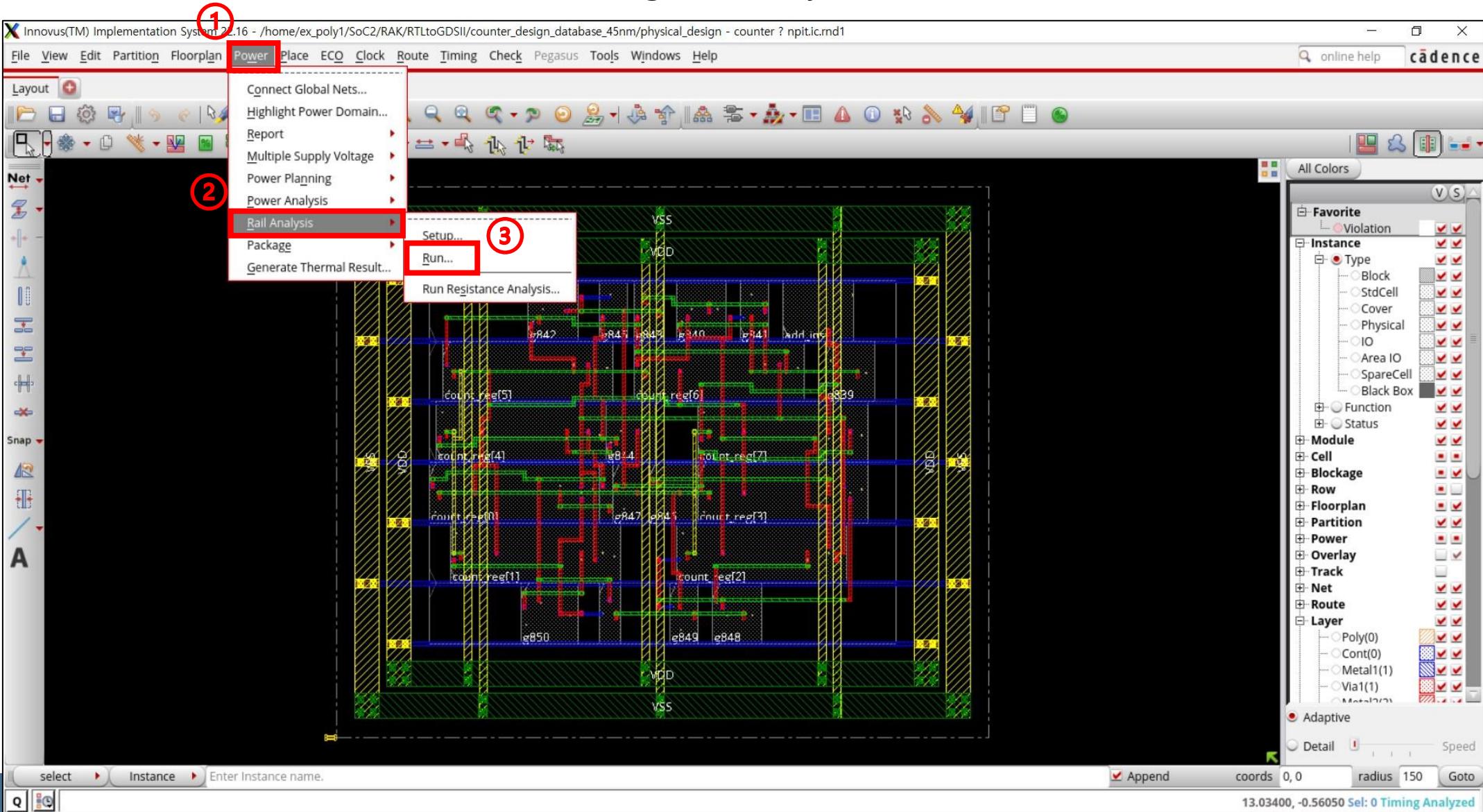
파일이 비활성화 되어
있으므로 직접 기입



Auto PnR

Innovus

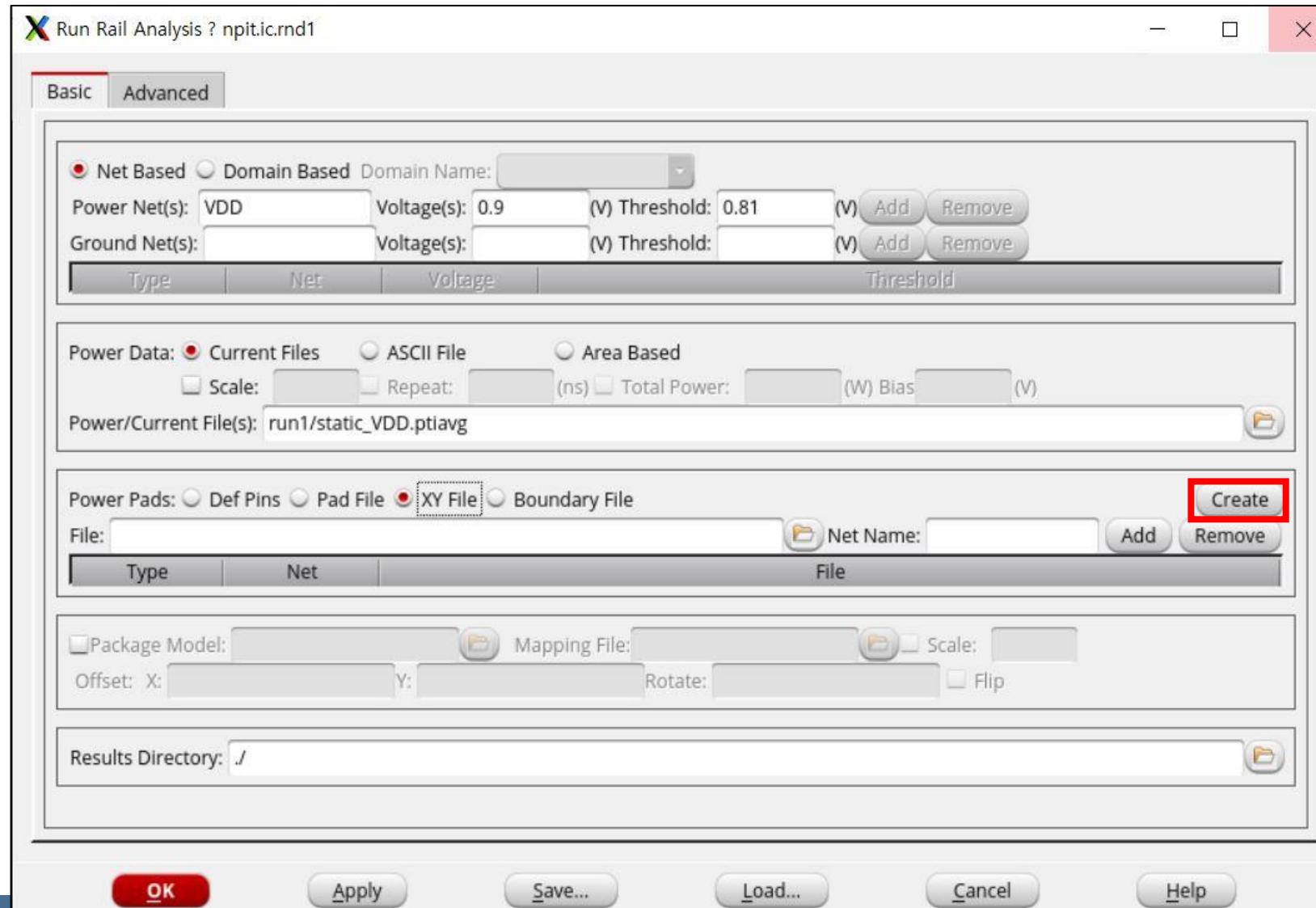
- Running Rail Analysis - Run



Auto PnR

Innovus

- Running Rail Analysis - Run
- 오른쪽 창과 똑같이 설정 후 Create 클릭

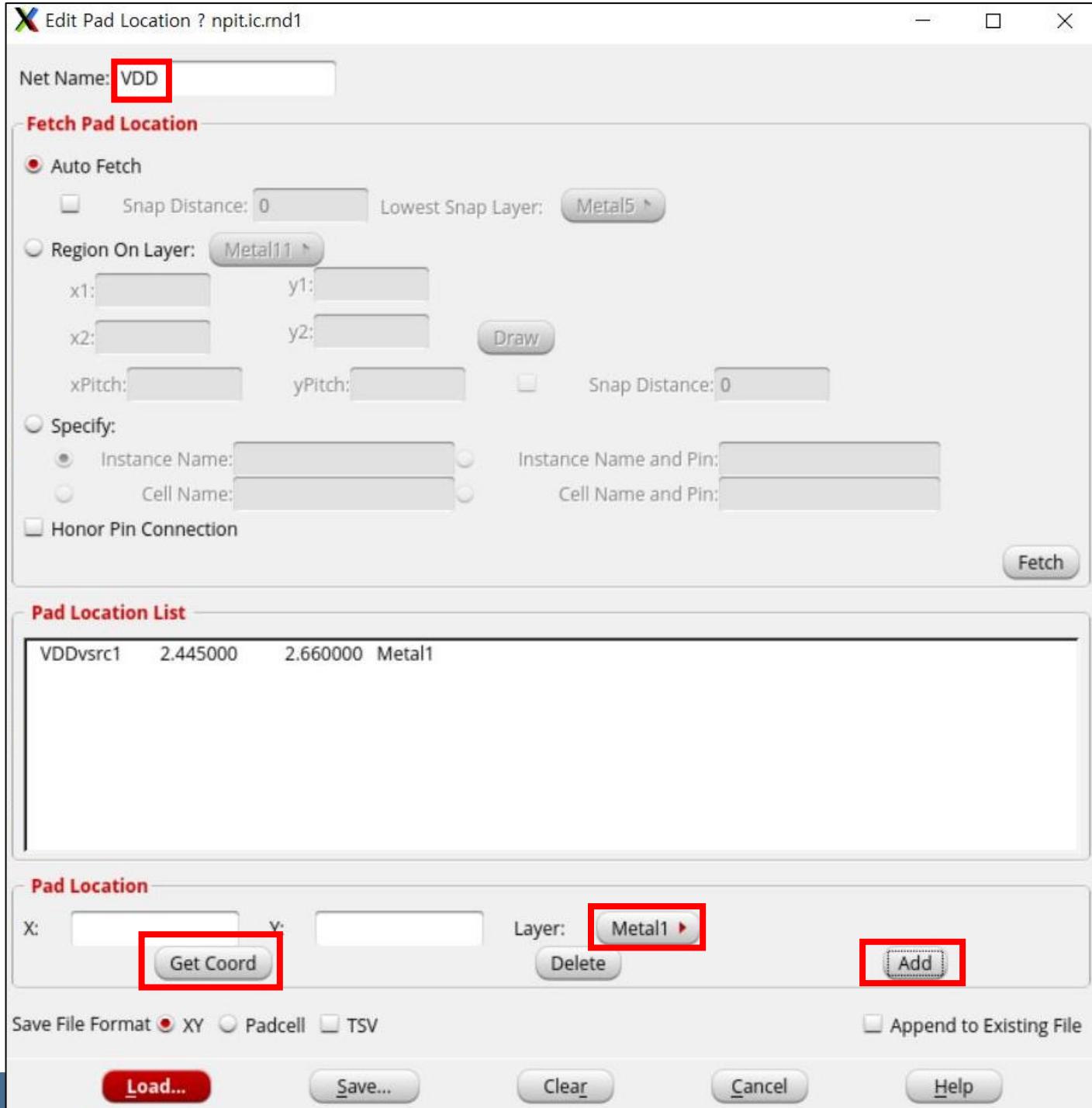


Auto PnR

Innovus

- Running Rail Analysis - Run

1. Net Name 설정
2. Get Coord 클릭
3. Gui에서 결과를 보기 원하는 Metal 클릭
4. 해당 Metal Layer 설정
5. Add 클릭

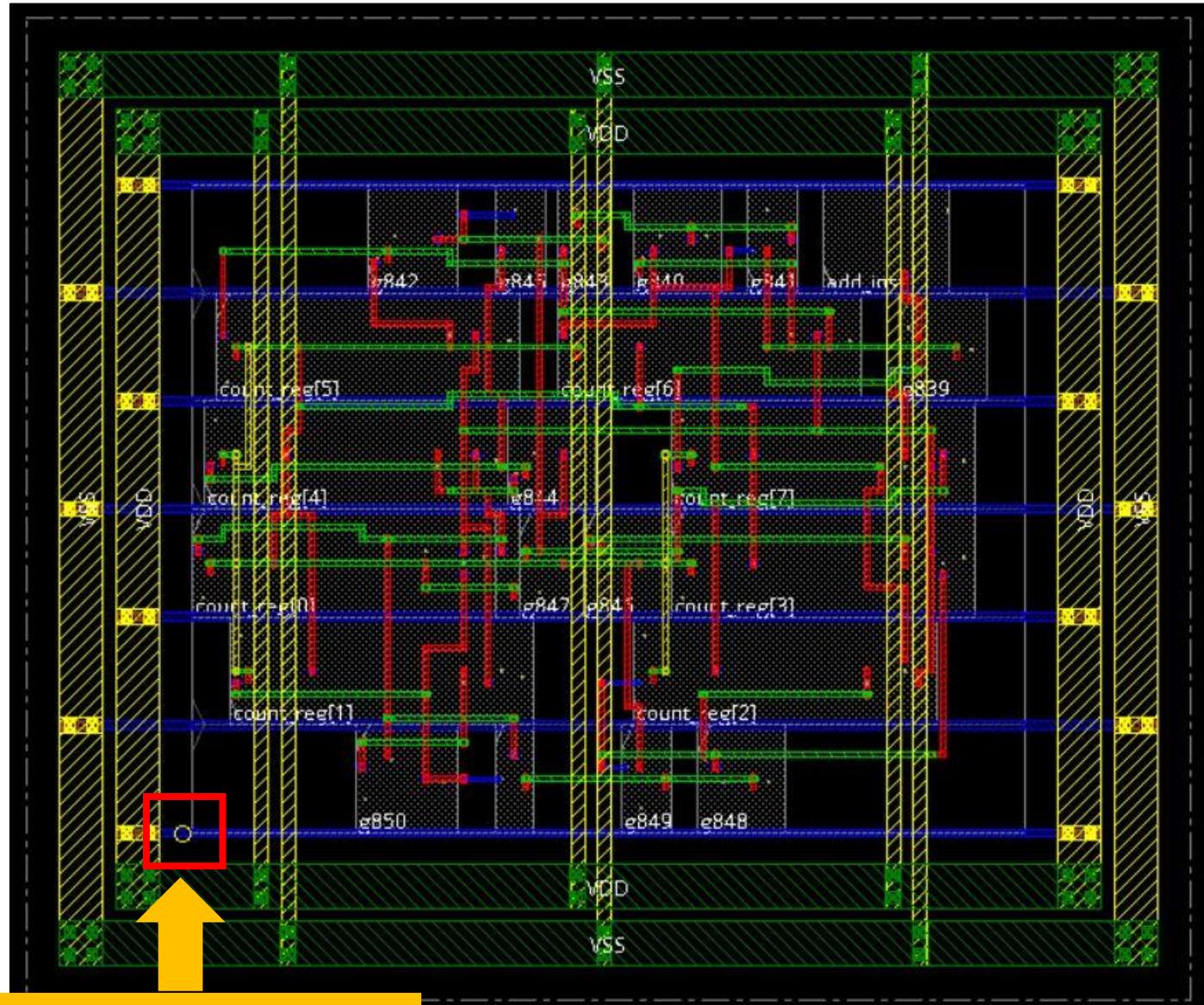


Auto PnR

Innovus

- Running Rail Analysis - Run

1. Net Name 설정
2. Get Coord 클릭
3. Gui에서 결과를 보기 원하는 Metal 클릭
4. 해당 Metal Layer 설정
5. Add 클릭

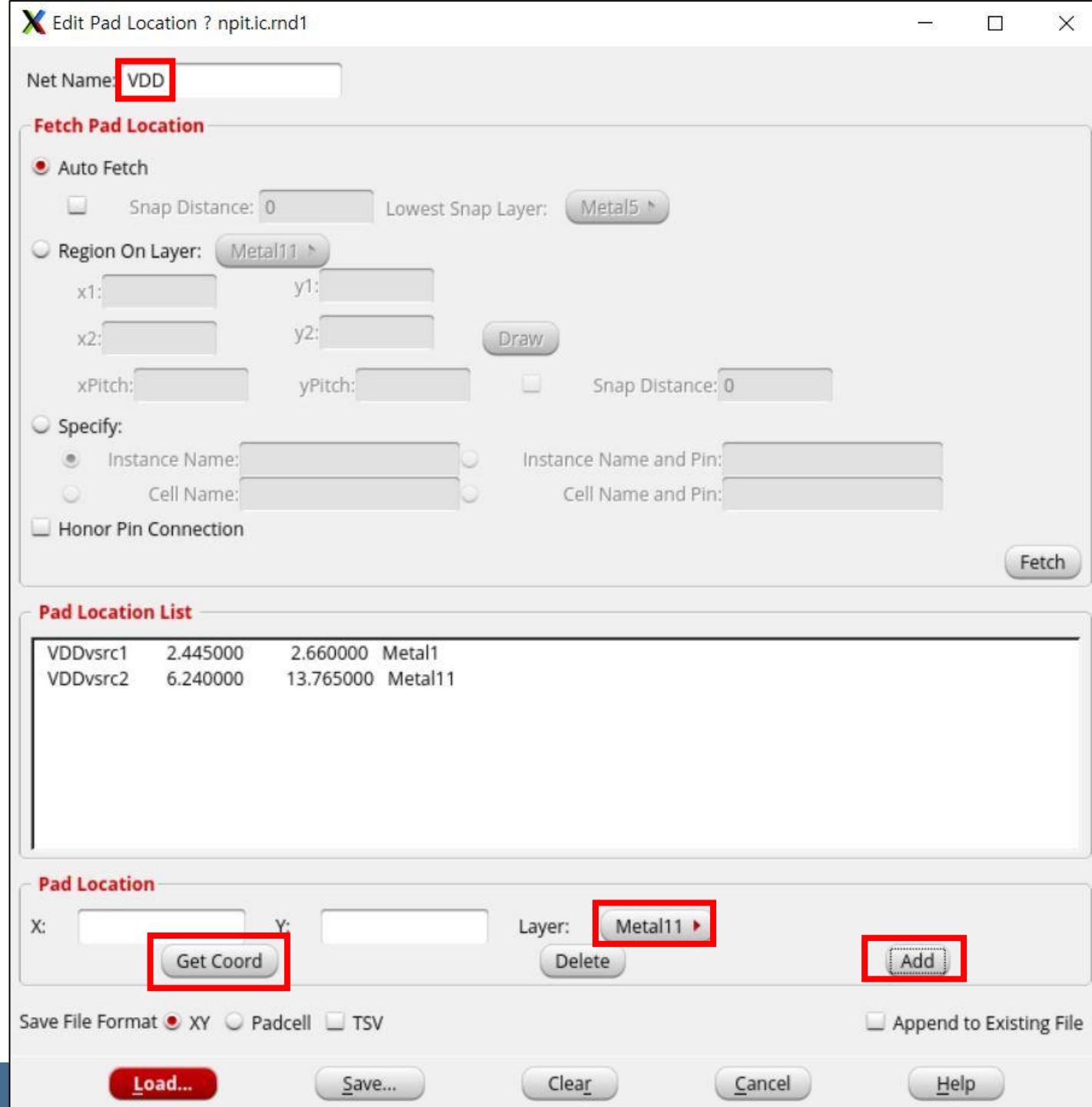


선택한 부분이 동그라미로
표시됨

Auto PnR

Innovus

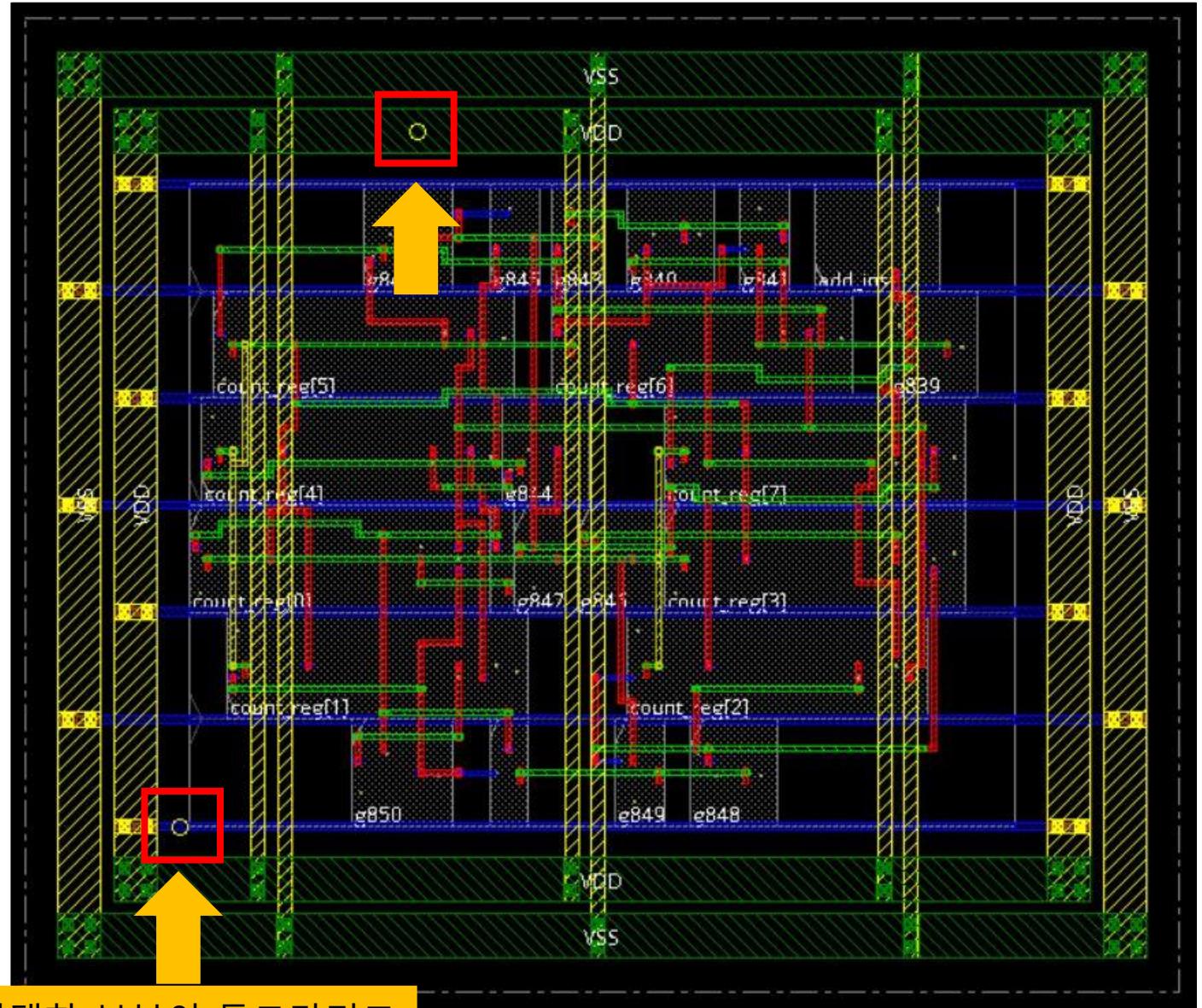
- Running Rail Analysis – Run
- 똑같은 과정으로 한번 더 진행



Auto PnR

Innovus

- Running Rail Analysis – Run
- 똑같은 과정으로 한번 더 진행

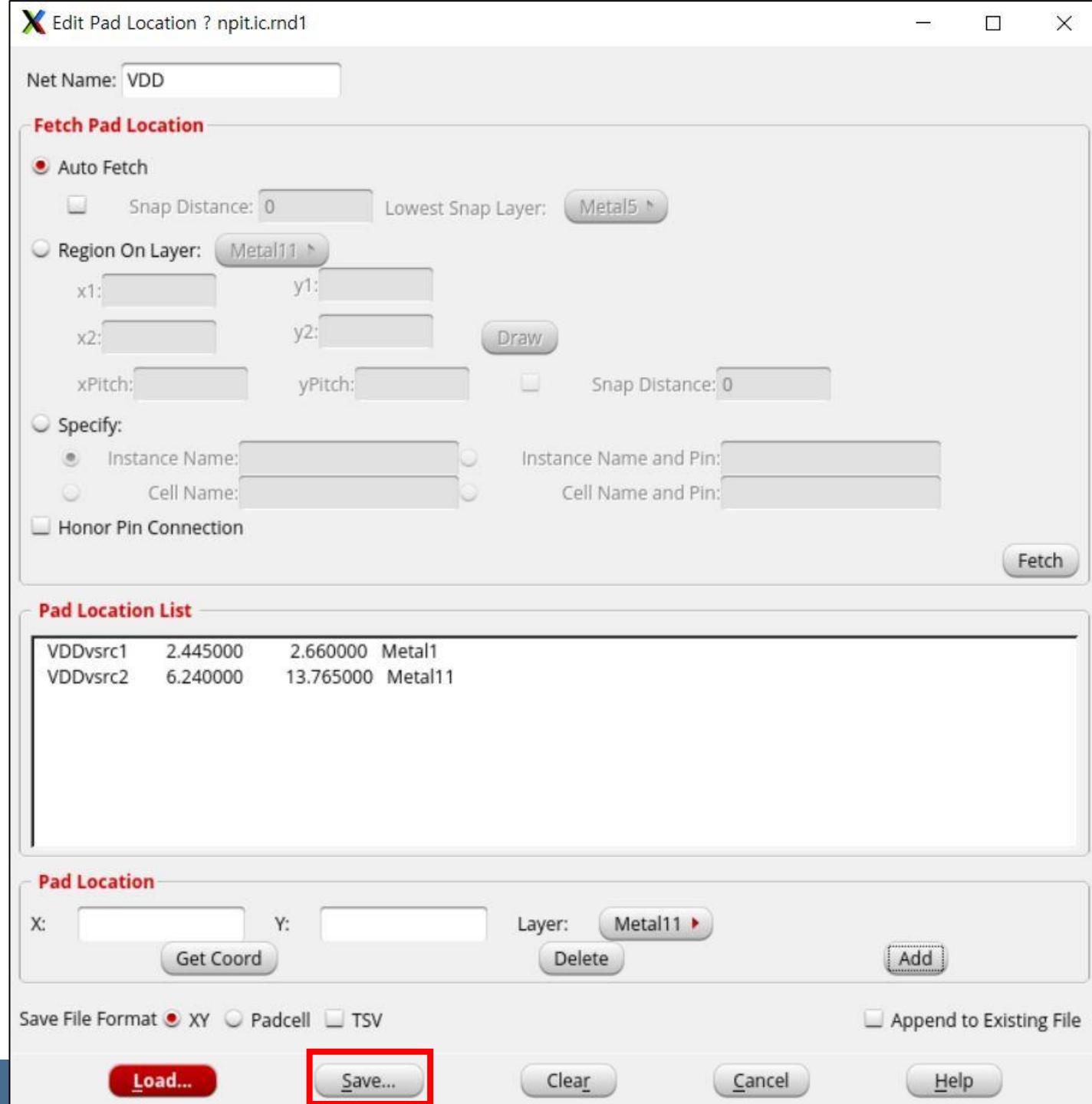


선택한 부분이
동그라미로
표시됨

Auto PnR

Innovus

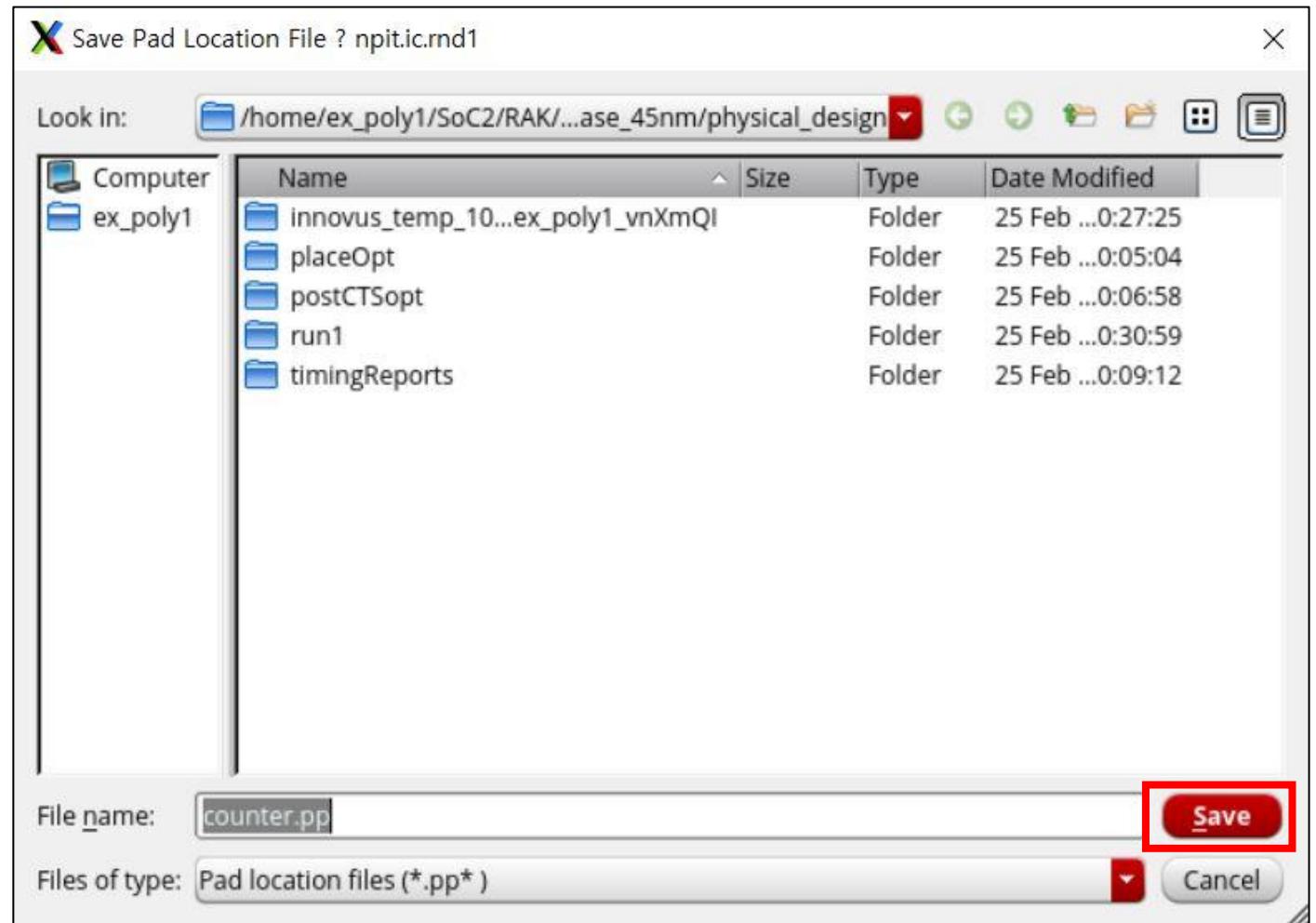
- Running Rail Analysis – Run
- Save 클릭



Auto PnR

Innovus

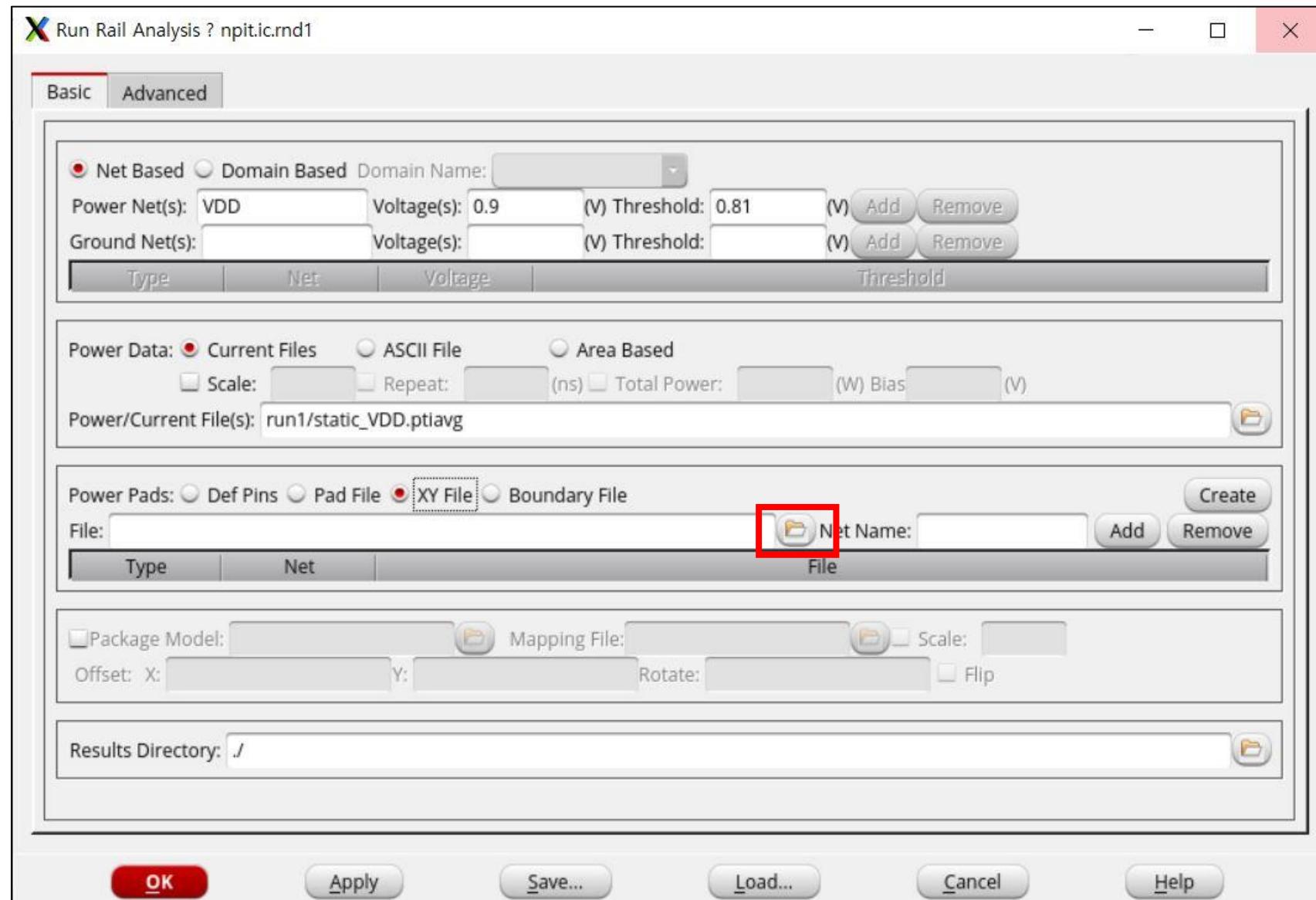
- Running Rail Analysis – Run
- Save 클릭



Auto PnR

Innovus

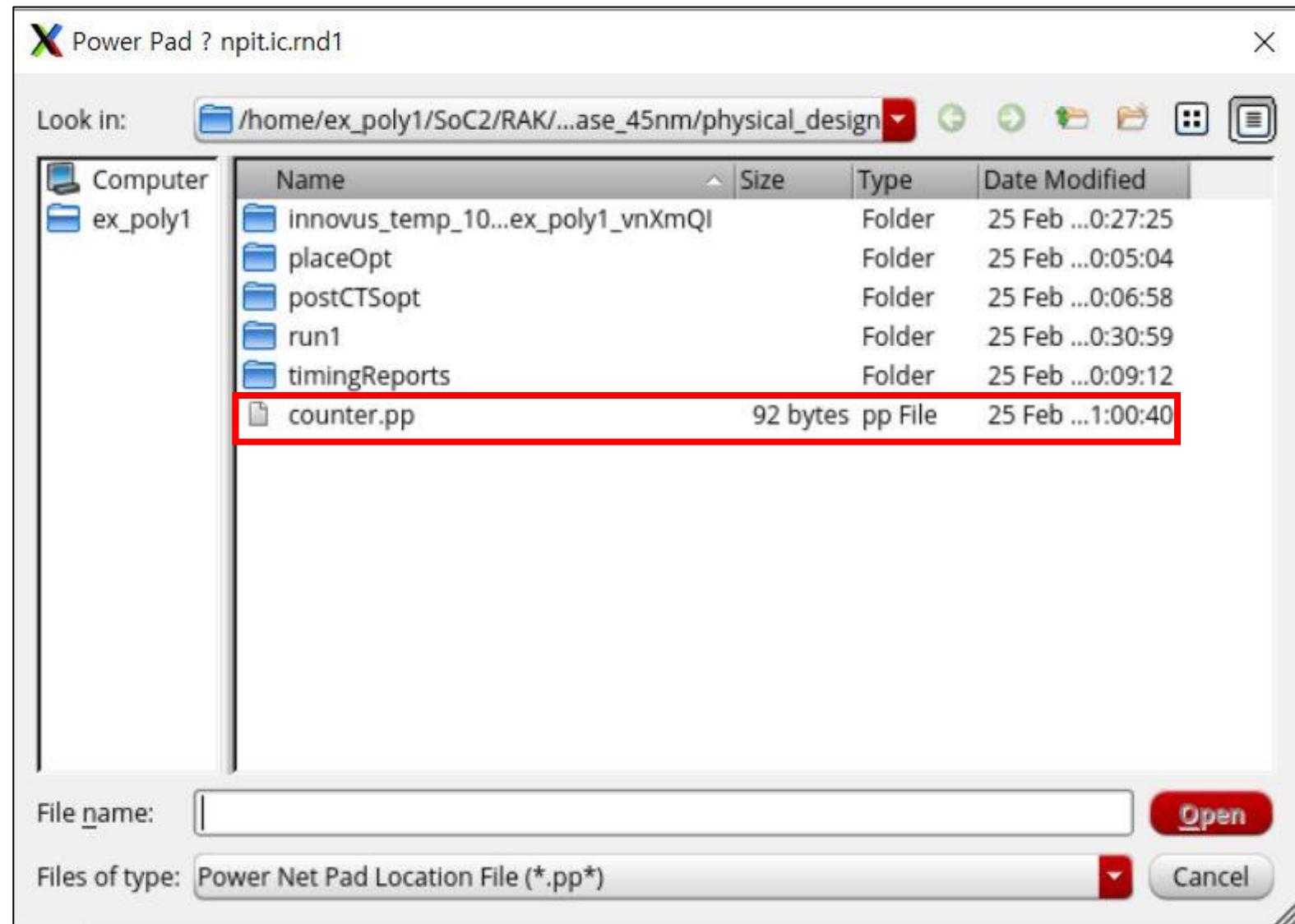
- Running Rail Analysis - Run
- 폴더그림 클릭



Auto PnR

Innovus

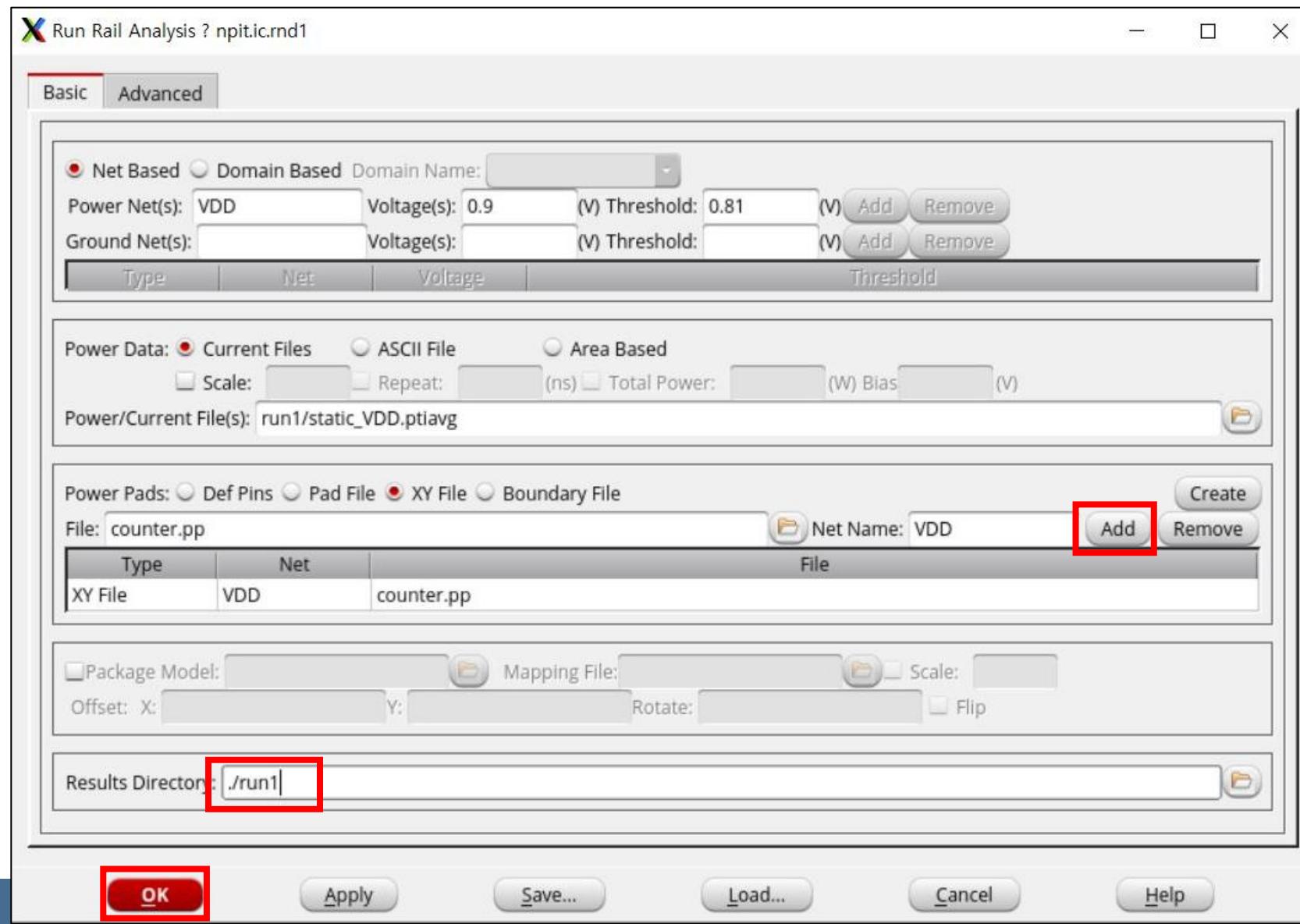
- Running Rail Analysis - Run
- counter.pp 더블 클릭



Auto PnR

Innovus

- Running Rail Analysis - Run
- 1. Add 클릭
- 2. 파일 이름 기입
- 3. OK 클릭



Auto PnR

Innovus

- Running Rail Analysis – Run
- 결과 확인

```
Rail Analysis Statistics:  
Warning messages:      0  
Error messages:       0
```

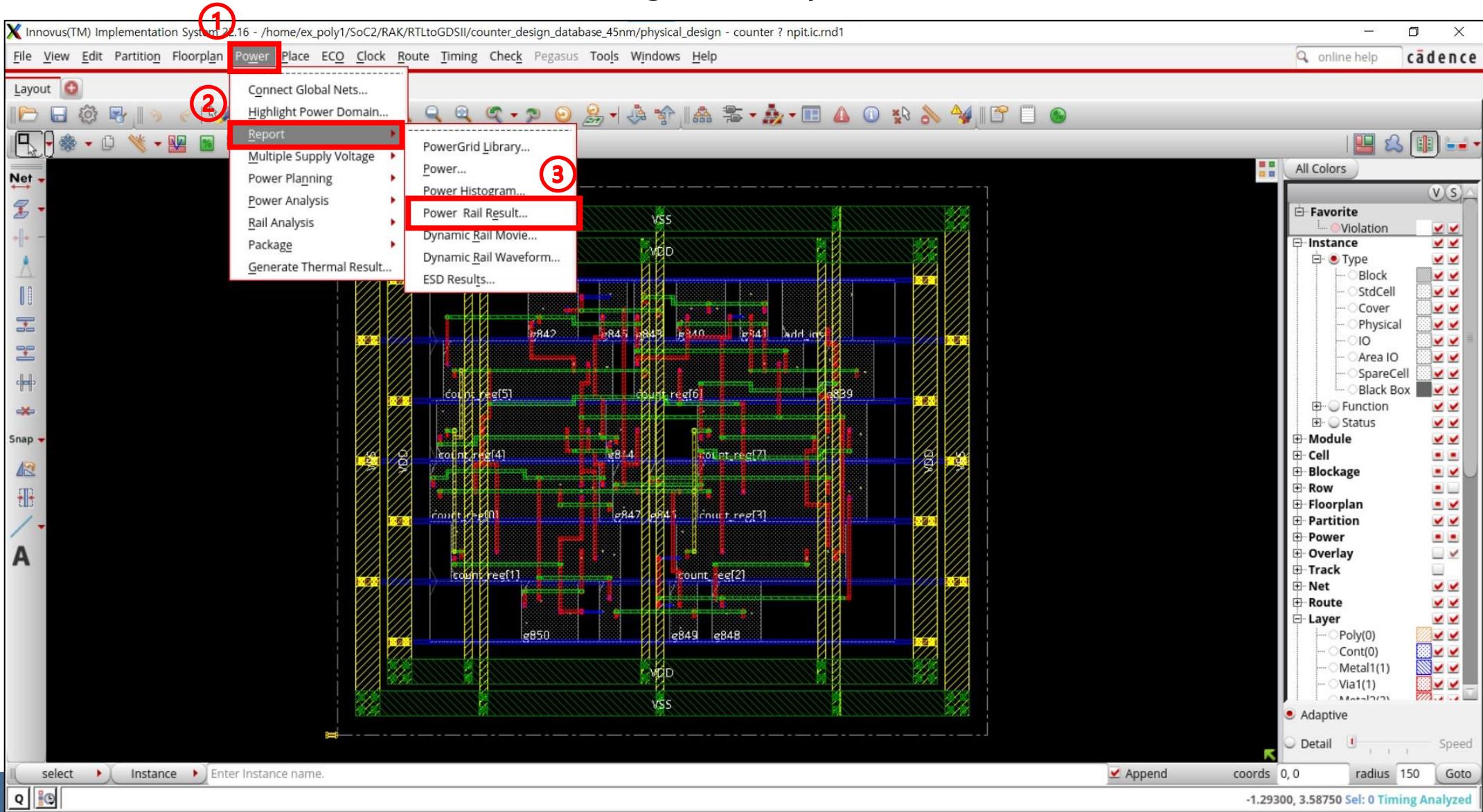
Rail Analysis completed successfully.

```
Finished Rail Analysis at 11:22:27 02/25/2025 (cpu=0:00:09, real=0:00:15, peak mem=2837.72MB)  
Current Innovus resource usage: (total cpu=0:04:44, real=1:23:48, mem=2794.46MB)
```

Auto PnR

Innovus

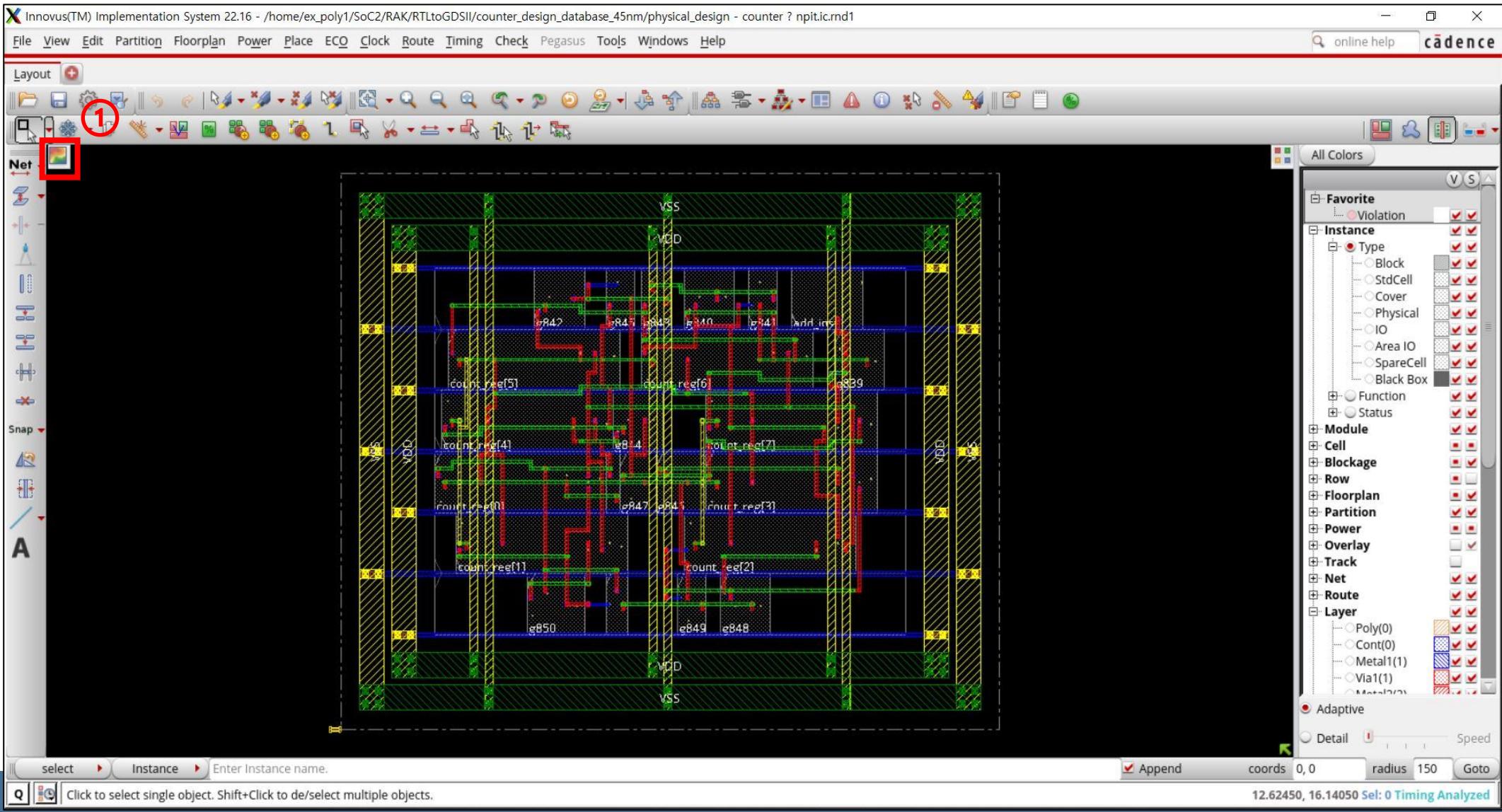
- Running Rail Analysis – Power Rail Result



Auto PnR

Innovus

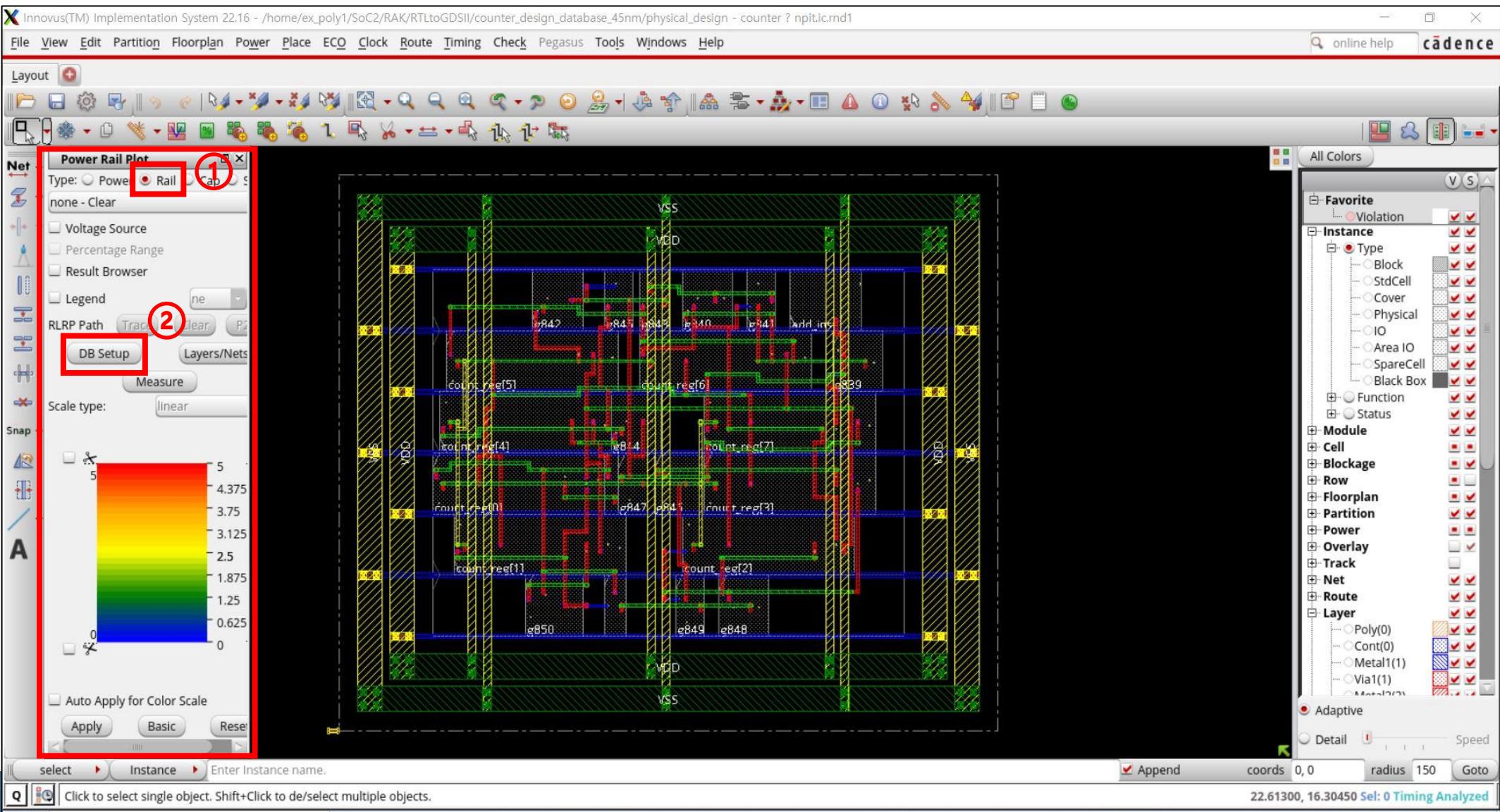
- Running Rail Analysis – Power Rail Result



Auto PnR

Innovus

- Running Rail Analysis – Power Rail Result



Auto PnR

Innovus

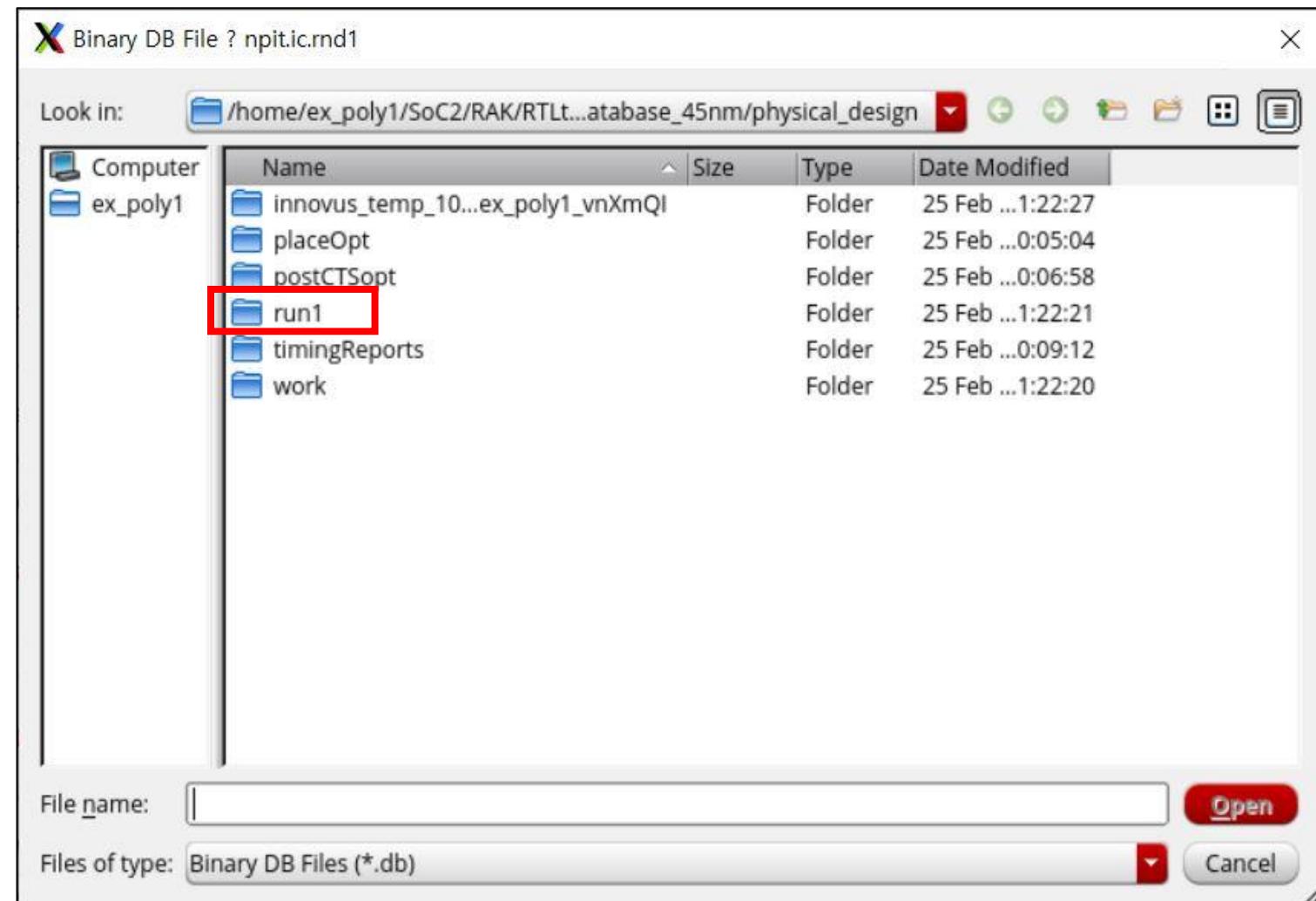
- Running Rail Analysis – Power Rail Result



Auto PnR

Innovus

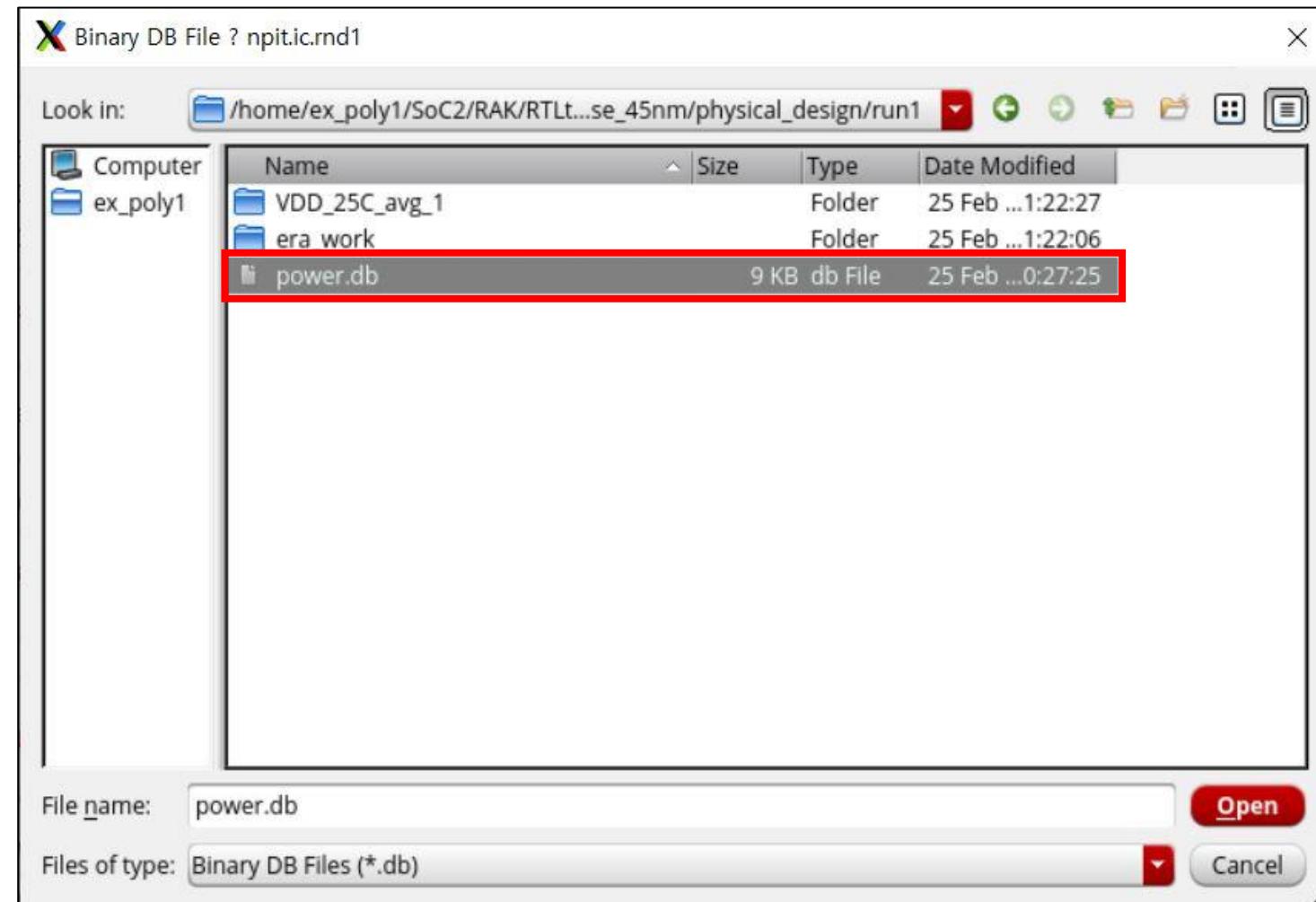
- Running Rail Analysis – Power Rail Result



Auto PnR

Innovus

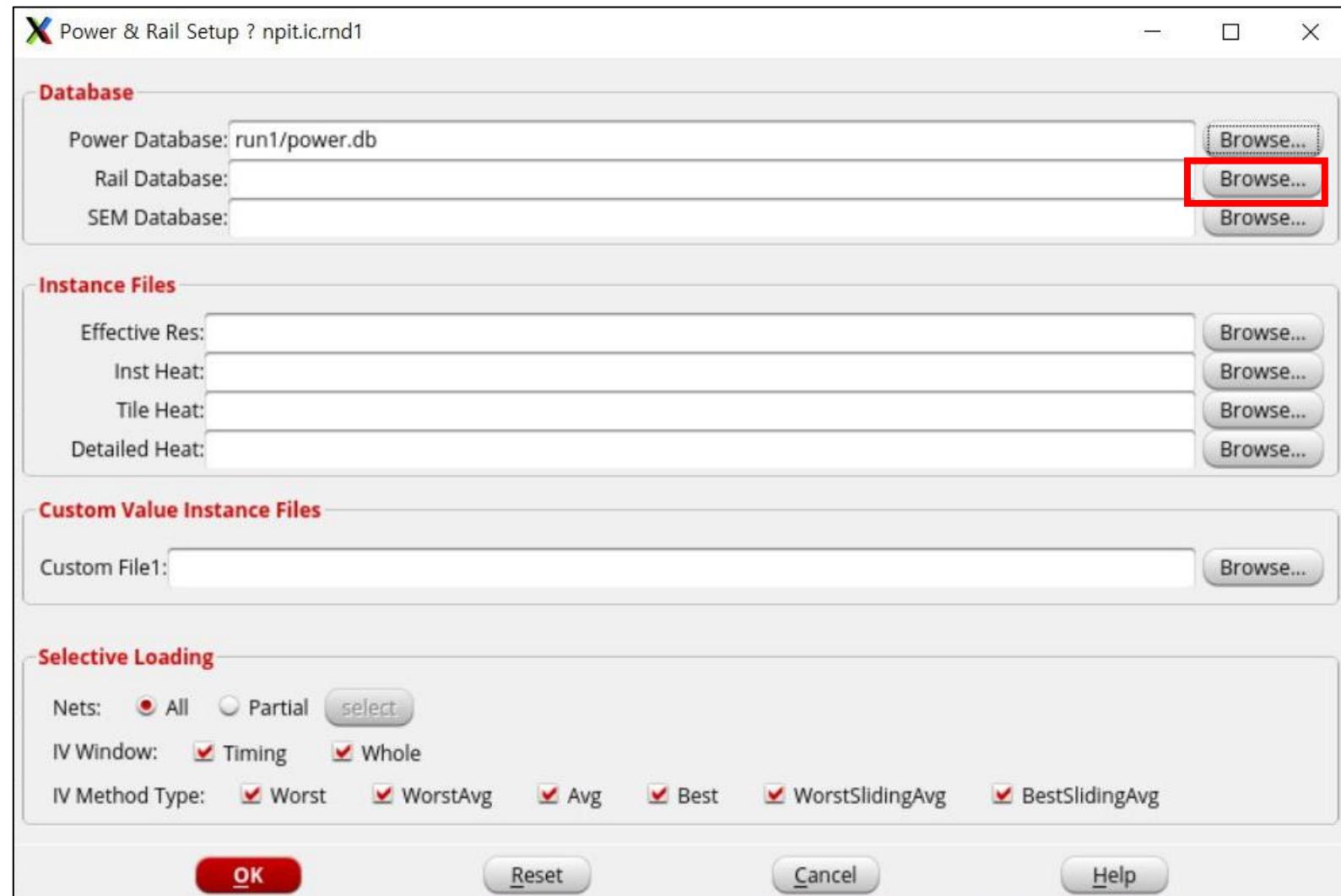
- Running Rail Analysis – Power Rail Result



Auto PnR

Innovus

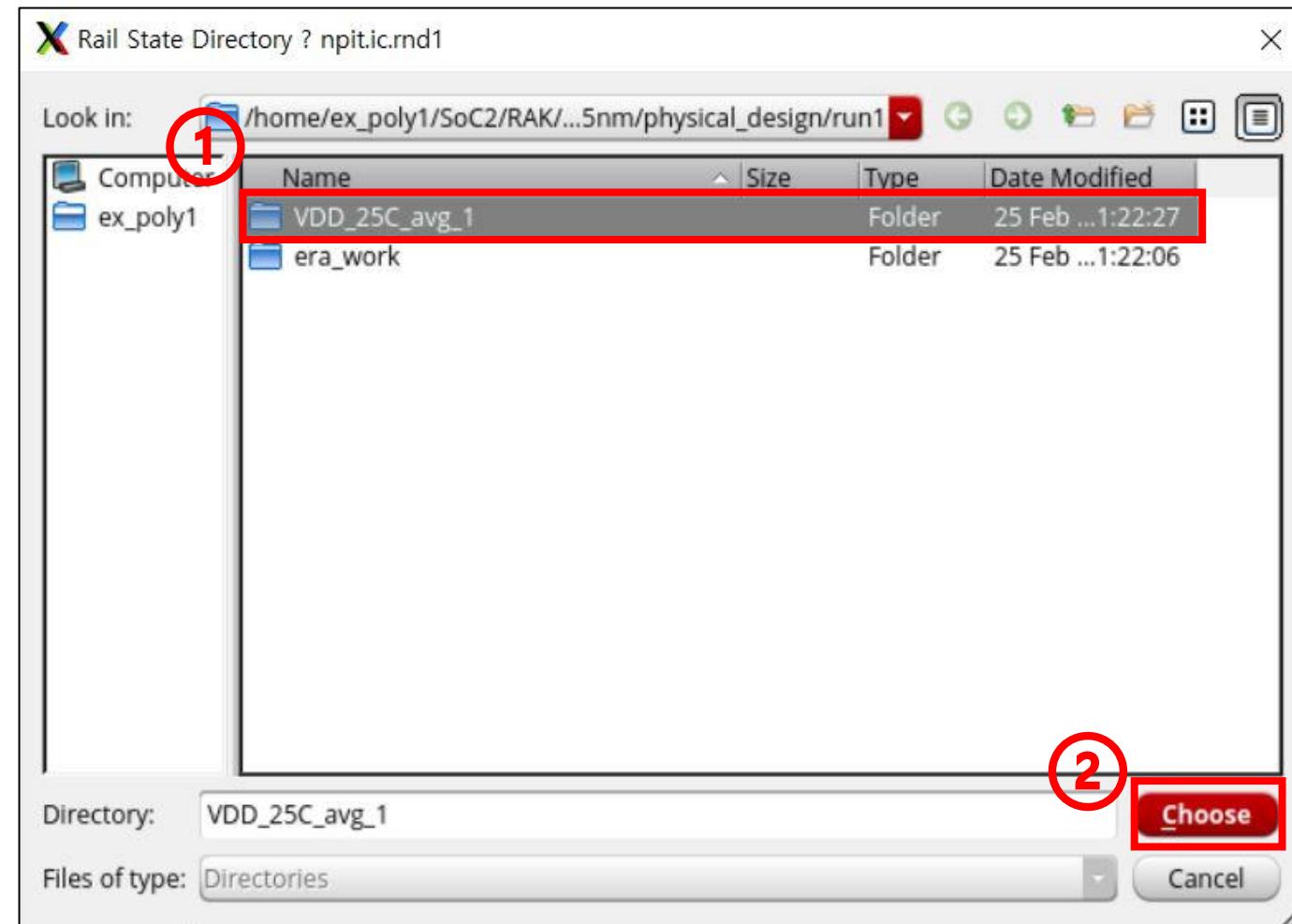
- Running Rail Analysis – Power Rail Result



Auto PnR

Innovus

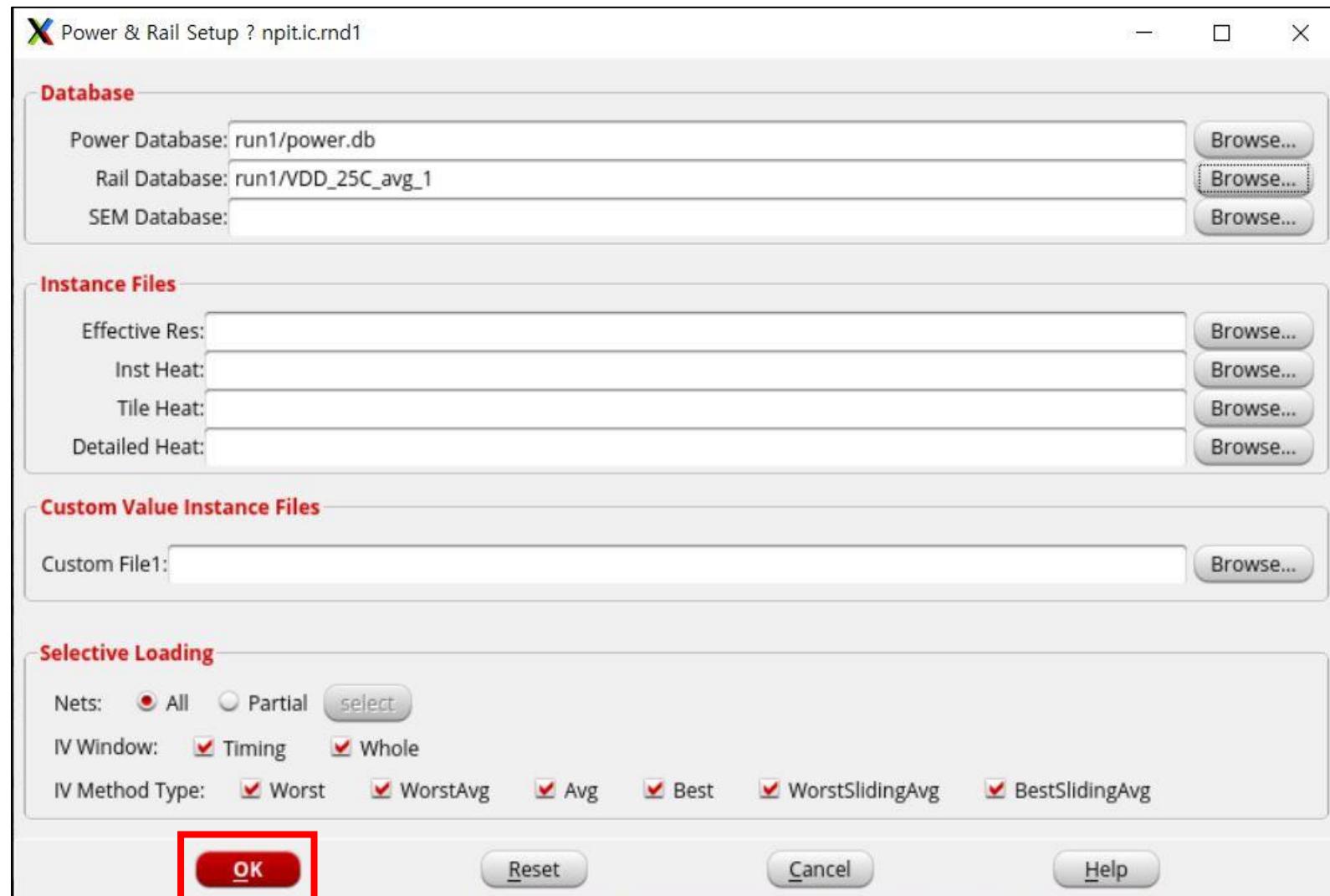
- Running Rail Analysis – Power Rail Result



Auto PnR

Innovus

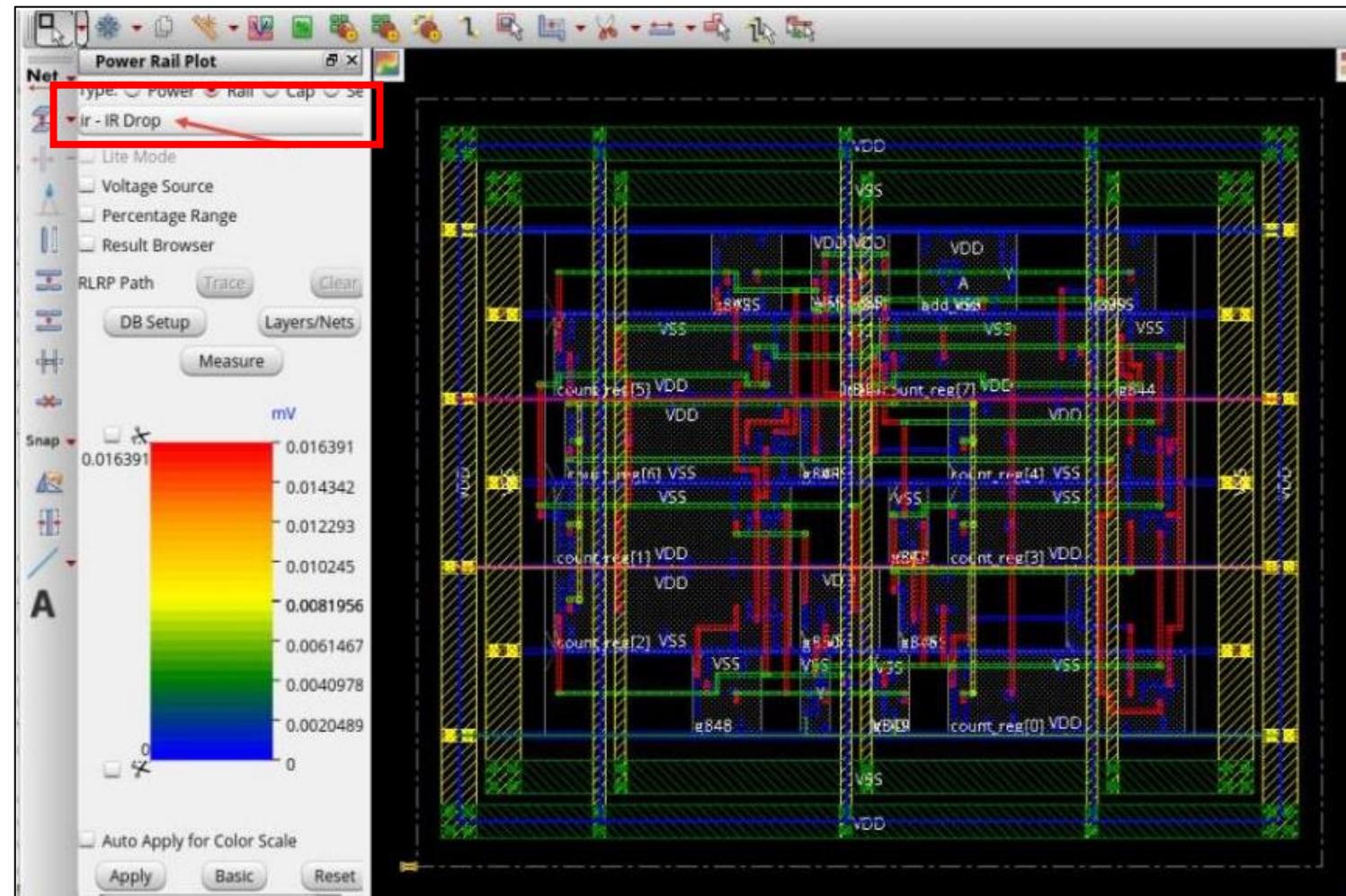
- Running Rail Analysis – Power Rail Result



Auto PnR

Innovus

- Running Rail Analysis – Power Rail Result
- IR-Drop 선택하여 결과 확인



Auto PnR

Innovus

- Running Rail Analysis – Power Rail Result
- 지금까지의 과정을 write_db counter.inn –lib 명령으로 저장함

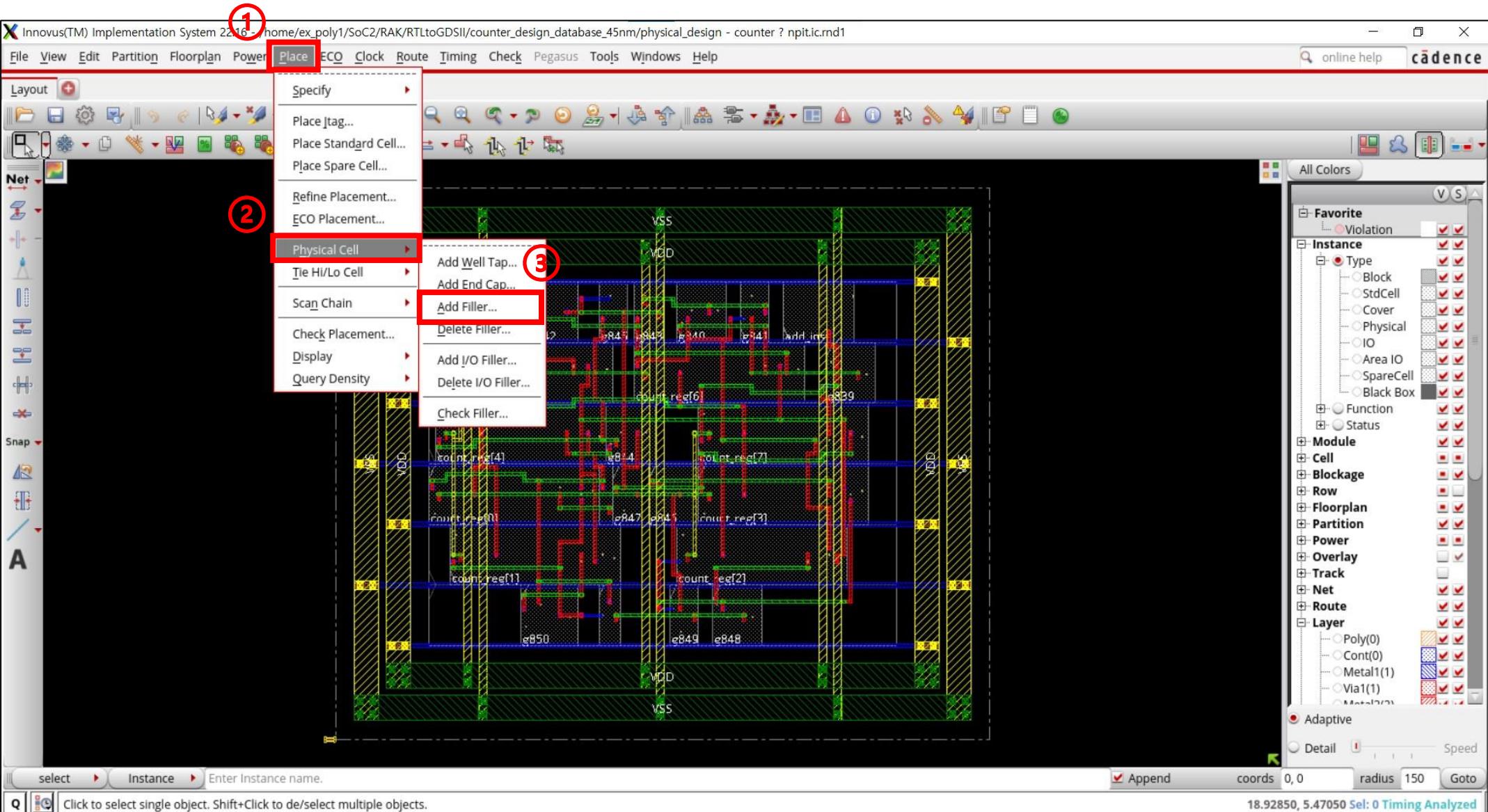
```
write_db counter.inn -lib
```

```
7M, current mem=2219.7M)
Saving SCANDEF file ...
*** Scan Trace Summary (runtime: cpu: 0:00:00.0 , real: 0:00:00.0):
Successfully traced 1 scan chain (total 8 scan bits).
Start applying DEF ordered sections ...
Successfully applied all DEF ordered sections.
*** Scan Sanity Check Summary:
*** 1 scan chain passed sanity check.
Saving property file counter.inn/counter.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=2915.8M) ***
#Saving pin access data to file counter.inn/counter.apa ...
#
% Begin Save power constraints data ... (date=02/25 11:46:59, mem=2219.7M)
% End Save power constraints data ... (date=02/25 11:46:59, total cpu=0:00:00.0, real=0:00:00.0, peak
res=2219.7M, current mem=2219.7M)
Generated self-contained design counter.inn
#% End save design ... (date=02/25 11:46:59, total cpu=0:00:01.8, real=0:00:02.0, peak res=2220.9M, c
urrent mem=2220.9M)
*** Message Summary: 0 warning(s), 0 error(s)
```

Auto PnR

Innovus

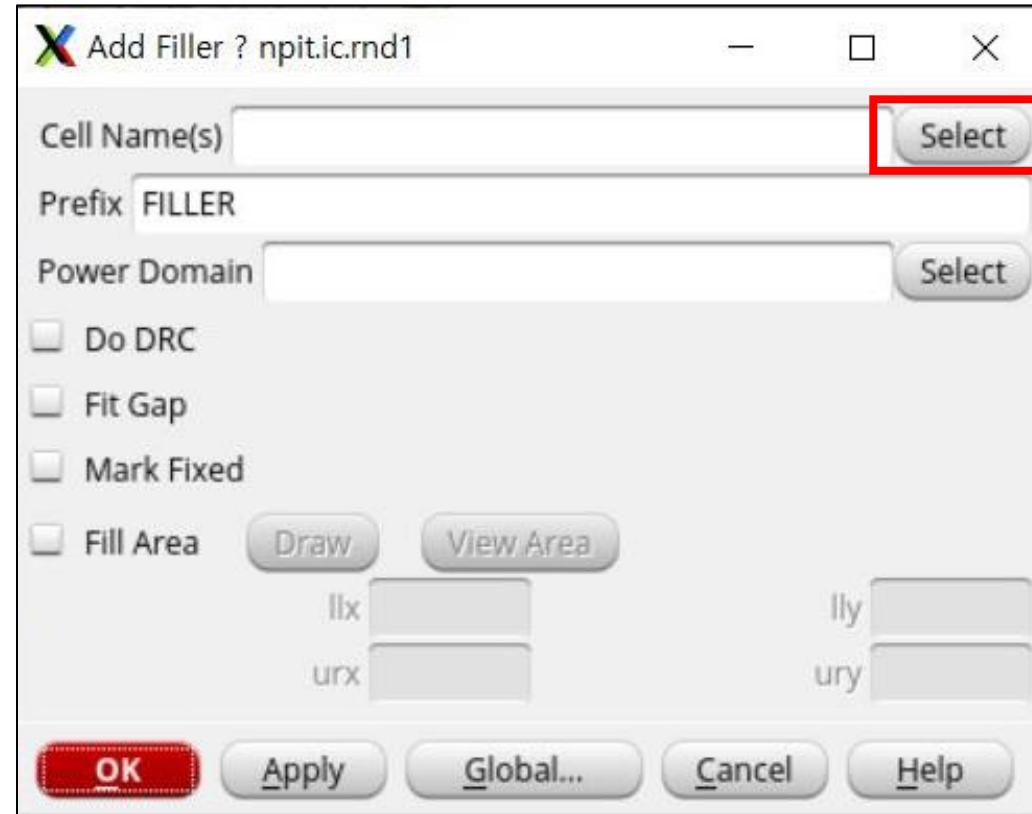
- Filler Cell Placement



Auto PnR

Innovus

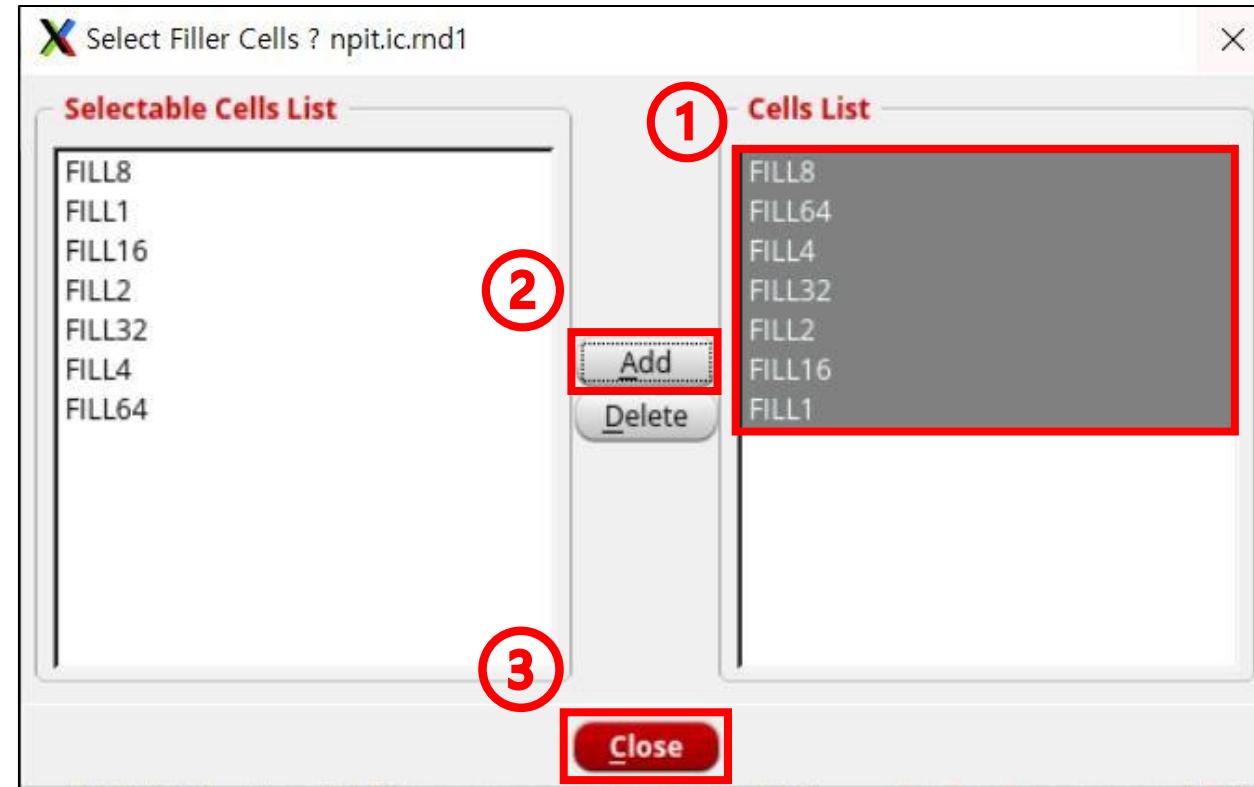
- Filler Cell Placement
- Select 클릭



Auto PnR

Innovus

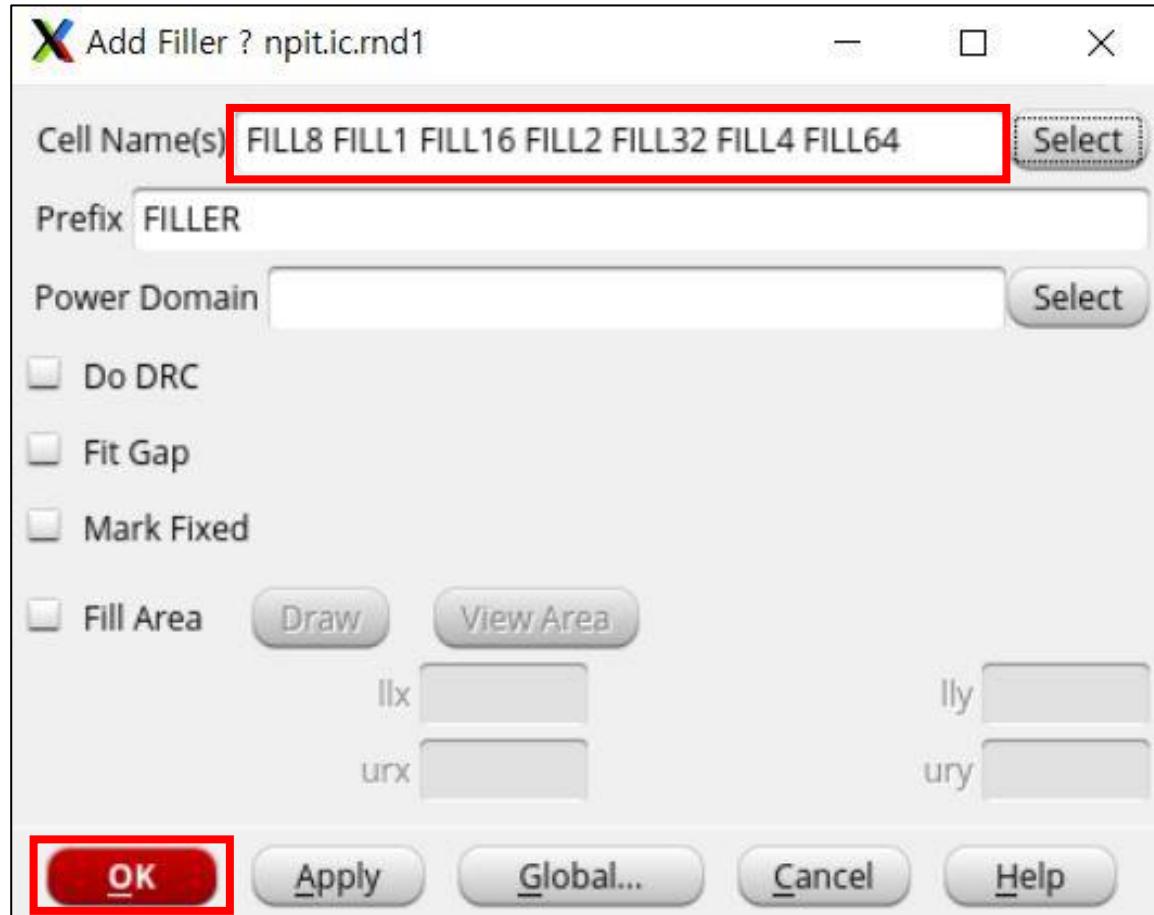
- Filler Cell Placement
- 전체 선택 후 Add



Auto PnR

Innovus

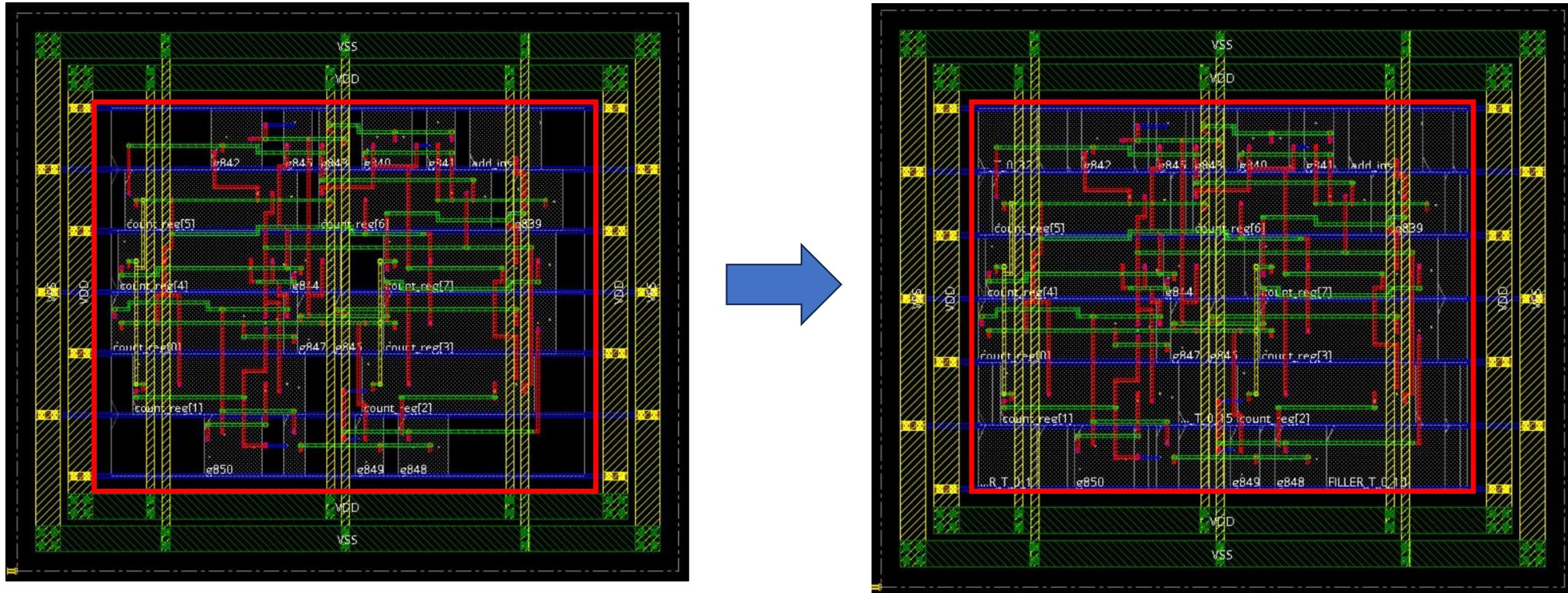
- Filler Cell Placement
- Filler 확인 후 OK 클릭



Auto PnR

Innovus

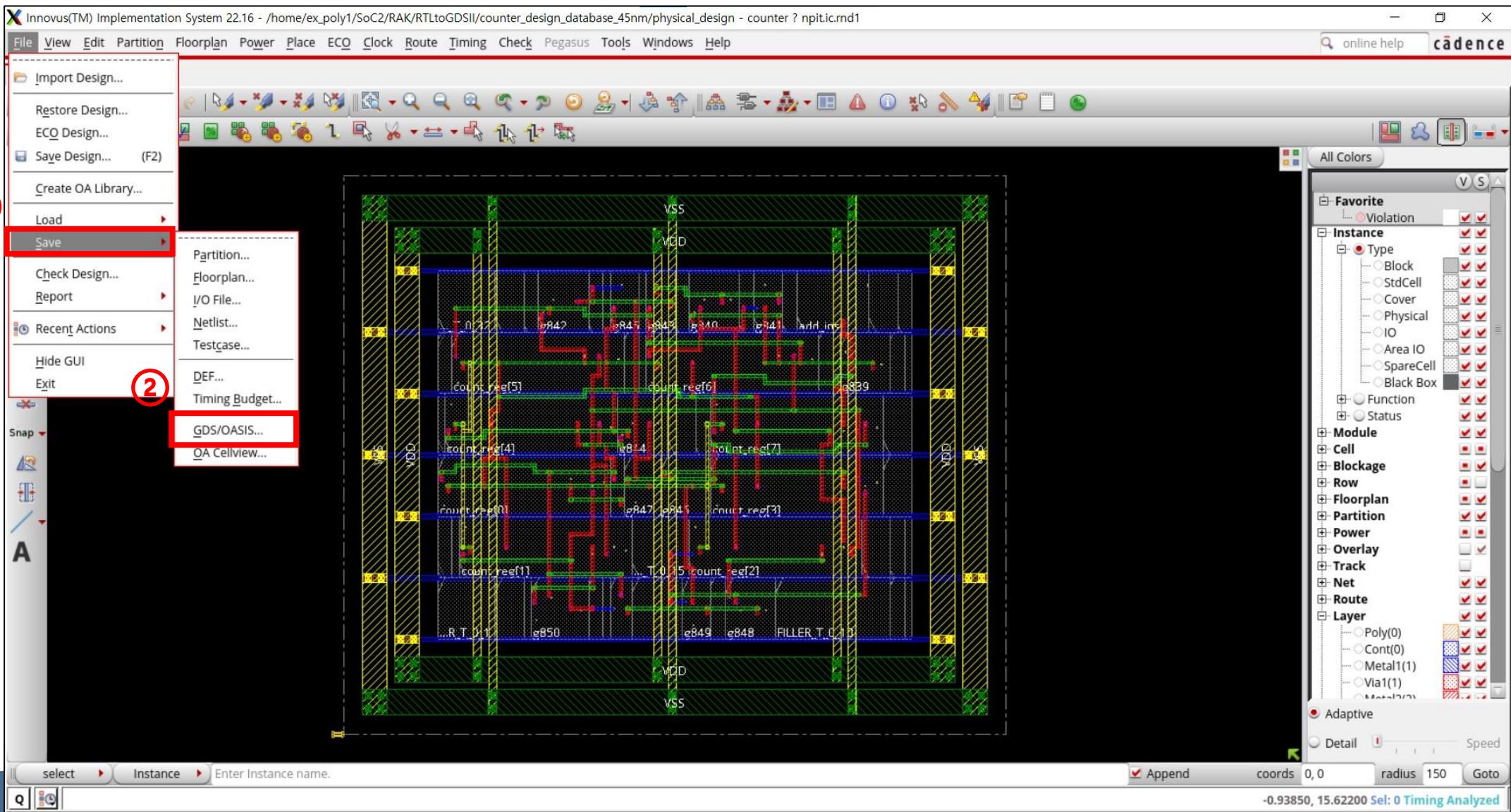
- Filler Cell Placement
- Core 부분에 흰색으로 Filler가 채워진 것을 확인할 수 있음



Auto PnR

Innovus

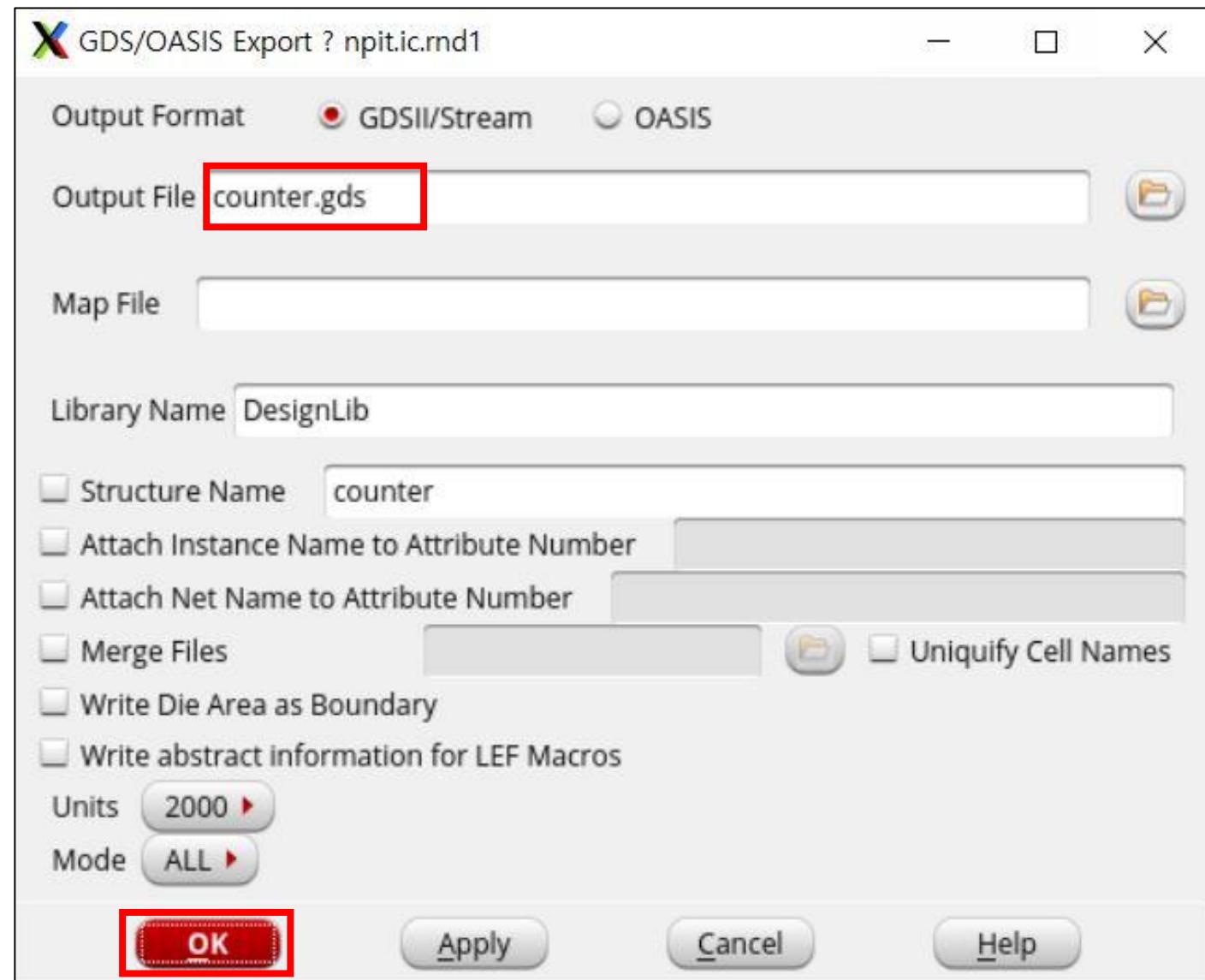
- Generating a Stream File



Auto PnR

Innovus

- Generating a Stream File
- File 이름 설정 후 OK 클릭



Auto PnR

Innovus

- Generating a Stream File
- .gds 파일이 생성됨

추후 머지에 사용되는
파일임

```
[ex_poly1@npit physical_design]$ ls
cellIDMap                      innovus.cmd2      innovus.logv4
collectGenusLibrary.log          innovus.cmd3      innovus.logv5
counter.conn.rpt                 innovus.cmd4      innovus.logv6
counter.conn.rpt.old            innovus.cmd5      innovus_temp_
ic.rnd1_ex_poly1_vnXmQI          place0pt
counter.drc.rpt                  innovus.cmd6      pm.ob
counter.drc.rpt.old             innovus.log       postCTSopt
counter.gds                      innovus.log1      power.tcl
counter.inn                      innovus.log2      rc_model.bin
counter.pp                       innovus.log3      readme
counter.scandef                  innovus.log4
counter.spef                     innovus.log5      run1
```