This document is a DRAFT!

The purpose is to describe how to create a U-BOOT-SPL based PRELOADER image for Altera CycloneV/ArriaV which enables the Offchip-Trace interface on the HPS DedicatedIO pins.
As reference platform we use the Altera Cyclone V SoC Development Kit.
See:

- https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-cyclone-v-soc.html

Sources:

- http://rocketboards.org/

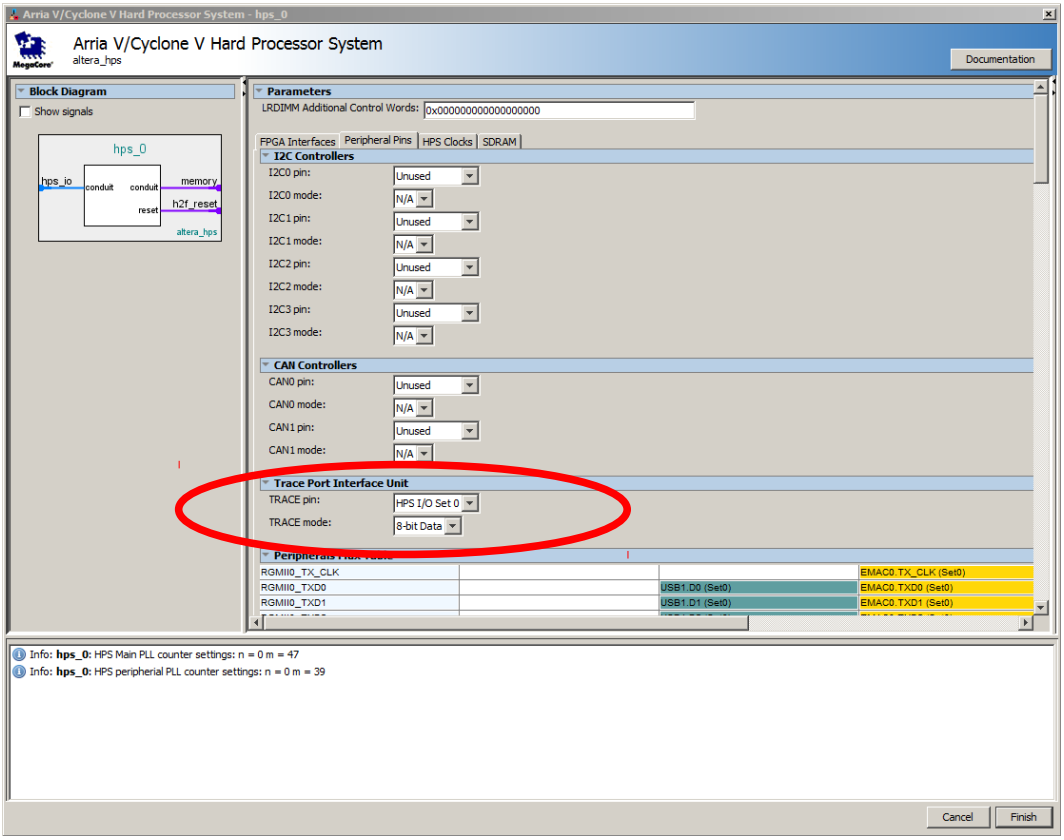
Quartus

Generate New Project.

- Select a Altera SoC device (e.g. a Cyclone V SoC)
- Open the QSYS Editor
- Add a new Hard Processing System

QSYS

Step 1: Export/Enable Trace Pins

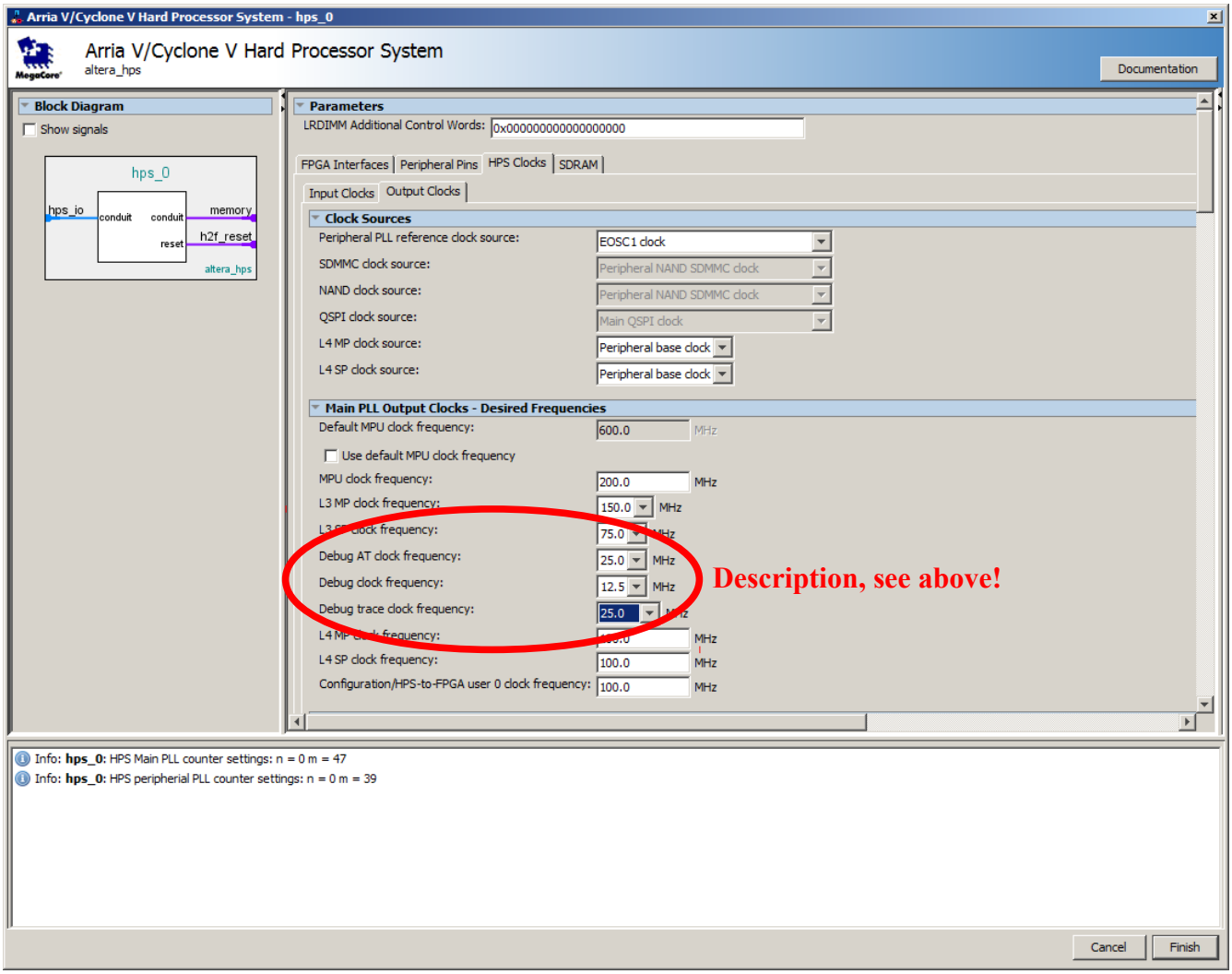


We select here a FULL 8-Bit Trace interface. This will export TRACEDATA[7..0] and TRACECLK.

Step 2: Trace Clock Configuration
Please set

- DBG_AT_CLOCK to to the maximum frequency (MPU_BASE_CLK/2)
  as this frequency is used for the SoC internal trace infrastructure
- DBG_TRACE_CLK between 200MHz to 250MHz
  this will result to 100MHz to 125MHz external DDR clock

Please note that these values might vary depending on the speedgrade of the device.



Step 3: Save QSYS + Generate HDL

Please save the project now, and integrate the QSYS project into your design.

For the next steps please refer to http://rocketboards.org .

Quartus

Please run Quartus now till the assembler phase (generate programming files). Quartus will now generate the FPGA Design and the PRELOADER Handoff files.

The files are typically located at:

<project path>/hps_isw_handoff/ ….

SoC Embedded Design Suite

Now we need to create the PRELOADER using the bsp-editor.

- Open the EDS console
- start the bsp-editor
- convert the handoff files from the previous steps into a PRELOADER project

now we need to compile the preloader. The PRELOADER project is typically located at:

<project path>/software/spl_bsp/....

SoC Embedded Design Suite

Now we can test the preloader using Trace32. E.g. Set the bootdevice to SD-Card and remove the SD-Card. This will stop the SoC in the BootROM regardless if the RESET line is wired or not.

An example script sequence is available at:

<T32>/demo/arm/cyclonevsoc/cyclone_v_soc_dev_kit

Example script:

```
WinCLEAR
RESet
SYStem.RESet
SYStem.CPU CYCLONEVSOC
; use e.g. SYStem.DETECT.ShowCHAIN for detection
SYStem.CONFIG DAPIRPRE  <your board sepecific parameter>
SYStem.CONFIG DAPIRPOST <your board sepecific parameter>
SYStem.CONFIG DAPDRPRE  <your board sepecific parameter>
SYStem.CONFIG DAPDRPOST <your board sepecific parameter>
CORE.ASSIGN 1.
SYStem.Mode.Attach

; disable WDOG
; disable Watchdog - Toggle RESET in PERMODRST
Data.Set A:0xFFD05014 %Long Data.Long(A:0xFFD05014)|0x40
Data.Set A:0xFFD05014 %Long
 Data.Long(A:0xFFD05014)&(~0x40)

; Load the Preloader
Data.LOAD.Elf <project path>/software/spl_bsp/uboot-
socfpga/spl/u-boot-spl /CYGDRIVE

; run the preloader till spl_boot_device
Go spl_boot_device /Onchip
WAIT !RUN() 3.s

; now setup the trace
ETM.Trace ON
ETM.ON
Trace.METHOD Analyzer
; use auto-calibration
Trace.AutoFocus

; load second stage bootloader …
Data.LOAD.Elf …/u-boot …
; or run a trace32-demo
DO ~~/demo/arm/compiler/gnu-pic/demo_sieve <RAM ADDRESS>
; disable the wdog
Data.Set A:0xFFD05014 %Long Data.Long(A:0xFFD05014)|0x40
Data.Set A:0xFFD05014 %Long
 Data.Long(A:0xFFD05014)&(~0x40)
```