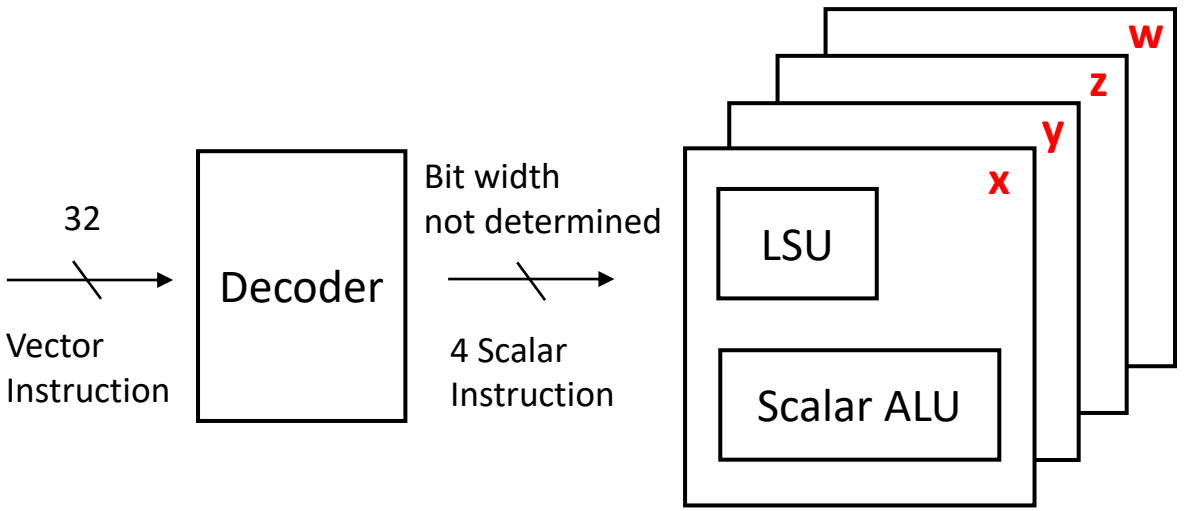
Architecture level design

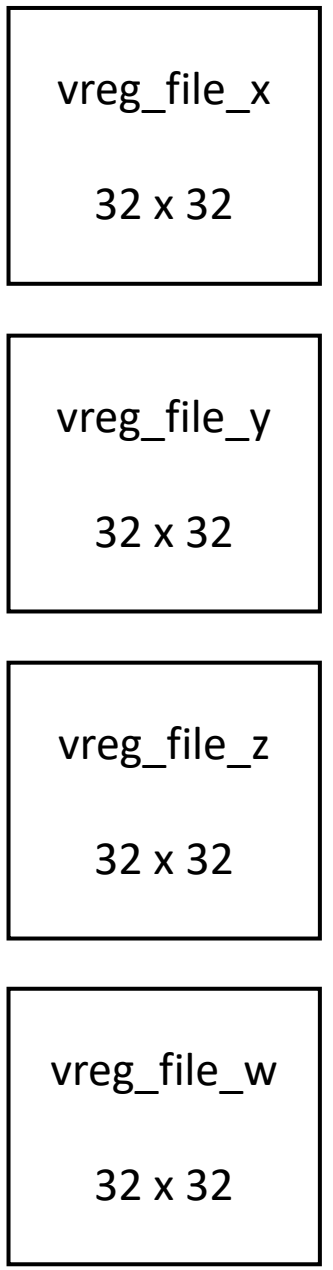
Vector register files

Shared data memory
➞ load, store 128bit vector

Vector processor(VP)
Each module is scalar processor(SP)



32 x 4



32 x 4

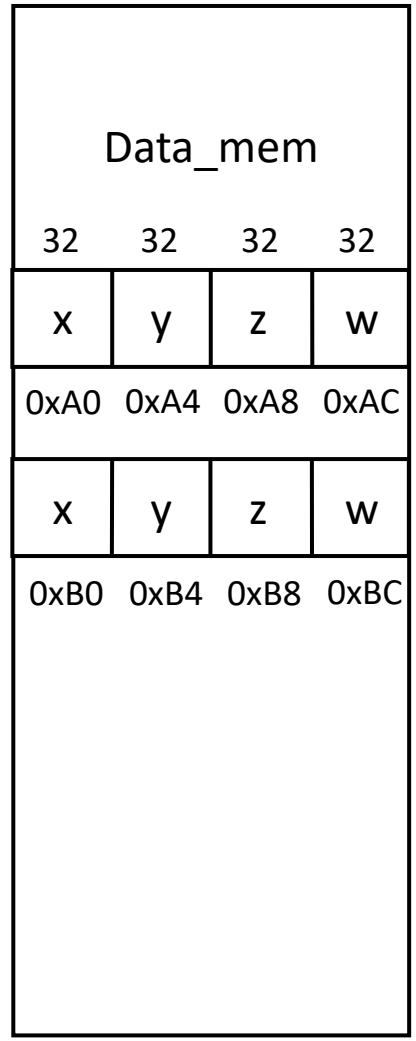
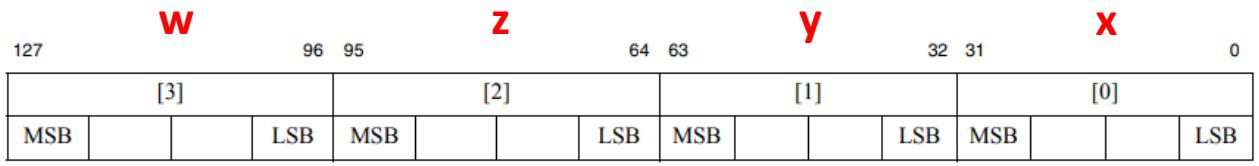
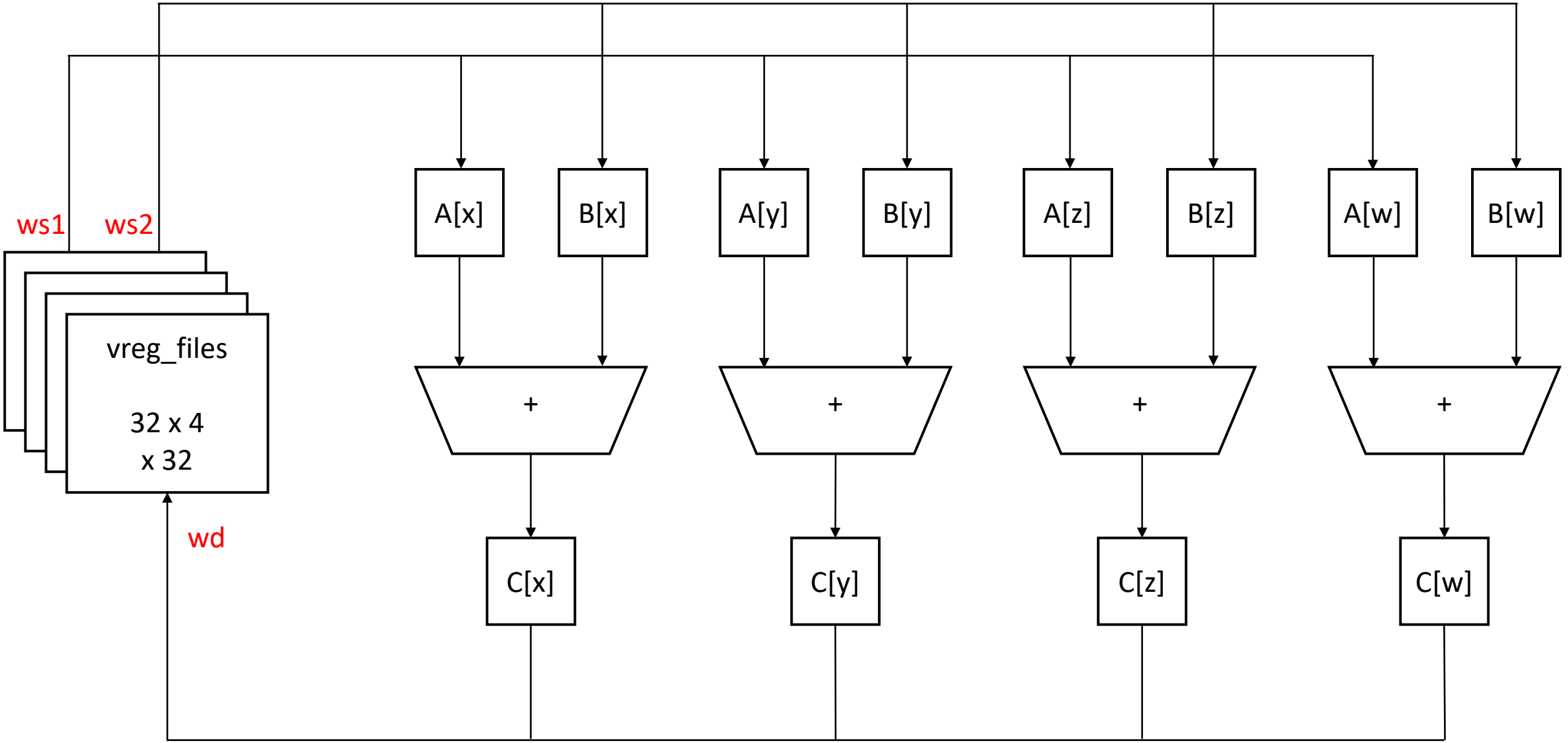


Figure 3-5 MSA Vector Register Word Elements

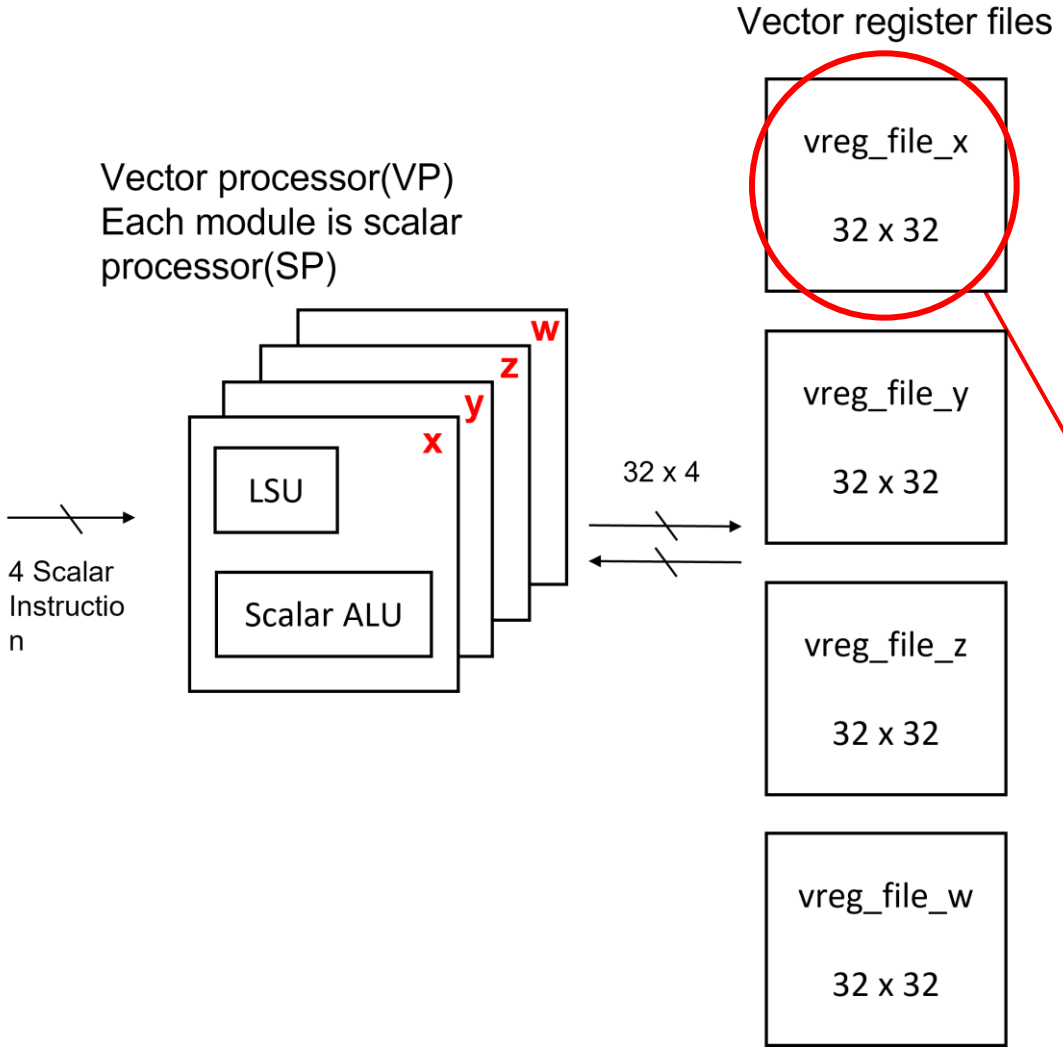


Behavior of 4 lanes for ADDV(C = A + B) per 1 clock cycle



Possibility

About bank & vector register file



P1. 우리가 구상한 각 register가 bank가 아닐까?
P2.각 element의 vreg_file instance를 합친 모듈이 VGPR?

➞ RTL 설계하면서 검토해보기