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IAA6007: Computer Architecture
Ch.7. Micro-programmed Control

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Outline

- 7.1 Control memory
- 7.2 Address sequencing
- 7.3 Micro-program example
- 7.4 Design of control unit

7.1 Control memory

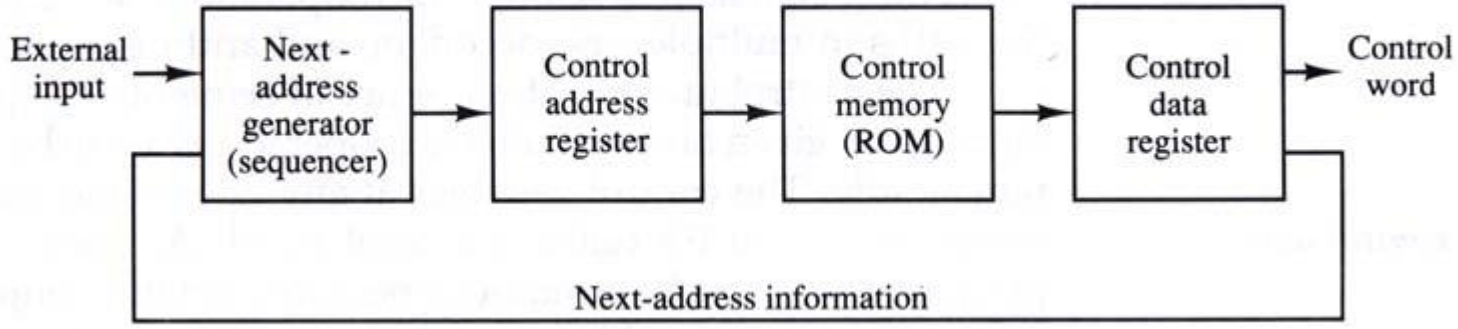
- Hard-wired control vs. micro-programmed control
  - How the control signals for micro operations are generated ?
  - Hard-wired: by hardware using conventional logic design technique (chapter 5)
  - Micro-programmed: by a program stored in control memory

- Control variable specifies a micro-operation
- Control word – values of control variables at any given time that can be represented by string 1's and 0's
- Control memory – ROM where control words are stored
- Micro-instruction – each word stored in control memory
- Micro-program – a sequence of micro-instructions

7.1 Control memory

- General configuration of a micro-programmed control unit
  - Control memory
  - Control address register
  - Control data register
  - Sequencer
    - address generator

Figure 7-1 Microprogrammed control organization.



7.1 Control memory

- Advantage
  - Once the hardware configuration is established, there should no need for further hardware or wiring changes
  - If we want to establish a different control sequence for the system, all we need to do is to specify a different set of micro-instructions for control memory
  - Simple logic of hardware control compared to hardwired control

- Disadvantage
  - Slower compared to hardwired control
    - Consume processing time due to control memory
  - Most computers based on RISC (Reduced Instruction Set Computer) use hardwired control rather than a micro-programmed control

7.2 Address sequencing

- Each instruction has its own micro-program routine
- Steps to go through to execute a single instruction
  - 1. Instruction fetch routine
  - 2. Routine that determines the effective address
  - 3. Routine for the fetched instruction, then control returns to fetch routine
- Mapping
  - Transformation from the instruction code bits to an address in control memory

7.2 Address sequencing

- Address sequencing for control memory
  1) Increment of CAR
  2) Conditional branching
  3) Mapping from instruction
  4) Subroutine call and return

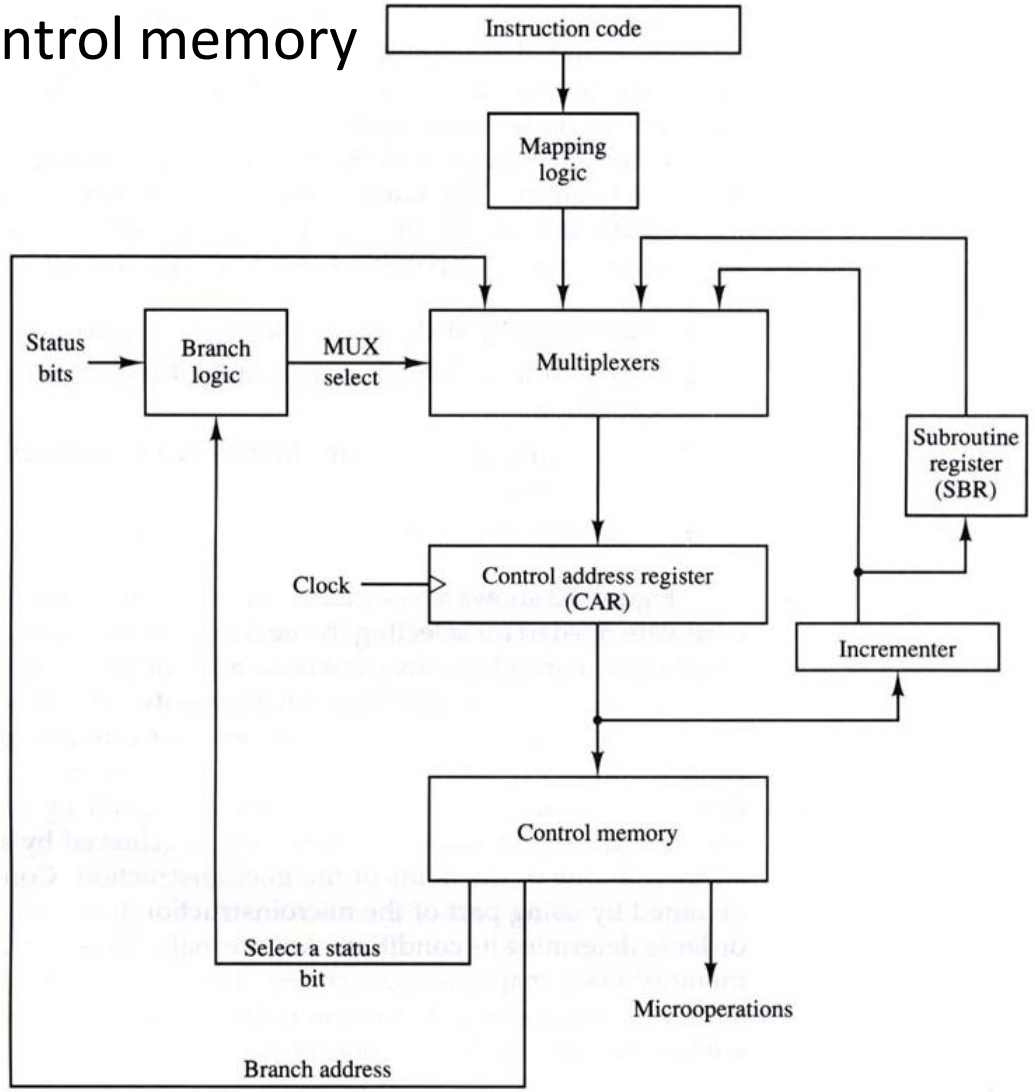
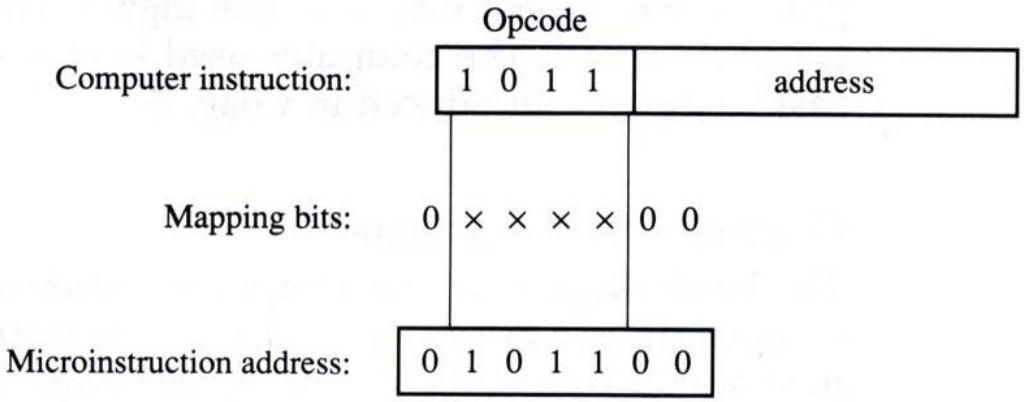


Figure 7-2 Selection of address for control memory.

7.2 Address sequencing

- Mapping of instruction
  - 1. Simple mapping

Figure 7-3 Mapping from instruction code to microinstruction address.



  - 2. Mapping ROM
    - Bits of instruction specify the address of a mapping ROM; mapping ROM contains the address of control memory
- Subroutines – micro-programs may contain identical sections of code

7.3 Micro-program example

- Computer configuration - the transfer of information among registers is done through multiplexer rather than a common bus

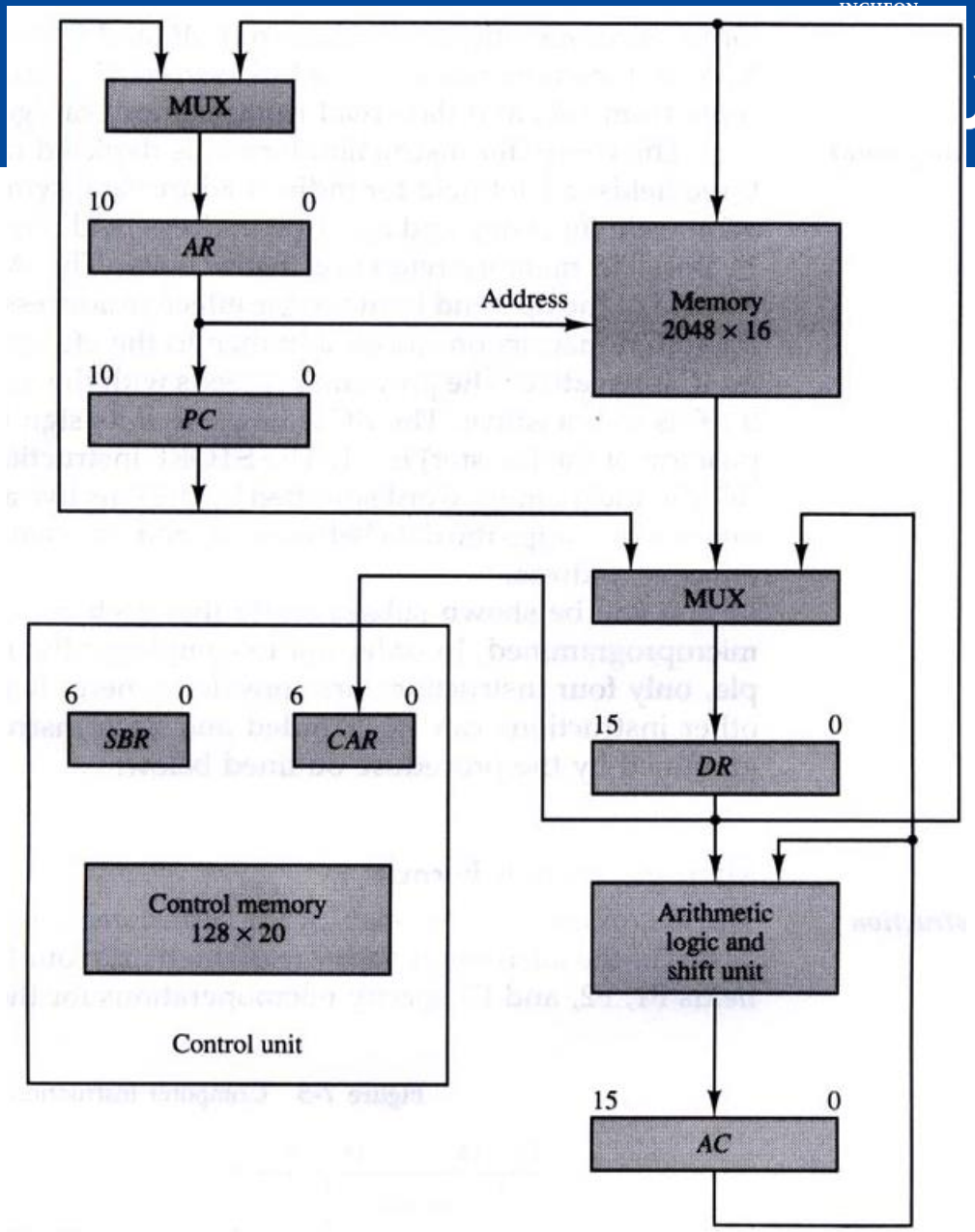
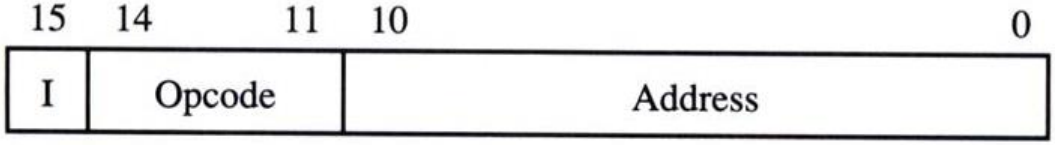


Figure 7-4 Computer hardware configuration.

7.3 Micro-program example

- Instruction format

Figure 7-5 Computer instructions.



(a) Instruction format

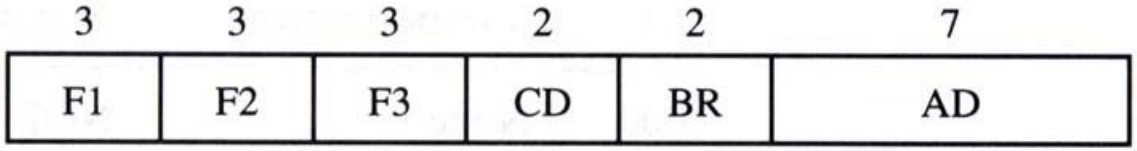
Symbol	Opcode	Description
ADD	0000	$AC \leftarrow AC + M\,[EA]$
BRANCH	0001	If $(AC < 0)$ then $(PC \leftarrow EA)$
STORE	0010	$M\,[EA] \leftarrow AC$
EXCHANGE	0011	$AC \leftarrow M[EA], M[EA] \leftarrow AC$

EA is the effective address

(b) Four computer instructions

7.3 Micro-program example

- Micro-instruction format



F1, F2, F3: Microoperation fields

CD: Condition for branching

BR: Branch field

AD: Address field

Figure 7-6 Microinstruction code format (20 bits).

7.3 Micro-program example

- Microinstruction format
  - F1, F2, F3: micro-operation fields
    - ex) 000 for no operation
    - F2 = 100 for DR ← M[AR]
    - F3 = 101 for PC ← PC + 1
    - No more than three micro-operations for a microinstruction
    - No conflicting micro-operations can be specified simultaneously
  - Control field specifies form status bit conditions
  - Branch field is used to choose the address of the next microinstruction
  - Address field – branch address

- Symbolic micro-instruction
  - The symbols defined in Table 7-1 are used to specify micro-instruction

7.3 Micro-program example

TABLE 7-1 Symbols and Binary Code for Microinstruction Fields

F1	Microoperation	Symbol
000	None	NOP
001	$AC \leftarrow AC + DR$	ADD
010	$AC \leftarrow 0$	CLRAC
011	$AC \leftarrow AC + 1$	INCAC
100	$AC \leftarrow DR$	DRTAC
101	$AR \leftarrow DR(0\text{–}10)$	DRTAR
110	$AR \leftarrow PC$	PCTAR
111	$M[AR] \leftarrow DR$	WRITE

F2	Microoperation	Symbol
000	None	NOP
001	$AC \leftarrow AC - DR$	SUB
010	$AC \leftarrow AC \vee DR$	OR
011	$AC \leftarrow AC \wedge DR$	AND
100	$DR \leftarrow M[AR]$	READ
101	$DR \leftarrow AC$	ACTDR
110	$DR \leftarrow DR + 1$	INCDR
111	$DR(0\text{-}10) \leftarrow PC$	PCTDR

F3	Microoperation	Symbol
000	None	NOP
001	$AC \leftarrow AC \oplus DR$	XOR
010	$AC \leftarrow \overline{AC}$	COM
011	$AC \leftarrow$ shl AC	SHL
100	$AC \leftarrow$ shr AC	SHR
101	$PC \leftarrow PC + 1$	INCPC
110	$PC \leftarrow AR$	ARTPC
111	Reserved	

CD	Condition	Symbol	Comments
00	Always = 1	U	Unconditional branch
01	$DR(15)$	I	Indirect address bit
10	$AC(15)$	S	Sign bit of AC
11	$AC = 0$	Z	Zero value in AC

BR	Symbol	Function
00	JMP	$CAR \leftarrow AD$ if condition = 1
		$CAR \leftarrow CAR + 1$ if condition = 0
01	CALL	$CAR \leftarrow AD$, $SBR \leftarrow CAR + 1$ if condition = 1
		$CAR \leftarrow CAR + 1$ if condition = 0
10	RET	$CAR \leftarrow SBR$ (Return from subroutine)
11	MAP	$CAR(2\text{–}5) \leftarrow DR(11\text{–}14)$, $CAR(0,1,6) \leftarrow 0$

7.3 Micro-program example

- Symbolic micro-program

TABLE 7-2 Symbolic Microprogram (Partial)

Label	Microoperations	CD	BR	AD
	ORG 0			
ADD:	NOP	I	CALL	INDRCT
	READ	U	JMP	NEXT
	ADD	U	JMP	FETCH
	ORG 4			
BRANCH:	NOP	S	JMP	OVER
	NOP	U	JMP	FETCH
OVER:	NOP	I	CALL	INDRCT
	ARTPC	U	JMP	FETCH
	ORG 8			
STORE:	NOP	I	CALL	INDRCT
	ACTDR	U	JMP	NEXT
	WRITE	U	JMP	FETCH
	ORG 12			
EXCHANGE:	NOP	I	CALL	INDRCT
	READ	U	JMP	NEXT
	ACTDR, DRTAC	U	JMP	NEXT
	WRITE	U	JMP	FETCH
	ORG 64			
FETCH:	PCTAR	U	JMP	NEXT
	READ, INCPC	U	JMP	NEXT
	DRTAR	U	MAP	
INDRCT:	READ	U	JMP	NEXT
	DRTAR	U	RET	

7.3 Micro-program example

- The fetch routine

  AR ← PC
  DR ← M[AR], PC ← PC + 1
  AR ← DR(0-10), CAR(2-5) ← DR(11-14), CAR(0,1,6) ← 0

7.3 Micro-program example

- The fetch routine

AR ← PC
DR ← M[AR], PC ← PC + 1
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```
        ORG 64
FETCH:  PCTAR          U    JMP    NEXT
        READ, INCPC    U    JMP    NEXT
        DRTAR          U    MAP
```

Binary Address	F1	F2	F3	CD	BR	AD
1000000	110	000	000	00	00	1000001
1000001	000	100	101	00	00	1000010
1000010	101	000	000	00	11	0000000

7.3 Micro-program example

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        ORG 64
FETCH:  PCTAR          U   JMP   NEXT
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0000000	000	000	000	01	01	1000011
0000001	000	100	000	00	00	0000010
0000010	001	000	000	00	00	1000000
0000011	000	000	000	00	00	1000000

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7.3 Micro-program example

- Binary micro-program
  - In empty words in ROM, NOP U JMP FETCH is placed

TABLE 7-3 Binary Microprogram for Control Memory (Partial)

Micro Routine	Address		Binary Microinstruction					
	Decimal	Binary	F1	F2	F3	CD	BR	AD
ADD	0	0000000	000	000	000	01	01	1000011
	1	0000001	000	100	000	00	00	0000010
	2	0000010	001	000	000	00	00	1000000
	3	0000011	000	000	000	00	00	1000000
BRANCH	4	0000100	000	000	000	10	00	0000110
	5	0000101	000	000	000	00	00	1000000
	6	0000110	000	000	000	01	01	1000011
	7	0000111	000	000	110	00	00	1000000
STORE	8	0001000	000	000	000	01	01	1000011
	9	0001001	000	101	000	00	00	0001010
	10	0001010	111	000	000	00	00	1000000
	11	0001011	000	000	000	00	00	1000000
EXCHANGE	12	0001100	000	000	000	01	01	1000011
	13	0001101	001	000	000	00	00	0001110
	14	0001110	100	101	000	00	00	0001111
	15	0001111	111	000	000	00	00	1000000
FETCH	64	1000000	110	000	000	00	00	1000001
	65	1000001	000	100	101	00	00	1000010
	66	1000010	101	000	000	00	11	0000000
INDRCT	67	1000011	000	100	000	00	00	1000100
	68	1000100	101	000	000	00	10	0000000

7.4 Design of control unit

- The number of control bits can be reduced by grouping mutually exclusive variables and encoding them
- Decoding of F fields
- Arithmetic logic shift unit (same as in Figs. 5-19, 5-20)

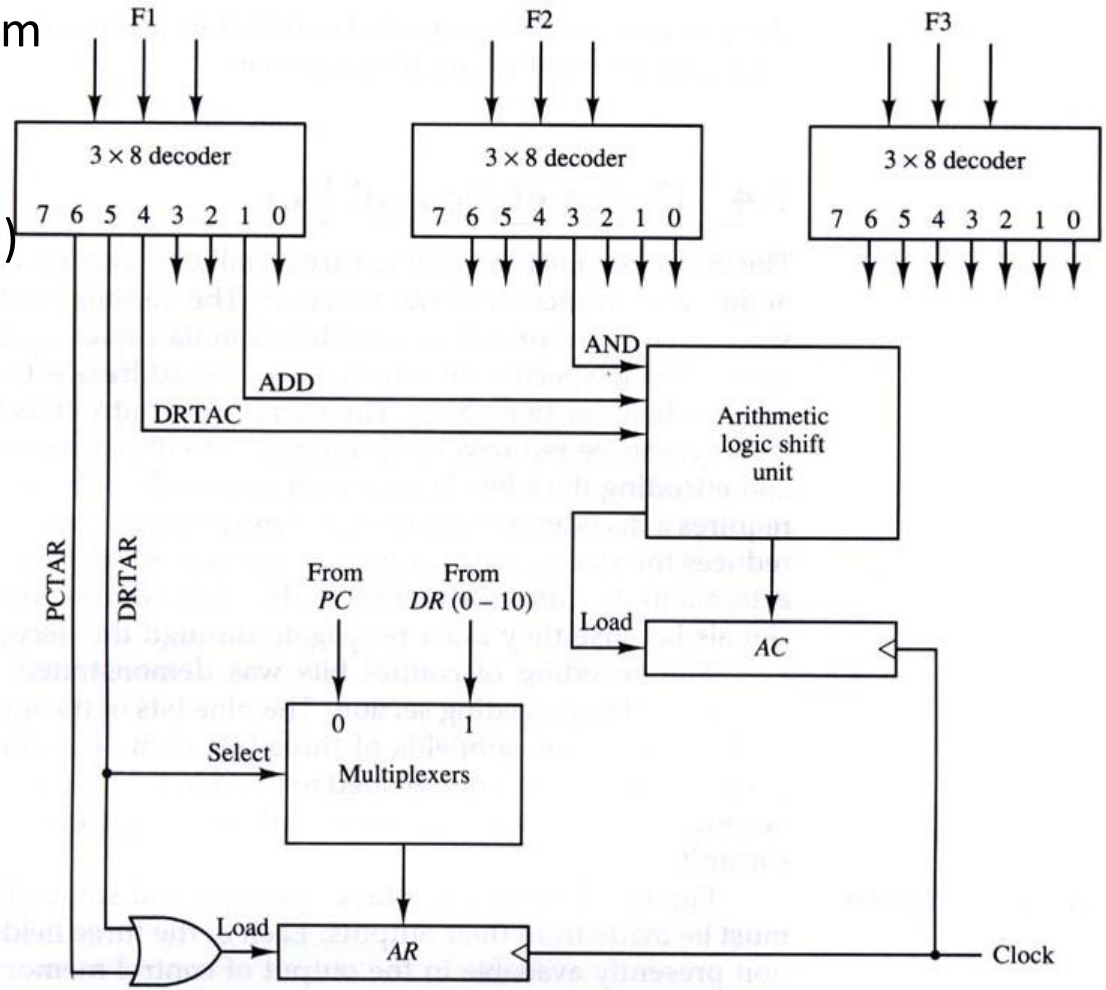

Figure 7-7 Decoding of microoperation fields.

7.4 Design of control unit

- Arithmetic logic shift unit (same as in Figs. 5-19, 5-20)
- Micro-program sequencer

BR	Symbol	Function
00	JMP	$CAR \leftarrow AD$ if condition = 1
		$CAR \leftarrow CAR + 1$ if condition = 0
01	CALL	$CAR \leftarrow AD$, $SBR \leftarrow CAR + 1$ if condition = 1
		$CAR \leftarrow CAR + 1$ if condition = 0
10	RET	$CAR \leftarrow SBR$ (Return from subroutine)
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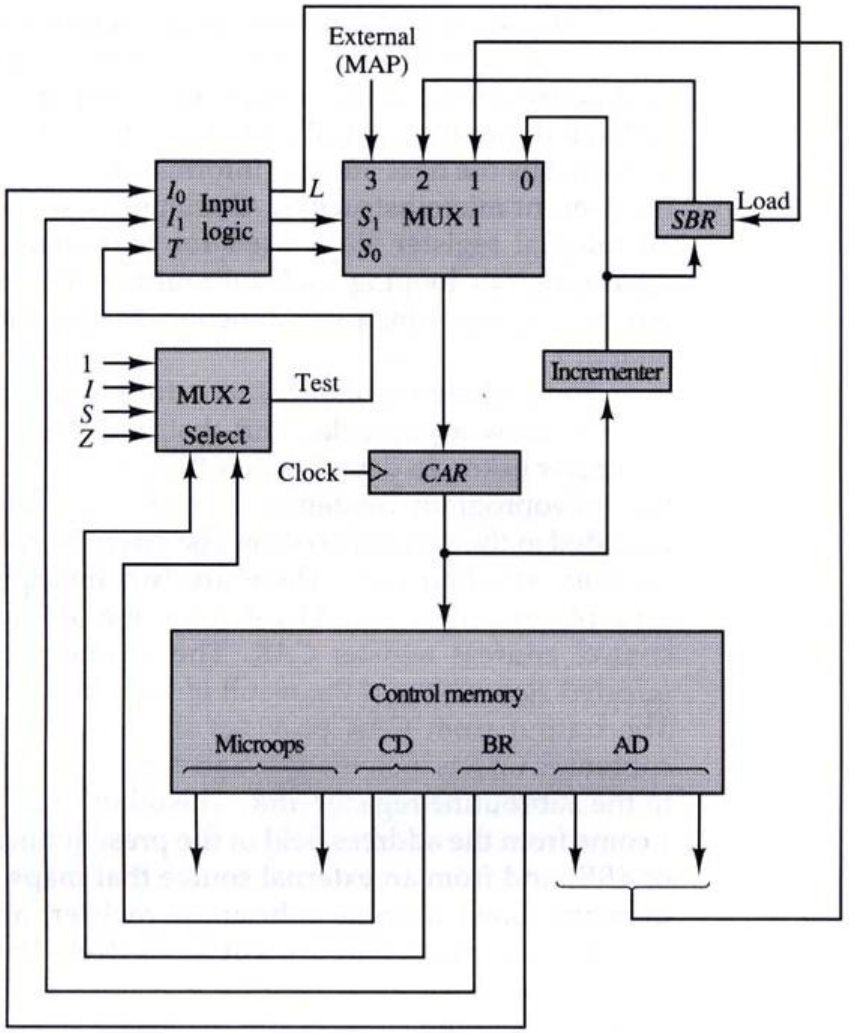

Figure 7-8 Microprogram sequencer for a control memory.

7.4 Design of control unit

- Arithmetic logic shift unit (same as in Figs. 5-19, 5-20)
- Micro-program sequencer

TABLE 7-4 Input Logic Truth Table for Microprogram Sequencer

BR Field	Input			MUX 1		Load *SBR*
	I_1	I_0	T	S_1	S_0	L
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	1	0	1	0	0	0
0	1	0	1	0	1	1
1	0	1	0	1	0	0
1	1	1	1	1	1	0

$$S_1 = I_1$$
$$S_0 = I_1 I_0 + I_1' T$$
$$L = I_1' I_0 T$$

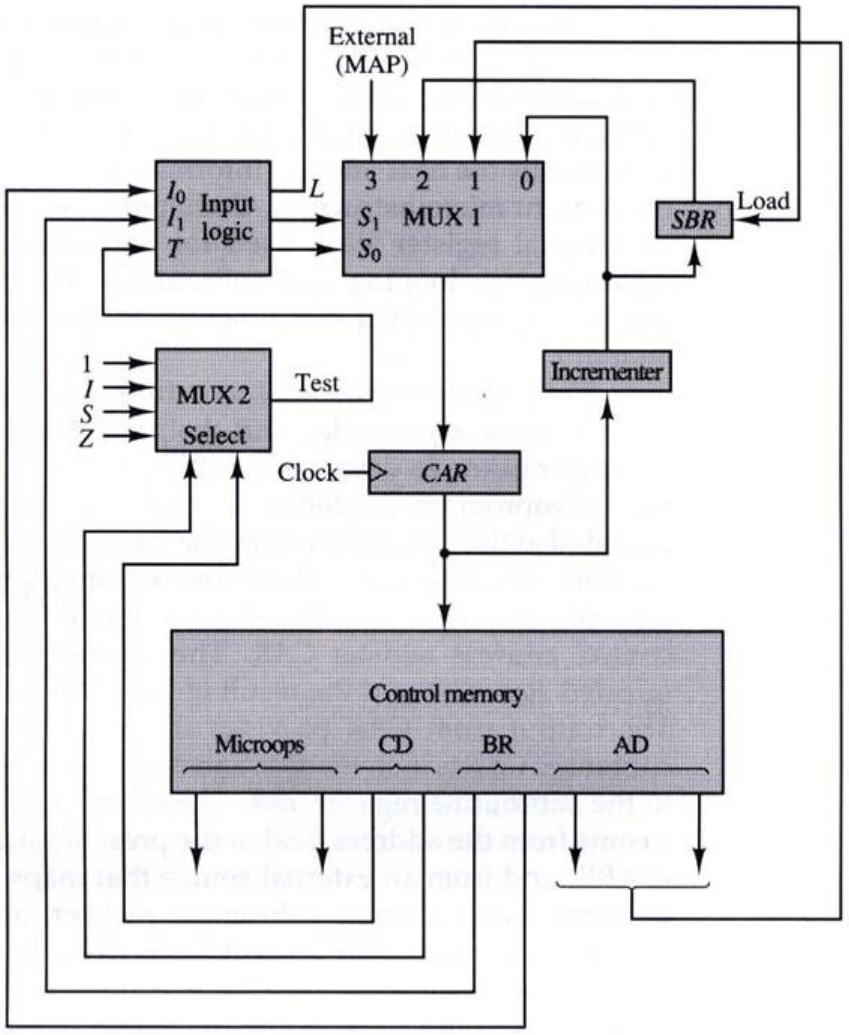

Figure 7-8 Microprogram sequencer for a control memory.

Problems

- 7-5, 7-6, 7-7, 7-11, 7-12, 7-13,
- 7-14, 7-15, 7-16, 7-19, 7-22