2019년 2학기

컴퓨터 구조 팀 프로젝트

|  |  |
| --- | --- |
| 제출일 | 2019년 12월 13일 |
| 담당교수 | 김우일 |
| 대표자  팀 원 | 김국현 201501411  홍승현 201601639  김대성 201801527  김민규 201702986 |

INDEX

**Introducing Main Circuit3**

Main circuit3

Bus system & Board3

Timing signal & Decode connection4

Timing Signal Logic gate4

Decode & Bus Calculate Logic gate4

**About Register, Adder & Logic5**

Address Register(AR)5

Program Counter(PC)5

Data Register(DR)6

Adder & Logic(A&L)6

1bit circuit6

8bit circuit7

Accumulator(AC)8

Instruction Register(IR)8

**Simulation9**

Micro operations9

Common bus select & Additional Information10

Fetch & Decode13

ADD17

AND20

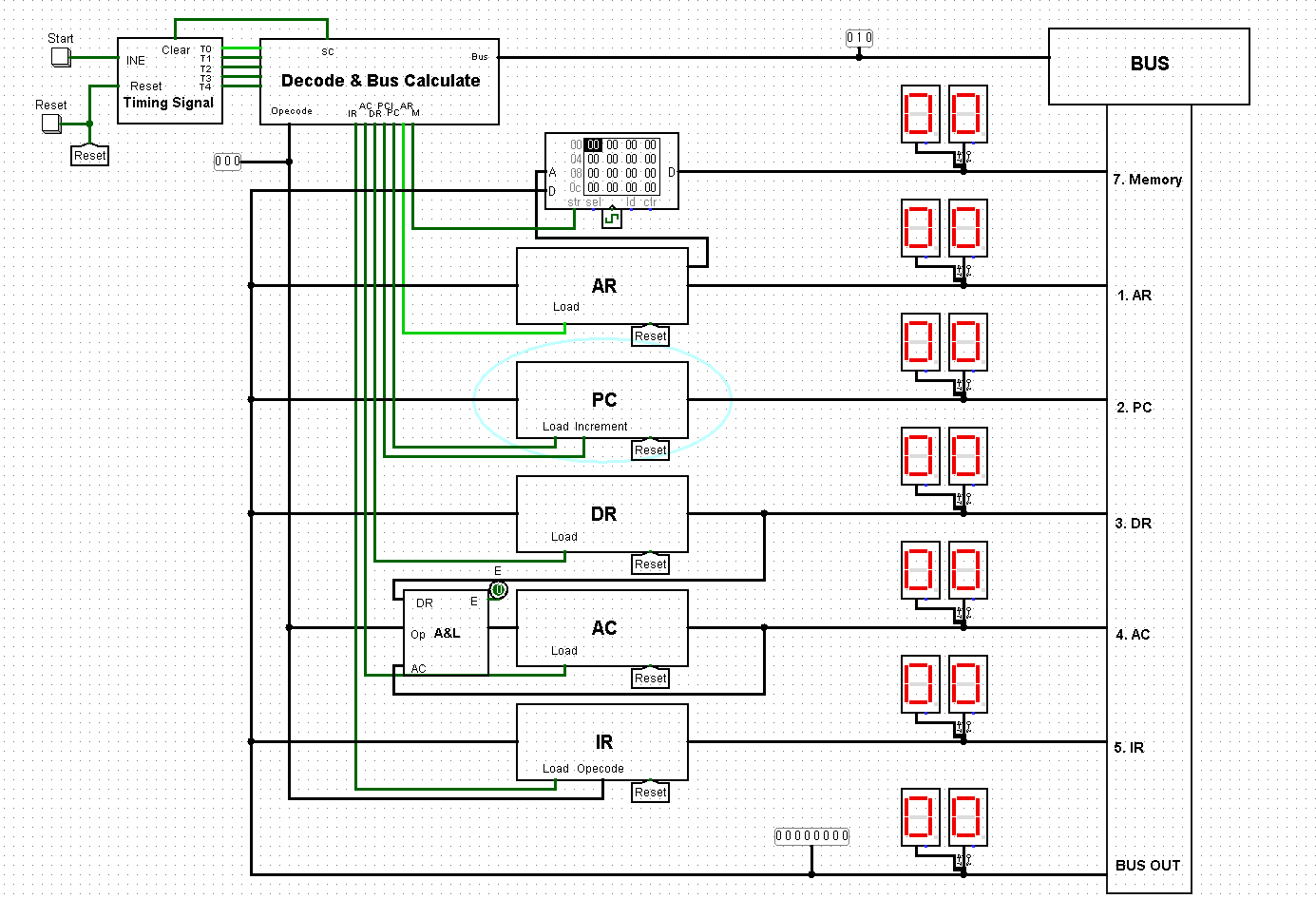
LDA23

STA26

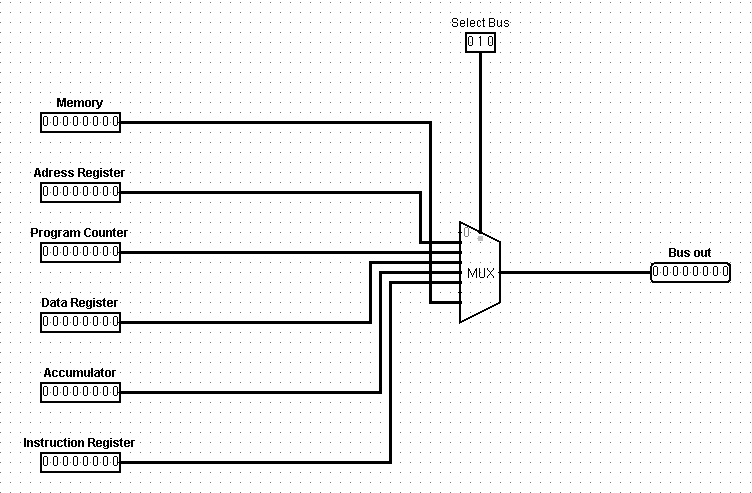
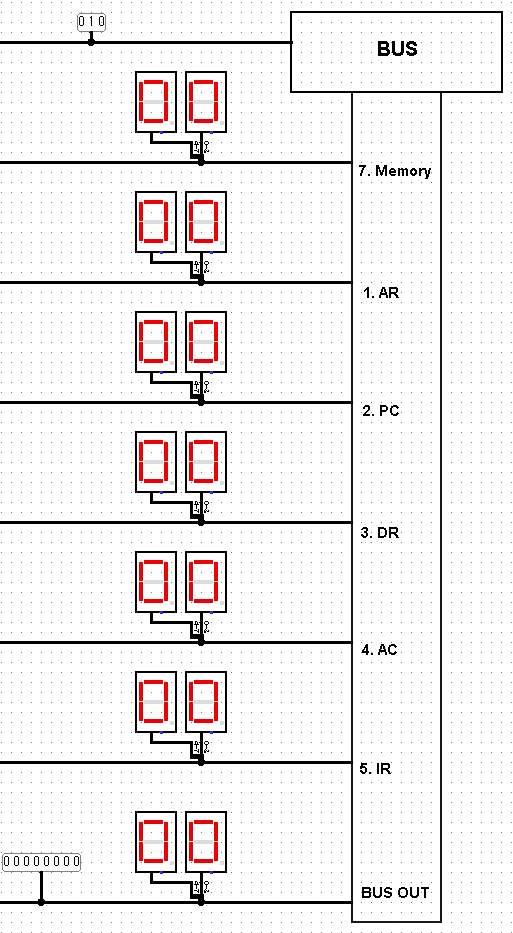
BUN28

**Introducing main circuit**

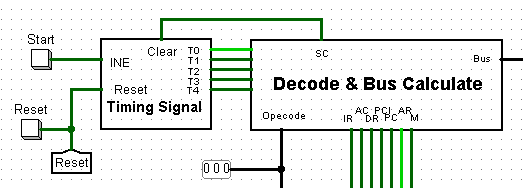
Main Circuit



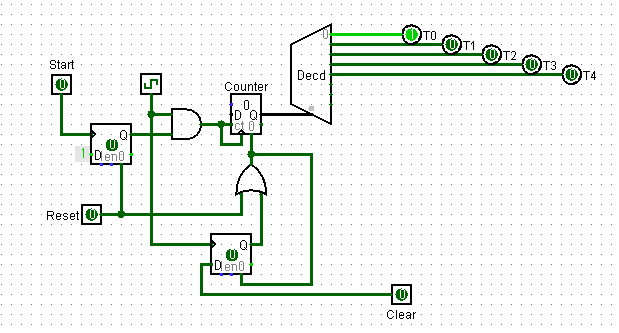
Bus system & Board



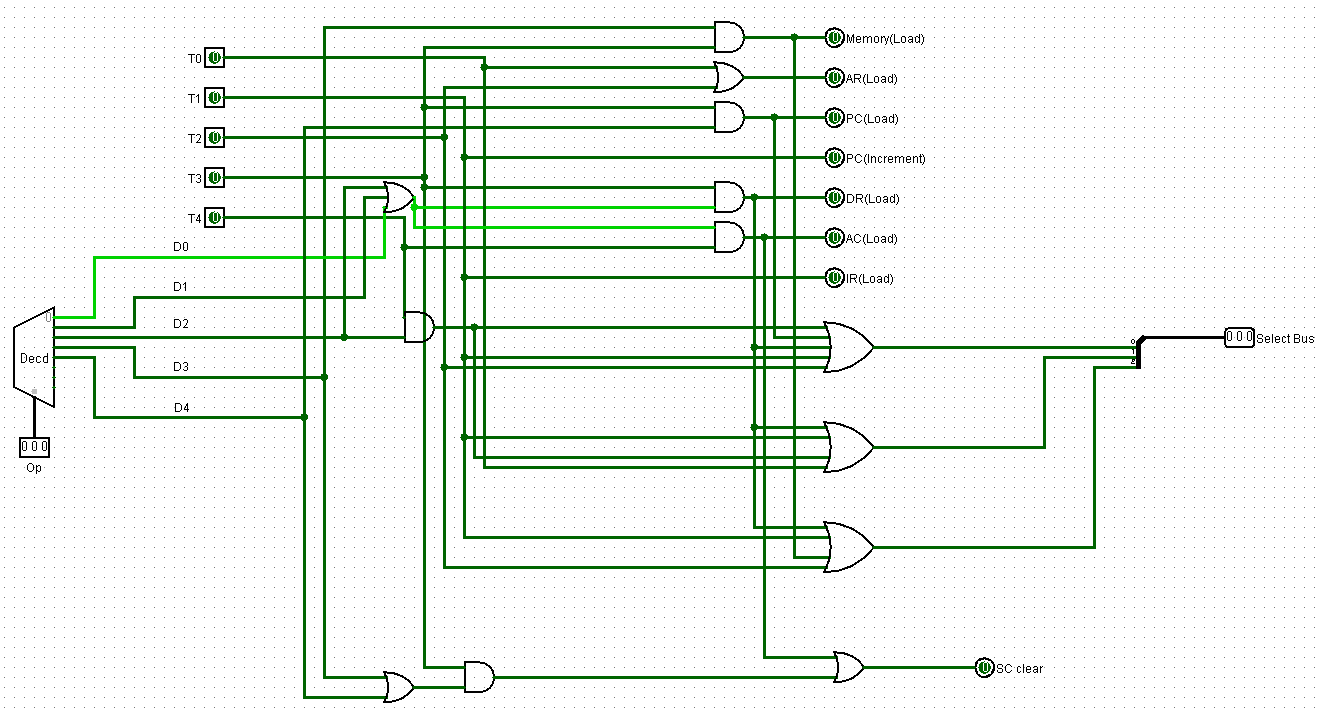
Timing signal & Decode connection



- Timing Signal Logic gate

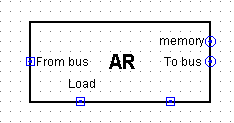
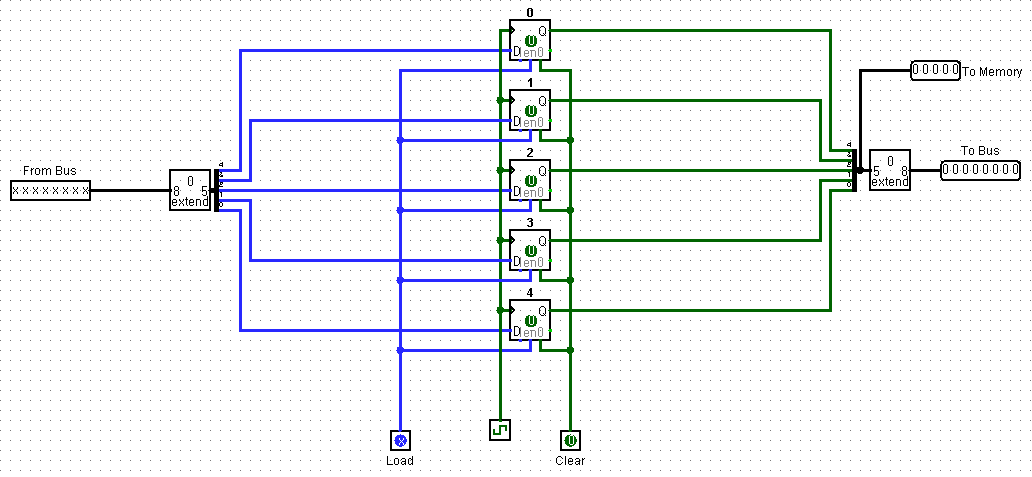


- Decode & Bus Calculate Logic gate

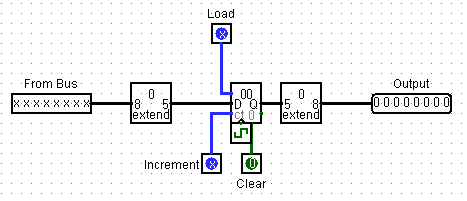


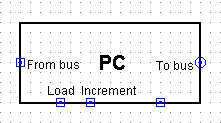
**About** **Register, Adder & Logic**

Address Register(AR)

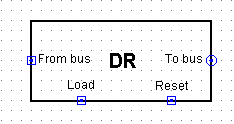
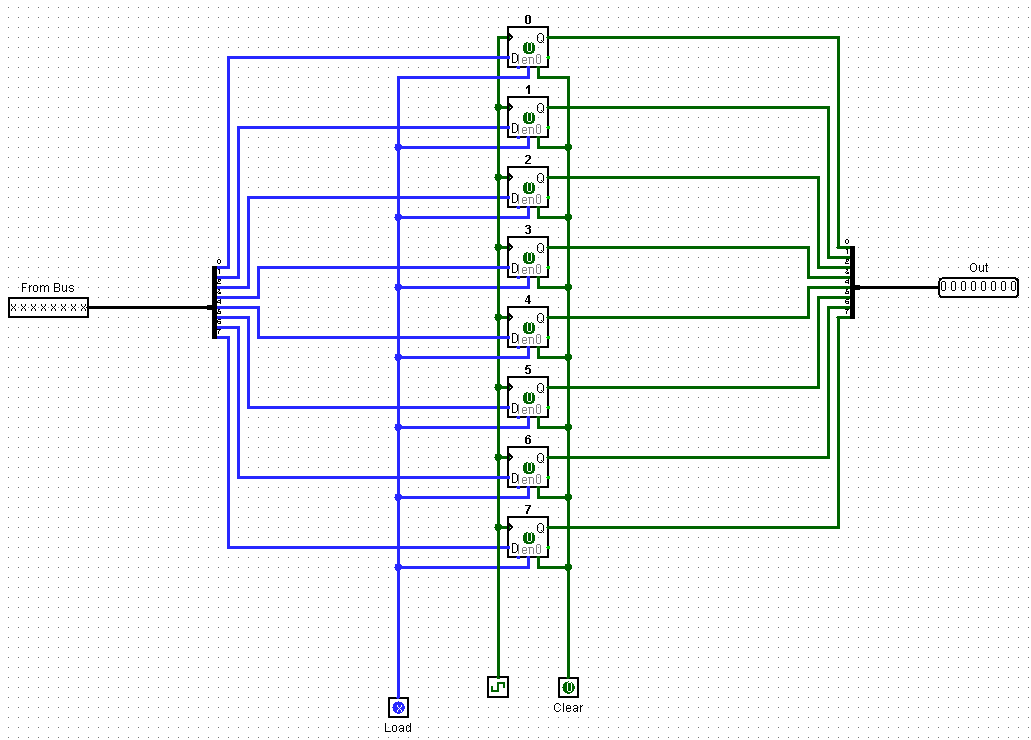


Program Counter(PC)

’

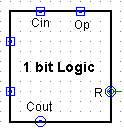
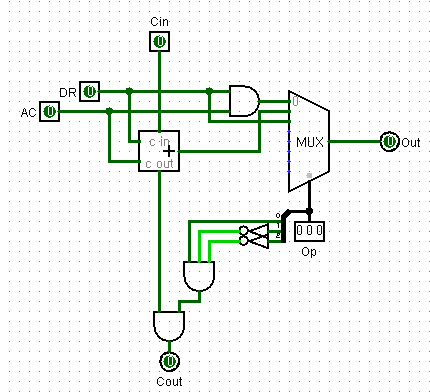


Data Register(DR)

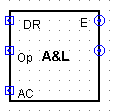
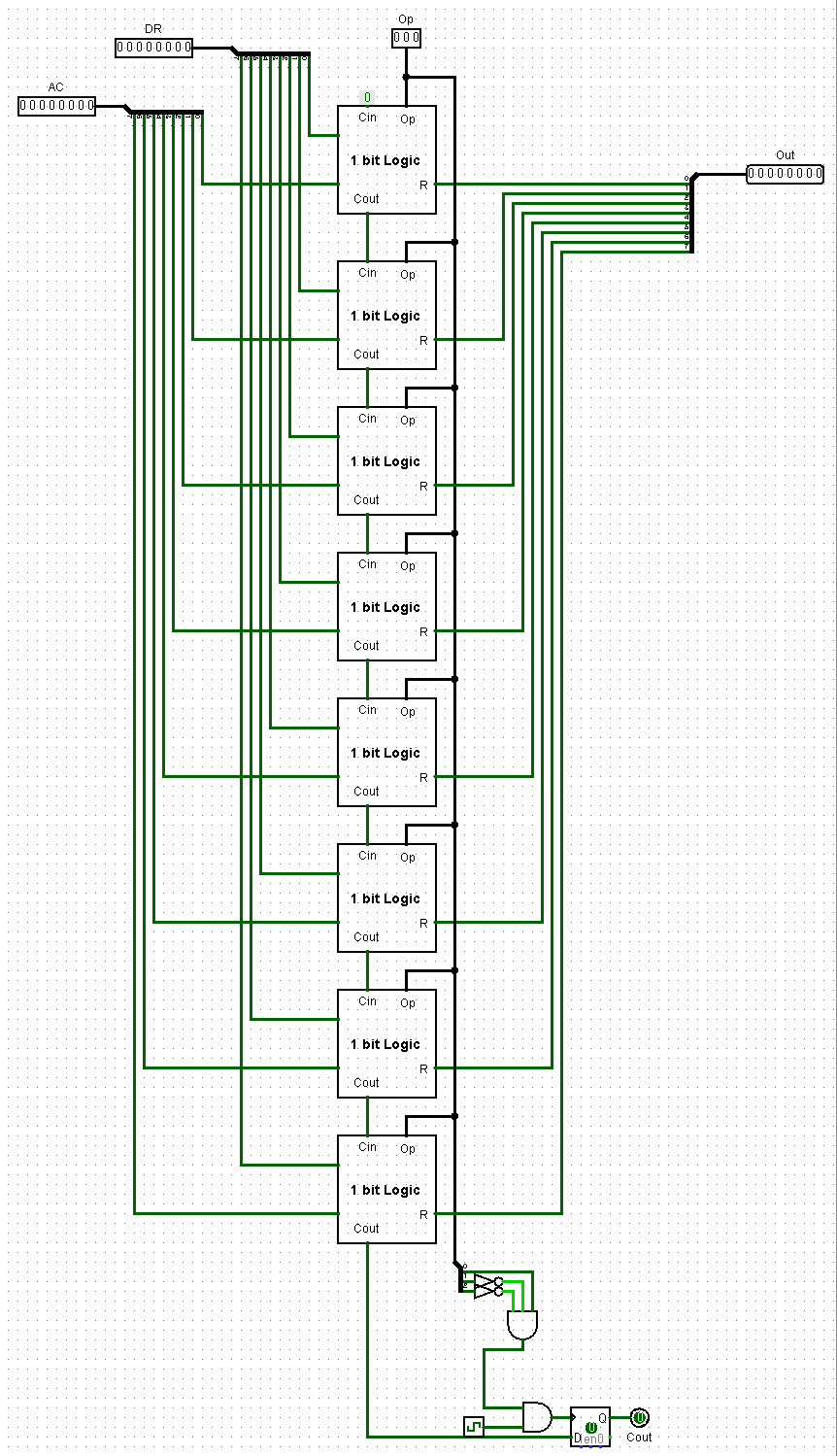


Adder & Logic(A&L)

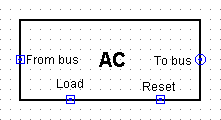
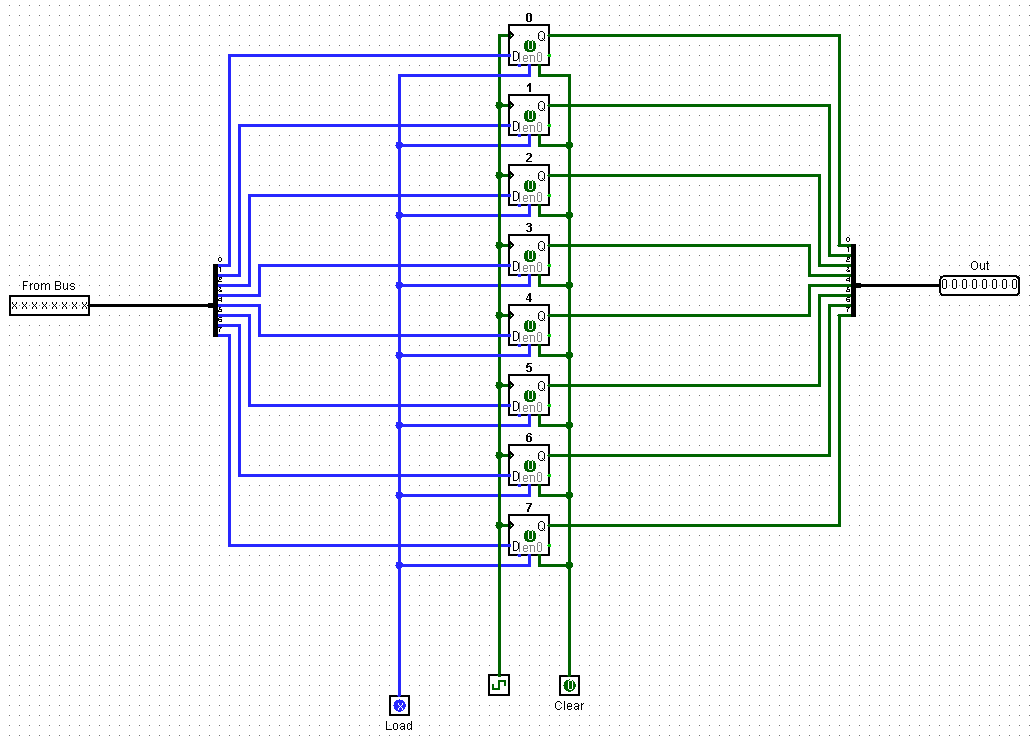
- 1bit logic



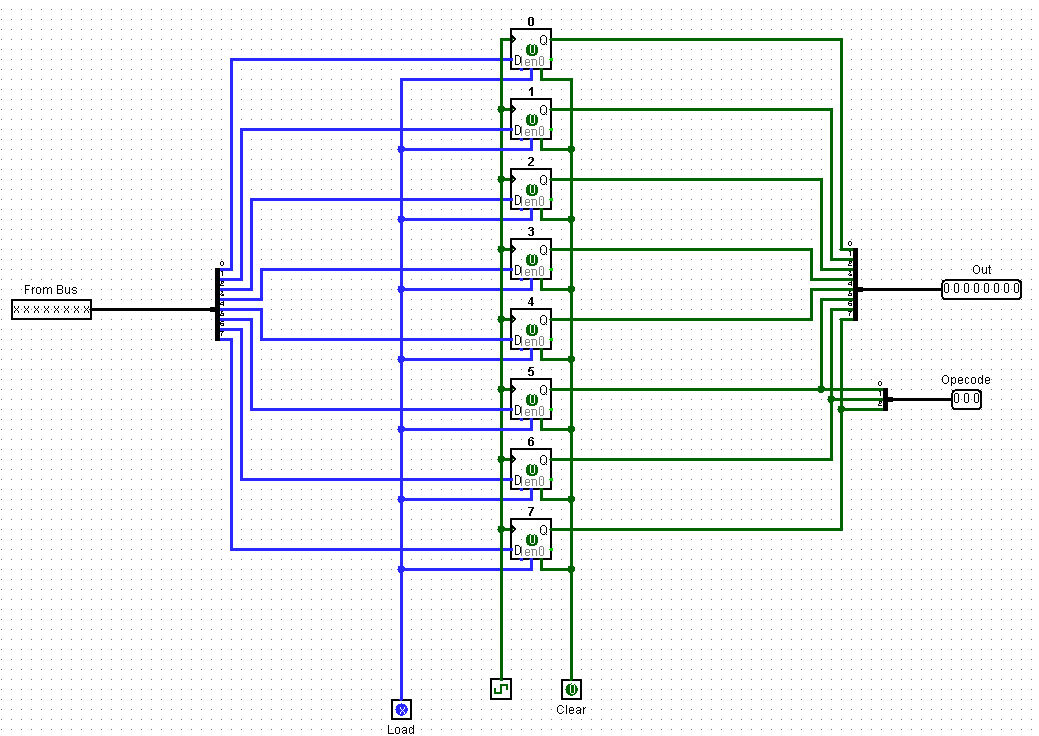
- 8bit logic

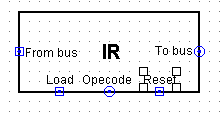


Accumulator(AC)



Instruction Register(IR)





**About Action**

**Micro operations**

|  |  |
| --- | --- |
| Fetch & Decode | |
| Fetch | T0:AR ← PC  T1: IR ← M[AR], PC ← PC + 1 |
| Decode | T2 : D0 …. D7 ← Decode IR(5~7), AR ← IR(0~4) |

|  |  |
| --- | --- |
| 메모리 참조(직접주소) | |
| AND | D0T3 : DR ← M[AR]  D0T4 : AC ←AC∧DR, SC ← 0 |
| ADD | D1T3 : DR ← M[AR]  D1T4 : AC ← AC + DR, E ← Cout, SC ← 0 |
| LDA | D2T3 : DR ← M[AR]  D2T4 : AC ← DR, SC ← 0 |
| STA | D3T3 : M[AR] ← AC, SC ← 0 |
| BUN | D4T3 : PC ← AR, SC ← 0 |

**Common bus Select**

|  |  |
| --- | --- |
| 공통 버스 선택 입력 /x0 = NONE/, /x1 = AR/, /x2 = PC//x3 = DR/, /x4 = AC/, /x5 = IR/ /x6 = NONE/, /x7 = Memory/ | |
| S0 | x1 + x3 + x5 + x7  = T2 + D2T4 + T1 + T3(D0 + D1 + D2) + D4T3 |
| S1 | x2 + x3 + x7  = T0 + D2T4 + T1 + T3(D0 + D1 + D2) |
| S2 | x4 + x5 + x7  T2 + T1+ T3(D0 + D1 + D2) + D3T3 |
| x0 | NULL |
| x1(AR) | D4T3 |
| x2(PC) | T0(Fetch) |
| x3(DR) | D2T4 |
| x4(AC) | D3T3 |
| x5(IR) | T2(Decode) |
| x6 | NULL |
| x7(M) | T1 + T3(D0 + D1 + D2) |

**Operation between registers**

|  |  |  |
| --- | --- | --- |
| 레지스터 간 신호 연산 | | |
| AR | Load | T0 + T2 |
| INR | NULL |
| Clear | 구현 |
| PC | Load | D4T3 |
| INR | T1 |
| Clear | 구현 |
| DR | Load | T3(D0 + D1 + D2) |
| INR | NULL |
| Clear | 구현 |
| AC | Load | T4(D0 + D1 + D2) |
| INR | NULL |
| Clear | 구현 |
| IR | Load | T1 |
| INR | NULL |
| Clear | 구현 |
| Memory | Load | D3T3 |
| INR | NULL |
| Clear | 구현 |

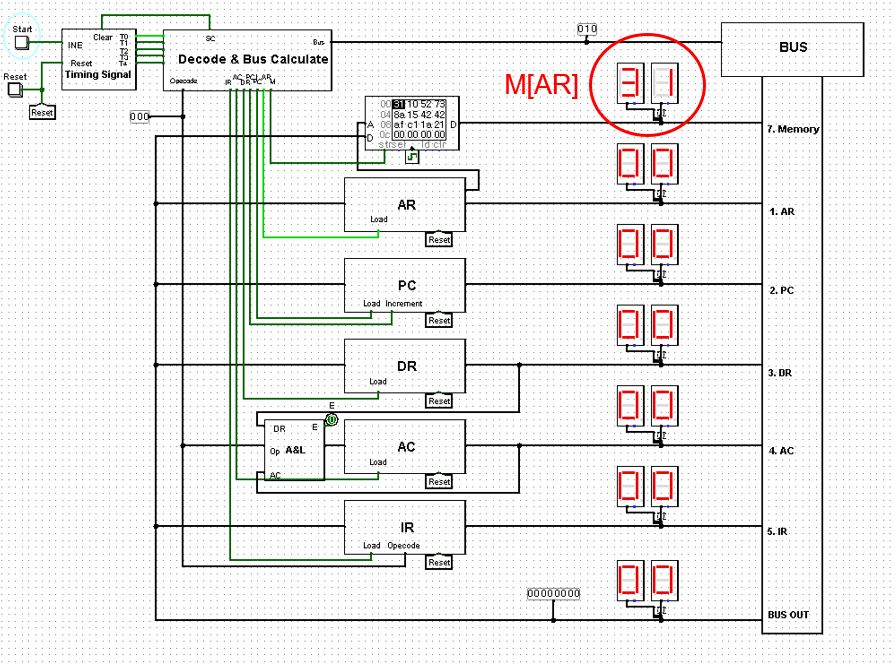
**Fetch Decoder & System Counter & Timing Decoder**

|  |  |  |
| --- | --- | --- |
| Fetch Decoder & System Counter & Timing DecoderM[AR]에 따른 명령어 유형 | | |
| AND | 000 00000  ~  000 11111 | 0~1f |
| ADD | 001 00000  ~  001 11111 | 20~3f |
| LDA | 010 00000  ~  010 11111 | 40~5f |
| STA | 011 00000  ~  011 11111 | 60~7f |
| BUN | 100 00000  ~  100 11111 | 80~9f |

Fetch & Decode

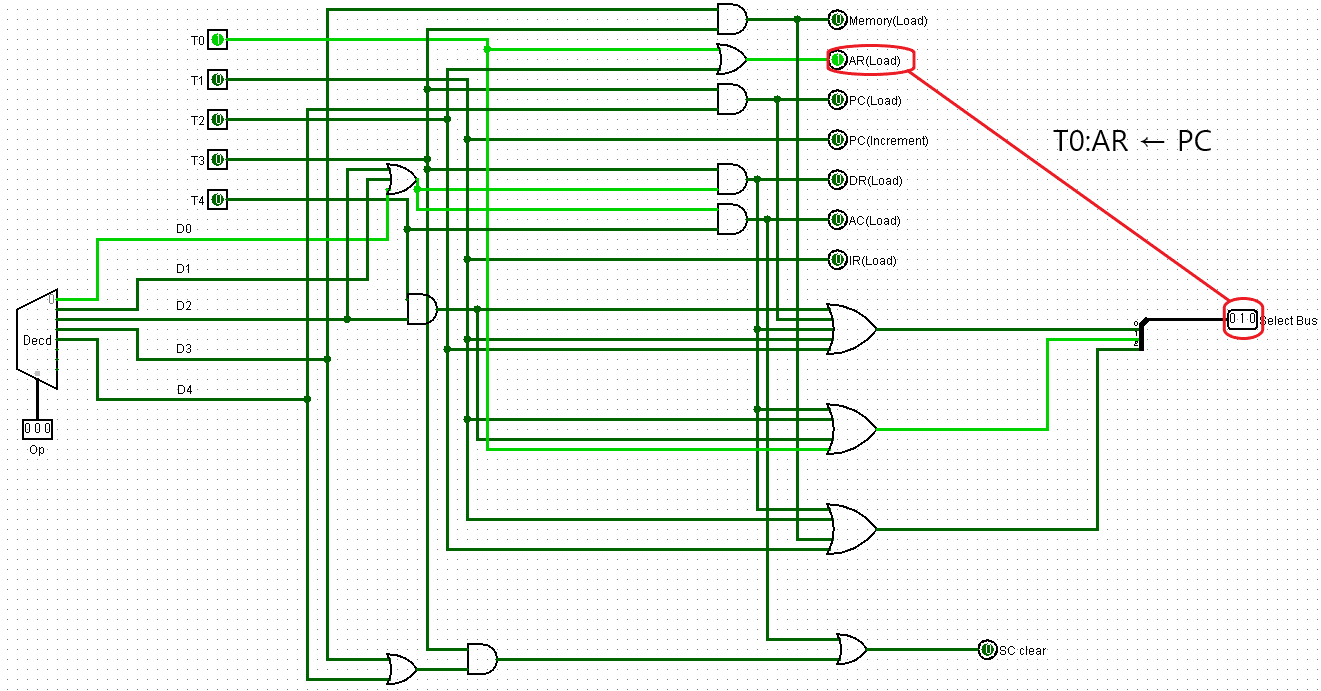
The value of the memory was selected by Team2, built to work in ADD AND LDA STA BUN order

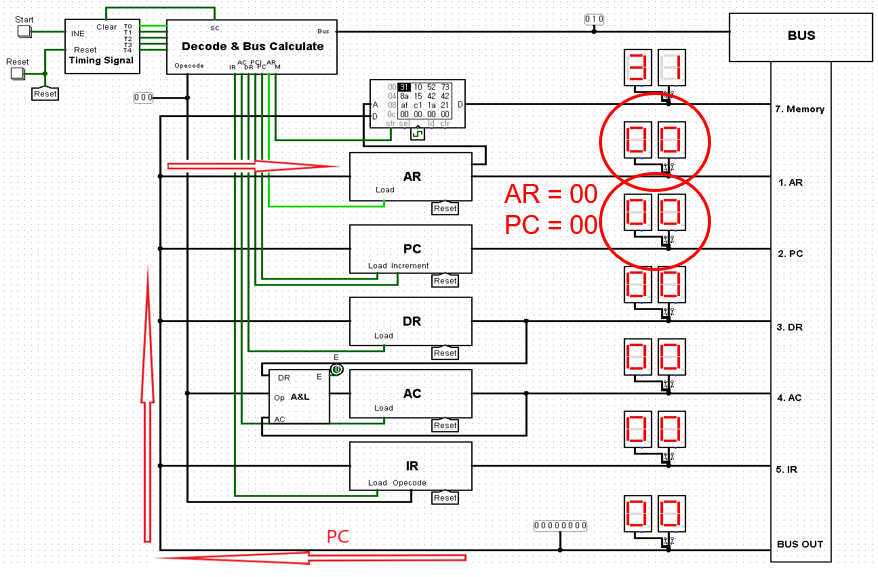
**Initial state**



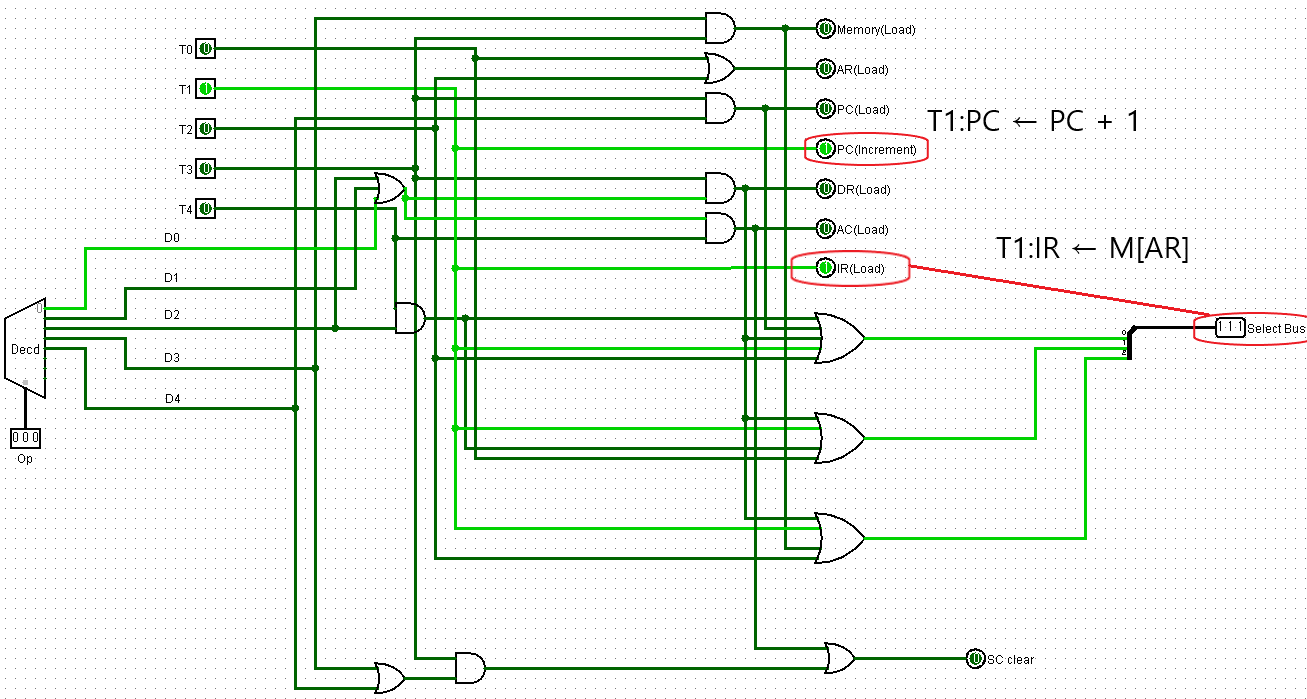
**Fetch**

**T0 : AR ← PC**





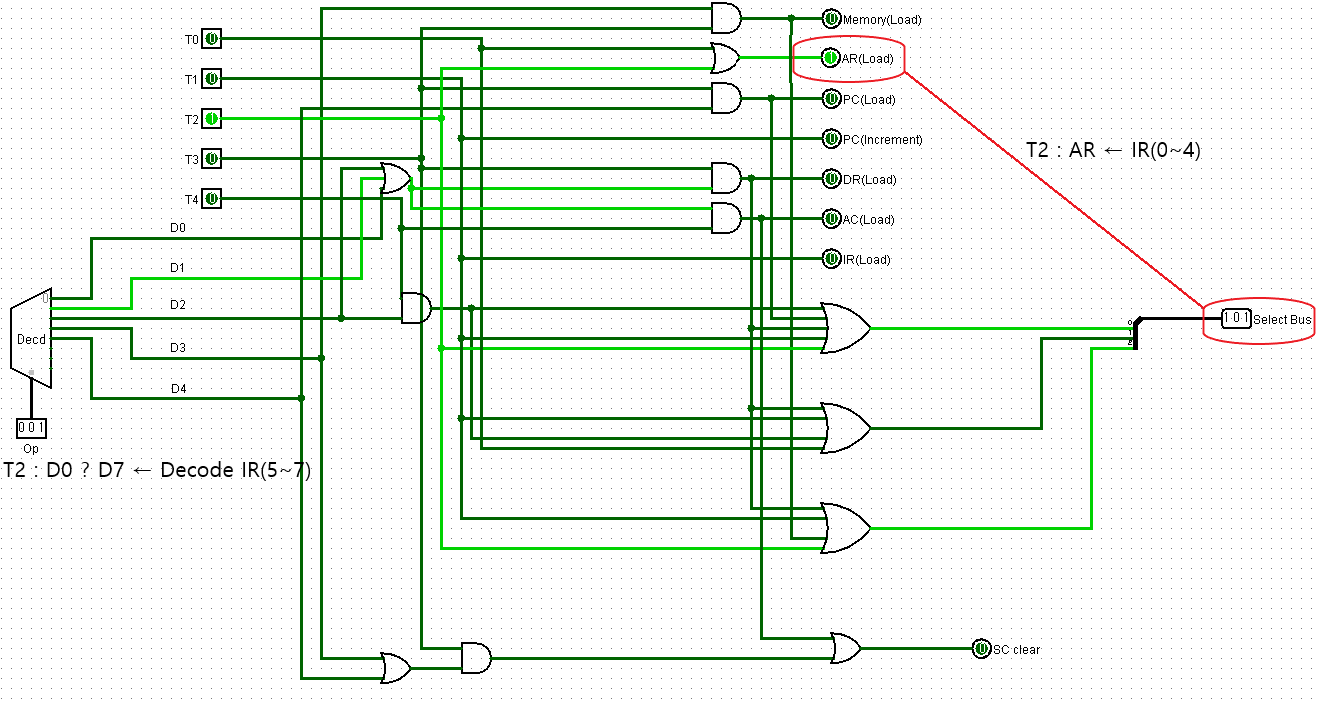
**T1: IR ← M[AR], PC ← PC + 1**

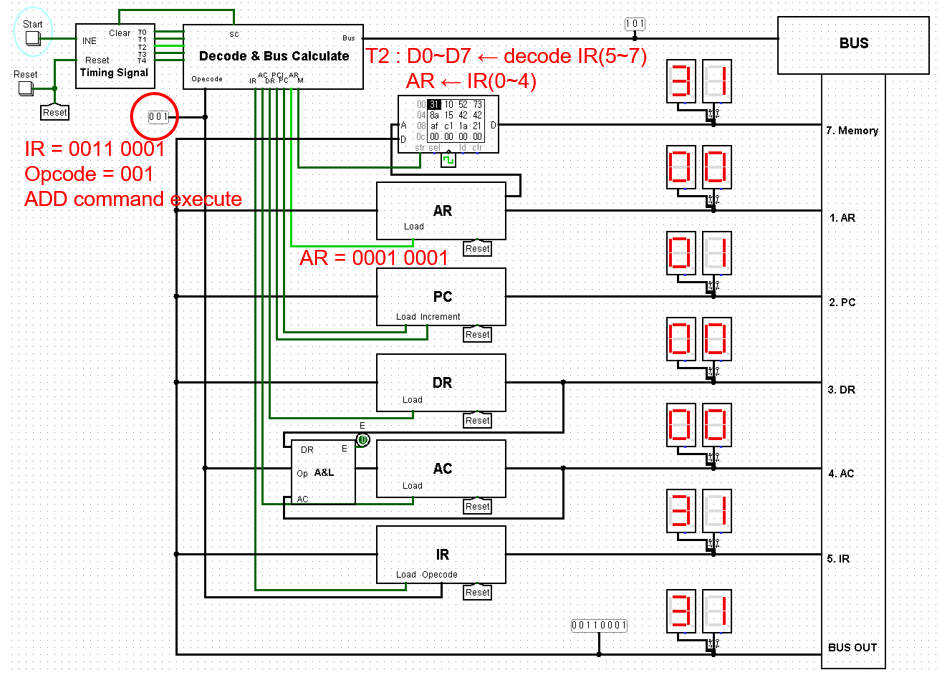


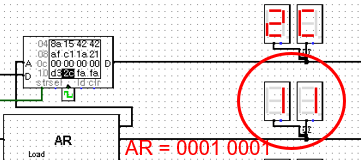


**Decode**

**T2 : D0 …. D7 ← Decode IR(5~7), AR ← IR(0~4)**

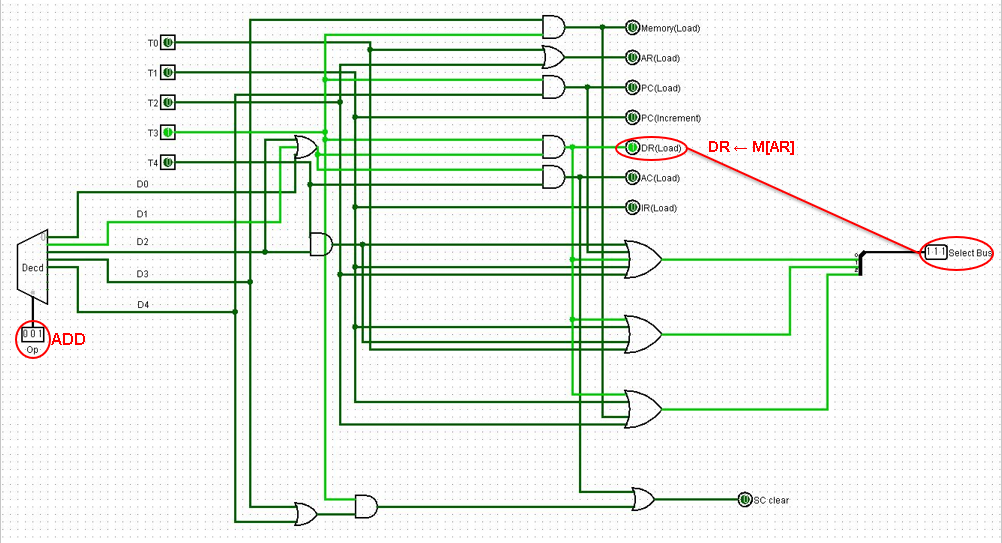


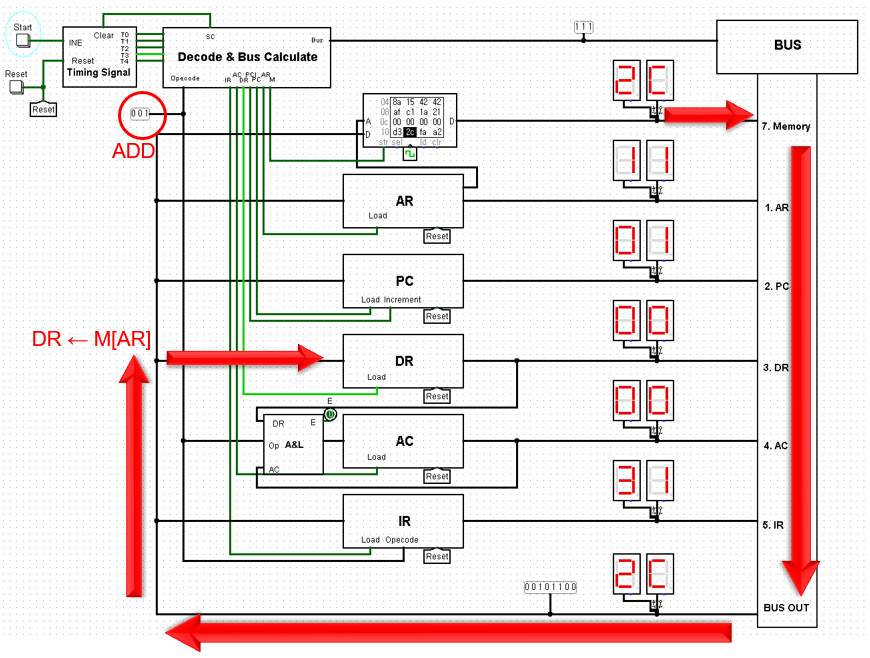


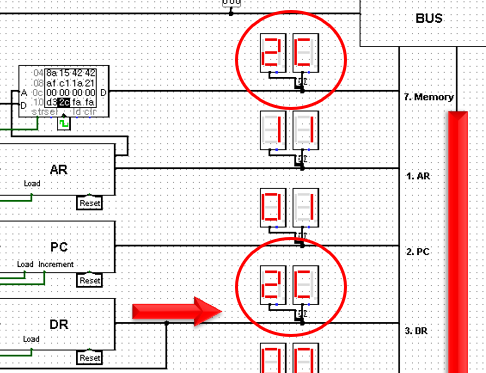


**ADD**

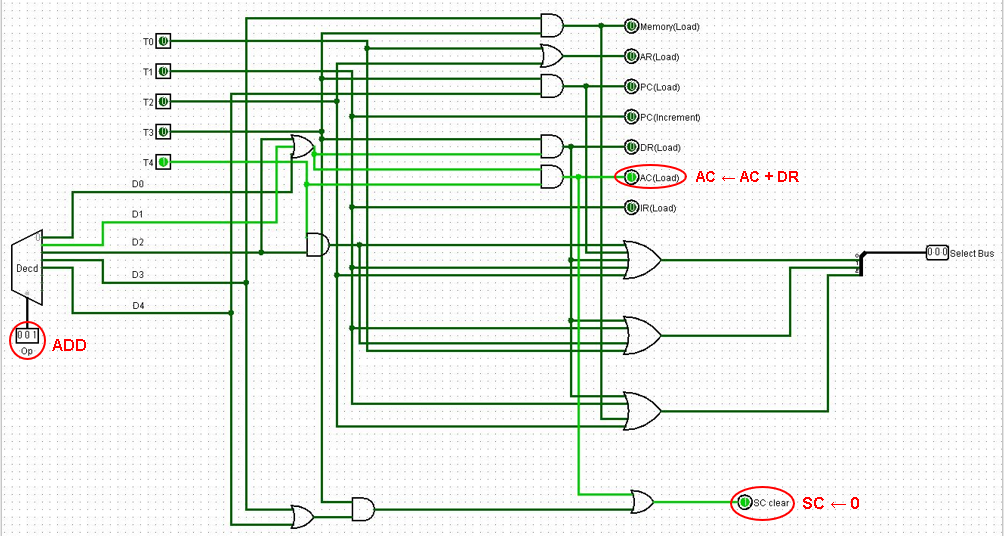
**D1T3 : DR ← M[AR]**

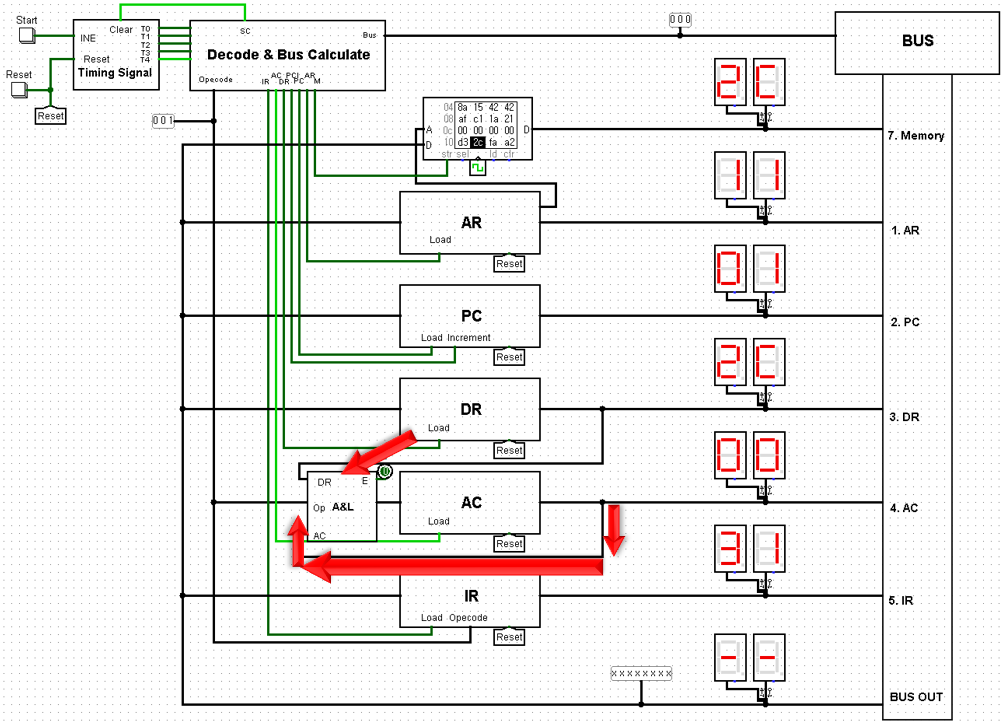


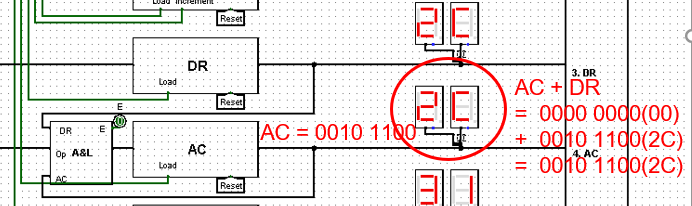




**D1T4 : AC ← AC + DR, E ← Cout, SC ← 0**

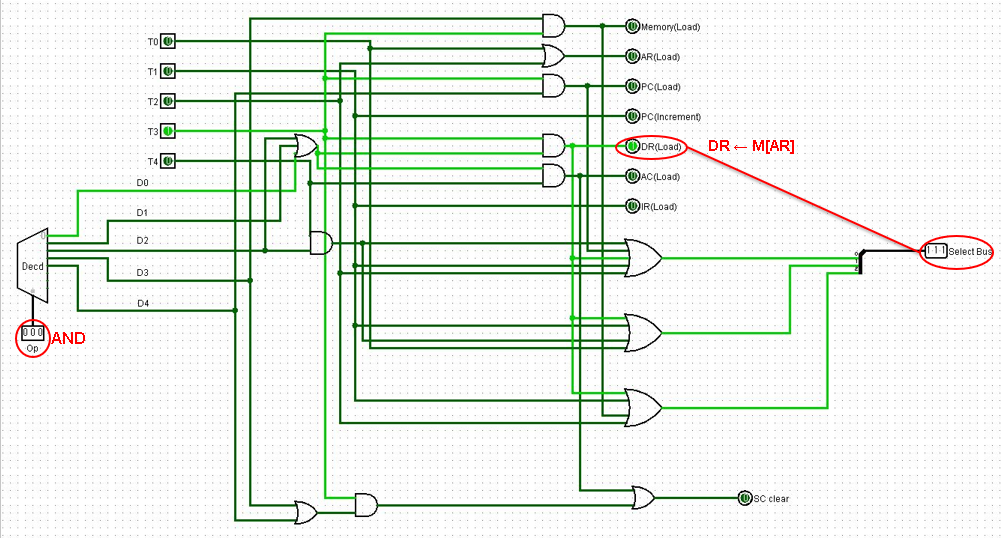


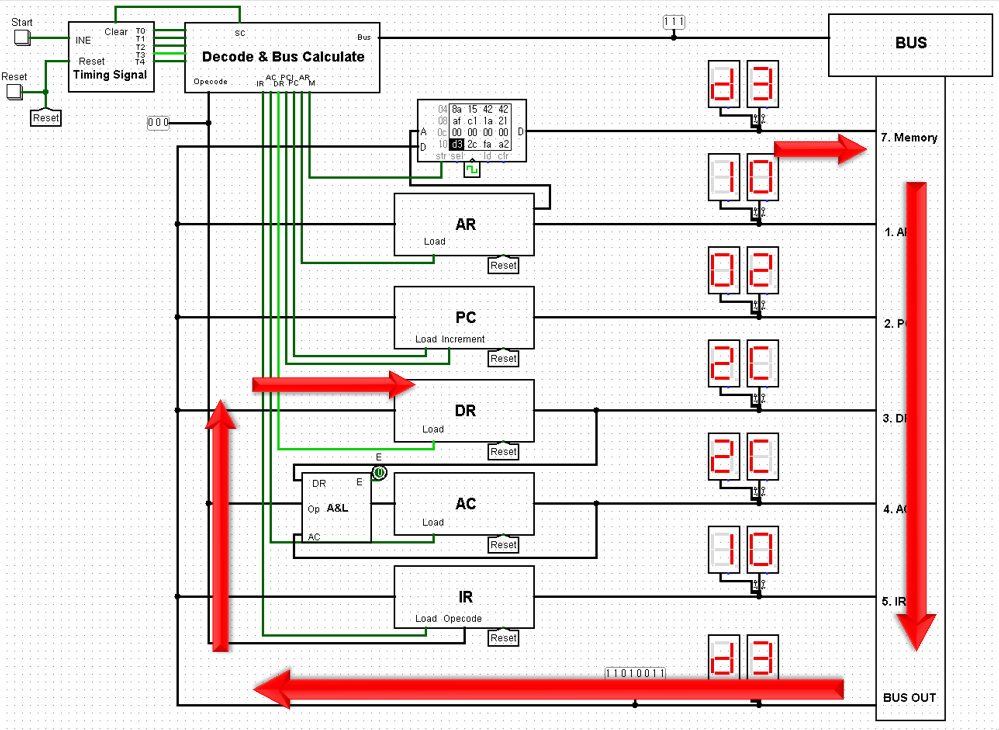


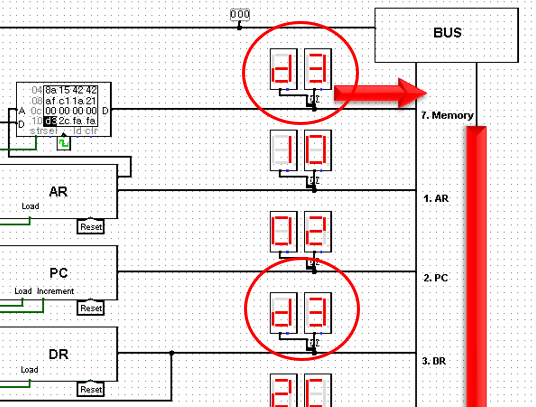


**AND**

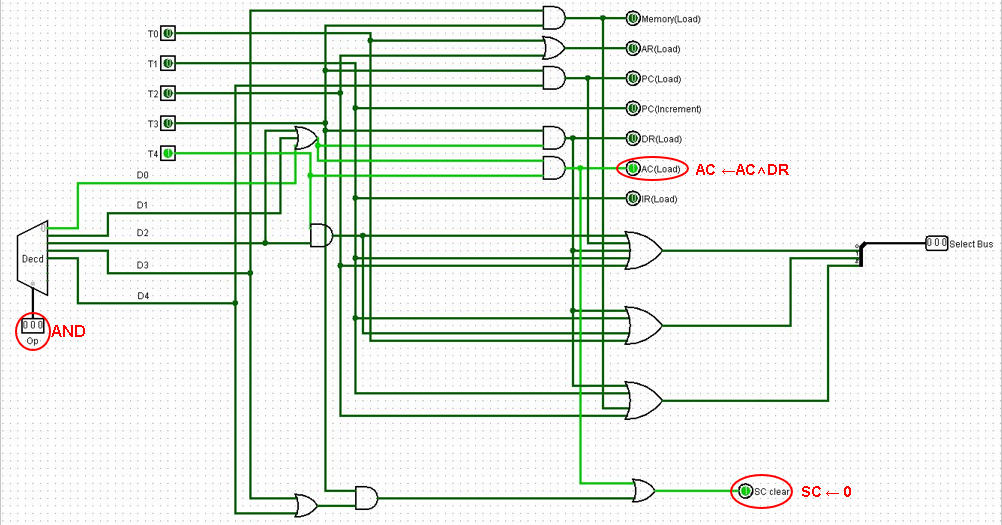
**D0T3 : DR ← M[AR]**

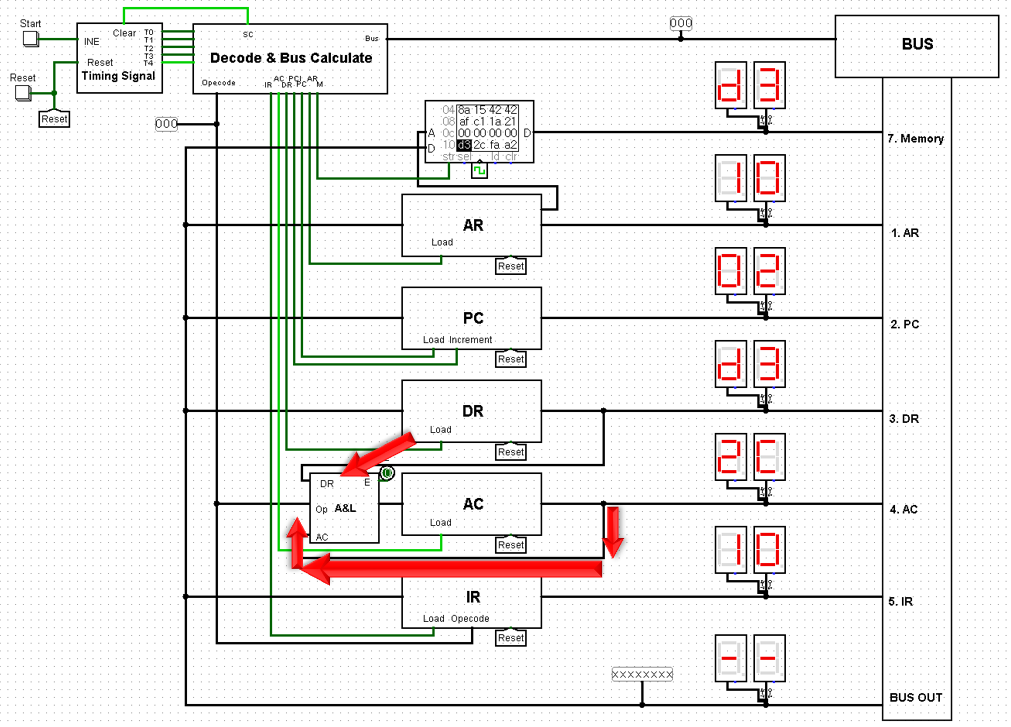


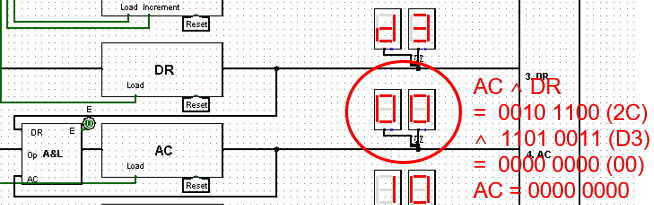




**D0T4 : AC ←AC∧DR, SC ← 0**

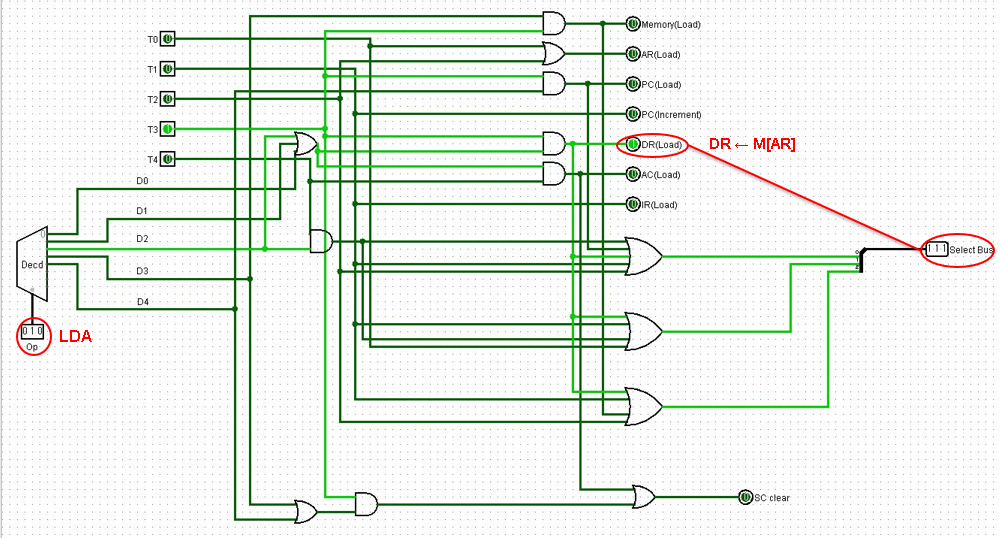


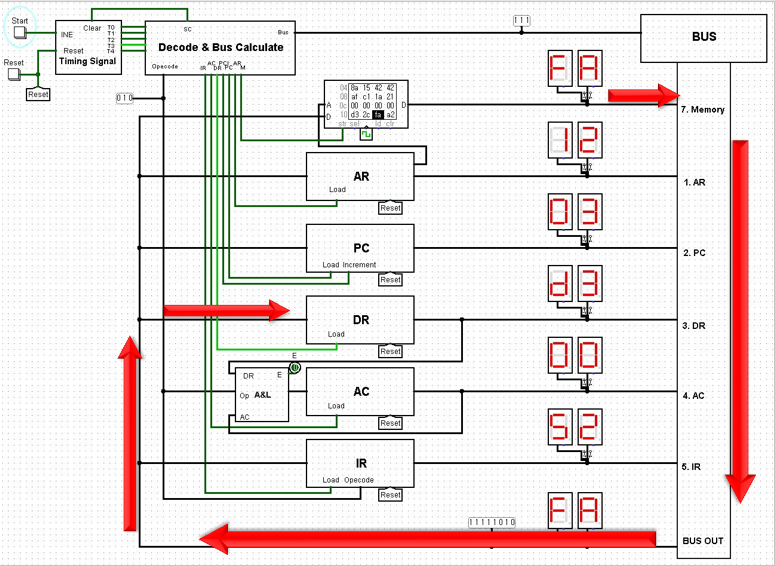


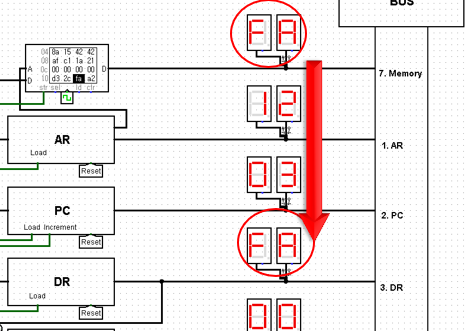


**LDA**

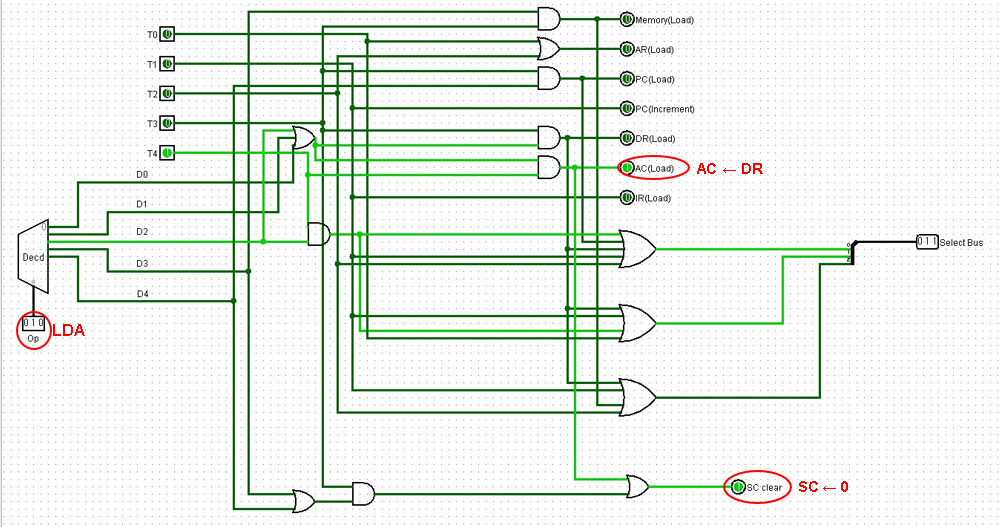
**D2T3 : DR ← M[AR]**

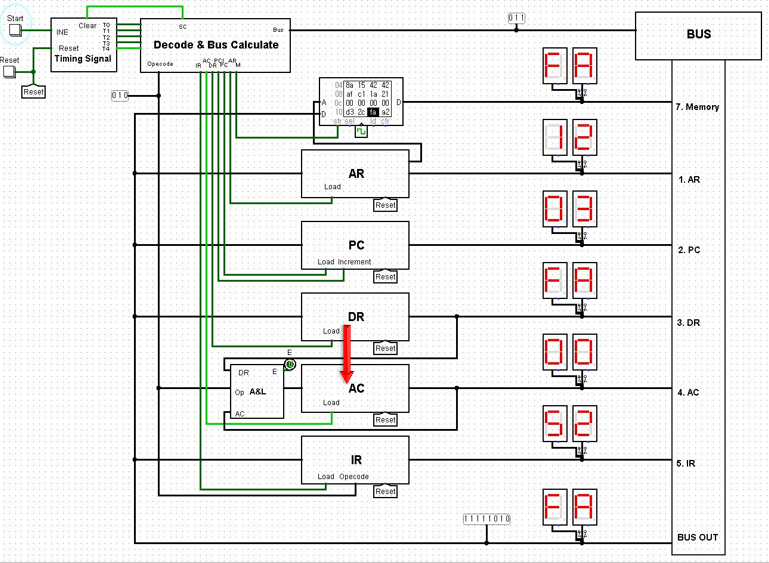


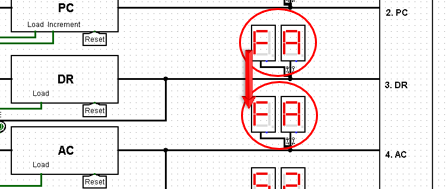




**D2T4 : AC ← DR, SC ← 0**

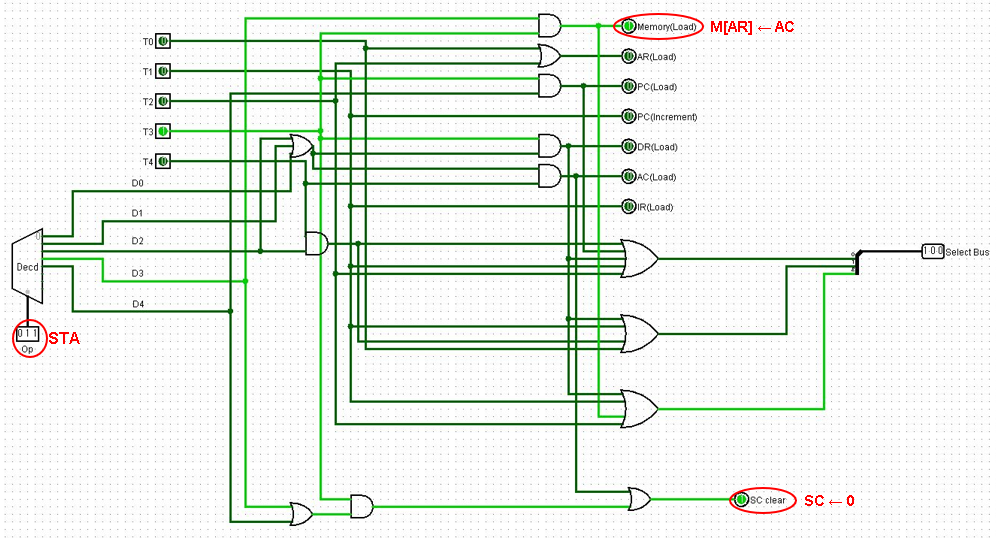


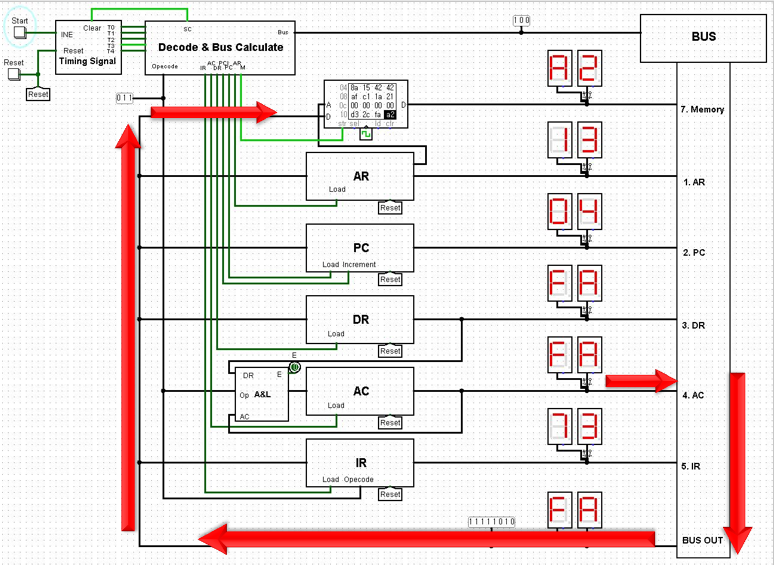


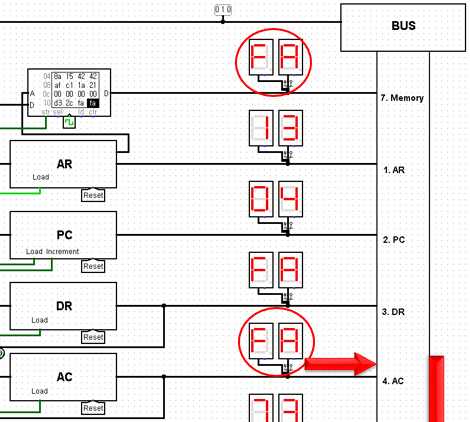


**STA**

**D3T3 : M[AR] ← AC, SC ← 0**







**BUN**

**D4T3 : PC ← AR, SC ← 0**

