INCHEON NATIONAL UNIVERSITY

IAA6007: Computer Architecture
Ch.2. Digital Components

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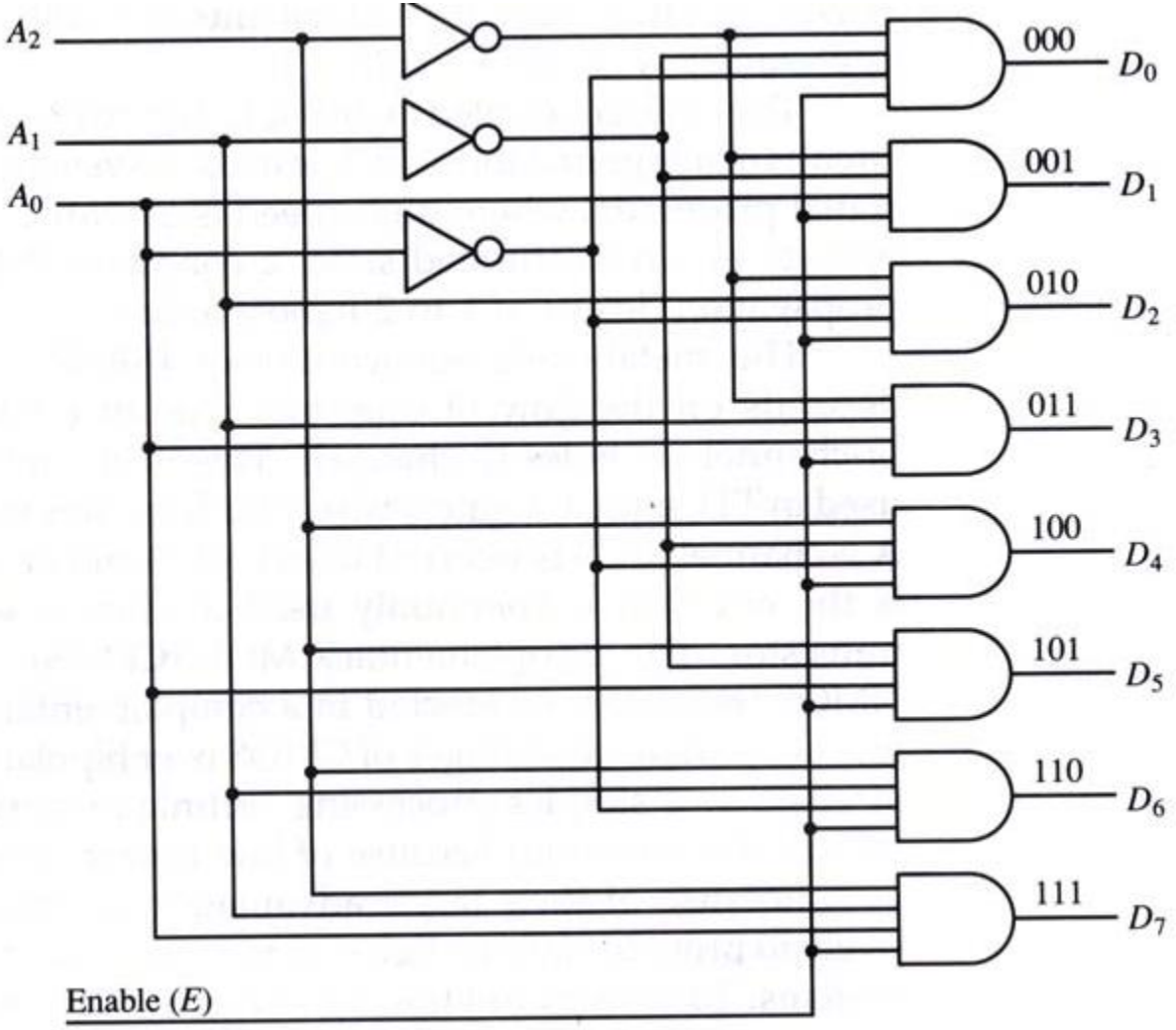
2-1. Integrated circuits

- Integrated circuits (IC)
  - SSI (Small Scale IC), MSI (Medium Scale IC), LSI (Large Scale IC), VLSI (Vey Large Scale IC)
- TTL (Transistor-Transistor Logic)
  - Standard, most widespread logic family
- ECL (Emitter-Coupled Logic)
  - High speech digital circuit
- MOS (Metal Oxide Semiconductor)
  - High component density
- CMOS (Complementary Metal Oxide Semiconductor)
  - Low power consumption

2-2. Decoders

- 3-to-8-line decoder



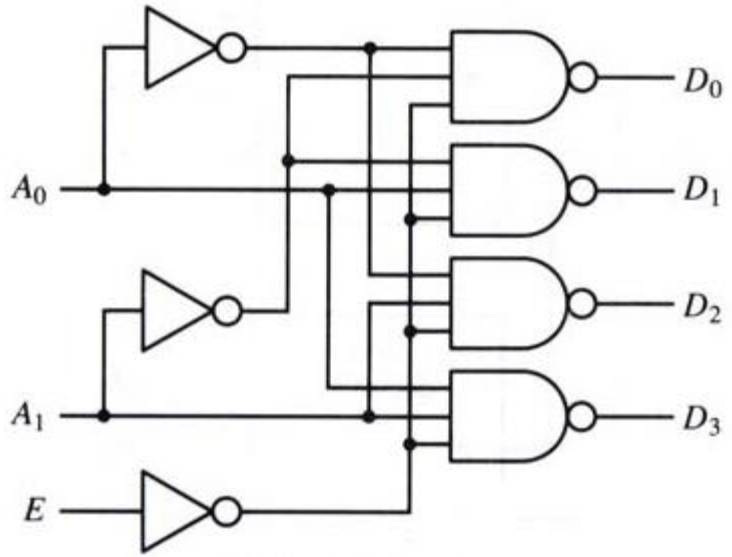
2-2. Decoders

- 3-to-8-line decoder

Enable	Inputs			Outputs							
E	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	×	×	×	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

2-2. Decoders

- NAND gate decoder
  - 2-to-4-line decoder



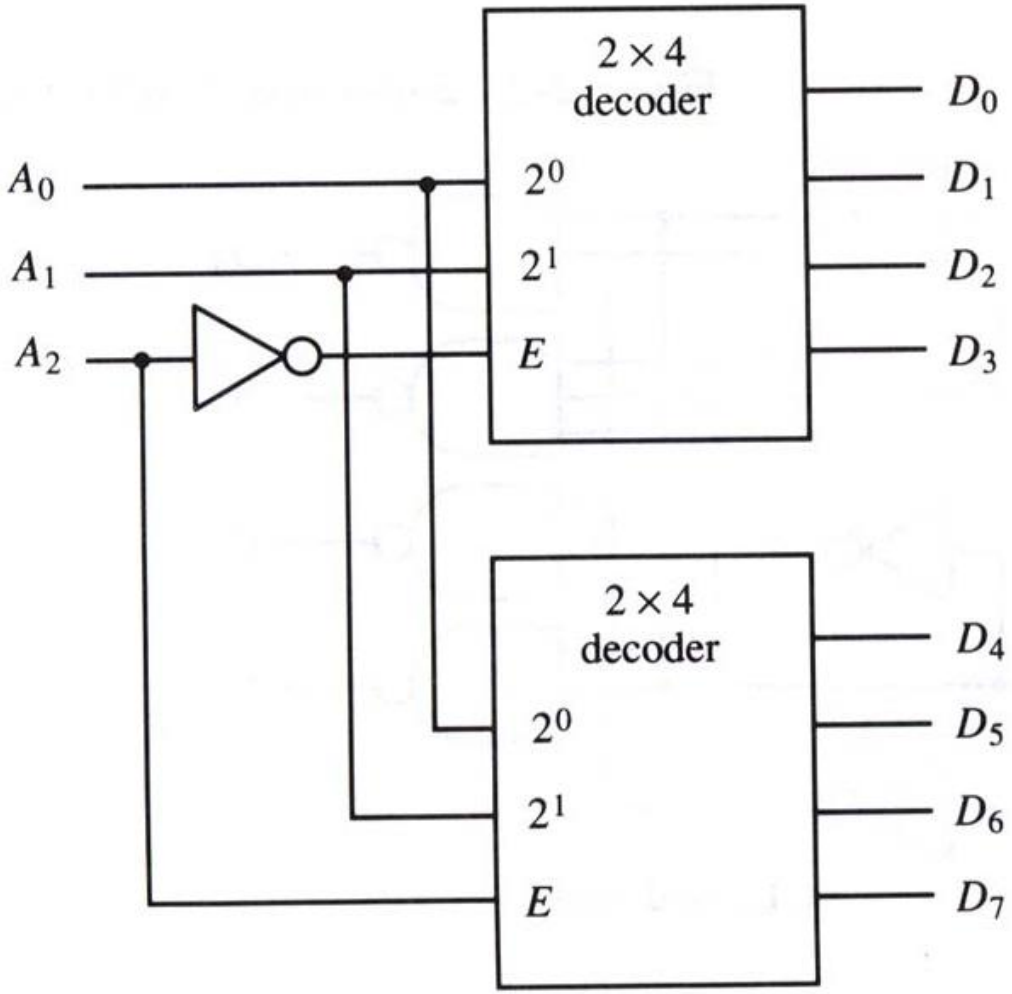
(a) Logic diagram

E	A_1	A_0	D_0	D_1	D_2	D_3
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	×	×	1	1	1	1

(b) Truth table

2-2. Decoders

- Decoder expansion



- 3x8 decoder constructed with two 2x4 decoders

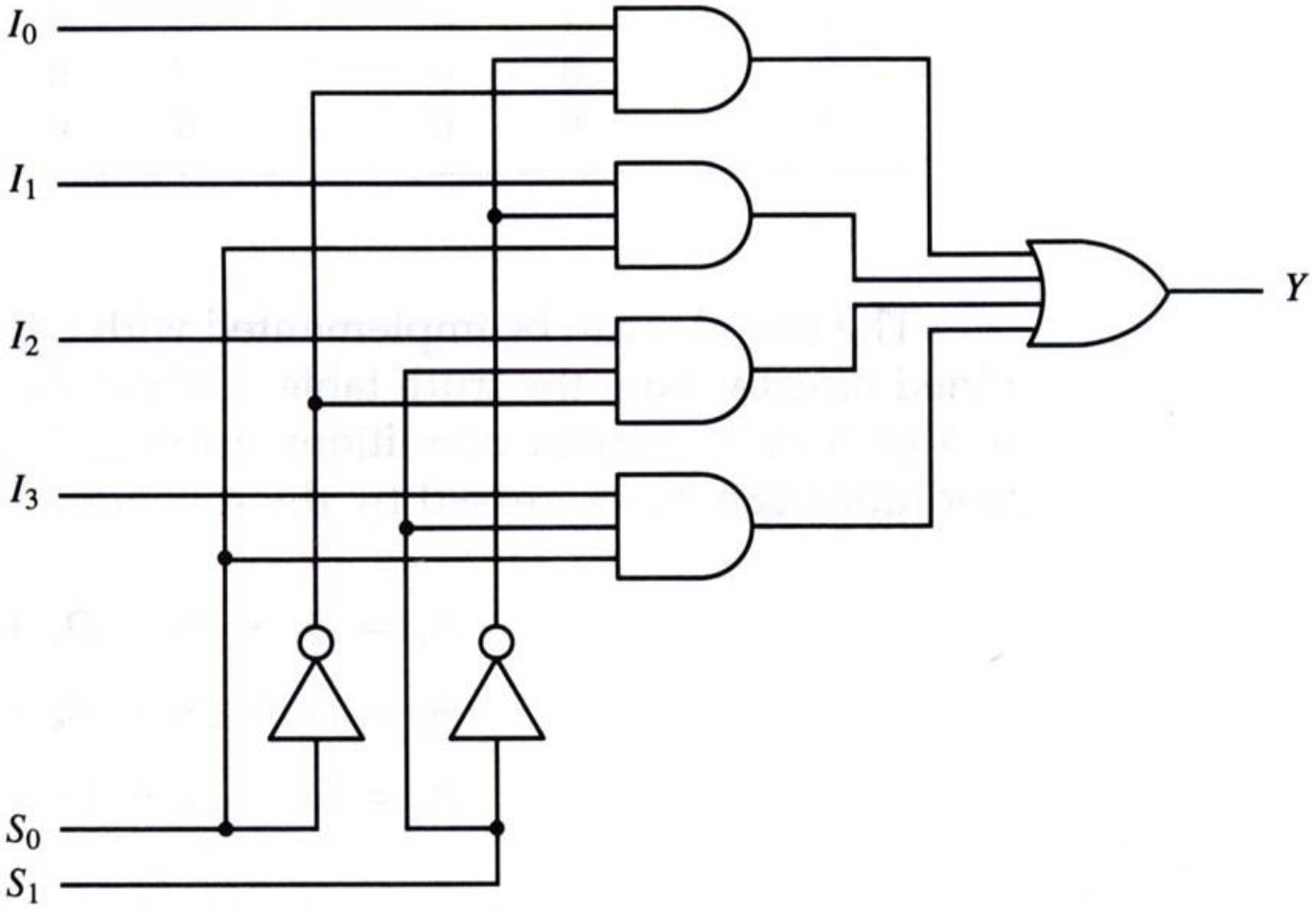
2-2. Decoders

- Encoders
  - Truth table for 8x3 encoder

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

2-3. Multiplexers

- 4-to-1-line multiplexer



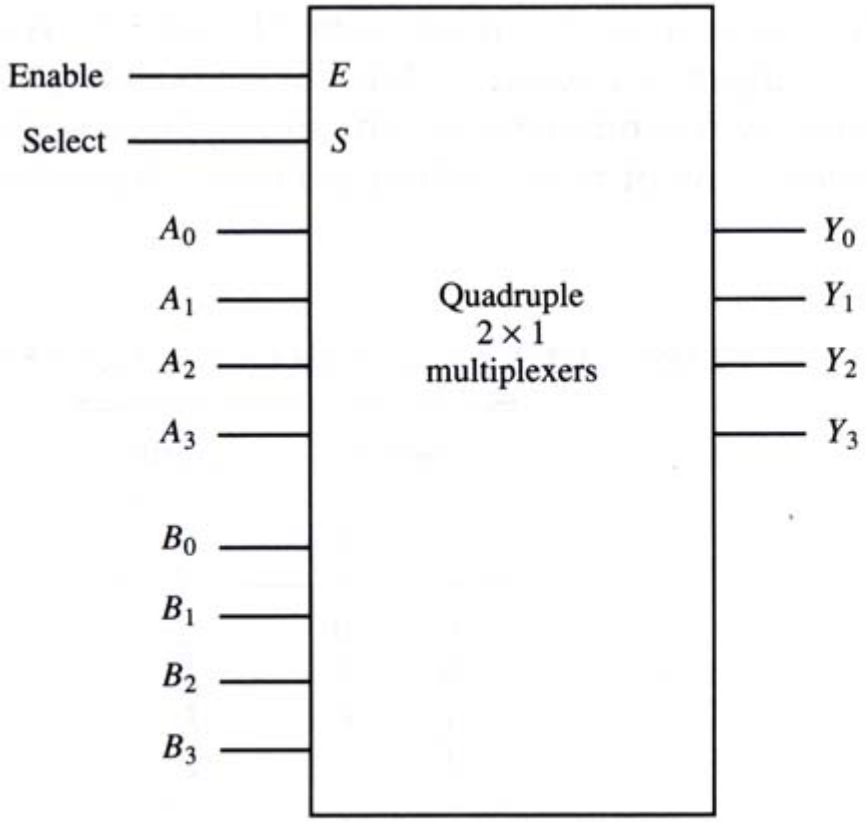
2-3. Multiplexers

- Function table for 4-to-1-line multiplexer

Select		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

2-3. Multiplexers

- Quadruple 2-to-1 line multiplexer



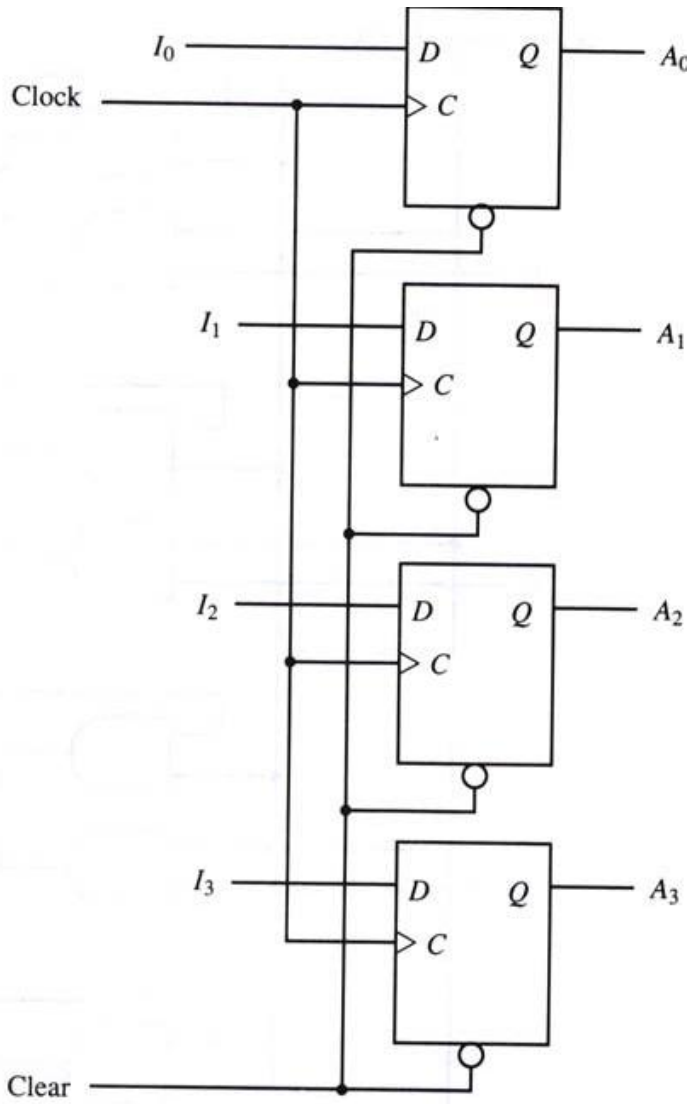
(a) Block diagram

E	S	Y
0	×	All 0's
1	0	A
1	1	B

(b) Function table

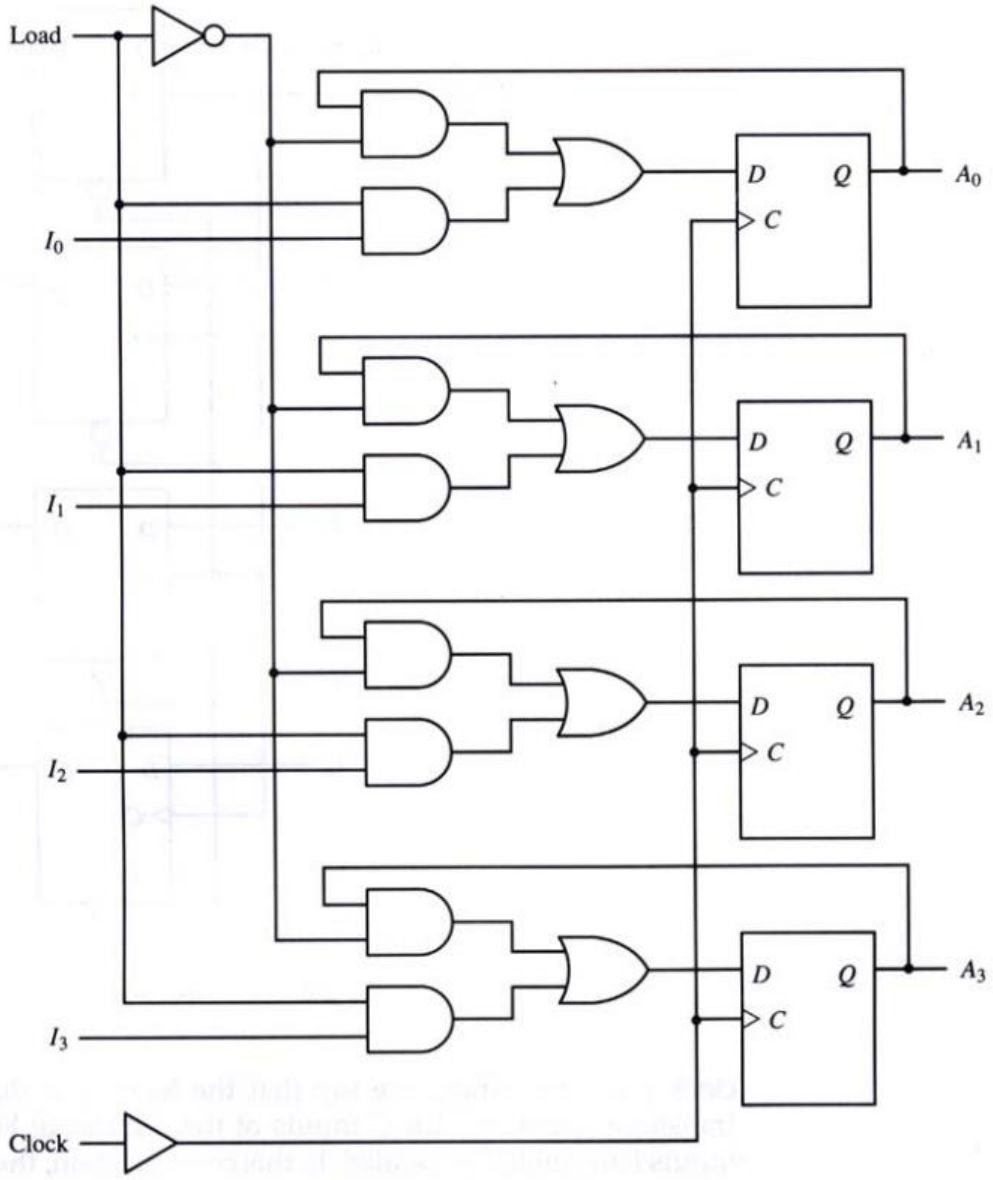
2-4. Registers

- A group of flip-flops with each flip-flop capable of storing one bit
- 4-bit register



2-4. Registers

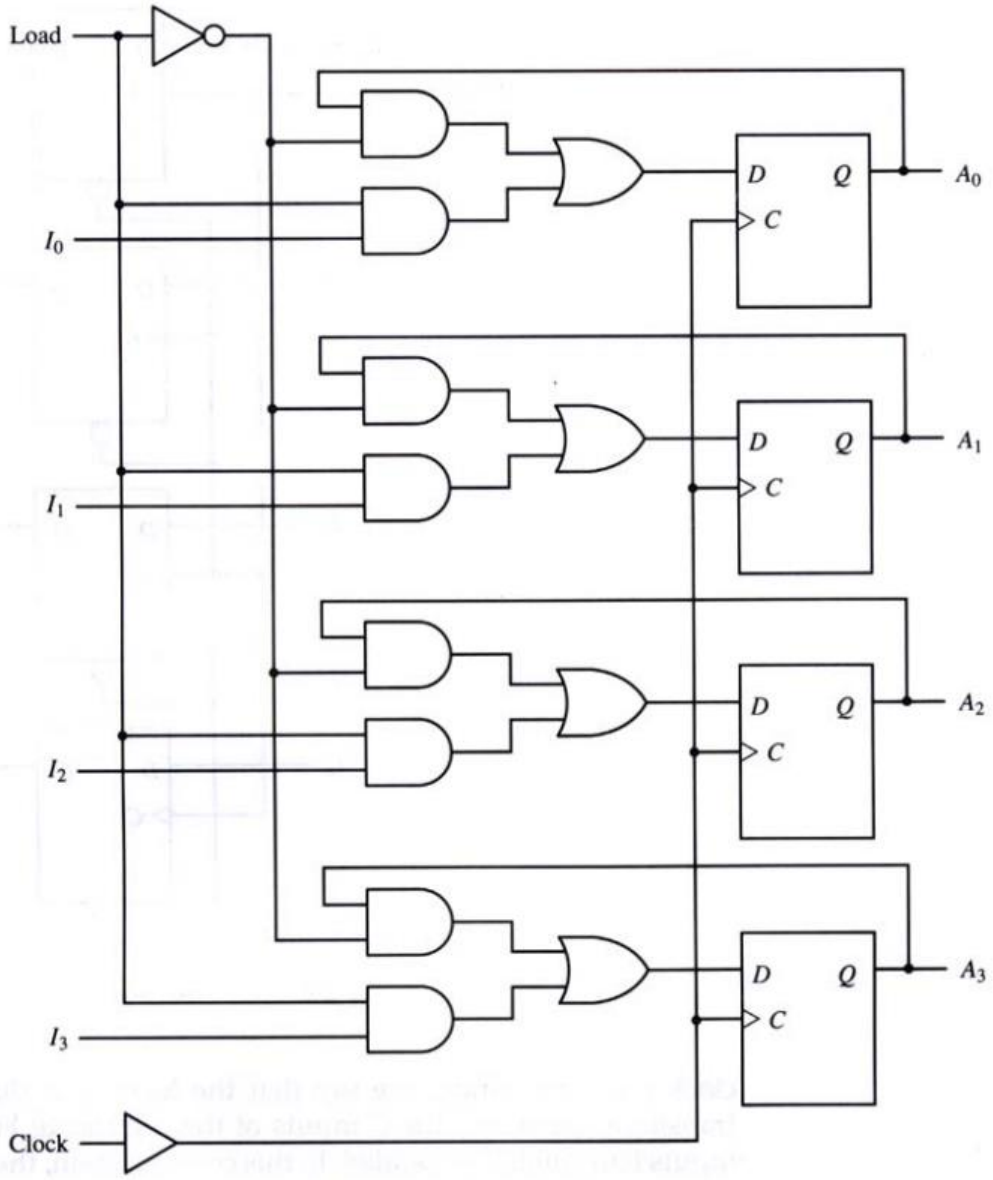
- Register with parallel load



2-4. Registers

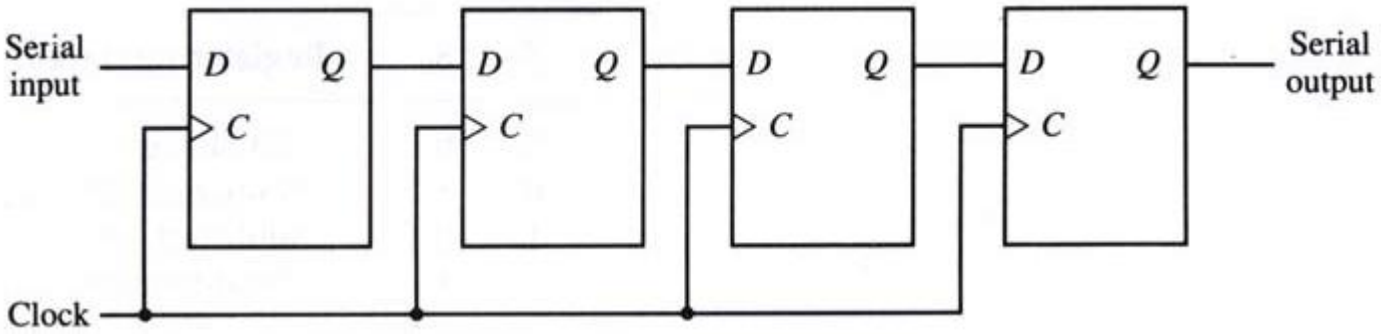
- Register with parallel load

$$D_n = L'A_n + LI_n$$



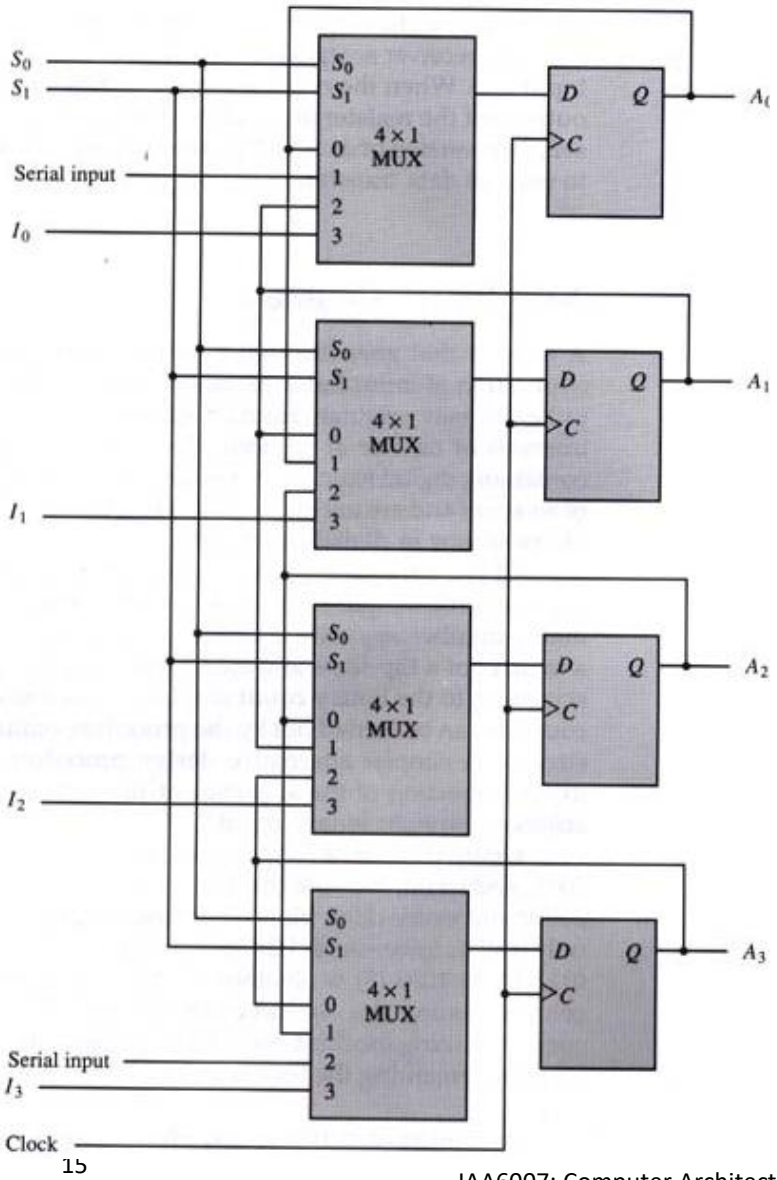
2-5. Shift registers

- 4-bit shift register



2-5. Shift registers

- Bidirectional shift register with parallel load



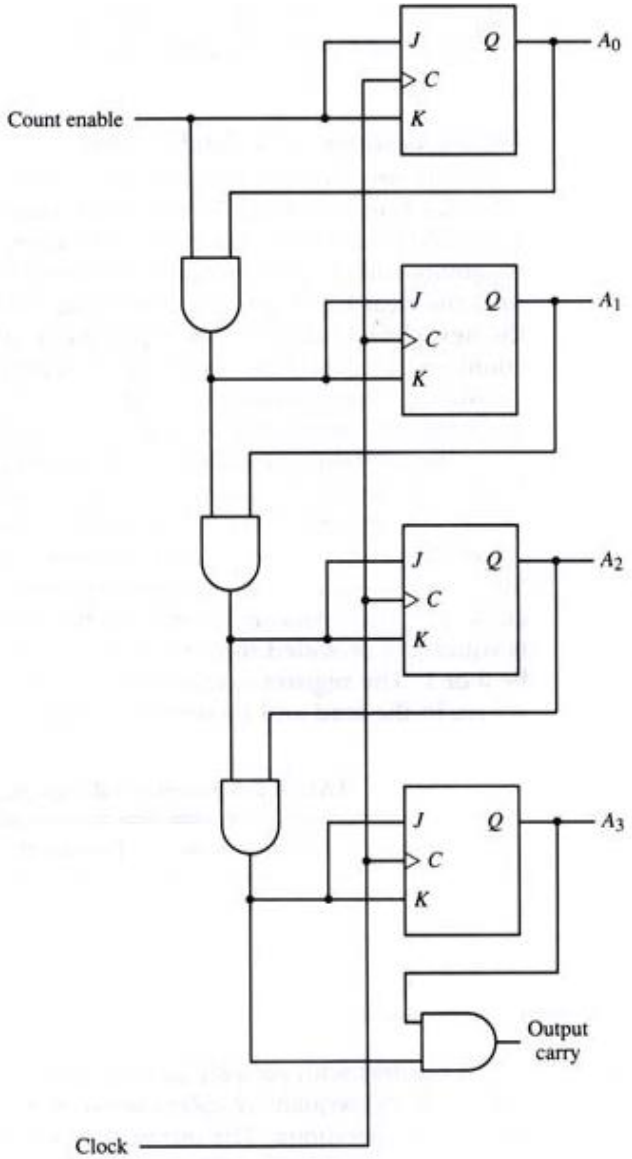
2-5. Shift registers

- Function table for bidirectional shift register with parallel load

Mode control		
S_1	S_0	Register operation
0	0	No change
0	1	Shift right (down)
1	0	Shift left (up)
1	1	Parallel load

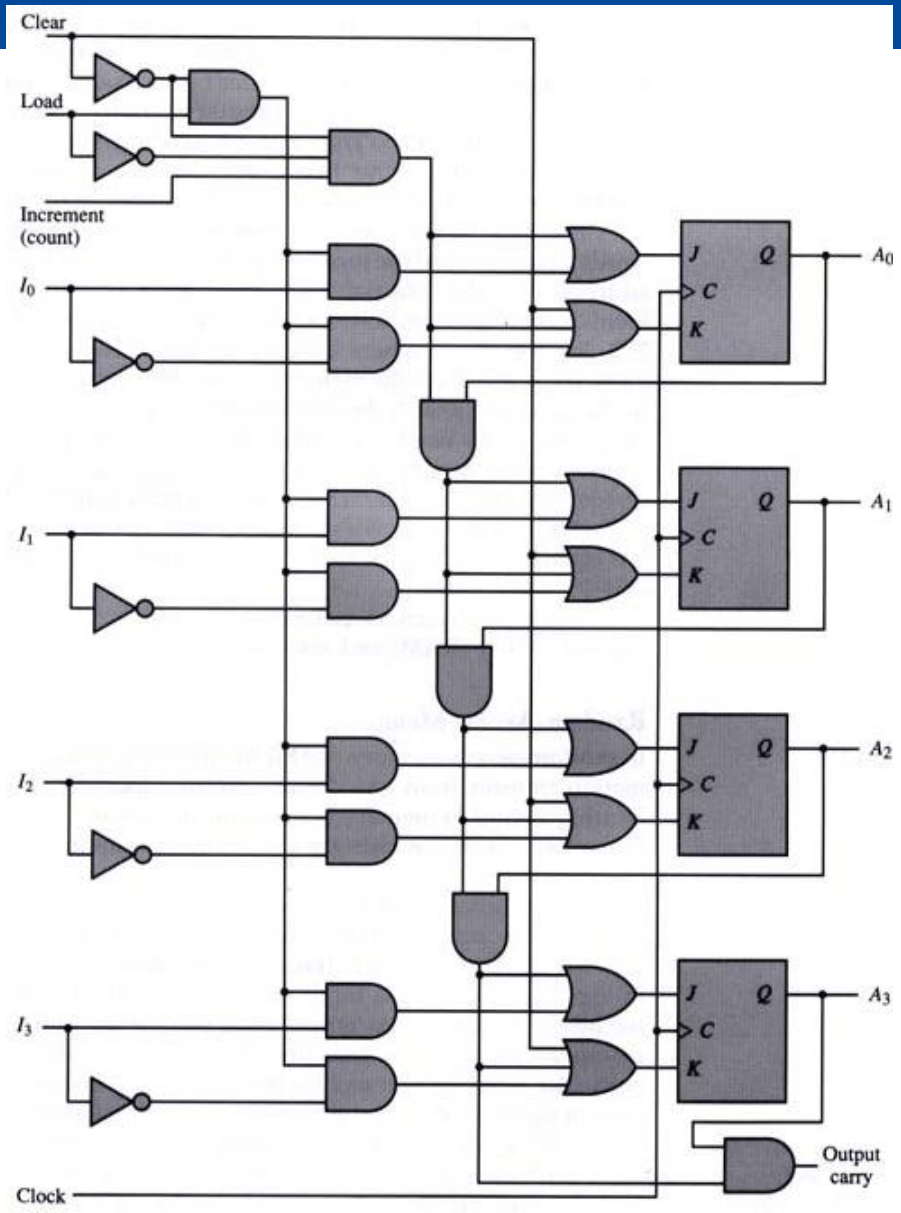
2-6. Binary counters

- 4-bit synchronous binary counter



2-6. Binary counters

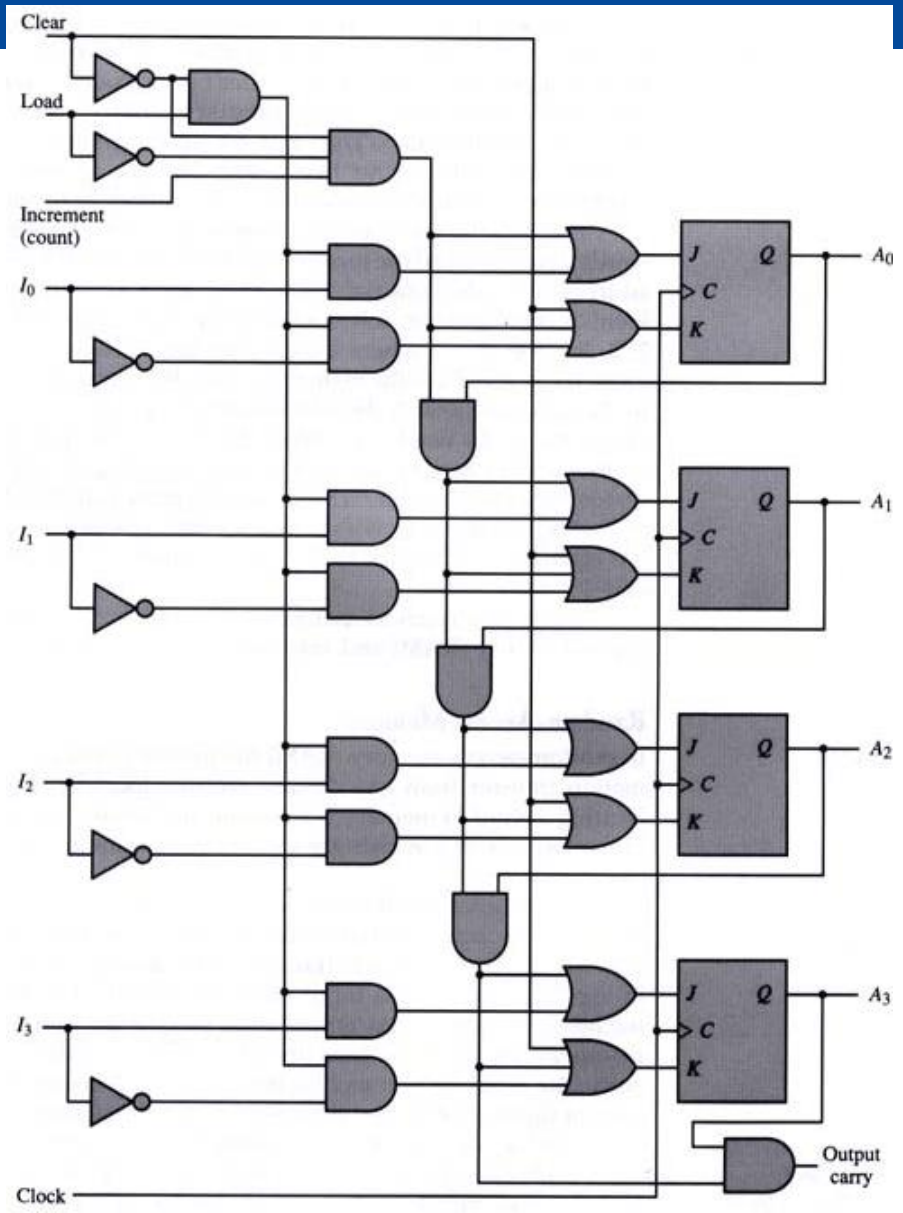
- Binary counter with parallel load



2-6. Binary counters

- Binary counter with parallel load

$$J_0 = C'L'I + C'LI_0$$
$$K_0 = C + C'L'I + C'LI_0'$$



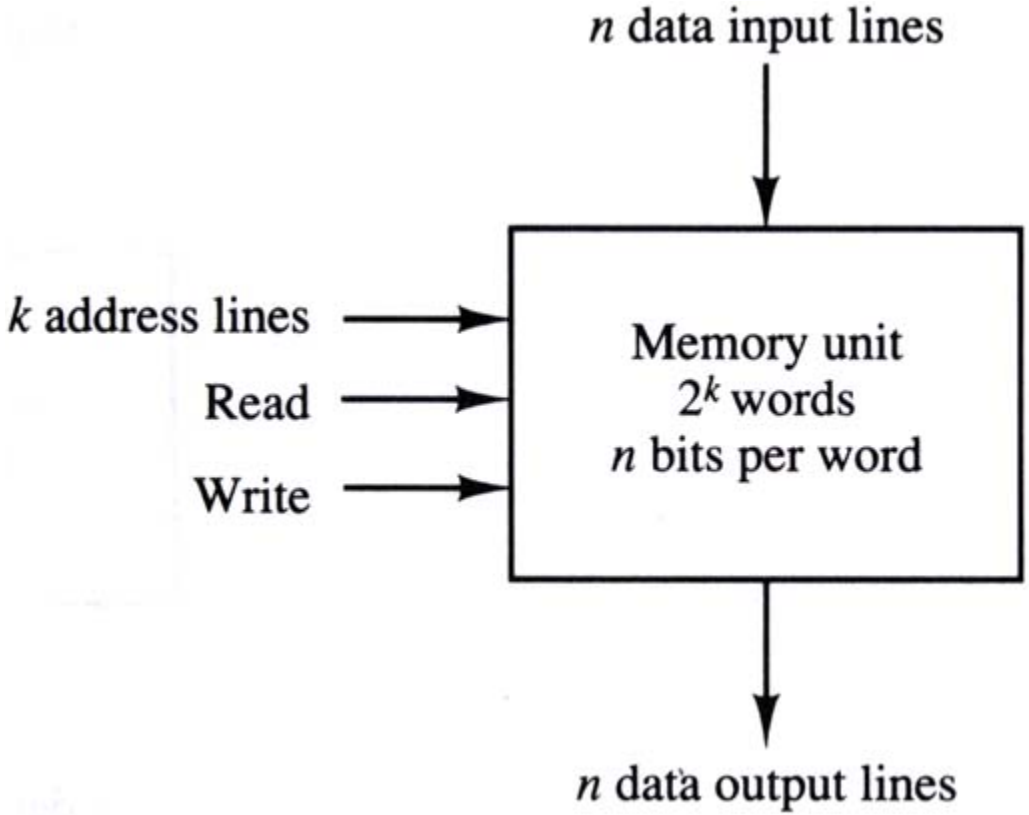
2-6. Binary counters

- Function table for the binary counter with parallel load

Clock	Clear	Load	Increment	Operation
↑	0	0	0	No change
↑	0	0	1	Increment count by 1
↑	0	1	×	Load inputs I_0 through I_3
↑	1	×	×	Clear outputs to 0

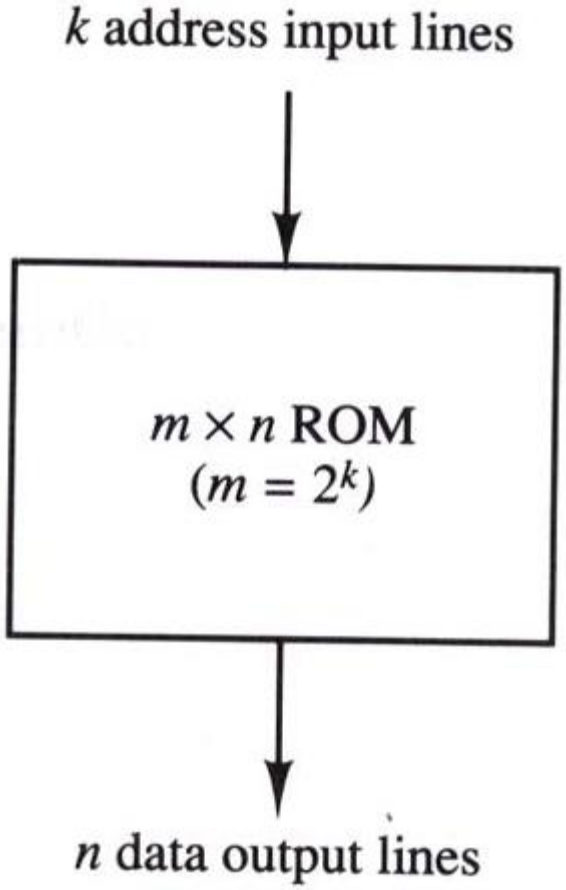
2-7. Memory units

- Word: an entity of bits that move in and out of a storage unit
- RAM (Random Access Memory)



2-7. Memory units

- ROM (Read Only Memory)
- Types of ROM
  - PROM (Programmable ROM)
  - EPROM (Erasable PROM)
  - EFPROM (Electronically Erasable PROM)



Problems

- 2-3, 2-4, 2-6, 2-8, 2-9, 2-11
- 2-12, 2-16, 2-17, 2-19, 2-20