

Motor Controller Concepts (Draft)

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Page 1 sketches the theory of nMOS and pMOS transistors -- Need to find relationship between output current and gate current.

Page 2 sketches the design of CMOS transistors which are constructed from one of each nMOS and pMOS. The V_{in} signal can be seen to be inverted in the V_{out} signal.

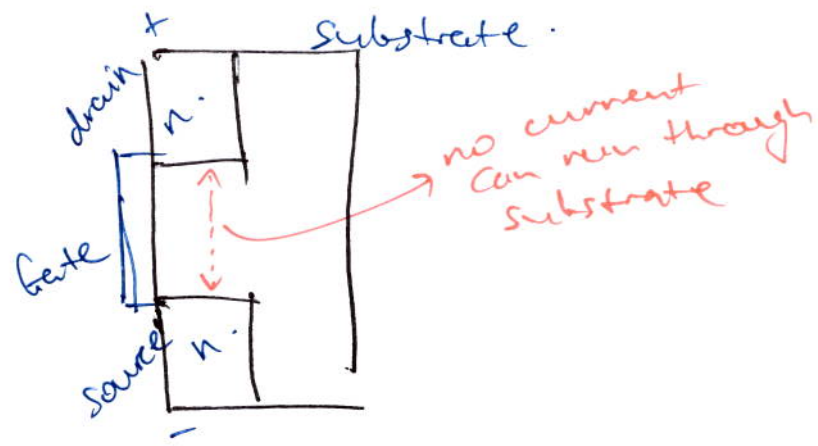
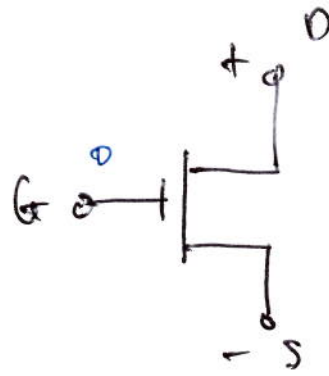
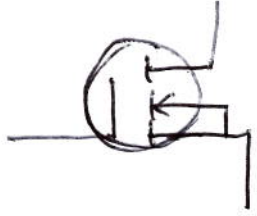
Page 3 Shows the BLDC motor's rotating magnetic field in the electrically commutated stator (clockwise rotation)|

Page 4 Shows a basic 3 phase BLDC motor with the motor commutating controllers; consisting of 6 MOSFETS (which can be replaced with 3 CMOS) and 3 Hall Sensors

Page 5 shows a simplified version of the commutation control with 3 Half Bridge circuits connecting to each phase. Also shows Hall Sensor and Switch timing.

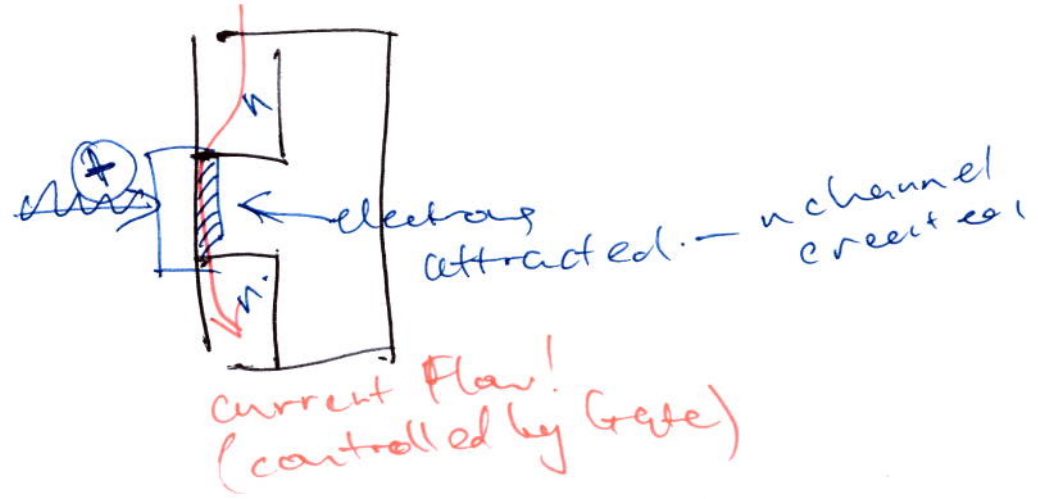
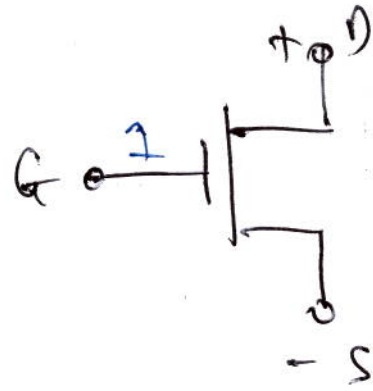
Page 6 shows the PID regulation for speed control (lots of work to do here)

NMOS



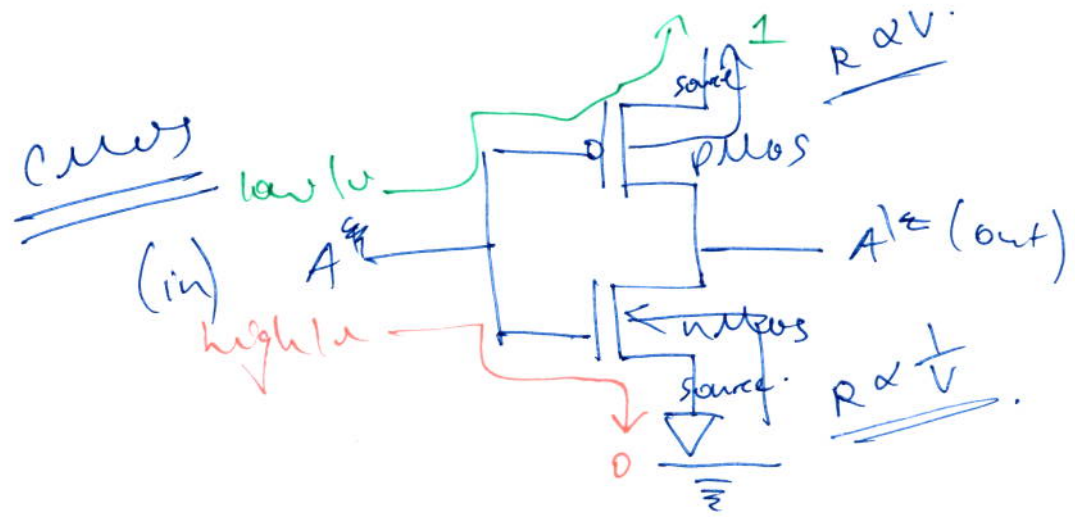
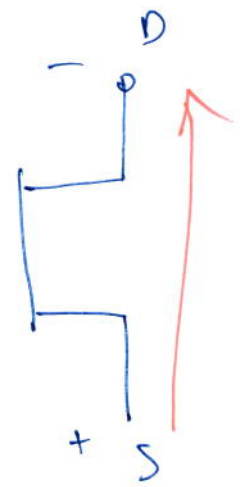
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Applying
a
voltage
at the
Gate



PMOS

digital
0
NOT

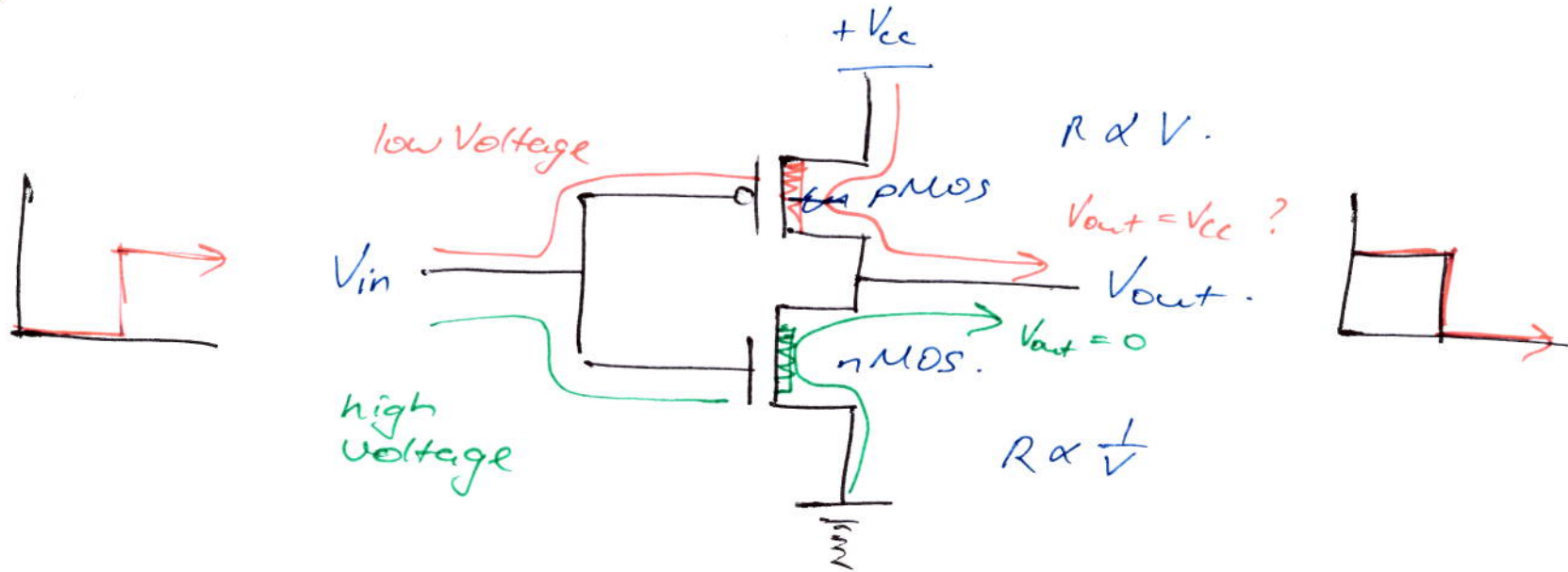


- high noise immunity
- low static power consumption.

CMOS

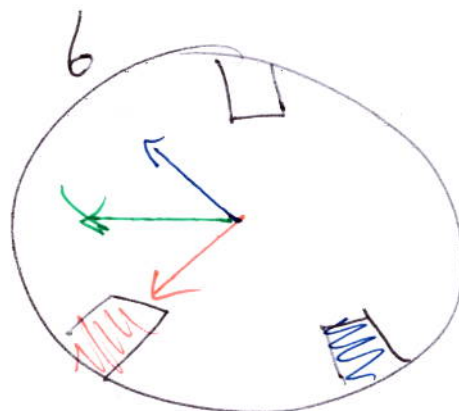
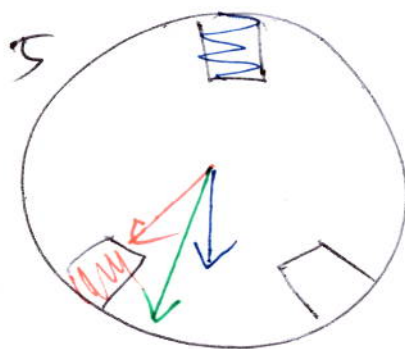
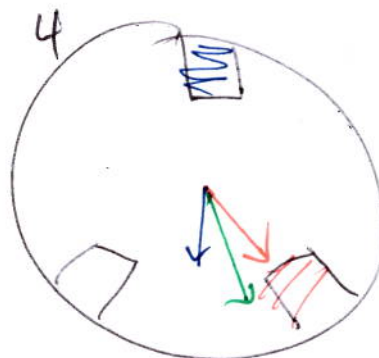
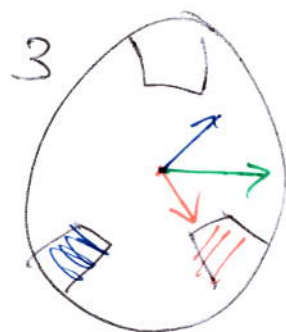
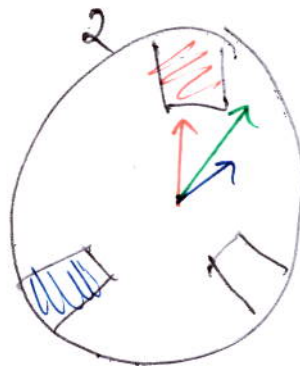
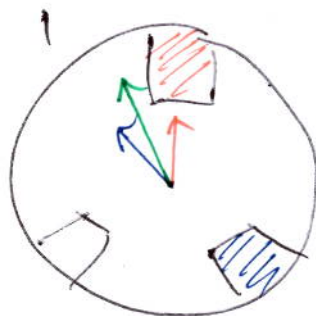
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CMOS Inverter

V_{in}	V_{out}
low	high
high	low



clockwise rotation of
Magnetic field.

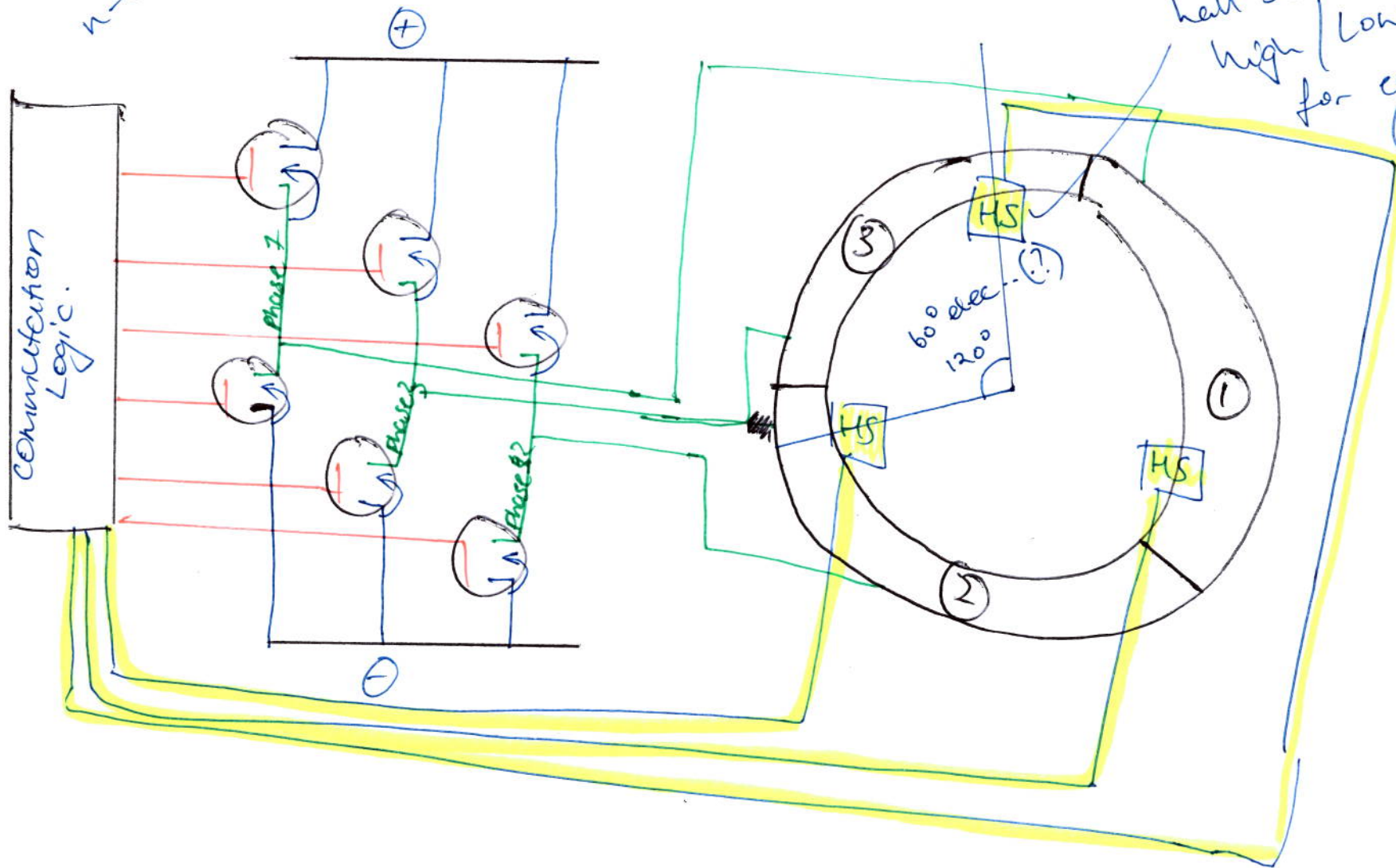
n-channel MOSFETS?
two MOSFETS
to make CWD
?

Motor Controller
Design.

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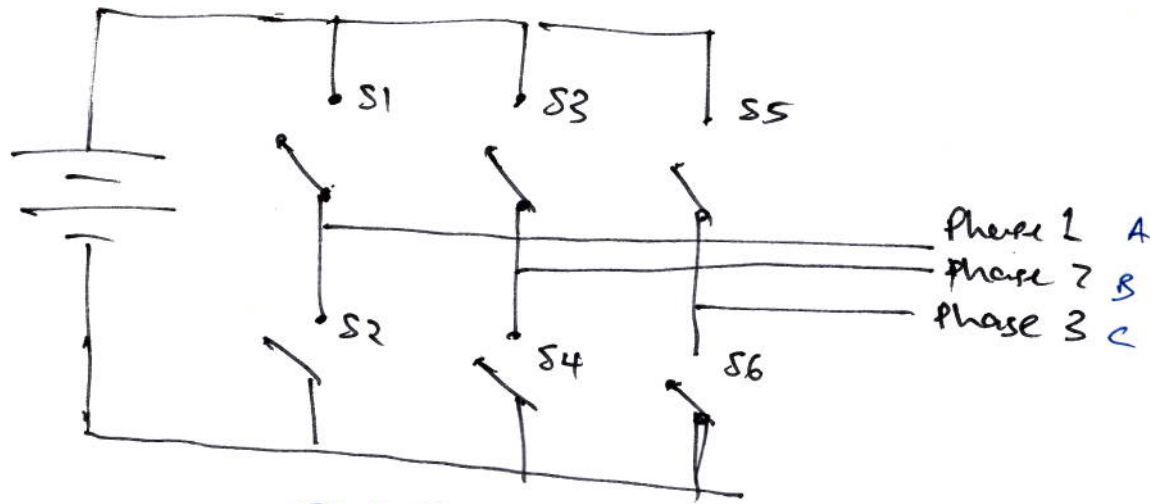
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hall sensors.
high / low state
for ca. 180°
(electrall).



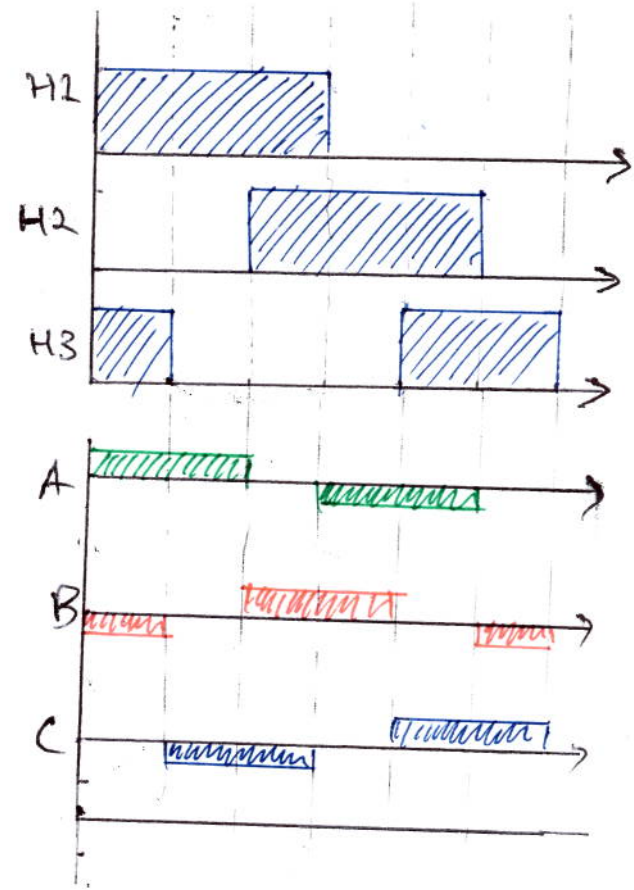
Commutation Logic

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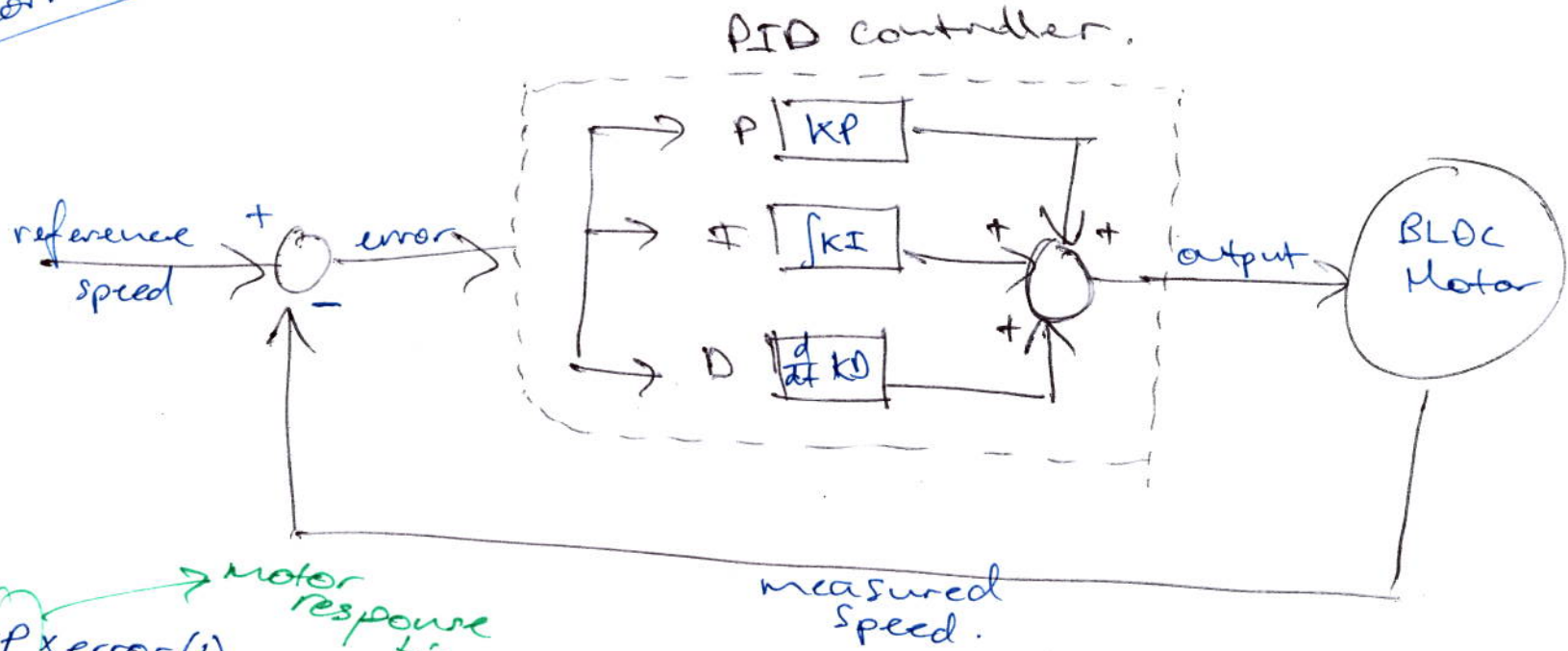
CW Rotation.

Hall Sensors (H3 H2 H1)			Phase	Switches.
101			A-B	1, 4
001			A-C	1, 6
011			B-C	3, 6
010			B-A	3, 2
110			C-A	5, 2
100			C-B	5, 4



Prof.

PID regulation for speed correction:
28/10/14.



$$\text{output} = \underbrace{K_P}_{\text{motor response time}} \times \text{error}(t) + K_I \int \text{error}(t) dt + K_D \frac{d}{dt} (\text{error}(t))$$

Where $\text{error}(t) = \text{Reference speed} - \text{measured speed}$.