BLDC Electronic Speed Controler Design

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Last Updated: January 12, 2015

Contents

1 Preface

This BLDC ESC is to be used in Shell's Eco-Marathon for the University of Western Austalia's running team in 2015, *EnVe*. The Shell Eco-Marathon challenges students from around the world to design, build and test ultra energy efficient vehicles.

2 Motor Parameters

The motor selection is the first step taken in order to design the motor controller. The motor was selected based on the application it was to be used in. The vehicles average and maximum speeds, and peak acceleration/deceleration was used as the criterion. The motor selected was the Turnigy G46 Brushless Outrunner.

2.1 Motor Demands

The boundary parameters mentioned previously are also essential in selecting the components for the power stage of the motor controller. These parameters are as follows;

Parameter	Value
Recommended Battery	4-5 Cells @ 14.4-18.5V
RPM	670kv
Max Current	40A
No Load Current	10V/3.9A
Current Capacity	55A/15sec
Internal Resistance	0.04 ohm
Weight	303g
Diameter of Shaft	6mm
Dimensions	76x50mm

Figure 1: Motor Parameters

Parameter	Value
Average Speed	30 km h^{-1}
Peak Speed	52 km h^{-1}
Wheel diameter	0.6m
Wheel Reduction Ratio	1:10
Average RPM (for switching frequency)	2653 RPM
Peak RPM (for switching frequency)	4598 RPM
Peak Acceleration (for dv/dt FET capabilities)	0.856 RPM s^{-1}

Figure 2: Motor Boundaries

3 MOSFETs

The selected MOSFET based on the motor parameters was the IRF1405

A summary of the MOSFETs parameters is below:

	Parameter	Value	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55V	$V_{GS} = 0V,\ I_D = 250\mu A$
I_D	Continuous Drain Current	169A	$V_{GS} = 10V,\ T_C = 25°C$
I_D	Continuous Drain Current	118A	$V_{GS} = 10V,\ T_C = 100°C$
I_{DM}	Pulsed Drain Current	680A	
T_J	Operating Junction Temperature Range	$-55°C - 175°C$	
Q_G	Total Gate Charge	$170nC - 260nC$	$I_D = 101A,\ V_{DS} = 44V,\ V_{GS} = 10V$
Q_{gs}	Gate-to-Source Charege	$44nC - 66nC$	$I_D = 101A,\ V_{DS} = 44V,\ V_{GS} = 10V$
Q_{gd}	Gate-to-Drain (Miller) Charge	$62nC - 93nC$	$I_D = 101A,\ V_{DS} = 44V,\ V_{GS} = 10V$
t_r	Rise time	190ns	$V_{DD} = 38V,\ I_D = 101A,\ R_G = 1.1\Omega,\ V_{GS} = 10V,$
t_f	Fall time	110ns	$V_{DD} = 38V,\ I_D = 101A,\ R_G = 1.1\Omega,\ V_{GS} = 10V,$

Figure 3: IRF1405 Specifications

The H-bridge was chosen to be designed with two N-channel MOSFETs despite the extra complexity involved in maintaining a sufficent gate voltage to the high side N-channel MOSFETs, compared to the simplier P-channel MOSFETs. This is because N-channel MOSFETs exhibit lower on resistances and hence minimized power losses.

3.1 Switching Frequency

3.2 Bootstrapping

The N-Channel MOSFET proposed to be used on the high side of the power stage requires a gate voltage above the source voltage by a minimum determined by the gate threshold voltage, $V_{GS(Th)}$. In order to reach these voltages, the simplest, and most widely used circuitry is the bootstrap charge circuit. [1]

The necessary calculations are:

$$\Delta V_{boot} \leq V_{CC} - (V_{fbs} + V_{GS(min)} + V_{source}) \tag{1}$$

Where;

- V_{CC} is the supply voltage to the gate driver
- V_{fbs} is the static foward bias voltage across the bootstrap didode
- V_{GS} is the minimum gate-to-source voltage required for the low on resistance across the MOSFET
- V_{source} is the floating voltage of the source pin on the FET when connected to the load and driver

$$C_{boot} = \frac{Q_{total}}{\Delta V_{boot}} \tag{2a}$$

$$Q_{total} = Q_g + t_{on} \cdot (I_{LK} + I_{QBS}) + Q_{LS} \tag{2b}$$

$$I_{LK} = I_{LK,GS} + I_{LK,H} + I_{LK,D} \tag{2c}$$

$$\tag{2d}$$

Where;

- Q_g is the gate charge on the FET
- I_{QBS} is the operating current in the Gate Driver
- t_{on} is the turning on interval of the FET
- Q_{LS} is the level shift charge required per cycle
- I_{LK} is the total leakage current
- LK, GS indicates the gate leakage of the FET
- LK, H indicates the high side floating supply leakage current
- LK, D indicates the leakage current through the bootstap didoe

[1] Fairchild AN9052: Design Guide for Selection of Bootstrap Components

3.2.1 Bootstrap Didodes

The bootstrap diode (D_{BS}) needs to be able to block the full power rail voltage, which is seen when the high side MOSFET is switched on. [2]. The current rating can be the product of total charge and switching frequency. Finally, certain characteristics of the D_{BS} is preferable; fast recovery time to minimize leakage current (100nS or less)[3]

Due to the low voltages involved[4]

3.2.2 Level Shifters

3.2.3 Disadvantages

Whilst bootstrapping has the advantage of being a simple and low cost implementation, it is not without disadvantages. The duty-cycle and on-time is limited by the requirement to refresh the charge in the bootstrap capacitor.

Negative voltage 2

3.2.4 Latch Up on Source

In the case of negative voltage in the source[5]

4 Gate Driver

The N-Channel MOSFET gate driver is selected based on the MOSFET specifications. Additional criteria such as functionality and minimal power dissipation is secondary.

4.1 Peak Current Drive Requirements

This is the primary criterion for the driver selection. This is primarly based on how fast the application (motor) requires the MOSFET to be turned on and off (rise and fall time of the gate voltage).

This turn on/off speed, dT, is in turn related to how fast the gate capacitance of the MOSFET can be charged and discharged.

$$dT = \frac{[dV \times C]}{I} = \frac{Q}{I} \tag{3}$$

Where;

- dV = Gate voltage
- C = Gate capacitance
- I = Peak drive current
- Q = Total gate charge

In the case of the IRF1405, the total gate charge is 260nC and a turn on/off time of $t = t_r + t_f = 300ns$

not sure, used max total gate charge

[2] IRF Design Tip 98-02: Bootstrap Component Selection for Control IC's
[3] IXYS AN-400: IX2127 Design Considerations
[4] Community Forums, answer by John Popelish
[5] Fairchild AN-6076: Design and Application Guide for Bootstrap Circuit for High Voltage Gate Drive IC

Thus we have a required average current draw of

$$I = \frac{Q}{dT} = \frac{260 \times 10^{-9}}{300 \times 10^{-9}} = 0.9A \tag{4}$$

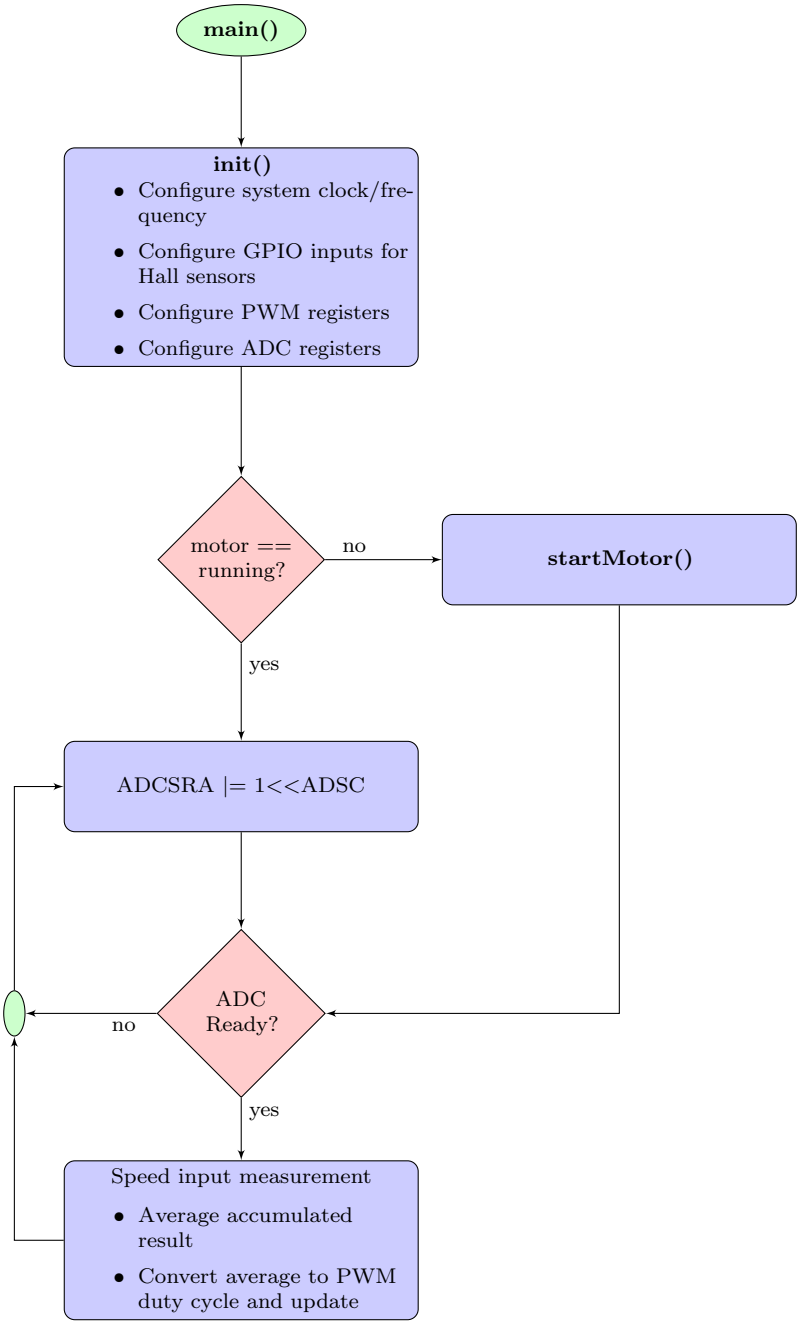
4.2 Power Dissipation

There are three elements due to the charging and discharging of the gate capacitance of the MOSFET [6]:

1. Power dissipation due to the charging and discharging of the gate capacitance of the MOSFET, P_C
2. Power dissipation due to quiescent current draw of the MOSFET driver, P_Q
3. Power dissipation due to cross-conduction (shoot-through) current in the MOSFET driver, P_S

[6] Microchip AN799: Matching MOSFET Drivers to MOSFETs

5 Firmware


main()
init()
• Configure system clock/frequency
• Configure GPIO inputs for Hall sensors
• Configure PWM registers
• Configure ADC registers
motor == running?
no
startMotor()
yes
ADCSRA |= 1<<ADSC
ADC Ready?
no
yes
Speed input measurement
• Average accumulated result
• Convert average to PWM duty cycle and update