TMS320F2810, TMS320F2811, and TMS320F2812 Digital Signal Processors Silicon Errata

SPRZ193G
January 2003
Revised August 2004

REVISION HISTORY

This revision history highlights the technical change made to the SPRZ193F errata to make it an SPRZ193G revision. This revision is a correction to an error in Table 1. Other modifications to advisories that were changed in SPRZ193F are shown as well to make clear the changes made since SPRZ193E.

Scope: Modified several advisories

PAGE(s) NO.	ADDITIONS/CHANGES/DELETIONS
5	Removed F silicon revision from Table 1 to correct documentation error. There is no silicon F revision available at this time.
6	Modified advisory for ADC − EOS BUF2 and EOS BUF1 Bits in ADCST Register Corrupted When INT MOD SEQ1 and INT MOD SEQ2 Are Used Simultaneously
7	Removed code samples from the advisory for CAN − CPU Access to the eCAN Registers May Fail If It Is in Conflict With an eCAN Access to the eCAN Registers and added a note explaining where to find code on the Web.

Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320F2810, TMS320F2811, and TMS320F2812 digital signal processors. The updates are applicable to:

- TMS320F2812 (179-ball MicroStar BGA™, GHH suffix)
- TMS320F2812 (176-pin low-profile quad flatpack [LQFP], PGF suffix)
- TMS320F2811 (128-pin LQFP, PBK suffix)
- TMS320F2810 (128-pin LQFP, PBK suffix)

1.1 Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device was tested over a particular temperature range and voltage range should not, in any way, be construed as a warranty of performance.

TMP Definition

TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

TMS Definition

Fully-qualified production device

1.2 Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package. The locations of the lot trace codes for the GHH and PGF packages are shown in Figure 1. The location of the lot trace code for the PBK package is shown in Figure 2. Table 1 shows how to determine the silicon revision from the lot trace code.

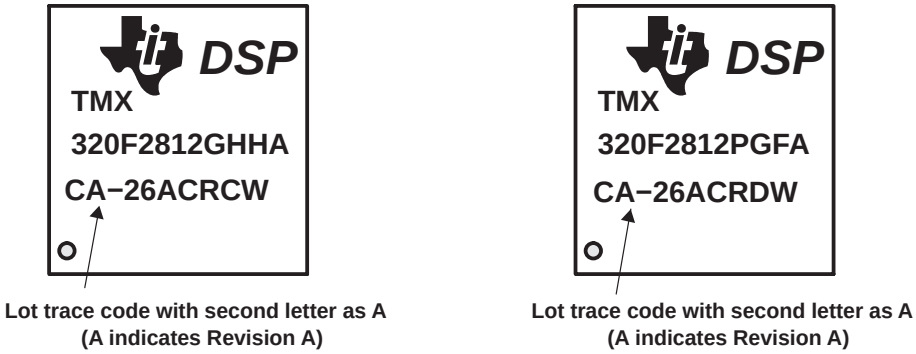

Figure 1. Example, Lot Trace Code for TMX320F2812 (GHH and PGF)

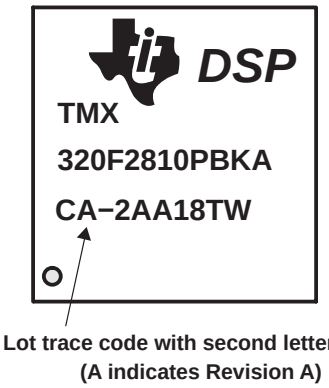

Figure 2. Example, Lot Trace Code for TMX320F2810 (PBK)

Table 1. Determining Silicon Revision From Lot Trace Code

Second Letter in Prefix of Lot Trace Code	Silicon Revision	Revision ID (0x0883)	Comments
Blank (no second letter in prefix)	Indicates Revision 0	0x0000	This silicon revision is available as TMX only.
A	Indicates Revision A	0x0001	This silicon revision is available as TMX only.
B	Indicates Revision B	0x0002	Internal
C	Indicates Revision C	0x0003	TMP/TMX/TMS
D	Indicates Revision D	0x0003	Internal
E	Indicates Revision E	0x0005	Production device (TMS)

2 Known Design Marginality/Exceptions to Functional Specifications

2.1 Advisories for Revisions 0, A, B, C, D, and E

Advisory	*WD − WDFLAG Bit Does Not Work as Intended*

Revision(s) Affected: 0, A, B, C, D, and E

Details: The WDFLAG bit in F281x devices cannot be used to reliably distinguish a watchdog-initiated reset from a power-on (or warm) reset. This is because the device expects the $\overline{\text{XRS}}$ pin to be pulled high (by the external reset circuit) within 4 SYSCLKOUT cycles (8 OSCLK cycles at power up) after the end of the watchdog-initiated reset pulse, which is 512 OSCCLK cycles. Most of the external $\overline{\text{XRS}}$ circuits cannot provide the fast rise-time requirement (due to the capacitance); therefore, the WDFLAG bit should not be used in applications .

Workaround: None. This bit should not be used.

Advisory	*ADC − EOS BUF1/2 Bits in ADCST Corrupted at the End of Conversion of Sequencer 1/2 When INT MOD SEQ1/2 is Enabled*

Revision(s) Affected: 0, A, B, C, D, and E

Details: Setting the INT MOD SEQx bit in ADCTRL2 as per the user guide should result in the ADC wrapper generating INT SEQx at the end of every other conversion rather than at the end of every conversion. Also EOS BUFx will be set at the end of every conversion to track the status of the SEQx in use. However, a conversion on SEQ1 will cause EOS_BUF2 to be set if INT_MOD_SEQ2 is enabled for that sequencer, even if INT_MOD_SEQ1 is not enabled.

For example, if INT_MOD_SEQ2 is set, a conversion on SEQ1 will cause the EOS_BUF2 bit to be set incorrectly. This will cause INT SEQ2 to be set incorrectly after the next SEQ2 completion. If EOS_BUF2 is already set (from previous SEQ conversion), a conversion on SEQ1 will cause EOS_BUF2 to be cleared causing the interrupt to be missed. The above relationship is also true for SEQ2 affecting SEQ1. In all cases, the sequencers do work correctly, with the exception that EOS BUFx gets corrupted.

Workaround: Do not use the INT_MOD_SEQx feature if both SEQ1 and SEQ2 will be used before two completions of sequence have completed on the INT_MOD_SEQ selected sequencer.

Advisory	*CAN − CPU Access to the eCAN Registers May Fail If It Is in Conflict With an eCAN Access to the eCAN Registers*

Revision(s) Affected: 0, A, B, C, D, and E

Details: If contention exists between the CPU and the eCAN controller for access to certain eCAN register areas, a CPU read may erroneously read all zeros (0x00000000), and a CPU write may erroneously fail to execute. Specifically:

1) If the CPU reads the eCAN mailbox RAM area (MSGID, MSGCTRL, MDL, or MDH registers) at the same time that the eCAN controller is accessing (reading or writing) the LAM/MOTO/MOTS register area, the CPU may erroneously read all zeros (0x00000000).

CAN − CPU Access to the eCAN Registers May Fail If It Is in Conflict With an eCAN Access to the eCAN Registers (Continued)

Workaround: For all CPU reads from the eCAN mailbox RAM area, check to see if the read returns all zeros. If so, the CPU should perform a second read. If the second read returns zero as well, then the data is correctly zero. If the second read returns a non-zero value, then the second data is the correct value. Note that interrupts must be disabled during the consecutive CPU reads. See Note 5.

Details: 2) If the CPU writes to the eCAN mailbox RAM area (MSGID, MSGCTRL, MDL, or MDH register) at the same time that the eCAN controller is accessing (reading or writing) the LAM/MOTO/MOTS register area, the CPU write may fail to execute.

Workaround: For all CPU writes to the eCAN mailbox RAM area, the CPU should write the data twice. Note that interrupts must be disabled during the consecutive CPU writes. See Note 5.

Details: 3) If the CPU reads the LAM/MOTO/MOTS register area at the same that the eCAN controller is accessing (reading or writing) the eCAN mailbox RAM area (MSGID, MSGCTRL, MDL, or MDH registers), the CPU may erroneously read all zeros (0x00000000).

Workaround: For all CPU reads from the LAM/MOTO/MOTS register area, check to see if the read returns all zeros. If so, the CPU should perform a second read. If the second read returns zero as well, then the data is correctly zero. If the second read returns a non-zero value, then the second data is the correct value. Note that interrupts must be disabled during the consecutive CPU reads. See Note 5.

Details: 4) If the CPU writes to the LAM/MOTO/MOTS register area at the same that the eCAN controller is accessing (reading or writing) the eCAN mailbox RAM area (MSGID, MSGCTRL, MDL, or MDH registers), the CPU write may fail to execute.

Workaround: For all CPU writes to the LAM/MOTO/MOTS register area, the CPU should write the data twice with a minimum of 4 CPU cycles in between the writes. Note that interrupts must be disabled during the consecutive CPU writes. See Note 5.

NOTES:
1. An example of the eCAN controller reading the LAM/MOTO/MOTS register area is a read of the LAMn register to check if a received message passes the acceptance mask filtering criterion. This happens during reception of a frame.
2. An example of the eCAN controller writing to the LAM/MOTO/MOTS register area is a write to the MOTSn register to update the time-stamp upon successful transmission of a frame.
3. An example for the eCAN controller attempting to read the mailbox RAM area (MSGID, MSGCTRL, MDL & MDH registers) is right before transmission.
4. An example for the eCAN controller attempting to write to the mailbox RAM area (MSGID, MSGCTRL, MDL & MDH registers) is right after reception.
5. A “C callable assembly” implementation of the workaround can be downloaded from the TI Website (literature number SPRC180).

Advisory	*SPI − Slave-Mode Operation*

Revision(s) Affected: 0, A, B, C, D, and E

Details: When in slave mode, the SPI does not resynchronize received words based on SPISTE. A spurious SPICLK pulse could therefore throw the data stream out of sync.

Workaround: If the circuit board is not noisy enough to generate spurious SPICLK pulses, then this is not an issue. If noise is an issue, then the McBSP in SPI-slave mode may be used, since the McBSP resynchronizes on each new word.

Advisory	*McBSP − Receive FIFO Read Conflict*

Revision(s) Affected: 0, A, B, C, D, and E

Details: The McBSP peripheral operates with or without FIFOs. The receive FIFO has interrupt generation logic that initiates interrupts based on the 5-bit FIFO status bits (12−8) and interrupt level bits (4−0) in the MFFRX register.

If the CPU reads the receive FIFO while the McBSP module writes new data into the FIFO, there is a potential conflict. The CPU read will not be stalled and read data will not be valid. The FIFO write gets the priority. The receive FIFO will be updated after every word is received in DRR2/1 registers. The DRR2/1 register update time will primarily depend on the word size and CLKR rate. For example for 8-bit word, it should be typically 8 times the CLKR cycle time. This conflict will be more pronounced if data transferred on the receive channel is back-to-back with no delays between words.

Workaround: The receive FIFOs should be read based on receive interrupts and within the next word receive time. To avoid the read conflict, additional checks could be used before initiating receive FIFO read. In most McBSP configurations, the FSR is a receiving sync pulse either active high or low (based on the FSR polarity bit) and will go inactive during word transfer time. These active and inactive phases can be detected by checking the FSR flag bit MCFFST (bit 3) register or checking the status of the FSR pin. See the FSR flag bit description for details.

Advisory	*McBSP − Read Operations Decrement the McBSP FIFO*

Revision(s) Affected: 0, A, B, C, D, and E

Details: A read operation from any of the following locations will cause the McBSP receive FIFO contents to decrement by 1, as if the McBSP DRR1 register had been read:

- 0x7001 Reserved
- 0x7401 EV−A T1CNT
- 0x7C01 Reserved

McBSP − Read Operations Decrement the McBSP FIFO (Continued)

The actual value read from the location is correct and is not affected by this issue.

Workaround(s):

1. Ensure that the McBSP receive FIFO is empty before performing any read operation from any of these addresses.
2. If McBSP traffic is common in the application and a timer count needs to be monitored, consider using a timer other then EV Timer1.

Advisory — *SCI Bootloader Does Not Clear the ABD Bit Before Auto-Baud Lock*

Revision(s) Affected: 0, A, B, C, D, and E

Details: The SCI ROM bootloader code does not correctly clear the Auto-Baud Detect (ABD) bit in the SCIFFCT register before the auto-baud process begins. The bootloader code fragment is shown below:

```
// Prepare for autobaud detection
// Set the CDC bit to enable autobaud detection
// and clear the ABD bit
SCIARegs.SCIFFCT.all = 0x2000;
```

The comments incorrectly state that the ABD bit is cleared. The ABD bit is cleared by writing a 1 to the ABD_CLR bit (bit 14) of the SCIFFCT register. This situation does not hinder operation from power up or reset because the ABD bit is cleared by default after reset. If, however, the bootloader is invoked a second time from software, then the ABD bit will not be cleared and autobaud lock will not occur properly.

Workaround: If the bootloader is going to be re-invoked by software, the user's code must first clear the ABD bit before calling the bootloader. To do this, write a 1 to the ABD CLR bit (bit 14) in the SCIFFCT register.

Advisory — *EV − QEP Circuit*

Revision(s) Affected: 0, A, B, C, D, and E

Details: After a DSP reset, the QEP module fails to detect the first transition that occurs on QEP input pins. (This problem also manifests itself when an external clock is used for the EV timers.) Therefore, if the first transition occurs after a GP timer has been initialized and enabled as the QEP counter (i.e., to use QEP as source of clock), the first transition will not be counted by the GP timer. The result is an error of one count in the GP timer out of a total of 1024 counts for a 256-line encoder, or 4096 counts for a 1024-line encoder. However, the issue is not a concern under any of the following conditions:

1. *The first transition happens **before** the GP timer is initialized and enabled as QEP counter.* This ensures that all transitions are counted after initialization.
2. *After the first index pulse is received and if the index pulse is used to recalibrate the GP Timer (through capture interrupt).* The recalibration corrects the error in the GP timer; therefore, from the time the first index pulse is received, the QEP counter becomes accurate.

EV − QEP Circuit (Continued)

Workaround(s):

1. Make the first transition happen before the GP timer is initialized and enabled as QEP counter. This is usually the case because typically the rotor shaft is locked to a known position before the GP timer is initialized. Locking the rotor shaft will generate transitions on QEP input pins, unless the rotor shaft is exactly aligned to the known position (which is a rare case). Disturbing the rotor shaft on purpose takes care of the rare case.
2. Use the index pulse of the encoder to recalibrate the GP timer used as QEP counter.
3. The counter has to be forced to count before the application actually uses the QEP. During initialization, configure the internal clock (HSPCLK) to be the counter source. After the first count is done, the counter should be reconfigured for external signals (QEP/TCLKIN) and reset to 0. Now the counter will also count the first edge of the QEP.

Advisory *Logic-High Level for XCLKIN Pin*

Revision(s) Affected: 0, A, B, C, D, and E

Details: This advisory is applicable only when an external oscillator is used to clock the device. The X1/XCLKIN pin is referenced to the core power supply (V_{DD}), rather than the 3.3-V I/O supply (V_{DDIO}). Therefore, the logic-high level for the input clock should not exceed V_{DD}. This requirement remains the same for future silicon revisions as well.

Workaround: A clamping diode may be used to clamp a buffered clock signal to ensure that the logic-high level does not exceed V_{DD} (1.8 V or 1.9 V). Otherwise, 1.8-V oscillators may be used.

Advisory *ADC − Reserved Bits in Autosequence Status Register (ADCASEQSR)*

Revision(s) Affected: 0, A, B, C, D, and E

Details: SEQ2 STATE2−0 and SEQ1 STATE3−0 bit fields (bits 6 through 0) are the pointers of SEQ2 and SEQ1, respectively. These bits are reserved for TI testing and should not be used in customer applications.

Workaround: None

Advisory *ADC Result Register Update Delay*

Revision(s) Affected: 0, A, B, C, D, and E

Details: The ADC result status flags INT_SEQ1 and INT_SEQ2 bit fields (bits 0 and 1 respectively) in the ADC_ST_FLG register indicate the availability of new ADC results after conversions and initiation of the ADC interrupts.

The update of the ADC result register requires one extra ADC cycle to complete after the status flags INT_SEQ1 and INT_SEQ2 bit(s) are set. The result of reading the result register prior to this extra cycle will result in old data being read (reset value/previous conversion result).

ADC Result Register Update Delay (Continued)

If auto-sequencers are enabled with a non-zero value in the MAXCONV register, the last result register update takes an additional ADC cycle from the time the INT_SEQ1 or INT_SEQ2 flag is set.

Workaround: Delay the read of the ADC result register(s) by at least one ADC clock period. This delay can be implemented by using software delay loops.

If the ADC result register(s) are read using the ADC interrupt, rather than polling, the wait period introduced by the ISR (interrupt service routine) could minimize the delay needed in software. This ISR branching delay is generally greater than 8 SYSCLKOUT cycles.

The ratio of the ADC clock (ADCCLK) to the CPU clock (SYSCLKOUT) determines the size of the software delay. For example, if ADCCLK = 10 MHz the software delay should be at least 100 ns.

Timing example to estimate the software delay:

1) Get the HSPCLK prescaler value − HISPCP
2) Get the ADCCLK prescaler value − ADCCLKPS
3) Get the CPS (ADCCTRL1[7]) value − CPS
4) Software wait-period in CPU cycles (SYSCLKOUT) before the ADC result register read is defined as:

```
Software wait  = (HISPCP *2) * (ADCCLKPS * 2) * (CPS +1)  cycles

If HISPCP  or ADCCLKPS is 0, then the respective terms should be (HISPCP +1)
or (ADCCLKPS+1)
```

Advisory — *ADC Sequencer Reset While Dual Sequencers Are Running*

Revision(s) Affected: 0, A, B, C, D, and E

Details: In the TMS320F2812/TMS320F2811/TMS320F2810 on-chip ADC, there are two sequencers for performing ADC conversions; SEQ1 and SEQ2. If one of the sequencers is reset while the other sequencer is running, it will result in the running sequencer never completing its current sequence. The sequencer busy bit (bit 3/bit2 in ADCST register) for the sequencer will remain active and an “End-of-sequence (EOS)” interrupt for the running sequencer will never be generated. For example, if SEQ1 is reset while SEQ2 is performing a sequence, then SEQ2 will never complete.

Workaround: If dual sequencers are enabled, then the software handling the ADC module should make sure that SEQ1 BSY/ SEQ2 BSY bits are not set before performing a reset of either sequencer.

2.2 Advisory for Revision D Only

Advisory — *DEVICE-ID Register of the Silicon*

Revision(s) Affected: D

Details: The DEVICE-ID register of the rev D silicon contains the same value (0x0003) as that of the rev C silicon.

Workaround: The next revision (Rev E) of the silicon has a DEVICE-ID value of 0x0005.

2.3 Advisories for Revisions 0 and A Only

These revisions are not to be used in development or production.

Advisory — *ADC − Device Has Higher Gain Error Than the Design Goal of 1% FSR on All of the B0−B7 Channels*

Revision(s) Affected: 0 and A

Details: The device has a higher gain error than the design goal of 1% FSR on all of the B0−B7 channels. The gain error varies across channels A0−A7 and B0−B7.

Based on the current data obtained on B group channels, all B group channels show a uniform gain error as high as 2 to 3%.

Workaround: The channel-to-channel gain error data across channels are listed in Table 2. This should help in calibrating in software or hardware until the next revision of the silicon.

Table 2. Channel-to-Channel Offset Error Data Across Channels (176-Pin PGF)

ADC Channels	A0	A1	A2	A3	A4	A5	A6	A7	B0	B1	B2	B3	B4	B5	B6	B7
Gain Error in %	0.20	0.18	0.52	0.53	0.53	0.55	0.54	0.54	2.92	2.92	2.92	2.93	2.93	2.93	2.93	2.97
Offset in LSB Counts	14.80	15.64	4.86	9.82	5.82	−14.57	−13.98	−31.78	20.94	21.98	22.48	23.39	22.39	23.14	23.64	24.91

Note:

The data provided are typical values only. These values are obtained from bench characterization at room temperature on a few devices.

TMX samples are not fully screened for all ADC parameters. If there are devices that have worse performance than suggested issues/values, it is recommended that the part be replaced.

Advisory *ADC − Device Has Higher Offset Error Than the Design Goal (0.5 to 1%) on Some Channels*

Revision(s) Affected: 0 and A

Details: Based on the current data obtained on all channels, some channels show an offset error as high as 1%.

Workaround: The channel-to-channel offset error data across channels are listed in Table 2. This should help in calibrating in software or hardware until the next revision of the silicon.

Note:

The data provided are typical values only. These values are obtained from bench characterization at room temperature on a few devices.

TMX samples are not fully screened for all ADC parameters. If there are devices that have worse performance than suggested issues/values, it is recommended that the part be replaced.

Advisory *ADC − Device Has Higher Non-Linearity Than the Design Goal of 2 LSBs*

Revision(s) Affected: 0 and A

Details: Based on the current data obtained on all channels, some channels show non-linearity as high as 12 LSBs in the mid-scale range. That is, the mid-range conversions will be off by about 12 LSB counts.

Workaround: This issue is corrected in the next revision of the silicon. The following option could be used to correct for INL errors only for the TMX Revision A silicon.

The INL issue is across all channels. Use the ADC results only for 9-bit data accuracy on this revision of the silicon and ignore the rest of the bits. This will mitigate the INL effect in the application provided the algorithm can tolerate 9-bit accuracy.

Note:

The data provided are typical values only. These values are obtained from bench characterization at room temperature on a few devices.

TMX samples are not fully screened for all ADC parameters. If there are devices that have worse performance than suggested issues/values, it is recommended that the part be replaced.

Advisory — *XINTF − XREADY Signal is not Sampled Properly When Using Asynchronous Sampling Mode*

Revision(s) Affected: 0 and A

Details: In case of asynchronous ready mode, if the XREADY signal is high within the Lead period, then access will complete in the number of cycles programmed in LEAD + ACTIVE + TRAIL counters even if XREADY goes low before the start of the ACTIVE period. In this case, XREADY is not being used properly to extend the access.

Workaround: Try one of the following possible workarounds:

- Ensure that the XREADY signal is not low at the start of an access when using asynchronous sampling mode. If the XINTF sees the XREADY signal low from the start of an access, then the ACTIVE period will be extended as desired.
- Use the XTIMING register wait-state values to extend the access such that timings are met without using XREADY.
- Use the synchronous XREADY sampling mode. This problem is not observed in synchronous mode.

This issue is fixed in the next revision of the silicon.

Advisory — *Set Device Emulation Register Bits for On-Chip RAM Performance*

Revision(s) Affected: 0 and A

Details: To get the best performance of on-chip RAM blocks M0/M1/L0/L1/H0, the internal control register bits have to be enabled. The bits are in the Device Emulation Registers.

Workaround: All device initialization code should include the following register updates. These are EALLOW-protected registers.

Register Address	Value
0x950	0x0300
0x951	0x0300
0x952	0x0300
0x953	0x0300
0x954	0x0300

Code Example:

```
EALLOW
MOVL    XAR1,#0x0950
MOVL    XAR2,#0x0300
MOV     *XAR1++,AR2
MOV     *XAR1++,AR2
MOV     *XAR1++,AR2
MOV     *XAR1++,AR2
MOV     *XAR1++,AR2
EDIS
```

The Code Composer GEL init files will initialize these for emulation and debug environment. From the next silicon revision onward, this initialization is automatically done upon reset.

Advisory *OTP Memory*

Revision(s) Affected: 0 and A

Details: The 1K-word OTP memory is not available.

Workaround: This is fixed in the next revision of the silicon.

Advisory *A Low Output on GPIOF14 Can Disable the PLL and Watchdog if the Watchdog Fires a Reset*

Revision(s) Affected: 0 and A

Details: If, during program execution, the XF_$\overline{\text{XPLLDIS}}$/GPIOF14 signal is changed to either of the following:

- A general-purpose output and driven low
- The XF functionality and driven low

and a watchdog reset occurs, then the low output state of the XF_$\overline{\text{XPLLDIS}}$/GPIOF14 pin will be latched into the $\overline{\text{XPLLDIS}}$ signal. The result of this is that the PLL and the reset function of the watchdog will be disabled. The watchdog itself is not disabled.

Workaround: One of the following workarounds can be used:

- Do not toggle XF/GPIOF14 in user code. Instead, use another GPIO signal for status.
- Set the watchdog to fire an interrupt instead of reset.

This is fixed in the next revision of the silicon.

Advisory *PLL − PLL x4 and x8 Multiplier Ratios*

Revision(s) Affected: 0 and A

Details: When the PLL multiplier is set to x4 or x8 (by writing 0004 or 0008, respectively, in the PLLCR register), the watchdog is re-enabled and resets the device upon a WD overflow. With noisy board conditions, this problem may be observed with other PLL multipliers as well.

Workaround: Do not use these multiplier values for these revisions.
This is fixed in the next revision of the silicon.

Advisory	*Low-Power Modes − STANDBY Mode*

Revision(s) Affected: 0 and A

Details: When the device is put into STANDBY mode, the watchdog is re-enabled and resets the device upon a WD overflow.

Workaround: Do not use the STANDBY mode for these revisions.
This is fixed in the next revision of the silicon.

3 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com**

To access documentation on the web site:

1. Go to **http://www.ti.com**
2. Click on **DSP Product Tree**
3. Click on the **C2000** tab
4. Click on **TMS320C28x DSP Generation**
5. Click on a device name and then click on the documentation type you prefer.

For further information regarding the TMS320F2810 and TMS320F2812, please see the following publication:

- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812 Digital Signal Processors* data manual (literature number SPRS174)

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