TEXAS INSTRUMENTS
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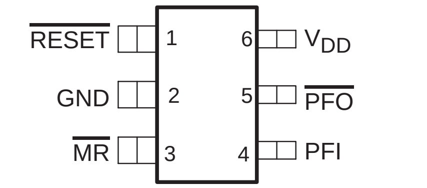
features

- **Precision Supply Voltage Supervision Range: 0.9 V, 1.2 V, 1.5 V, 1.6 V, 2 V, 3.3 V**
- **High Trip Point Accuracy: 0.75%**
- **Supply Current of 1.2 μA (Typ)**
- **RESET Defined With Input Voltages as Low as 0.4 V**
- **Power On Reset Generator With a Delay Time of 130 ms**
- **Push/Pull or Open-Drain $\overline{\text{RESET}}$ Outputs**
- **SOT23-6 Package**
- **Temperature Range . . . −40°C to 85°C**

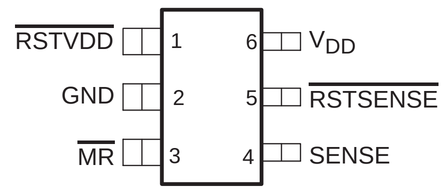
typical applications

- **Applications Using Low-Power DSPs, Microcontrollers or Microprocessors**
- **Portable/Battery-Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communication Systems**
- **Programmable Controls**
- **Industrial Equipment**
- **Notebook/Desktop Computers**
- **Automotive Systems**

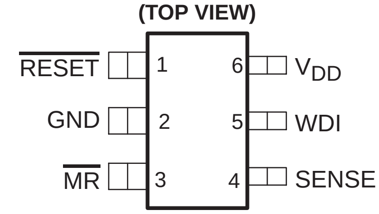
TPS3103
DBV PACKAGE
(TOP VIEW)



TPS3106
DBV PACKAGE
(TOP VIEW)



TPS3110
DBV PACKAGE
(TOP VIEW)

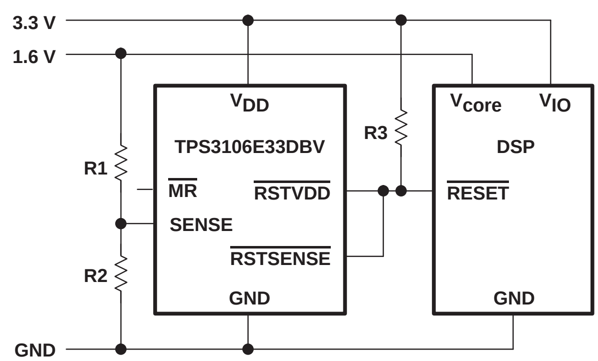


description

The TPS310x, TPS311x families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD}) becomes higher than 0.4 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps the $\overline{\text{RESET}}$ output active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state to ensure proper system reset. The delay time starts after V_{DD} has risen above the V_{IT}. When the V_{DD} drops below the V_{IT}, the output becomes active again.

typical application circuit



All the devices of this family have a fixed-sense threshold voltage (V_{IT}) set by an internal voltage divider.

description (continued)

The TPS3103 and TPS3106 have an active-low, open drain $\overline{\text{RESET}}$ output. The TPS3110 has an active-low push/pull $\overline{\text{RESET}}$.

The product spectrum is designed for supply voltages of 0.9 V up to 3.3 V. The circuits are available in a 6-pin SOT-23 package. The TPS31xx family is characterized for operation over a temperature range of −40°C to 85°C.

AVAILABLE OPTIONS

DEVICE	$\overline{\text{RESET}}$ OUTPUT	$\overline{\text{RSTSENSE}}$, $\overline{\text{RSTVDD}}$ OUTPUT	SENSE INPUT	WDI INPUT	$\overline{\text{PFO}}$ OUTPUT
TPS3103	✓ Open drain				✓ Open drain
TPS3106		✓ Open drain	✓		
TPS3110	✓ Push-pull		✓	✓	

PACKAGE INFORMATION

T_A	DEVICE NAME		THRESHOLD VOLTAGE, V_{IT}	MARKING
−40°C to 85°C	TPS3103E12DBVR‡	TPS3103E12DBVT§	1.142 V	PFWI
	TPS3103E15DBVR‡	TPS3103E15DBVT§	1.434 V	PFXI
	TPS3103H20DBVR‡	TPS3103H20DBVT§	1.84 V	PFYI
	TPS3103K33DBVR‡	TPS3103K33DBVT§	2.941 V	PGRI
	TPS3106E09DBVR†‡	TPS3106E09DBVT§	0.86 V	PFZI
	TPS3106E16DBVR‡	TPS3106E16DBVT§	1.521 V	PGSI
	TPS3106K33DBVR‡	TPS3106K33DBVT§	2.941 V	PGBI
	TPS3110E09DBVR‡	TPS3110E09DBVT§	0.86 V	PGII
	TPS3110E12DBVR‡	TPS3110E12DBVT§	1.142 V	PGJI
	TPS3110E15DBVR‡	TPS3110E15DBVT§	1.434 V	PGKI
	TPS3110K33DBVR†‡	TPS3110K33DBVT§	2.941 V	PGLI

† TPS3106E09 and TPS3110K33 will be available in August 2001; all other versions will be available in October 2001.
‡ The DBVR passive indicates tape and reel of 3000 parts.
§ The DBVT passive indicates tape and reel of 250 parts.

ordering information

TPS31 03 E 15 DBV R

- TPS31 — Family
- 03 — Functionality
- E — Typical Reset Threshold Voltage
- 15 — Nominal Supply Voltage
- DBV — Package
- R — Reel

DEVICE NAME	NOMINAL SUPPLY VOLTAGE, $V_{N(dc)}$	DEVICE NAME	TYPICAL $\overline{RESET}$ THRESHOLD VOLTAGE, V_{IT}
TPS310xx09DBV TPS311xx09DBV	0.9 V	TPS310XEXXDBV TPS311XEXXDBV	$V_{N(dc)}$ − 5%
TPS310xx12DBV TPS311xx12DBV	1.2 V	TPS310XHXXDBV	$V_{N(dc)}$ − 8%
TPS310xx15DBV TPS311xx15DBV	1.5 V	TPS310XKXXDBV TPS311XKXXDBV	$V_{N(dc)}$ − 11%
TPS310xx16DBV	1.6 V		
TPS310xx20DBV	2 V		
TPS310xx33DBV- TPS311xx33DBV	3.3 V		

Function Tables

TPS3110†

$\overline{MR}$	$V_{(SENSE)} > 0.551$ V	$V_{DD} > V_{IT}$	$\overline{RESET}$
L	x	x	L
H	0	0	L
H	0	1	L
H	1	0	L
H	1	1	H

† Function of watchdog-timer not shown
x = Don’t care

TPS3103

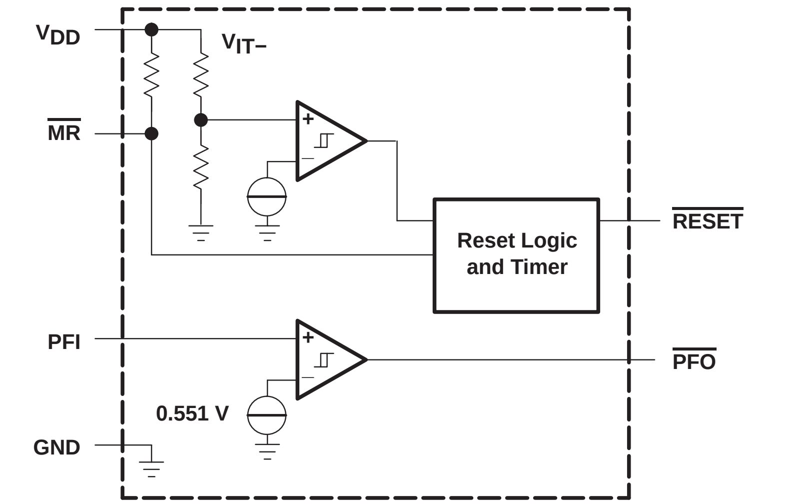
$\overline{MR}$	$V_{(PFI)} > 0.551$ V	$V_{DD} > V_{IT}$	$\overline{RESET}$	$\overline{PFO}$
L	0	x	L	L
L	1	x	L	H
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

TPS3106

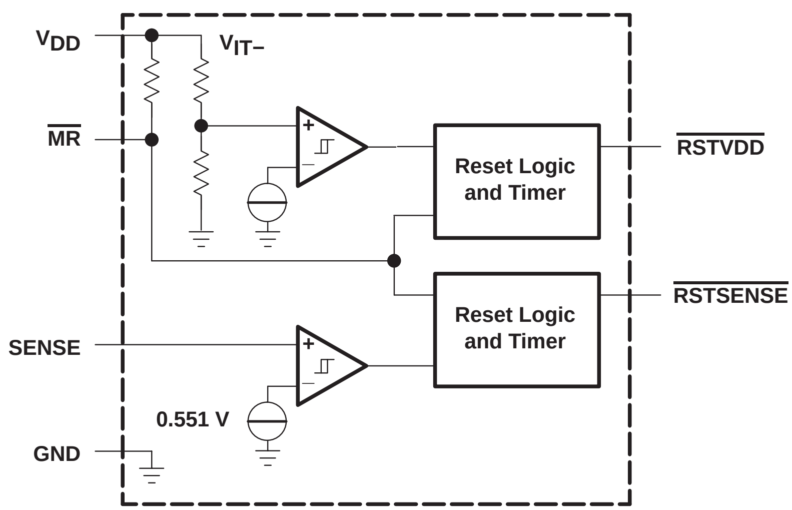
$\overline{MR}$	$V_{(SENSE)} > 0.551$ V	$V_{DD} > V_{IT}$	$\overline{RSTVDD}$	$\overline{RSTSENSE}$
L	x	x	L	L
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

functional block diagram

TPS3103

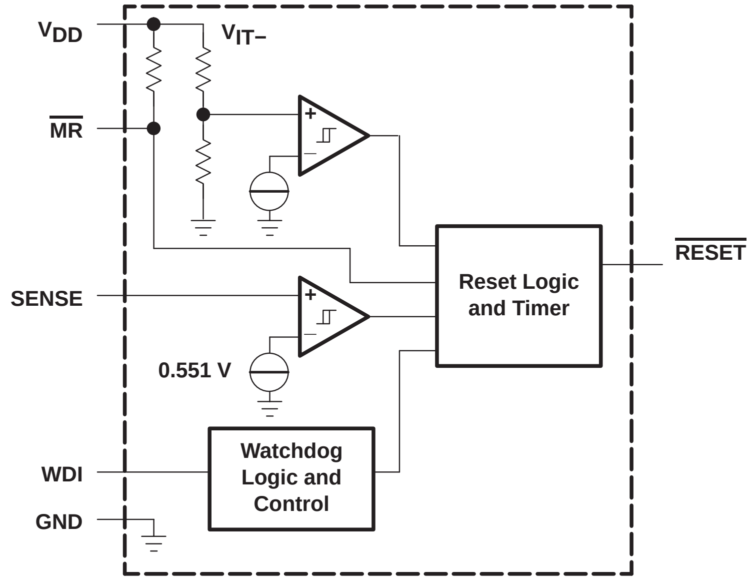


TPS3106



functional block diagram (continued)

TPS3110



timing diagram

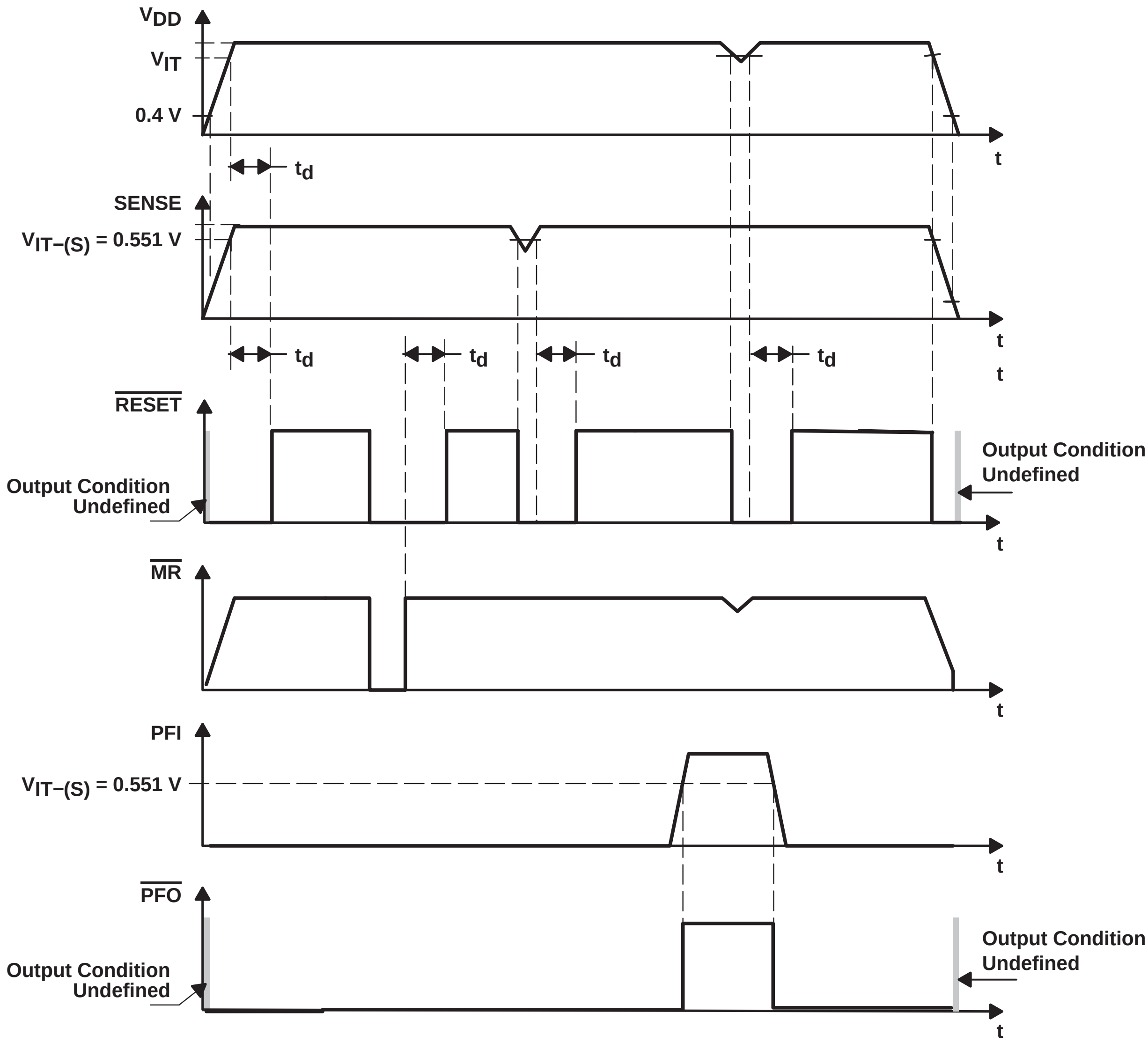


Figure 1. Timing Diagram for TPS3103

timing diagram

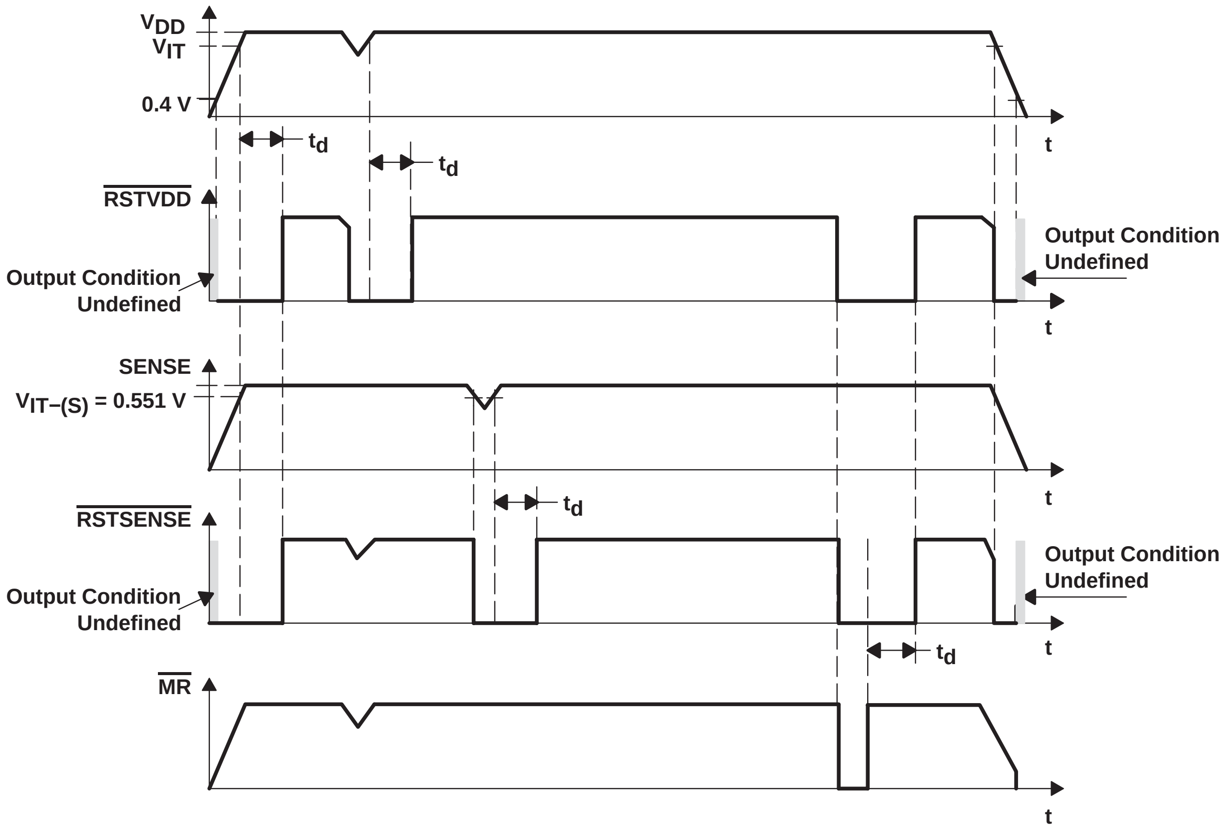


Figure 2. Timing Diagram for TPS3106

timing diagram

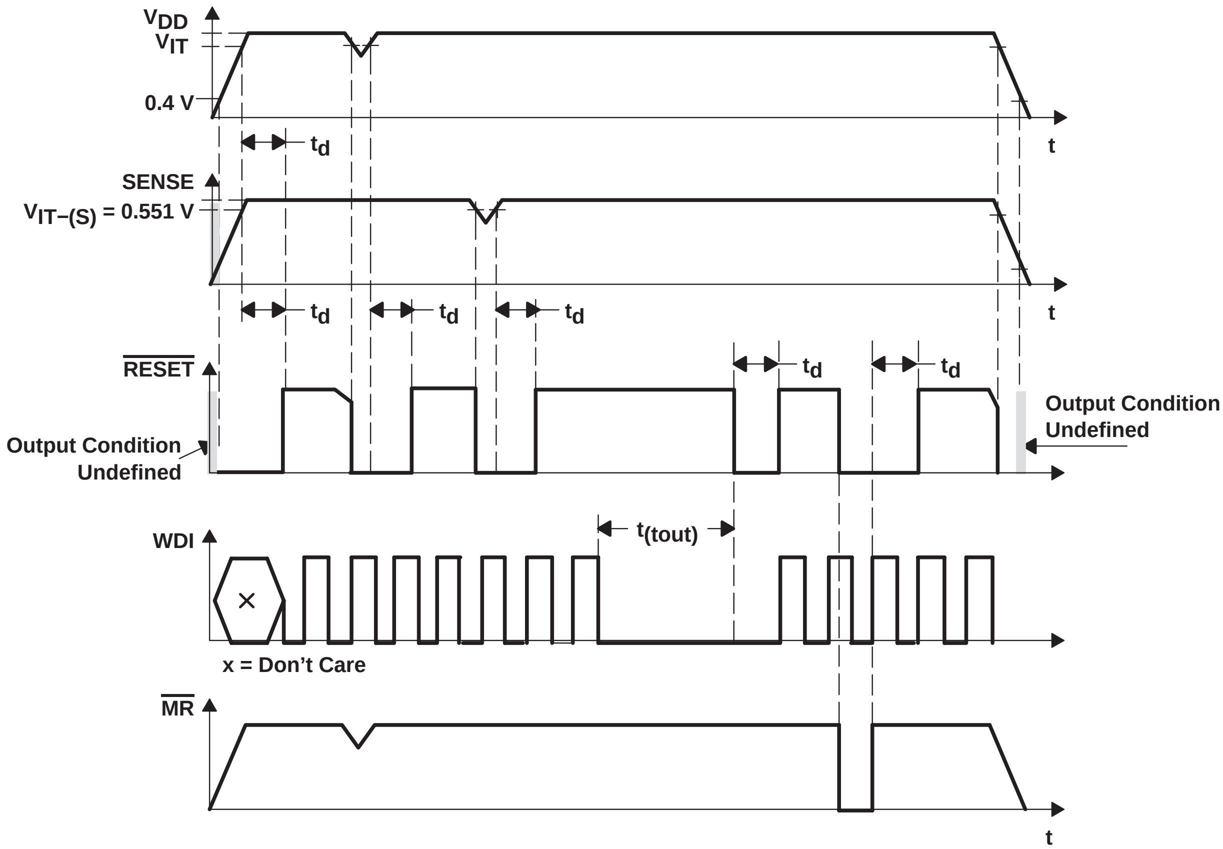


Figure 3. Timing Diagram for TPS3110

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	PART	NO.		
GND	ALL	2		GND
$\overline{\text{MR}}$	ALL	3	I	Manual-reset input. Pull low to force a reset. $\overline{\text{RESET}}$ remains low as long as $\overline{\text{MR}}$ is low and for the timeout period after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to V_{DD} when unused.
PFI	TPS3103	4	I	Power-fail input compares to 0.551 V with no additional delay. Connect to V_{DD} if not used.
$\overline{\text{PFO}}$	TPS3103	5	O	Power-fail output. Goes high when voltage at PFI rises above 0.551 V.
$\overline{\text{RESET}}$	TPS3103 TPS3110	1	O	Active-low reset output. Either push-pull or open-drain output stage
$\overline{\text{RSTSENSE}}$	TPS3106	5	O	Active-low reset output. Logic level at $\overline{\text{RSTSENSE}}$ only depends on the voltage at SENSE and the status of $\overline{\text{MR}}$.
$\overline{\text{RSTVDD}}$	TPS3106	1	O	Active-low reset output. Logic level at $\overline{\text{RSTVDD}}$ only depends on the voltage at V_{DD} and the status of $\overline{\text{MR}}$.
SENSE	TPS3106 TPS3110	4 4	I	A reset will be asserted if the voltage at SENSE is lower than 0.551 V. Connect to V_{DD} if unused
V_{DD}	ALL	6		Supply voltage. Powers the device and monitors its own voltage
WDI	TPS3110	5	I	Watchdog timer input. If WDI remains high or low longer than the time-out period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge.

detailed description

watchdog

The TPS3110 device integrates a watchdog timer that must be periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, RESET becomes active for the time period (t_d). This event also reinitializes the watchdog timer.

manual reset ($\overline{\text{MR}}$)

Many µC-based products require manual-reset capability, allowing an operator or logic circuitry to initiate a reset. Logic low at $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low and for a time period (t_d) after $\overline{\text{MR}}$ returns high. The input has an internal 100-kΩ pull-up resistor, so it can be left open if it is unused.

Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual reset function. External debounce is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in noisy environments, connecting a 0.1-µF capacitor from $\overline{\text{MR}}$ to GND provides additional noise immunity.

PFI, $\overline{\text{PFO}}$

The TPS3103 has an integrated power-fail (PFI) comparator with a separate open drain ($\overline{\text{PFO}}$) output can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail input (PFI) will be compared with an internal voltage reference of 0.551 V. If the input voltage falls below the power-fail threshold ($V_{IT-(S)}$), the power-fail output ($\overline{\text{PFO}}$) goes low. If it goes above 0.551 V plus approximately 15-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltage above 0.551 V. The sum of both resistors should be approximately 1 MΩ, to minimize power consumption and to assure that the current into the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to GND and leave $\overline{\text{PFO}}$ unconnected. For proper operation of the PFI-comparator the supply voltage (V_{DD}) must be higher than 0.8 V.

SENSE

The voltage at the SENSE input is compared with a reference voltage of 0.551 V. If the voltage at SENSE falls below the sense-threshold ($V_{IT-(S)}$), reset is asserted. On the TPS3106, a dedicated $\overline{\text{RSTSENSE}}$ output is available. On the TPS3110, the logic signal from SENSE is OR-wired with the logic signal from V_{DD} or $\overline{\text{MR}}$. An internal timer delays the return of the output to the inactive state, once the voltage at SENSE goes above 0.551 V plus about 15 mV of hysteresis. For proper operation of the SENSE-comparator, the supply voltage must be higher than 0.8 V.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE (UNLESS OTHERWISE NOTED)(1)

Supply voltage, V_{DD} (2) . . . . 3.6 V
All other pins (2) . . . . −0.3 V to 3.6 V
Maximum low output current, I_{OL} . . . . 5 mA
Maximum high output current, I_{OH} . . . . −5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . ±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . ±10 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Soldering temperature . . . . 260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 3.6 V for more than t=1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD} (1)	0.4	3.3	V
Input voltage, V_I	0	$V_{DD} + 0.3$	V
High-level input voltage, V_{IH} at $\overline{\text{MR}}$, WDI	$0.7 \times V_{DD}$		V
Low-level input voltage, V_{IL} at $\overline{\text{MR}}$, WDI		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at $\Delta t/\Delta V$ at MR, WDI		100	ns/V
Operating free-air temperature range, T_A	−40	85	°C

(1) For proper operation of SENSE, PFI, and WDI functions: $V_{DD} \ge 0.8$ V

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 3.3 V, I_{OH} = −3 mA	$0.8 \times V_{DD}$			V
			V_{DD} = 1.8 V, I_{OH} = −2 mA				
			V_{DD} = 1.5 V, I_{OH} = −1 mA				
			V_{DD} = 0.9 V, I_{OH} = −0.4 mA				
			V_{DD} = 0.5 V, I_{OH} = −5 μA	$0.7 \times V_{DD}$			
V_{OL}	Low-level output voltage		V_{DD} = 3.3 V, I_{OL} = 3 mA			0.3	V
			V_{DD} = 1.5 V, I_{OL} = 2 mA				
			V_{DD} = 1.2 V, I_{OL} = 1 mA				
			V_{DD} = 0.9 V, I_{OL} = 500 μA				
		$\overline{\text{RESET}}$ only	V_{DD} = 0.4 V, I_{OL} = 5 μA			0.1	
V_{IT-}	Negative-going input threshold voltage (1)	TPS31xxE09	T_A = 25°C	0.854	0.86	0.866	V
		TPS31xxE12		1.133	1.142	1.151	
		TPS31xxE15		1.423	1.434	1.445	
		TPS31xxE16		1.512	1.523	1.534	
		TPS31xxH20		1.829	1.843	1.857	
		TPS31xxK33		2.919	2.941	2.963	
$V_{IT-(S)}$	Negative-going input threshold voltage (1)	SENSE, PFI	$V_{DD} \geq 0.8$ V, T_A = 25°C	0.542	0.551	0.559	V
V_{hys}	Hysteresis at V_{DD} input		0.8 V ≤ V_{IT} < 1.5 V		20		mV
			1.6 V ≤ V_{IT} < 2.4 V		30		
			2.5 V ≤ V_{IT} < 3.3 V		50		
$T_{(K)}$	Temperature coefficient of V_{IT-}, PFI, SENSE		T_A = −40°C to 85°C		−0.012	−0.019	%/K
V_{hys}	Hysteresis at SENSE, PFI input		$V_{DD} \geq 0.8$ V		15		mV
I_{IH}	High-level input current	$\overline{\text{MR}}$	$\overline{\text{MR}} = V_{DD}$, V_{DD} = 3.3 V	−25		25	nA
		SENSE, PFI, WDI	SENSE, PFI, WDI = V_{DD}, V_{DD} = 3.3 V	−25		25	
I_{IL}	Low-level input current	$\overline{\text{MR}}$	$\overline{\text{MR}}$ = 0 V, V_{DD} = 3.3 V	−47	−33	−25	μA
		SENSE, PFI, WDI	SENSE, PFI, WDI = 0 V, V_{DD} = 3.3 V	−25		25	nA
I_{OH}	High-level output current at $\overline{\text{RESET}}$ (2)	Open drain	$V_{DD} = V_{IT}$ + 0.2 V, V_{OH} = 3.3 V			200	nA
I_{DD}	Supply current		$V_{DD} > V_{IT}$ (average current), V_{DD} < 1.8 V		1.2	3	μA
			$V_{DD} > V_{IT}$ (average current), V_{DD} > 1.8 V		2	4.5	
			$V_{DD} < V_{IT}$, V_{DD} < 1.8 V			22	
			$V_{DD} < V_{IT}$, V_{DD} > 1.8 V			27	
	Internal pull-up resistor at $\overline{\text{MR}}$			70	100	130	kΩ
C_i	Input capacitance at $\overline{\text{MR}}$, SENSE, PFI, WDI		V_I = 0 V to V_{DD}		1		pF

(1) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed close to the supply terminals.
(2) Also refers to $\overline{\text{RSTVDD}}$ and $\overline{\text{RSTSENSE}}$

TIMING REQUIREMENTS AT R_L = 1 MΩ, C_L = 50 PF, T_A = −40°C TO 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Time-out period	at WDI	V_{DD} ≥ 0.85 V	0.55	1.1	1.65	s
t_w	Pulse width	at V_{DD}	V_{IH} = 1.1 × V_{IT}, V_{IL} = 0.9 × V_{IT-}, V_{IT-} = 0.86 V	20			µs
		at $\overline{MR}$	V_{DD} ≥ V_{IT} + 0.2 V, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	0.1			
		at SENSE	V_{DD} ≥ V_{IT}, V_{IH} = 1.1 × $V_{IT-(S)}$, V_{IL} = 0.9 × $V_{IT-(S)}$	20			
		at PFI	V_{DD} ≥ 0.85 V, V_{IH} = 1.1 × $V_{IT-(S)}$,V_{IL} = 0.9 × $V_{IT-(S)}$	20			
		at WDI	V_{DD} ≥ V_{IT}, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}	0.3			

SWITCHING CHARACTERISTICS AT R_L = 1 MΩ, C_L = 50 PF, T_A = −40°C TO 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		V_{DD} ≥ 1.1 × V_{IT}, $\overline{MR}$ = 0.7 × V_{DD}, See timing diagram	65	130	195	ms
t_{PHL}	Propagation delay time, high-to-low level output	V_{DD} to $\overline{RESET}$ or $\overline{RSTVDD}$ delay	V_{IH} = 1.1 × V_{IT}, V_{IL} = 0.9 × V_{IT}			40	µs
t_{PLH}	Propagation delay time, low-to-high level output	V_{DD} to RESET or RSTVDD delay	V_{IH} = 1.1 × V_{IT}, V_{IL} = 0.9 × V_{IT}			40	
t_{PHL}	Propagation delay time, high-to-low level output	SENSE to $\overline{RESET}$ or $\overline{RSTSENSE}$ delay	V_{DD} ≥ 0.8 V, V_{IH} = 1.1 × V_{IT}, V_{IL} = 0.9 × V_{IT}			40	µs
t_{PLH}	Propagation delay time, high-to-low level output	SENSE to RESET or RSTSENSE delay	V_{DD} ≥ 0.8 V, V_{IH} = 1.1 × V_{IT}, V_{IL} = 0.9 × V_{IT}			40	µs
t_{PHL}	Propagation delay time, high-to-low level output	PFI to $\overline{PFO}$ delay	V_{DD} ≥ 0.8 V, V_{IH} = 1.1 × V_{IT}, V_{IL} = 0.9 × V_{IT}			40	µs
t_{PLH}	Propagation delay time, low-to-high level output	PFI to $\overline{PFO}$ delay	V_{DD} ≥ 0.8 V, V_{IH} = 1.1 × V_{IT}, V_{IL} = 0.9 × V_{IT}			300	µs
t_{PHL}	Propagation delay time, low-to-high level output	$\overline{MR}$ to $\overline{RESET}$. $\overline{RSTVDD}$, $\overline{RSTSENSE}$ delay	V_{DD} ≥ 1.1 × V_{IT}, V_{IL} = 0.3 × V_{DD}, V_{IH} = 0.7 × V_{DD}		1	5	µs
t_{PLH}	Propagation delay time, low-to-high level output	$\overline{MR}$ to RESET. RSTVDD, RSTSENSE delay					

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Supply current	vs Supply voltage at T_A = −40°C, 0°C, 25°C, 85°C	4
V_{OL}	Low-level output voltage	vs Low-level output current at T_A = −40°C, 0°C, 25°C, 85°C at 0.9 V, 3.3 V	5, 6
V_{OH}	High-level output voltage	vs High-level output current at T_A = −40°C, 0°C, 25°C, 85°C at 0.9 V, 3.3 V	7, 8
t_w	Minimum pulse duration at V_{DD}	vs Threshold overdrive voltage	9
V_{IT}	Normalized threshold voltage	vs Free-air temperature	10

TPS3110E09
SUPPLY CURRENT vs SUPPLY VOLTAGE

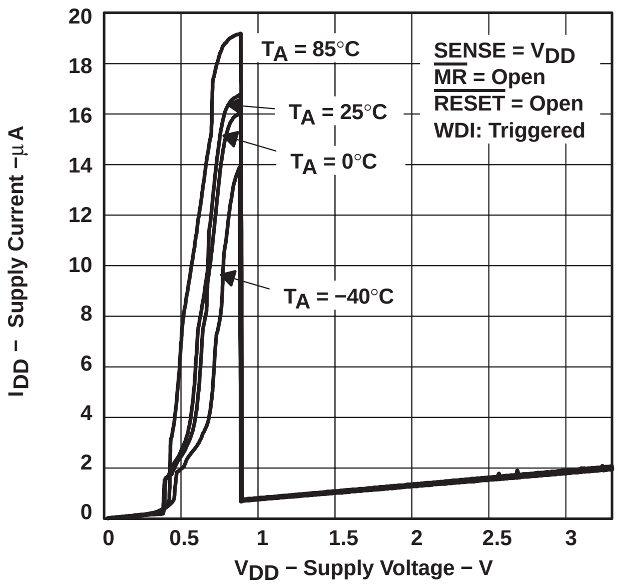


Figure 4

TPS3110E09
LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

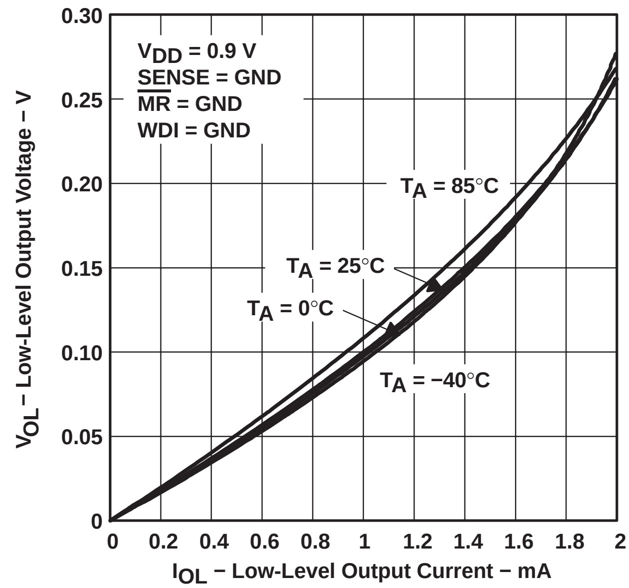


Figure 5

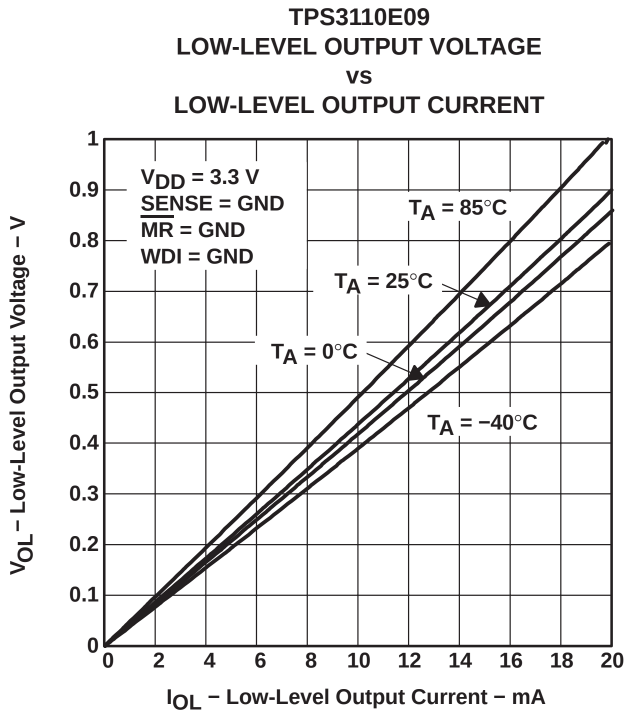


Figure 6

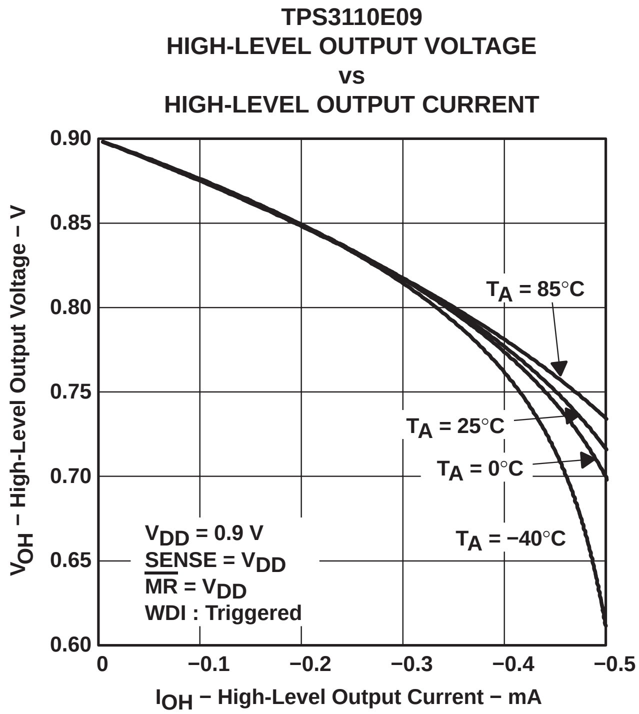


Figure 7

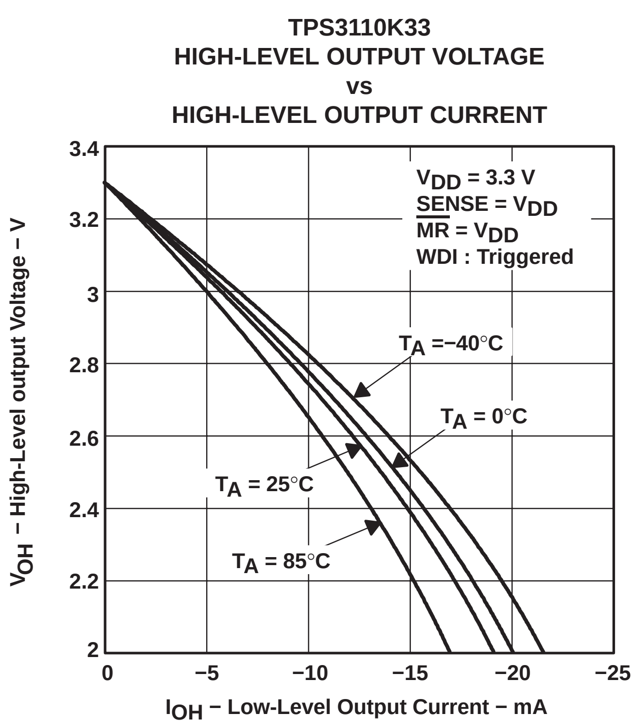


Figure 8

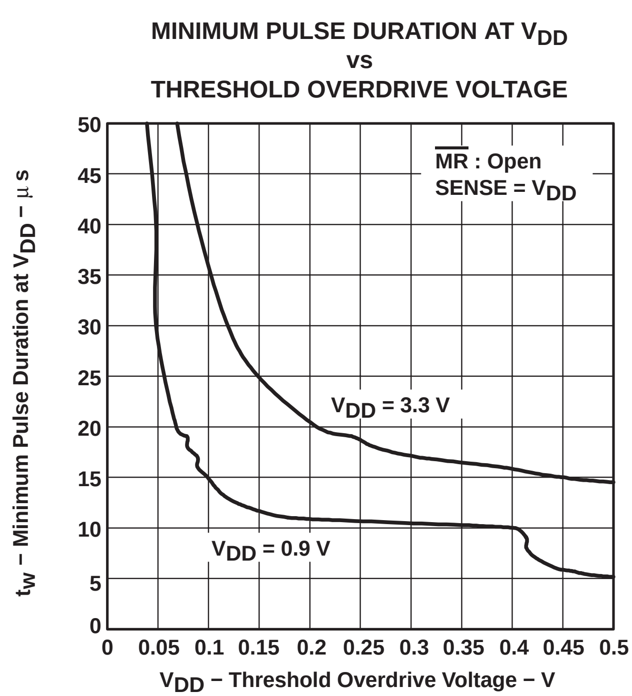


Figure 9

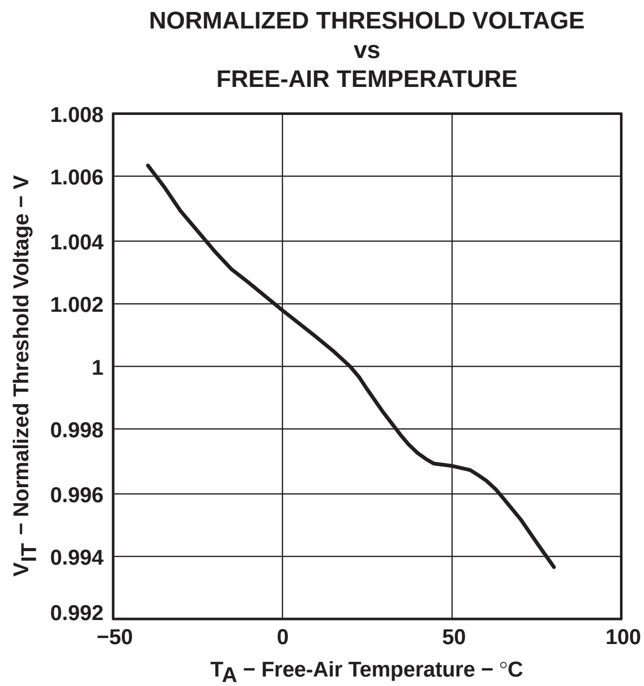


Figure 10

APPLICATION INFORMATION

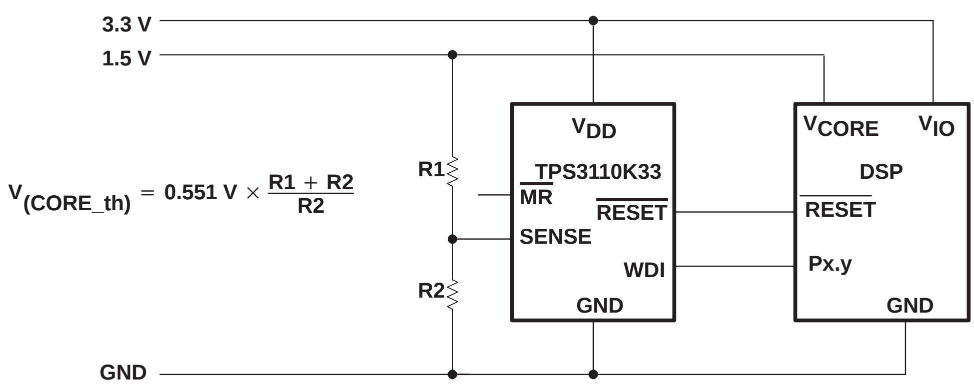
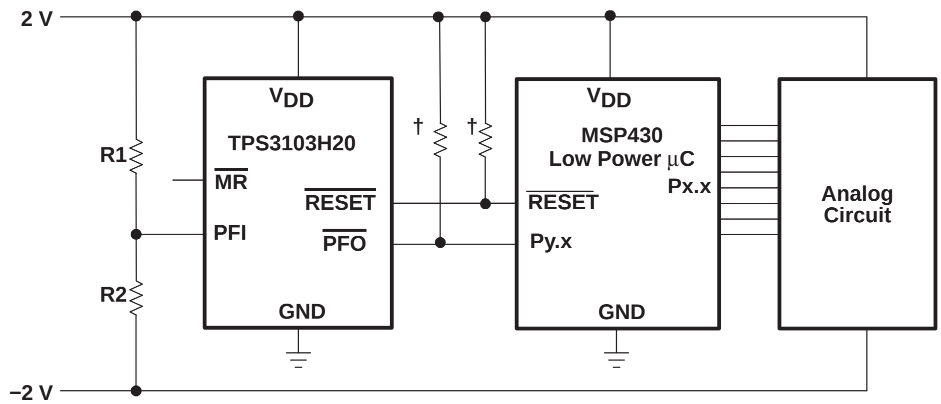


Figure 11. TPS3110 in a DSP-System Monitoring Both Supply Voltages

APPLICATION INFORMATION



$$V_{(neg\_th)} = 0.551\ V - \frac{R2}{R1}\left(V_{DD} - 0.551\ V\right)$$

† Resistor may be integrated in µC

Figure 12. TPS3103 Monitoring a Negative Voltage

APPLICATION INFORMATION

The TPS310x family has a quiescent current in the 1-µA to 2-µA range. When $\overline{\text{RESET}}$, triggered by the voltage monitored at V_{DD}, is active, the quiescent current increases to about 20 µA (see electrical characteristics).

In some applications it is necessary to minimize the quiescent current even during the reset period. This is especially true when the voltage of a battery is supervised and the $\overline{\text{RESET}}$ is used to shut down the system or for an early warning. In this case the reset condition will last for a longer period of time. Especially when the battery is discharged, the current drawn from the battery should almost be zero.

For this kind of applications the TPS3103 or TPS3106 are a good fit. To minimize current consumption it must be assured to select a version where the threshold voltage is lower than the voltage monitored at V_{DD}. The TPS3106 has two reset outputs. One output ($\overline{\text{RSTVDD}}$) is triggered from the voltage monitored at V_{DD}. The other output ($\overline{\text{RSTSENSE}}$) is triggered from the voltage monitored at SENSE. In the application shown in Figure 13, the TPS3106E09 is used to monitor the input voltage of two NiCd or NiMH cells. The threshold voltage ($V_{(th)}$ = 0.86 V) was chosen as low as possible to ensure that the supply voltage is always higher than the threshold voltage at V_{DD}. The voltage of the battery is monitored using the SENSE input. The voltage divider was calculated to assert a reset using the $\overline{\text{RSTSENSE}}$ output at 2 x 0.8 V = 1.6 V.

$$R1 = R2 \times \left(\frac{V_{TRIP}}{V_{IT(S)}} - 1\right)$$

Where:

V_{TRIP} is the voltage of the battery at which a reset is asserted
$V_{IT(S)}$ is the threshold voltage at SENSE = 0.551 V.

R1 was chosen for a resistor current in the 1-µA range.

With V_{TRIP} = 1.6 V:

$R1 \approx 1.9 \times R2$
R1 = 820 k, R2 = 430 k

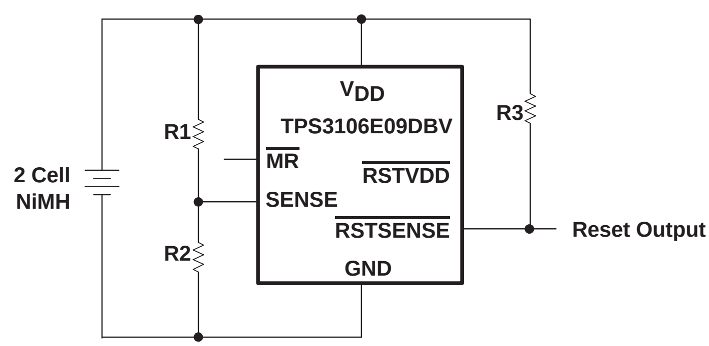
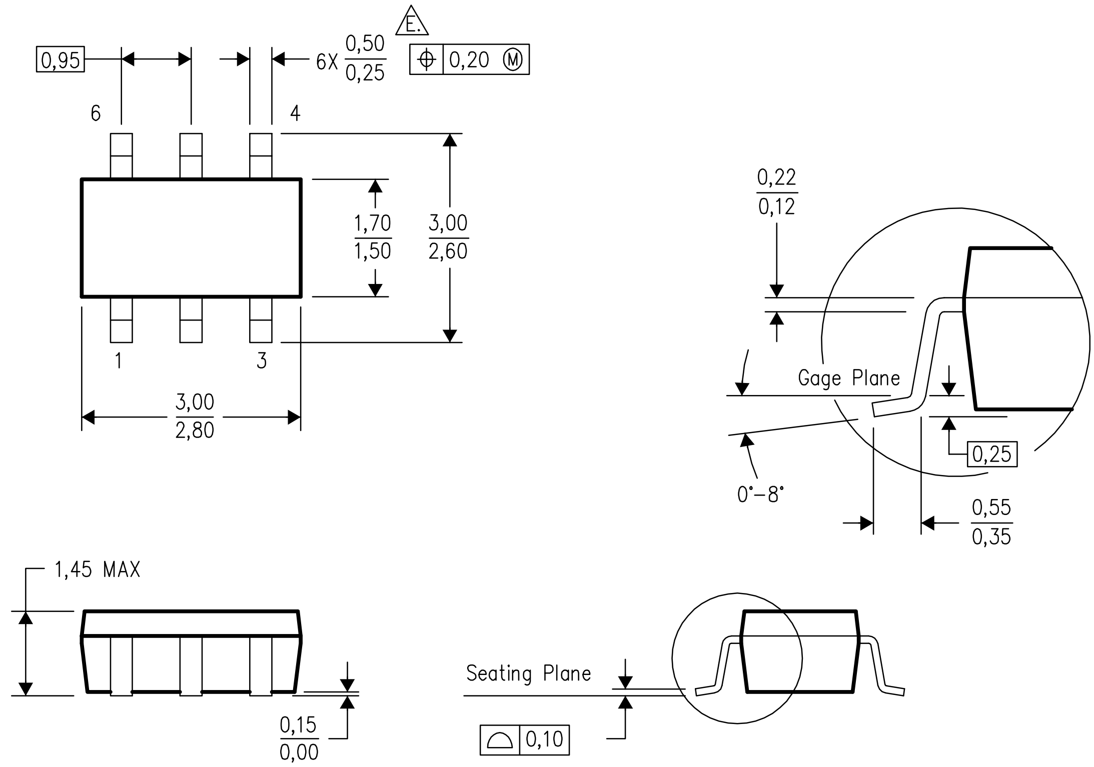


Figure 13. Battery Monitoring With 3-µA Supply Current for Device and Resistor Divider

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.