

# ULTRALOW SUPPLY-CURRENT/SUPPLY-VOLTAGE SUPERVISORY CIRCUITS

SLVS363B – AUGUST 2001 – REVISED SEPTEMBER 2004

## features

- Precision Supply Voltage Supervision  
Range: 0.9 V, 1.2 V, 1.5 V, 1.6 V, 2 V, 3.3 V
- High Trip Point Accuracy: 0.75%
- Supply Current of 1.2  $\mu$ A (Typ)
- RESET Defined With Input Voltages as Low as 0.4 V
- Power On Reset Generator With a Delay Time of 130 ms
- Push/Pull or Open-Drain  $\overline{\text{RESET}}$  Outputs
- SOT23-6 Package
- Temperature Range . . .  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

## typical applications

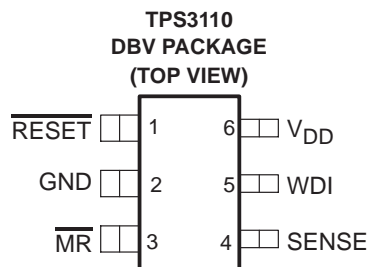
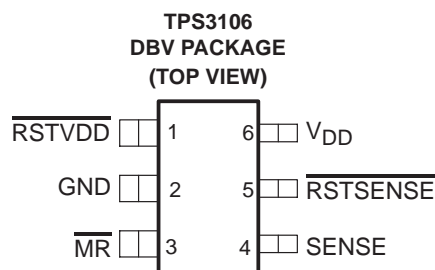
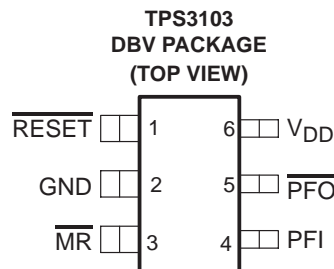
- Applications Using Low-Power DSPs, Microcontrollers or Microprocessors
- Portable/Battery-Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Programmable Controls
- Industrial Equipment
- Notebook/Desktop Computers
- Automotive Systems

## description

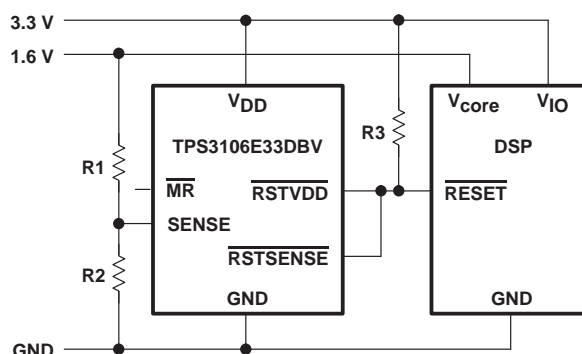
The TPS310x, TPS311x families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power on,  $\overline{\text{RESET}}$  is asserted when the supply voltage ( $V_{\text{DD}}$ ) becomes higher than 0.4 V. Thereafter, the supervisory circuit monitors  $V_{\text{DD}}$  and keeps the  $\overline{\text{RESET}}$  output active as long as  $V_{\text{DD}}$  remains below the threshold voltage ( $V_{\text{IT}}$ ). An internal timer delays the return of the output to the inactive state to ensure proper system reset. The delay time starts after  $V_{\text{DD}}$  has risen above the  $V_{\text{IT}}$ . When the  $V_{\text{DD}}$  drops below the  $V_{\text{IT}}$ , the output becomes active again.

All the devices of this family have a fixed-sense threshold voltage ( $V_{\text{IT}}$ ) set by an internal voltage divider.



## typical application circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**description (continued)**

The TPS3103 and TPS3106 have an active-low, open drain  $\overline{\text{RESET}}$  output. The TPS3110 has an active-low push/pull  $\overline{\text{RESET}}$ .

The product spectrum is designed for supply voltages of 0.9 V up to 3.3 V. The circuits are available in a 6-pin SOT-23 package. The TPS31xx family is characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**AVAILABLE OPTIONS**

DEVICE	$\overline{\text{RESET}}$ OUTPUT	$\overline{\text{RSTSENSE}}$ , $\overline{\text{RSTVDD}}$ OUTPUT	SENSE INPUT	WDI INPUT	$\overline{\text{PFO}}$ OUTPUT
TPS3103	✓ Open drain				✓ Open drain
TPS3106		✓ Open drain	✓		
TPS3110	✓ Push-pull		✓	✓	

**PACKAGE INFORMATION**

$T_A$	DEVICE NAME		THRESHOLD VOLTAGE, $V_{IT}$	MARKING
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	TPS3103E12DBVR†	TPS3103E12DBVT§	1.142 V	PFWI
	TPS3103E15DBVR†	TPS3103E15DBVT§	1.434 V	PFXI
	TPS3103H20DBVR†	TPS3103H20DBVT§	1.84 V	PFYI
	TPS3103K33DBVR†	TPS3103K33DBVT§	2.941 V	PGRI
	TPS3106E09DBVR†‡	TPS3106E09DBVT§	0.86 V	PFZI
	TPS3106E16DBVR†	TPS3106E16DBVT§	1.521 V	PGSI
	TPS3106K33DBVR†	TPS3106K33DBVT§	2.941 V	PGBI
	TPS3110E09DBVR†	TPS3110E09DBVT§	0.86 V	PGII
	TPS3110E12DBVR†	TPS3110E12DBVT§	1.142 V	PGJI
	TPS3110E15DBVR†	TPS3110E15DBVT§	1.434 V	PGKI
	TPS3110K33DBVR†‡	TPS3110K33DBVT§	2.941 V	PGLI

† TPS3106E09 and TPS3110K33 will be available in August 2001; all other versions will be available in October 2001.

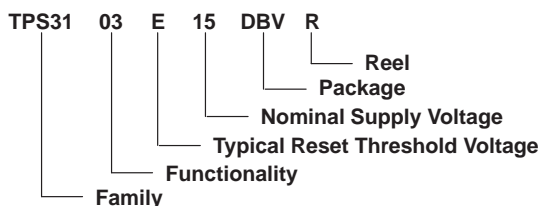
‡ The DBVR passive indicates tape and reel of 3000 parts.

§ The DBVT passive indicates tape and reel of 250 parts.

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## ordering information



DEVICE NAME	NOMINAL SUPPLY VOLTAGE, $V_{N(dc)}$	DEVICE NAME	TYPICAL RESET THRESHOLD VOLTAGE, $V_{IT}$
TPS310xx09DBV TPS311xx09DBV	0.9 V	TPS310XEXXDBV TPS311XEXXDBV	$V_{N(dc)} - 5\%$
TPS310xx12DBV TPS311xx12DBV	1.2 V	TPS310XHXXDBV	$V_{N(dc)} - 8\%$
TPS310xx15DBV TPS311xx15DBV	1.5 V	TPS310KXXDBV TPS311KXXDBV	$V_{N(dc)} - 11\%$
TPS310xx16DBV	1.6 V		
TPS310xx20DBV	2 V		
TPS310xx33DBV- TPS311xx33DBV	3.3 V		

## Function Tables

TPS3110†

$\overline{MR}$	$V_{(SENSE)} > 0.551 \text{ V}$	$V_{DD} > V_{IT}$	$\overline{RESET}$
L	x	x	L
H	0	0	L
H	0	1	L
H	1	0	L
H	1	1	H

† Function of watchdog-timer not shown  
x = Don't care

TPS3103

$\overline{MR}$	$V_{(PFI)} > 0.551 \text{ V}$	$V_{DD} > V_{IT}$	$\overline{RESET}$	$\overline{PFO}$
L	0	x	L	L
L	1	x	L	H
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

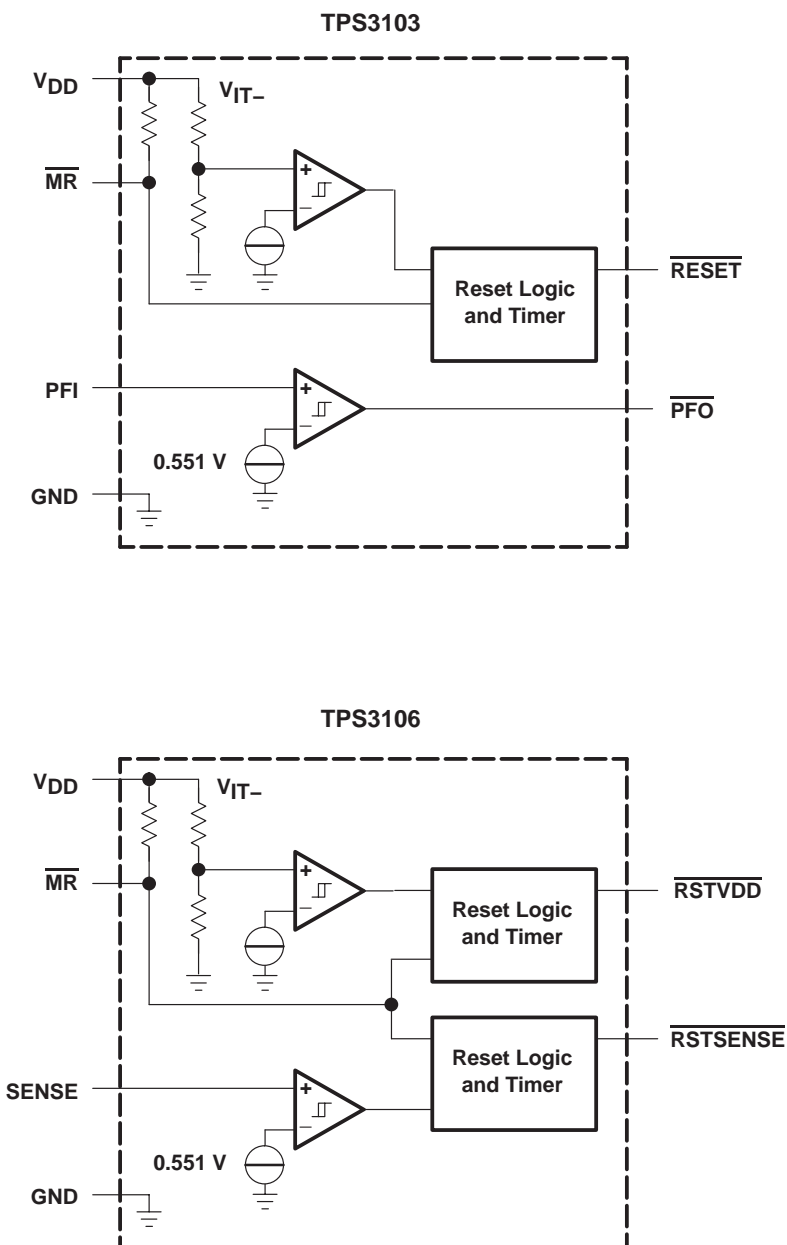
TPS3106

$\overline{MR}$	$V_{(SENSE)} > 0.551 \text{ V}$	$V_{DD} > V_{IT}$	$\overline{RSTVDD}$	$\overline{RSTSENSE}$
L	x	x	L	L
H	0	0	L	L
H	0	1	H	L
H	1	0	L	H
H	1	1	H	H

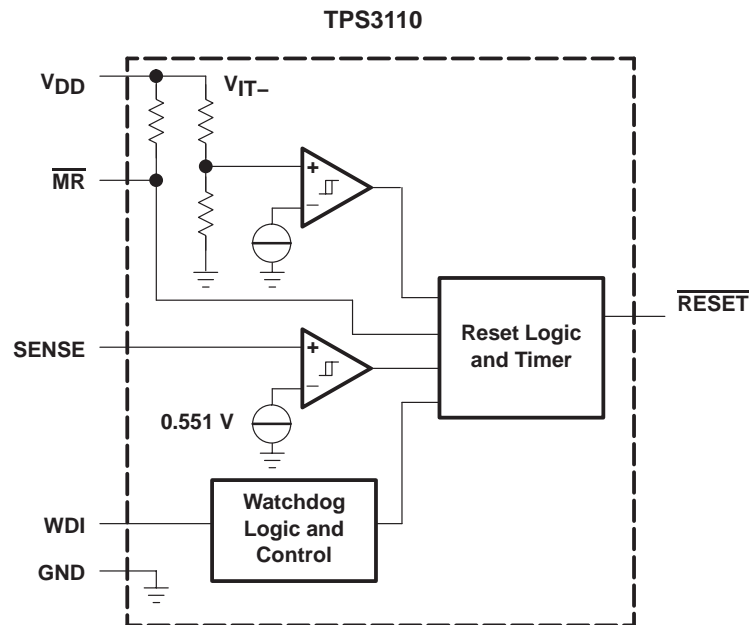
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## functional block diagram

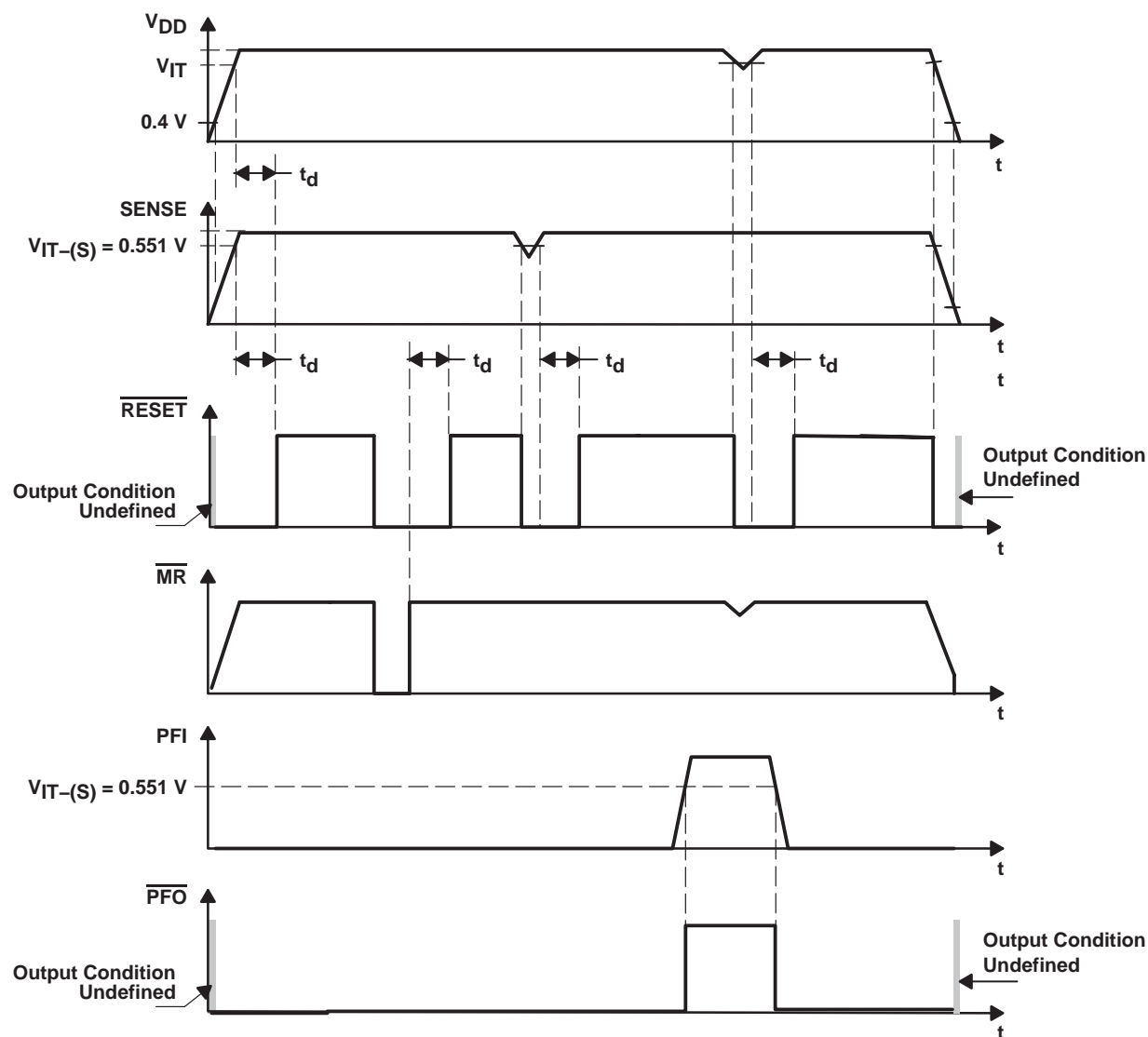


functional block diagram (continued)



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**timing diagram****Figure 1. Timing Diagram for TPS3103**

timing diagram

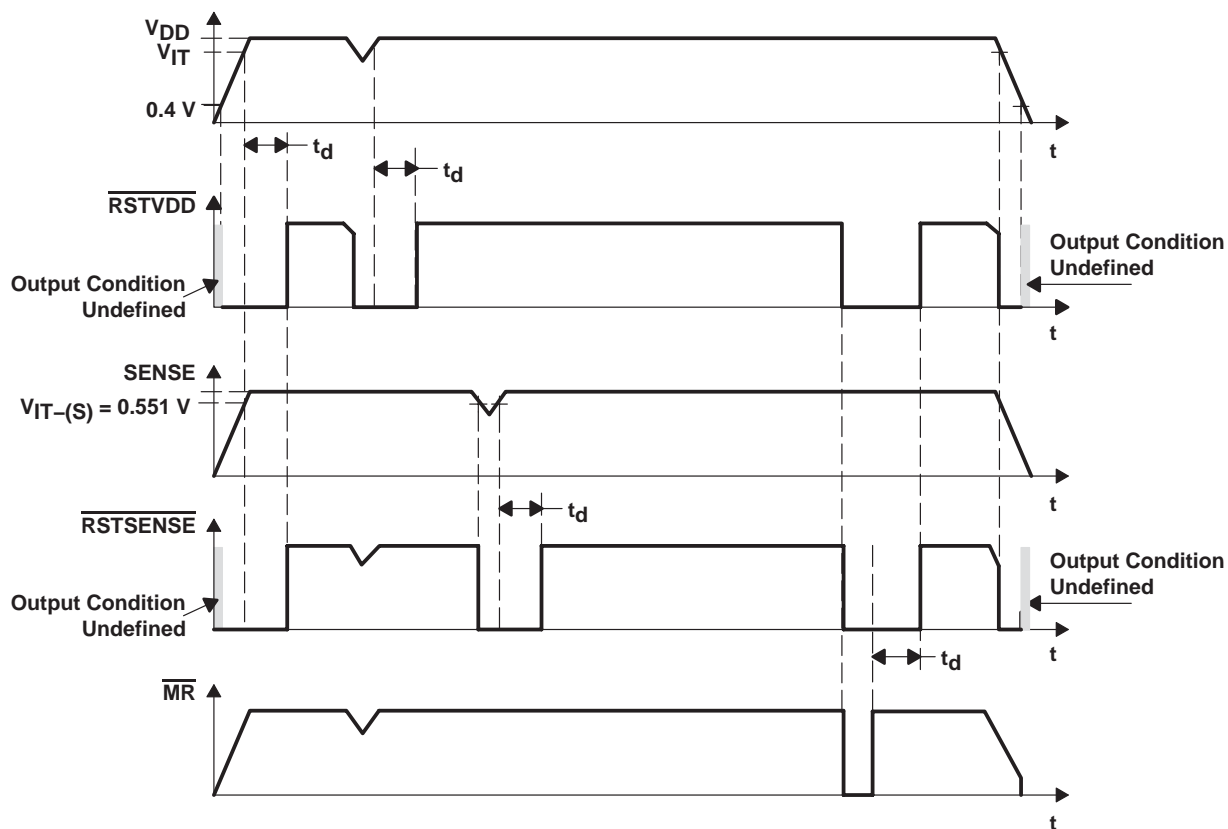
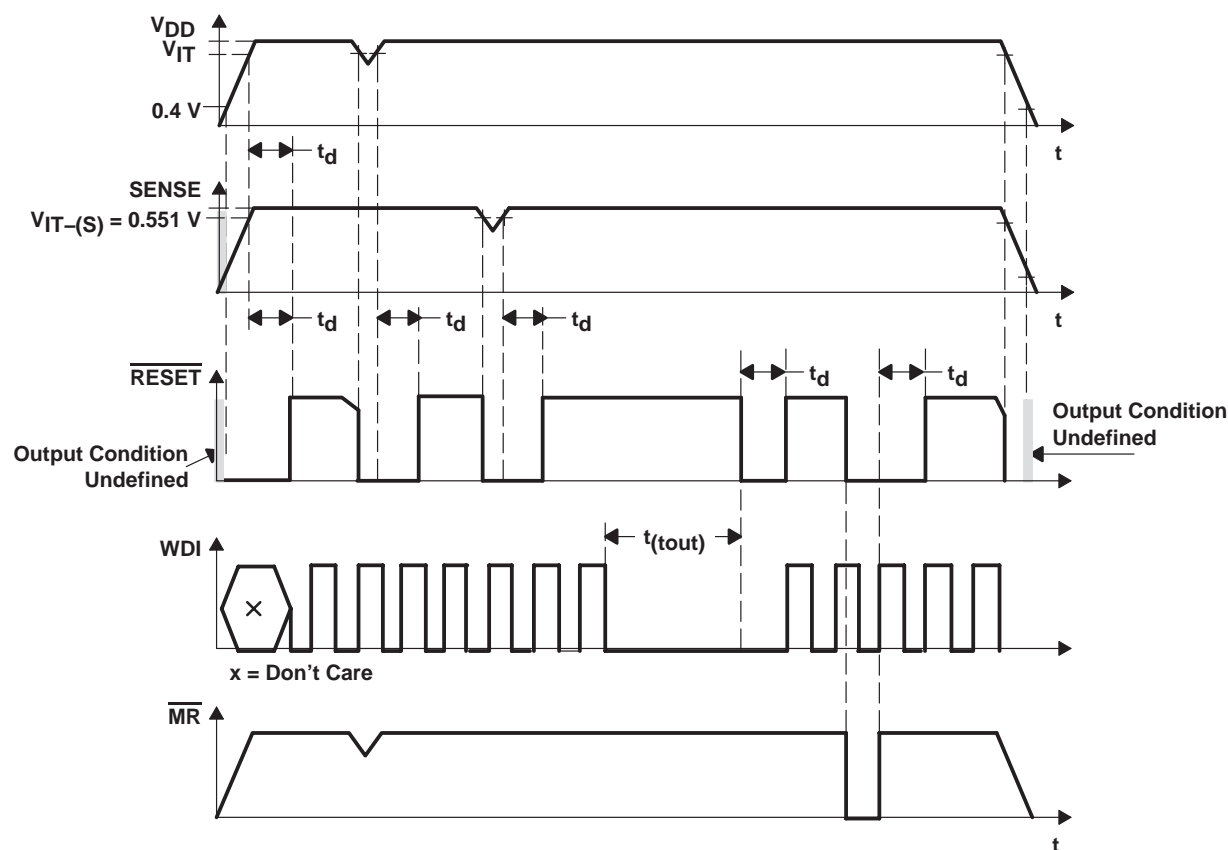


Figure 2. Timing Diagram for TPS3106

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**timing diagram****Figure 3. Timing Diagram for TPS3110**



### Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	PART	NO.		
GND	ALL	2		GND
$\overline{\text{MR}}$	ALL	3	I	Manual-reset input. Pull low to force a reset. $\overline{\text{RESET}}$ remains low as long as $\overline{\text{MR}}$ is low and for the timeout period after $\overline{\text{MR}}$ goes high. Leave unconnected or connect to $V_{\text{DD}}$ when unused.
PFI	TPS3103	4	I	Power-fail input compares to 0.551 V with no additional delay. Connect to $V_{\text{DD}}$ if not used.
$\overline{\text{PFO}}$	TPS3103	5	O	Power-fail output. Goes high when voltage at PFI rises above 0.551 V.
$\overline{\text{RESET}}$	TPS3103 TPS3110	1	O	Active-low reset output. Either push-pull or open-drain output stage
$\overline{\text{RSTSENSE}}$	TPS3106	5	O	Active-low reset output. Logic level at $\overline{\text{RSTSENSE}}$ only depends on the voltage at SENSE and the status of $\overline{\text{MR}}$ .
$\overline{\text{RSTVDD}}$	TPS3106	1	O	Active-low reset output. Logic level at $\overline{\text{RSTVDD}}$ only depends on the voltage at $V_{\text{DD}}$ and the status of $\overline{\text{MR}}$ .
SENSE	TPS3106 TPS3110	4 4	I	A reset will be asserted if the voltage at SENSE is lower than 0.551 V. Connect to $V_{\text{DD}}$ if unused
$V_{\text{DD}}$	ALL	6		Supply voltage. Powers the device and monitors its own voltage
WDI	TPS3110	5	I	Watchdog timer input. If WDI remains high or low longer than the time-out period, then reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge.

### detailed description

#### watchdog

The TPS3110 device integrates a watchdog timer that must be periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, RESET becomes active for the time period ( $t_d$ ). This event also reinitializes the watchdog timer.

#### manual reset ( $\overline{\text{MR}}$ )

Many  $\mu\text{C}$ -based products require manual-reset capability, allowing an operator or logic circuitry to initiate a reset. Logic low at  $\overline{\text{MR}}$  asserts reset. Reset remains asserted while  $\overline{\text{MR}}$  is low and for a time period ( $t_d$ ) after  $\overline{\text{MR}}$  returns high. The input has an internal 100-k $\Omega$  pull-up resistor, so it can be left open if it is unused.

Connect a normally open momentary switch from  $\overline{\text{MR}}$  to GND to create a manual reset function. External debounce is not required. If  $\overline{\text{MR}}$  is driven from long cables or if the device is used in noisy environments, connecting a 0.1- $\mu\text{F}$  capacitor from  $\overline{\text{MR}}$  to GND provides additional noise immunity.

#### PFI, $\overline{\text{PFO}}$

The TPS3103 has an integrated power-fail (PFI) comparator with a separate open drain ( $\overline{\text{PFO}}$ ) output can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail input (PFI) will be compared with an internal voltage reference of 0.551 V. If the input voltage falls below the power-fail threshold ( $V_{\text{IT-(S)}}$ ), the power-fail output ( $\overline{\text{PFO}}$ ) goes low. If it goes above 0.551 V plus approximately 15-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltage above 0.551 V. The sum of both resistors should be approximately 1 M $\Omega$ , to minimize power consumption and to assure that the current into the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to GND and leave  $\overline{\text{PFO}}$  unconnected. For proper operation of the PFI-comparator the supply voltage ( $V_{\text{DD}}$ ) must be higher than 0.8 V.

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**SENSE**

The voltage at the SENSE input is compared with a reference voltage of 0.551 V. If the voltage at SENSE falls below the sense-threshold ( $V_{IT-(S)}$ ), reset is asserted. On the TPS3106, a dedicated  $\overline{RSTSENSE}$  output is available. On the TPS3110, the logic signal from SENSE is OR-wired with the logic signal from  $V_{DD}$  or  $\overline{MR}$ . An internal timer delays the return of the output to the inactive state, once the voltage at SENSE goes above 0.551 V plus about 15 mV of hysteresis. For proper operation of the SENSE-comparator, the supply voltage must be higher than 0.8 V.

**ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE (UNLESS OTHERWISE NOTED)<sup>(1)</sup>**

Supply voltage, $V_{DD}$ <sup>(2)</sup>	3.6 V
All other pins <sup>(2)</sup>	–0.3 V to 3.6 V
Maximum low output current, $I_{OL}$	5 mA
Maximum high output current, $I_{OH}$	–5 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )	$\pm 10$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )	$\pm 10$ mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	–40°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Soldering temperature	260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 3.6 V for more than  $t=1000$ h continuously.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

**recommended operating conditions**

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$ <sup>(1)</sup>	0.4	3.3	V
Input voltage, $V_I$	0	$V_{DD} + 0.3$	V
High-level input voltage, $V_{IH}$ at $\overline{MR}$ , WDI	$0.7 \times V_{DD}$		V
Low-level input voltage, $V_{IL}$ at $\overline{MR}$ , WDI		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at $\Delta t/\Delta V$ at $\overline{MR}$ , WDI		100	ns/V
Operating free-air temperature range, $T_A$	–40	85	°C

(1) For proper operation of SENSE, PFI, and WDI functions:  $V_{DD} \geq 0.8$  V

**electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level output voltage		V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = –3 mA	0.8 × V <sub>DD</sub>			V
			V <sub>DD</sub> = 1.8 V, I <sub>OH</sub> = –2 mA				
			V <sub>DD</sub> = 1.5 V, I <sub>OH</sub> = –1 mA				
			V <sub>DD</sub> = 0.9 V, I <sub>OH</sub> = –0.4 mA				
			V <sub>DD</sub> = 0.5 V, I <sub>OH</sub> = –5 μA	0.7 × V <sub>DD</sub>			
V <sub>OL</sub>	Low-level output voltage		V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 3 mA	0.3			V
			V <sub>DD</sub> = 1.5 V, I <sub>OL</sub> = 2 mA				
			V <sub>DD</sub> = 1.2 V, I <sub>OL</sub> = 1 mA				
			V <sub>DD</sub> = 0.9 V, I <sub>OL</sub> = 500 μA				
			RESET only	V <sub>DD</sub> = 0.4 V, I <sub>OL</sub> = 5 μA	0.1		
V <sub>IT–</sub>	Negative-going input threshold voltage (1)	TPS31xxE09	T <sub>A</sub> = 25°C	0.854	0.86	0.866	V
		TPS31xxE12		1.133	1.142	1.151	
		TPS31xxE15		1.423	1.434	1.445	
		TPS31xxE16		1.512	1.523	1.534	
		TPS31xxH20		1.829	1.843	1.857	
		TPS31xxK33		2.919	2.941	2.963	
V <sub>IT–(S)</sub>	Negative-going input threshold voltage (1)	SENSE, PFI	V <sub>DD</sub> ≥ 0.8 V, T <sub>A</sub> = 25°C	0.542	0.551	0.559	V
V <sub>hys</sub>	Hysteresis at V <sub>DD</sub> input		0.8 V ≤ V <sub>IT</sub> < 1.5 V	20			mV
			1.6 V ≤ V <sub>IT</sub> < 2.4 V	30			
			2.5 V ≤ V <sub>IT</sub> < 3.3 V	50			
T(K)	Temperature coefficient of V <sub>IT–</sub> , PFI, SENSE		T <sub>A</sub> = –40°C to 85°C	–0.012	–0.019		%/K
V <sub>hys</sub>	Hysteresis at SENSE, PFI input		V <sub>DD</sub> ≥ 0.8 V	15			mV
I <sub>IH</sub>	High-level input current	MR	MR = V <sub>DD</sub> , V <sub>DD</sub> = 3.3 V	–25		25	nA
		SENSE, PFI, WDI	SENSE, PFI, WDI = V <sub>DD</sub> , V <sub>DD</sub> = 3.3 V	–25		25	
I <sub>IL</sub>	Low-level input current	MR	MR = 0 V, V <sub>DD</sub> = 3.3 V	–47	–33	–25	μA
		SENSE, PFI, WDI	SENSE, PFI, WDI = 0 V, V <sub>DD</sub> = 3.3 V	–25		25	nA
I <sub>OH</sub>	High-level output current at RESET (2)	Open drain	V <sub>DD</sub> = V <sub>IT</sub> + 0.2 V, V <sub>OH</sub> = 3.3 V			200	nA
I <sub>DD</sub>	Supply current		V <sub>DD</sub> > V <sub>IT</sub> (average current), V <sub>DD</sub> < 1.8 V		1.2	3	μA
			V <sub>DD</sub> > V <sub>IT</sub> (average current), V <sub>DD</sub> > 1.8 V		2	4.5	
			V <sub>DD</sub> < V <sub>IT</sub> , V <sub>DD</sub> < 1.8 V			22	
			V <sub>DD</sub> < V <sub>IT</sub> , V <sub>DD</sub> > 1.8 V			27	
Internal pull-up resistor at MR				70	100	130	kΩ
C <sub>i</sub>	Input capacitance at MR, SENSE, PFI, WDI		V <sub>I</sub> = 0 V to V <sub>DD</sub>	1			pF

(1) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed close to the supply terminals.

(2) Also refers to RSTVDD and RSTSENSE

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**TIMING REQUIREMENTS AT  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ PF}$ ,  $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$** 

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>t(out)</sub>	Time-out period	at WDI	V <sub>DD</sub> ≥ 0.85 V	0.55	1.1	1.65	s
t <sub>w</sub>	Pulse width	at V <sub>DD</sub>	V <sub>IH</sub> = 1.1 × V <sub>IT</sub> , V <sub>IL</sub> = 0.9 × V <sub>IT−</sub> , V <sub>IT−</sub> = 0.86 V	20			μs
		at MR	V <sub>DD</sub> ≥ V <sub>IT</sub> + 0.2 V, V <sub>IL</sub> = 0.3 × V <sub>DD</sub> , V <sub>IH</sub> = 0.7 × V <sub>DD</sub>	0.1			
		at SENSE	V <sub>DD</sub> ≥ V <sub>IT</sub> , V <sub>IH</sub> = 1.1 × V <sub>IT−(S)</sub> , V <sub>IL</sub> = 0.9 × V <sub>IT−(S)</sub>	20			
		at PFI	V <sub>DD</sub> ≥ 0.85 V, V <sub>IH</sub> = 1.1 × V <sub>IT−(S)</sub> , V <sub>IL</sub> = 0.9 × V <sub>IT−(S)</sub>	20			
		at WDI	V <sub>DD</sub> ≥ V <sub>IT</sub> , V <sub>IL</sub> = 0.3 × V <sub>DD</sub> , V <sub>IH</sub> = 0.7 × V <sub>DD</sub>	0.3			

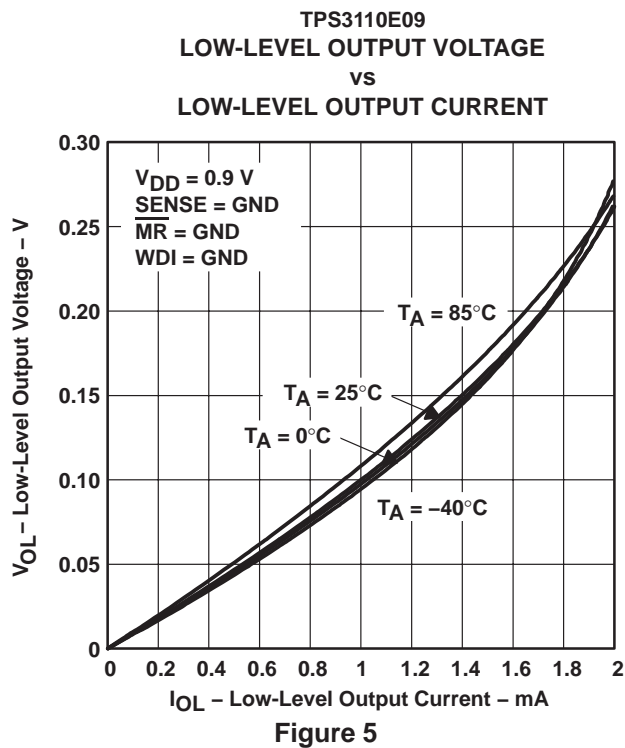
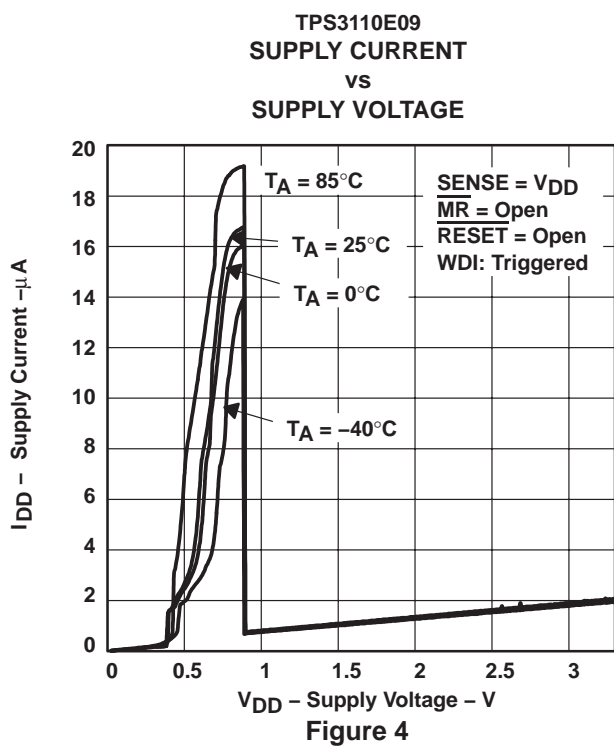
**SWITCHING CHARACTERISTICS AT  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ PF}$ ,  $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$** 

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_d$	Delay time	$V_{DD} \geq 1.1 \times V_{IT}$ , $\overline{\text{MR}} = 0.7 \times V_{DD}$ , See timing diagram	65	130	195	ms
$t_{PHL}$	Propagation delay time, high-to-low level output	$V_{DD}$ to $\overline{\text{RESET}}$ or $\overline{\text{RSTVDD}}$ delay $V_{IH} = 1.1 \times V_{IT}$ , $V_{IL} = 0.9 \times V_{IT}$			40	$\mu\text{s}$
$t_{PLH}$	Propagation delay time, low-to-high level output	$V_{DD}$ to $\overline{\text{RESET}}$ or $\overline{\text{RSTVDD}}$ delay $V_{IH} = 1.1 \times V_{IT}$ , $V_{IL} = 0.9 \times V_{IT}$			40	
$t_{PHL}$	Propagation delay time, high-to-low level output	$\overline{\text{SENSE}}$ to $\overline{\text{RESET}}$ or $\overline{\text{RSTSENSE}}$ delay $V_{DD} \geq 0.8\text{ V}$ , $V_{IH} = 1.1 \times V_{IT}$ , $V_{IL} = 0.9 \times V_{IT}$			40	$\mu\text{s}$
$t_{PLH}$	Propagation delay time, high-to-low level output	$\overline{\text{SENSE}}$ to $\overline{\text{RESET}}$ or $\overline{\text{RSTSENSE}}$ delay $V_{DD} \geq 0.8\text{ V}$ , $V_{IH} = 1.1 \times V_{IT}$ , $V_{IL} = 0.9 \times V_{IT}$			40	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high-to-low level output	PFI to $\overline{\text{PFO}}$ delay $V_{DD} \geq 0.8\text{ V}$ , $V_{IH} = 1.1 \times V_{IT}$ , $V_{IL} = 0.9 \times V_{IT}$			40	$\mu\text{s}$
$t_{PLH}$	Propagation delay time, low-to-high level output	PFI to $\overline{\text{PFO}}$ delay $V_{DD} \geq 0.8\text{ V}$ , $V_{IH} = 1.1 \times V_{IT}$ , $V_{IL} = 0.9 \times V_{IT}$			300	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, low-to-high level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ , $\overline{\text{RSTVDD}}$ , $\overline{\text{RSTSENSE}}$ delay $V_{DD} \geq 1.1 \times V_{IT}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$		1	5	$\mu\text{s}$
$t_{PLH}$	Propagation delay time, low-to-high level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ , $\overline{\text{RSTVDD}}$ , $\overline{\text{RSTSENSE}}$ delay $V_{DD} \geq 1.1 \times V_{IT}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$				

## TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
Supply current	vs Supply voltage at $T_A = -40^\circ\text{C}, 0^\circ\text{C}, 25^\circ\text{C}, 85^\circ\text{C}$		4
$V_{OL}$	Low-level output voltage	vs Low-level output current at $T_A = -40^\circ\text{C}, 0^\circ\text{C}, 25^\circ\text{C}, 85^\circ\text{C}$ at 0.9 V, 3.3 V	5, 6
$V_{OH}$	High-level output voltage	vs High-level output current at $T_A = -40^\circ\text{C}, 0^\circ\text{C}, 25^\circ\text{C}, 85^\circ\text{C}$ at 0.9 V, 3.3 V	7, 8
$t_w$	Minimum pulse duration at $V_{DD}$	vs Threshold overdrive voltage	9
$V_{IT}$	Normalized threshold voltage	vs Free-air temperature	10



## ULTRALOW SUPPLY-CURRENT/SUPPLY-VOLTAGE SUPERVISORY CIRCUITS

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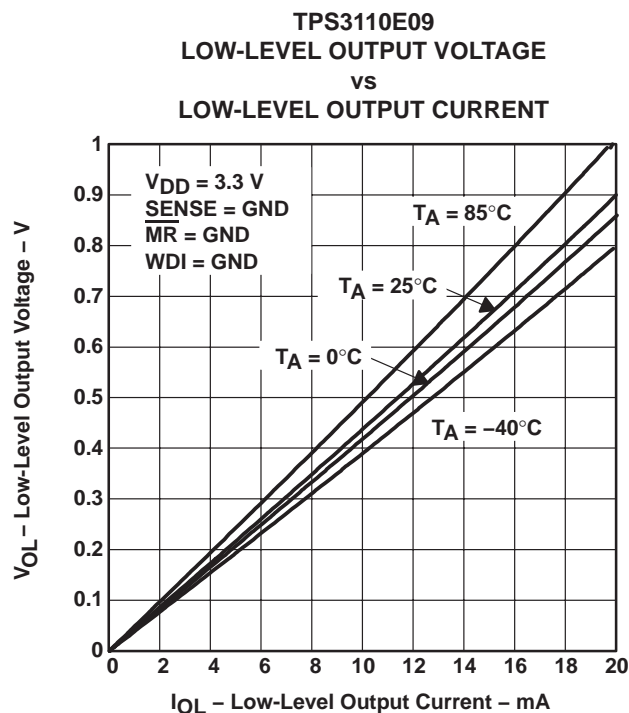


Figure 6

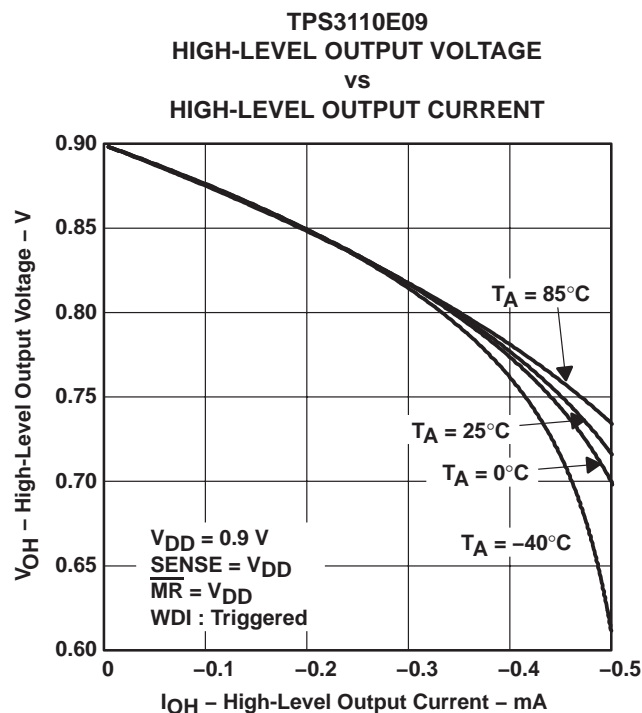


Figure 7

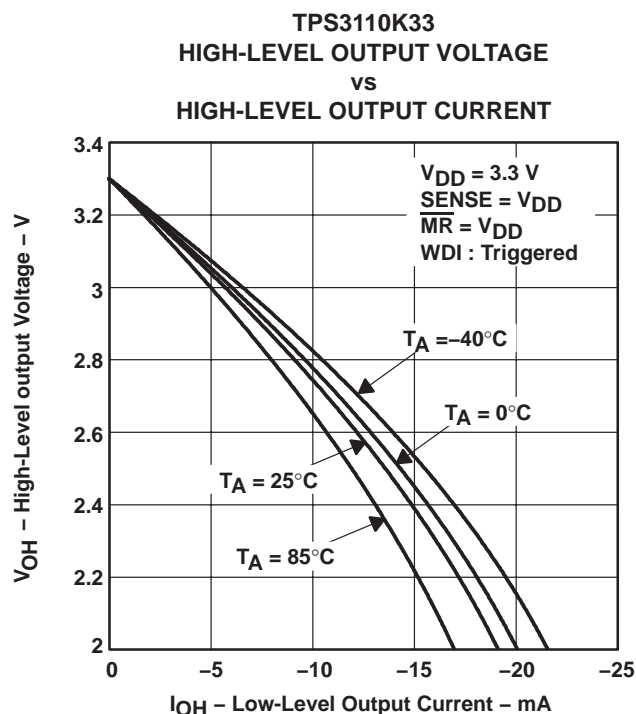


Figure 8

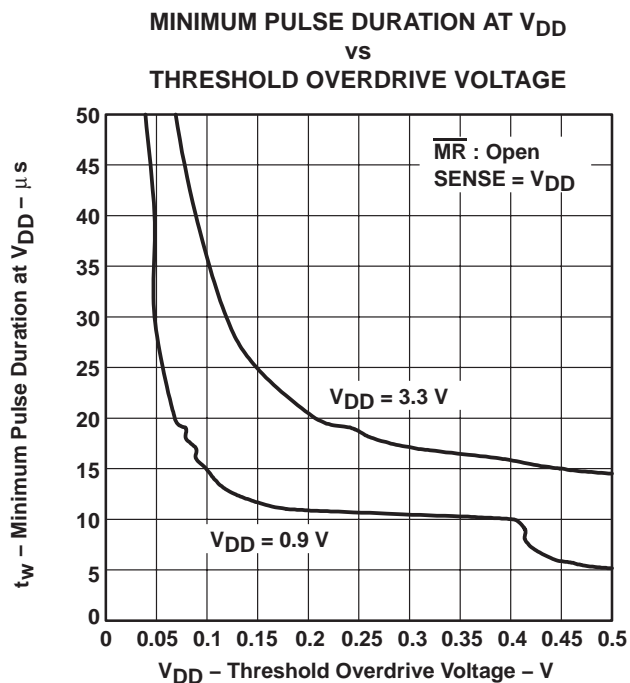


Figure 9

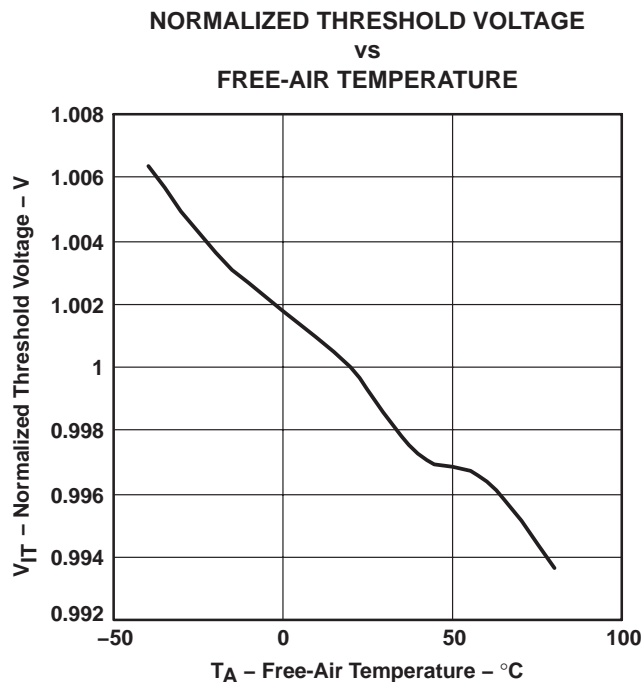


Figure 10

### APPLICATION INFORMATION

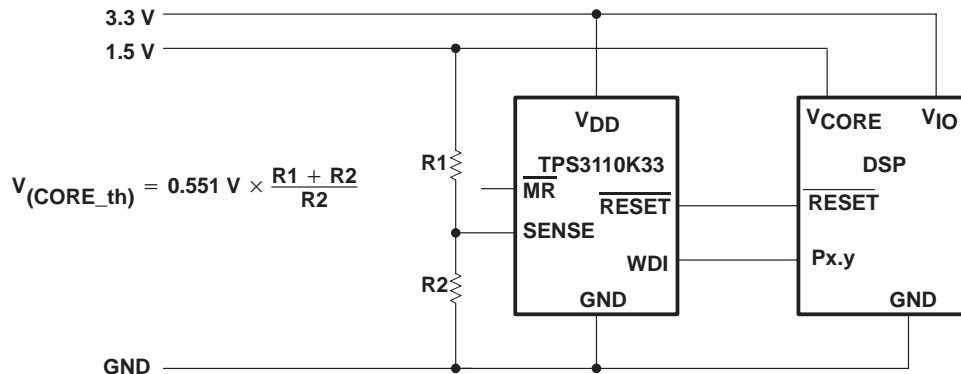
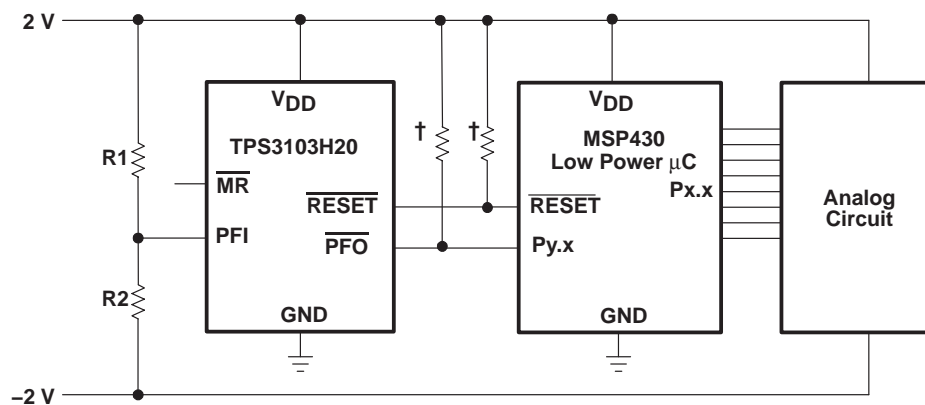


Figure 11. TPS3110 in a DSP-System Monitoring Both Supply Voltages

**ULTRALOW SUPPLY-CURRENT/SUPPLY-VOLTAGE SUPERVISORY CIRCUITS**

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**APPLICATION INFORMATION**

$$V_{(\text{neg\_th})} = 0.551 \text{ V} - \frac{R2}{R1} (V_{\text{DD}} - 0.551 \text{ V})$$

† Resistor may be integrated in  $\mu\text{C}$ **Figure 12. TPS3103 Monitoring a Negative Voltage**



## APPLICATION INFORMATION

The TPS310x family has a quiescent current in the 1- $\mu$ A to 2- $\mu$ A range. When  $\overline{\text{RESET}}$ , triggered by the voltage monitored at  $V_{DD}$ , is active, the quiescent current increases to about 20  $\mu$ A (see electrical characteristics).

In some applications it is necessary to minimize the quiescent current even during the reset period. This is especially true when the voltage of a battery is supervised and the  $\overline{\text{RESET}}$  is used to shut down the system or for an early warning. In this case the reset condition will last for a longer period of time. Especially when the battery is discharged, the current drawn from the battery should almost be zero.

For this kind of applications the TPS3103 or TPS3106 are a good fit. To minimize current consumption it must be assured to select a version where the threshold voltage is lower than the voltage monitored at  $V_{DD}$ . The TPS3106 has two reset outputs. One output ( $\overline{\text{RSTVDD}}$ ) is triggered from the voltage monitored at  $V_{DD}$ . The other output ( $\overline{\text{RSTSENSE}}$ ) is triggered from the voltage monitored at SENSE. In the application shown in Figure 13, the TPS3106E09 is used to monitor the input voltage of two NiCd or NiMH cells. The threshold voltage ( $V_{th}$ ) = 0.86 V was chosen as low as possible to ensure that the supply voltage is always higher than the threshold voltage at  $V_{DD}$ . The voltage of the battery is monitored using the SENSE input. The voltage divider was calculated to assert a reset using the  $\overline{\text{RSTSENSE}}$  output at  $2 \times 0.8 \text{ V} = 1.6 \text{ V}$ .

$$R1 = R2 \times \left( \frac{V_{TRIP}}{V_{IT(S)}} - 1 \right)$$

Where:

$V_{TRIP}$  is the voltage of the battery at which a reset is asserted

$V_{IT(S)}$  is the threshold voltage at SENSE = 0.551 V.

R1 was chosen for a resistor current in the 1- $\mu$ A range.

With  $V_{TRIP} = 1.6 \text{ V}$ :

$$R1 \approx 1.9 \times R2$$

$$R1 = 820 \text{ k}, R2 = 430 \text{ k}$$

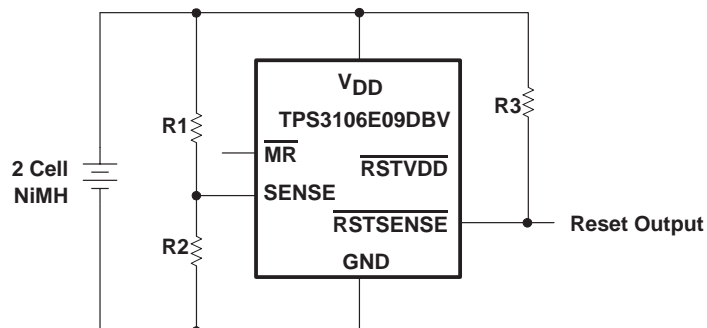
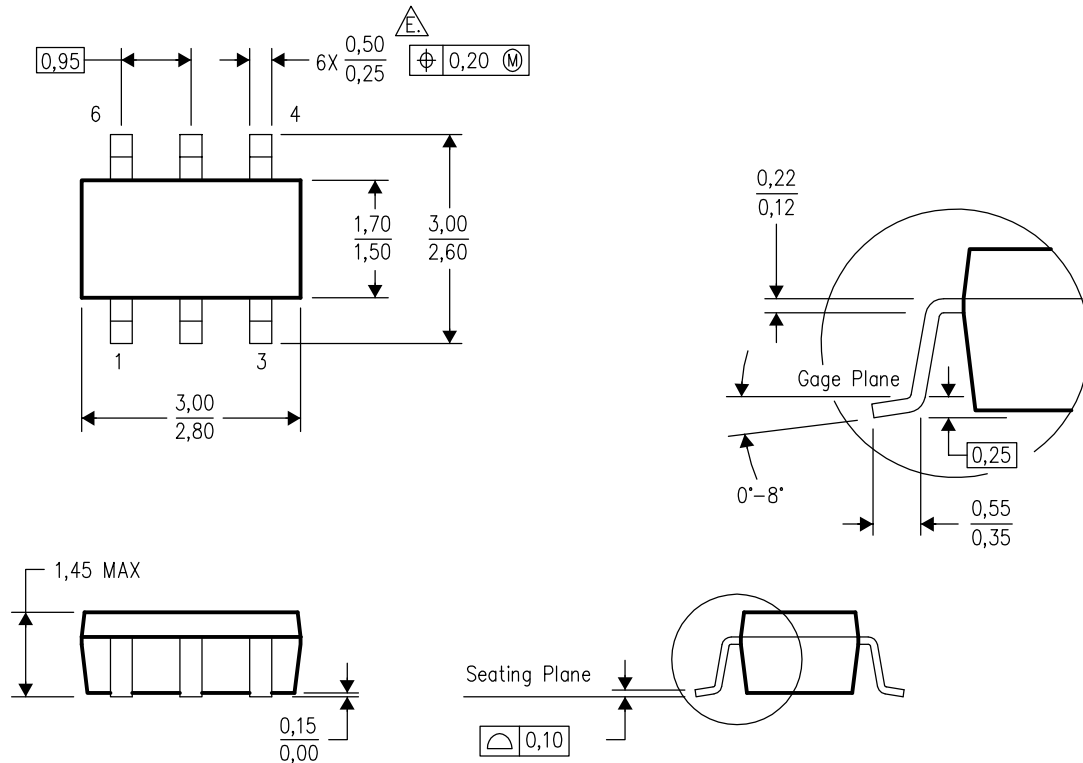



Figure 13. Battery Monitoring With 3- $\mu$ A Supply Current for Device and Resistor Divider

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-5/H 10/2003

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
-  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

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