TMS320x281x DSP Event Manager (EV) Reference Guide

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Chapter 1

Overview

The event-manager (EV) modules provide a broad range of functions and features that are particularly useful in motion control and motor control applications. The EV modules include general-purpose (GP) timers, full-compare/PWM units, capture units, and quadrature-encoder pulse (QEP) circuits. The two EV modules, EVA and EVB, are identical peripherals, intended for multi-axis/motion-control applications.

Each EV is capable of controlling three Half-H bridges, when each bridge requires a complementary PWM pair for control. Each EV also has two additional PWMs with no complementary outputs.

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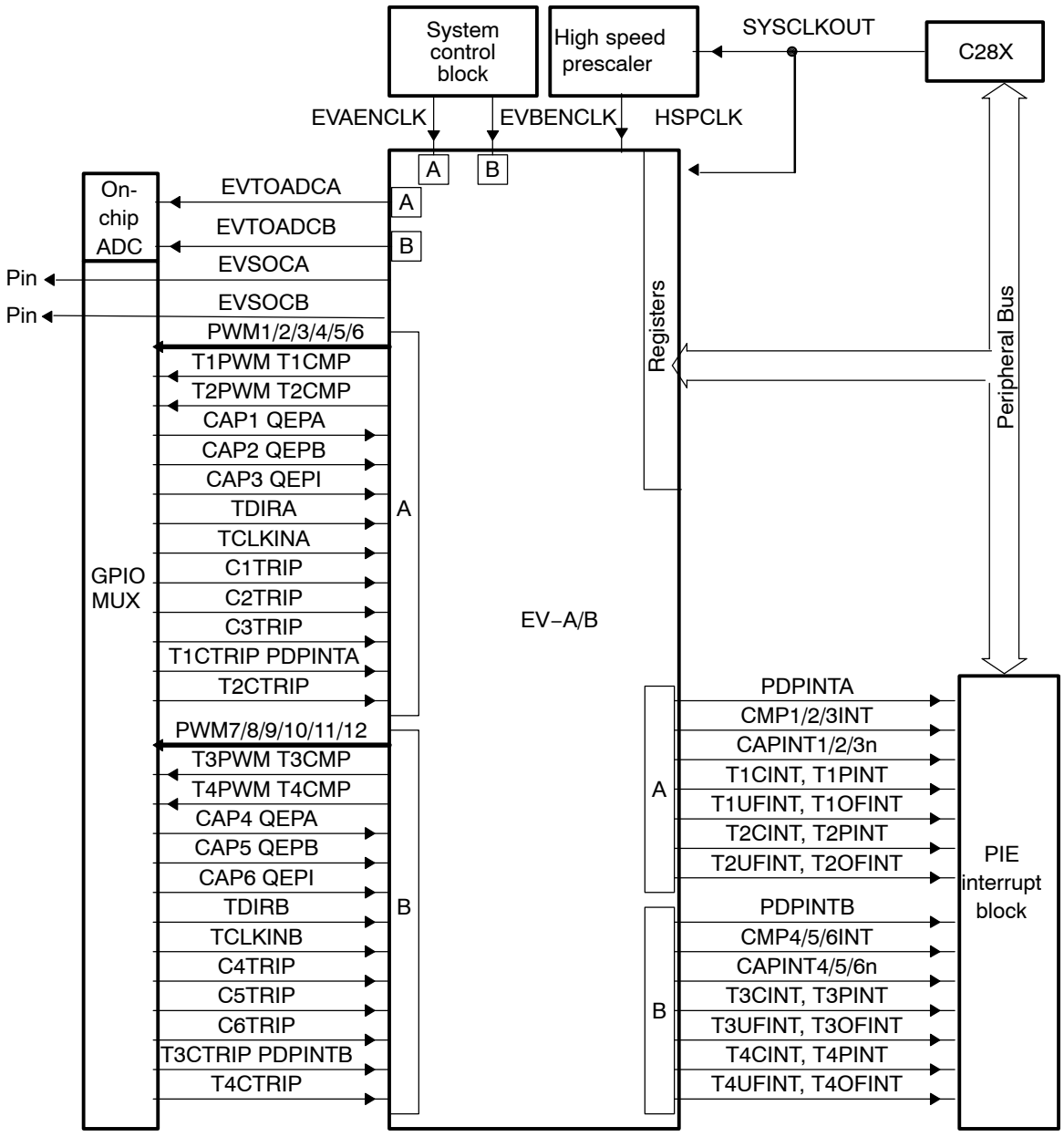
1.1 Event Manager Functions

EVA and EVB timers, compare units, and capture units function identically. However, timer/unit names differ for EVA and EVB. Table 1–1 shows the features and functionality available for the event-manager modules and highlights EVA nomenclature.

Event managers A and B have identical peripheral register sets with EVA starting at 7400h and EVB starting at 7500h. The paragraphs in this section describe the function of GP timers, compare units, capture units, and QEPs using EVA nomenclature. These paragraphs are applicable to EVB with regard to function; however, module/signal names differ.

Figure 1−1. Event Manager (EV) Device Interfaces



Note: EXTCONA is an added control register to enable and disable the added/modified features. It is required for compatibility with 240x EV. EXTCONA enables and disables the additions and modifications in features. All additions and modifications are disabled by default to keep compatibility with 240x EV. See Section 5.7 for details about the EXTCONx register.

Table 1−1. Module and Signal Names for EVA and EVB

Event Manager Modules	EVA		EVB	
	Module	**Signal**	**Module**	**Signal**
GP timers	GP Timer 1 GP Timer 2	T1PWM/T1CMP T2PWM/T2CMP	GP Timer 3 GP Timer 4	T3PWM/T3CMP T4PWM/T4CMP
Compare units	Compare 1 Compare 2 Compare 3	PWM1/2 PWM3/4 PWM5/6	Compare 4 Compare 5 Compare 6	PWM7/8 PWM9/10 PWM11/12
Capture units	Capture 1 Capture 2 Capture 3	CAP1 CAP2 CAP3	Capture 4 Capture 5 Capture 6	CAP4 CAP5 CAP6
QEP channels	QEP	QEP1 QEP2 QEPI1	QEP	QEP3 QEP4 QEP12
External timer inputs	Timer-direction external clock	TDIRA TCLKINA	Timer-direction external clock	TDIRB TCLKINB
External compare-output trip inputs	Compare	$\overline{\text{C1TRIP}}$ $\overline{\text{C2TRIP}}$ $\overline{\text{C3TRIP}}$		$\overline{\text{C4TRIP}}$ $\overline{\text{C5TRIP}}$ $\overline{\text{C6TRIP}}$
External timer-compare trip inputs		$\overline{\text{T1CTRIP}}$/ $\overline{\text{T2CTRIP}}$		$\overline{\text{T3CTRIP}}$/ $\overline{\text{T4CTRIP}}$
External trip inputs		$\overline{\text{PDPINTA}}$†		$\overline{\text{PDPINTB}}$†
External ADC SOC trigger outputs		EVASOC		EVBSOC

† In the 240x™-compatible mode, the $\overline{\text{T1CTRIP}}$/$\overline{\text{PDPINTA}}$ pin functions as $\overline{\text{PDPINTA}}$ and the $\overline{\text{T3CTRIP}}$/$\overline{\text{PDPINTB}}$ pin functions as $\overline{\text{PDPINTB}}$.

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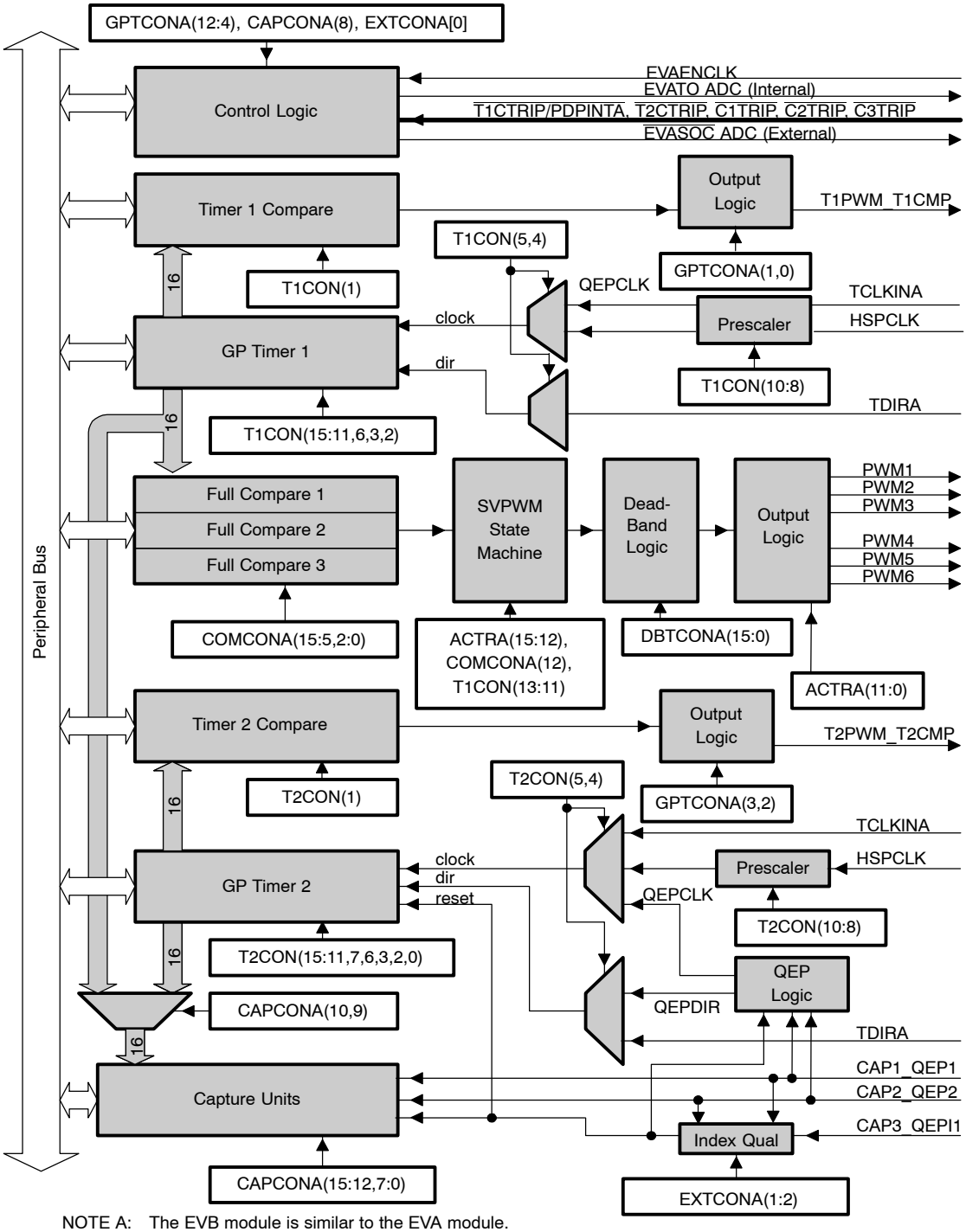
Figure 1–2. Event Manager A Functional Block Diagram



NOTE A: The EVB module is similar to the EVA module.

1.1.1 General-Purpose (GP) Timers

There are two GP timers in each EV module. The GP timer x (x = 1 or 2 for EVA; x = 3 or 4 for EVB) includes:

- A 16-bit timer, up-/down-counter, TxCNT, for reads or writes
- A 16-bit timer-compare register, TxCMPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-period register, TxPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-control register,TxCON, for reads or writes
- Selectable internal or external input clocks
- A programmable prescaler for internal or external clock inputs
- Control and interrupt logic, for four maskable interrupts: *underflow*, *overflow*, *timer compare*, and *period interrupts*
- A selectable direction input pin (TDIRx) (to count up or down when directional up-/down-count mode is selected)

The GP timers can be operated independently or synchronized with each other. The compare register associated with each GP timer can be used for compare function and PWM-waveform generation. There are three continuous modes of operations for each GP timer in up- or up/down-counting operations. Internal or external input clocks with programmable prescaler are used for each GP timer. GP timers also provide the time base for the other event-manager submodules: GP timer 1 for all the compares and PWM circuits, GP timer 2/1 for the capture units and the quadrature-pulse counting operations. Double-buffering of the period and compare registers allows programmable change of the timer (PWM) period and the compare/PWM pulse width as needed.

1.1.2 Full-Compare Units

There are three full-compare units on each event manager. These compare units use GP timer1 as the time base and generate six outputs for compare and PWM-waveform generation using programmable deadband circuit. The state of each of the six outputs is configured independently. The compare registers of the compare units are double-buffered, allowing programmable change of the compare/PWM pulse widths as needed.

1.1.3 Programmable Deadband Generator

The deadband generator circuit includes three 4-bit counters and an 16-bit compare register. Desired deadband values can be programmed into the

compare register for the outputs of the three compare units. The deadband generation can be enabled/disabled for each compare unit output individually. The deadband-generator circuit produces two outputs (with or without deadband zone) for each compare unit output signal. The output states of the deadband generator are configurable and changeable as needed by way of the double-buffered ACTRx register.

1.1.4 PWM Waveform Generation

Up to eight PWM waveforms (outputs) can be generated simultaneously by each event manager: three independent pairs (six outputs) by the three full-compare units with *programmable deadbands*, and two independent PWMs by the GP-timer compares.

1.1.5 PWM Characteristics

Characteristics of the PWMs are as follows:

- ❏ 16-bit registers
- ❏ Wide range of programmable deadband for the PWM output pairs
- ❏ Change of the PWM carrier frequency for PWM frequency wobbling as needed
- ❏ Change of the PWM pulse widths within and after each PWM period as needed
- ❏ External-maskable power and drive-protection interrupts
- ❏ Pulse-pattern-generator circuit, for programmable generation of asymmetric, symmetric, and eight-space vector PWM waveforms
- ❏ Minimized CPU overhead using auto-reload of the compare and period registers
- ❏ The PWM pins are driven to a high-impedance state when the $\overline{\text{PDPINTx}}$ pin is driven low and **after** $\overline{\text{PDPINTx}}$ signal qualification. The $\overline{\text{PDPINTx}}$ pin (after qualification) is reflected in bit 8 of the COMCONx register.
  - $\overline{\text{PDPINTA}}$ pin status is reflected in bit 8 of COMCONA register.
  - $\overline{\text{PDPINTB}}$ pin status is reflected in bit 8 of COMCONB register.

1.1.6 Capture Unit

The capture unit provides a logging function for different events or transitions. The values of the selected GP timer counter is captured and stored in the two-

level-deep FIFO stacks when selected transitions are detected on capture input pins, CAPx (x = 1, 2, or 3 for EVA; and x = 4, 5, or 6 for EVB). The capture unit consists of three capture circuits.

- Capture units include the following features:
  - One 16-bit capture control register, CAPCONx (R/W)
  - One 16-bit capture FIFO status register, CAPFIFOx
  - Selection of GP timer 1/2 (for EVA) or 3/4 (for EVB) as the time base
  - Three 16-bit 2-level-deep FIFO stacks, one for each capture unit
  - Three capture input pins (CAP1/2/3 for EVA, CAP4/5/6 for EVB)—one input pin per capture unit. [All inputs are synchronized with the device (CPU) clock. In order for a transition to be captured, the input must hold at its current level to meet two rising edges of the device clock. The input pins CAP1/2 and CAP4/5 can also be used as QEP inputs to the QEP circuit.]
  - User-specified transition (rising edge, falling edge, or both edges) detection
  - Three maskable interrupt flags, one for each capture unit

1.1.7 Quadrature-Encoder Pulse (QEP) Circuit

Two capture inputs (CAP1 and CAP2 for EVA; CAP4 and CAP5 for EVB) can be used to interface the on-chip QEP circuit with a quadrature encoder pulse. Full synchronization of these inputs is performed on-chip. Direction or leading-quadrature pulse sequence is detected, and GP timer 2/4 is incremented or decremented by the rising and falling edges of the two input signals (four times the frequency of either input pulse).

1.1.8 External Analog-to-Digital Converter (ADC) Start-of-Conversion

EVA/EVB start-of-conversion (SOC) can be sent to an external pin (EVASOC) for external ADC interface. EVASOC and EVBSOC are MUXed with $\overline{\text{T2CTRIP}}$ and $\overline{\text{T4CTRIP}}$, respectively.

1.1.9 Power Drive Protection Interrupt ($\overline{\text{PDPINTx}}$, x = A or B)

The $\overline{\text{PDPINTx}}$ is a safety feature that is provided for the safe operation of systems such as power converters and motor drives. $\overline{\text{PDPINTx}}$ can be used to inform the monitoring program of motor drive abnormalities such as over-voltage, over-current, and excessive temperature rise. If the $\overline{\text{PDPINTx}}$ inter-

rupt is unmasked, all PWM output pins will be put in the high-impedance state immediately after the $\overline{\text{PDPINTx}}$ pin is driven low. An interrupt will also be generated. See the EXTCONx register bit function for individual pulse-width modulation (PWM) pair, power protection, or trip functions.

The interrupt flag associated with $\overline{\text{PDPINTx}}$ is also set when such an event occurs; however, it must wait until the transition on $\overline{\text{PDPINTx}}$ has been qualified and synchronized with the internal clock. The qualification and synchronization cause a delay of two clock cycles. The setting of the flag does not depend on whether or not the $\overline{\text{PDPINTx}}$ interrupt is masked: it happens when a qualified transition occurs on the $\overline{\text{PDPINTx}}$ pin. This interrupt is enabled following reset. If the $\overline{\text{PDPINTx}}$ interrupt is disabled, the action of driving the PWM outputs to the high-impedance state (upon a valid $\overline{\text{PDPINTx}}$ interrupt) is also disabled.

1.1.10 EV Registers

The EV registers occupy two 64-word (16-bit) frames of address space. The EV module decodes the lower six-bits of the address; while the upper 10 bits of the address are decoded by the peripheral address decode logic, which provides a module select to the Event Manager when the peripheral address bus carries an address within the range designated for the EV on that device.

On 28x devices (as with the C240 device), EVA registers are located in the range 7400h to 7431h. EVB registers are located in the range of 7500h to 7531h.

The undefined registers and undefined bits of the EV registers all return zero when read by user software. Writes have no effect. See Section 1.3, *Event Manager(EV) Register Addresses*, on page 1-12.

1.1.11 EV Interrupts

Each EV interrupt group has multiple interrupt sources, the CPU interrupt requests are processed by the peripheral interrupt expansion (PIE) module. See the *Peripheral Interrupt Expansion Peripheral Reference Guide* (literature number SPRU045) for details. The stages of response are as follows:

1) *Interrupt source*. If peripheral interrupt conditions occur, the respective flag bits in registers EVxIFRA, EVxIFRB, or EVxIFRC (x = A or B) are set. Once set, these flags remain set until explicitly cleared by the software. It is mandatory to clear these flags in the software or future interrupts will not be recognized.

2) *Interrupt enable*. The Event Manager interrupts can be individually enabled or disabled by interrupt mask registers EVxIMRA, EVxIMRB, and

EVxIMRC (x = A or B). Each bit is set to 1 to enable/unmask the interrupt or cleared to 0 to disable/mask the interrupt.

3) *PIE request*. If both interrupt flag bits and interrupt mask bits are set, then the peripheral issues a peripheral interrupt request to the PIE module. The PIE module can receive more than one interrupt from the peripheral. The PIE logic records all the interrupt requests and generates the respective CPU interrupt. (INT1, 2, 3, 4, or 5) based on the preassigned priority of the received interrupts.

4) *CPU response*. On receipt of an INT1, 2, 3, 4, or 5 interrupt request, the respective bit in the CPU interrupt flag register (IFR) will be set. If the corresponding interrupt mask register (IER) bit is set and INTM bit is cleared, then the CPU recognizes the interrupt and issues an acknowledgement to the PIE. Following this, the CPU finishes executing the current instruction and jumps to the interrupt vector address corresponding to INT1.y, 2.y, 3.y, 4.y, or 5.y in the PIE vector table. At this time, the respective IFR bit will be cleared and the INTM bit will be set disabling further interrupt recognition. The interrupt vector contains an address for the interrupt service routine. From here, the interrupt response is controlled by the software.

5) *PIE response*. The PIE logic uses the acknowledge signal from the CPU to clear the PIEIFR bit. See the Peripheral Interrupt Expansion Peripheral Reference Guide (SPRU045) for enabling future interrupts.

6) *Interrupt software*. At this stage, the interrupt software has explicit responsibility to avoid improper interrupt response. After executing the interrupt specific code, the routine should clear the interrupt flag in the EVxIFRA, EVxIFRB, or EVxIFRC that caused the serviced interrupt. Before returning, the interrupt software should re-enable interrupts by clearing respective PIEACKx bits (by writing a 1 to the corresponding bit) and enabling the global interrupt bit INTM.

1.2 Enhanced EV Features

The F2810™ EV is largely the same as the 240x EV. A few enhancements are introduced in the F2810 EV; however, the F2810 EV is backward compatible with the 240x EV. Corresponding bits in the newly added register, EXTCON, must be set for all enhancements and changes to take effect. The following are enhancements and differences of the F2810 EV module with respect to the 240x device:

- Individual output enable bit for each timer and full compare unit
- Dedicated output trip pin for each timer and full compare unit as replacement of the PDPINT pin
- New control register added to activate and configure feature additions and modifications. This is key to maintaining compatibility.
- Trip enable bit for each trip pin. These changes allow the outputs of each compare to be enabled and disabled independently so that each compare can control a separate power stage, actuator, or drive.
- Renamed CAP3 pin can function as CAP3_QEPI (CAP3_QEPI1 for EVA, CAP6_QEPI2 for EVB). This pin is now allowed to reset Timer 2 when enabled. Also introduced a qualification mode where QEP1 and QEP2 can be used to qualify CAP3_QEPI. The QEP channel (3 pin) enables seamless interface to industry-standard three-signal quadrature encoders.
- EV ADC start-of-conversion outputs to allow synchronization with high-precision external ADCs.

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1.3 Event Manager (EV) Register Addresses

All EV-A registers are listed in Table 1−2 and EV-B are listed in Table 1−3.

Table 1−2. Summary of EV-A Registers

Name	Address	Description
Timer Registers		
GPTCONA	0x7400	Overall GP Timer Control Register A
T1CNT	0x7401	Timer 1 Counter Register
T1CMPR	0x7402	Timer 1 Compare Register
T1PR	0x7403	Timer 1 Period Register
T1CON	0x7404	Timer 1 Control Register
T2CNT	0x7405	Timer 2 Counter Register
T2CMPR	0x7406	Timer 2 Compare Register
T2PR	0x7407	Timer 2 Period Register
T2CON	0x7408	Timer 2 Control Register
EXTCONA	0x7409	Extension Control Register A
Compare Registers		
COMCONA	0x7411	Compare Control Register A
ACTRA	0x7413	Compare Action Control Register A
DBTCONA	0x7415	Dead−Band Timer Control Register A
CMPR1	0x7417	Compare Register 1
CMPR2	0x7418	Compare Register 2
CMPR3	0x7419	Compare Register 3
Capture Registers		
CAPCONA	0x7420	Capture Control Register A
CAPFIFOA	0x7422	Capture FIFO Status Register A
CAP1FIFO	0x7423	Two−Level Deep Capture FIFO Stack 1
CAP2FIFO	0x7424	Two−Level Deep Capture FIFO Stack 2
CAP3FIFO	0x7425	Two−Level Deep Capture FIFO Stack 3

Table 1–2. Summary of EV-A Registers (Continued)

Name	Address	Description
CAP1FBOT	0x7427	Bottom Register Of Capture FIFO Stack 1
CAP2FBOT	0x7428	Bottom Register Of Capture FIFO Stack 2
CAP3FBOT	0x7429	Bottom Register Of Capture FIFO Stack 3
Interrupt Registers		
EVAIMRA	0x742C	Interrupt Mask Register A
EVAIMRB	0x742D	Interrupt Mask Register B
EVAIMRC	0x742E	Interrupt Mask Register C
EVAIFRA	0x742F	Interrupt Flag Register A
EVAIFRB	0x7430	Interrupt Flag Register B
EVAIFRC	0x7431	Interrupt Flag Register C

Table 1–3. Summary of EV-B Registers

Name	Address	Description
Timer Registers		
GPTCONB	0x7500	Overall GP Timer Control Register B
T3CNT	0x7501	Timer 3 Counter Register
T3CMPR	0x7502	Timer 3 Compare Register
T3PR	0x7503	Timer 3 Period Register
T3CON	0x7504	Timer 3 Control Register
T4CNT	0x7505	Timer 4 Counter Register
T4CMPR	0x7506	Timer 4 Compare Register
T4PR	0x7507	Timer 4 Period Register
T4CON	0x7508	Timer 4 Control Register
EXTCONB	0x7509	Extension Control Register B
Compare Registers		
COMCONB	0x7511	Compare Control Register B

Table 1–3. Summary of EV-B Registers (Continued)

ACTRB	0x7513	Compare Action Control Register B
DBTCONB	0x7515	Dead–Band Timer Control Register B
CMPR4	0x7517	Compare Register 4
CMPR5	0x7518	Compare Register 5
CMPR6	0x7519	Compare Register 6
Capture Registers		
CAPCONB	0x7520	Capture Control Register B
CAPFIFOB	0x7522	Capture FIFO Status Register B
CAP4FIFO	0x7523	Two–Level Deep Capture FIFO Stack 4
CAP5FIFO	0x7524	Two–Level Deep Capture FIFO Stack 5
CAP6FIFO	0x7525	Two–Level Deep Capture FIFO Stack 6
CAP4FBOT	0x7527	Bottom Register Of Capture FIFO Stack 4
CAP5FBOT	0x7528	Bottom Register Of Capture FIFO Stack 5
CAP6FBOT	0x7529	Bottom Register Of Capture FIFO Stack 6
Interrupt Registers		
EVBIMRA	0x752C	Interrupt Mask Register A
EVBIMRB	0x752D	Interrupt Mask Register B
EVBIMRC	0x752E	Interrupt Mask Register C
EVBIFRA	0x752F	Interrupt Flag Register A
EVBIFRB	0x7530	Interrupt Flag Register B
EVBIFRC	0x7531	Interrupt Flag Register C

1.4 General-Purpose (GP) Timers

There are two general-purpose (GP) timers in each module. These timers can be used as independent time bases in applications such as:

- The generation of a sampling period in a control system
- Providing a time base for the operation of the quadrature encoder pulse (QEP) circuit (GP timer 2/4 only) and the capture units
- Providing a time base for the operation of the compare units and associated PWM circuits to generate PWM outputs

1.4.1 Timer Functional Blocks

Figure 1–3 shows a block diagram of a GP timer. Each GP timer includes:

- One readable and writable (RW) 16-bit up and up/down counter register TxCNT (x = 1, 2, 3, 4). This register stores the current value of the counter and keeps incrementing or decrementing depending on the direction of counting
- One RW 16-bit timer compare register (shadowed), TxCMPR (x = 1, 2, 3, 4)
- One RW 16-bit timer period register (shadowed), TxPR (x = 1, 2, 3, 4)
- RW 16-bit individual timer control register, TxCON (x = 1, 2, 3, 4)
- Programmable prescaler applicable to both internal and external clock inputs
- Control and interrupt logic
- One GP timer compare output pin, TxCMP (x = 1, 2, 3, 4)
- Output conditioning logic

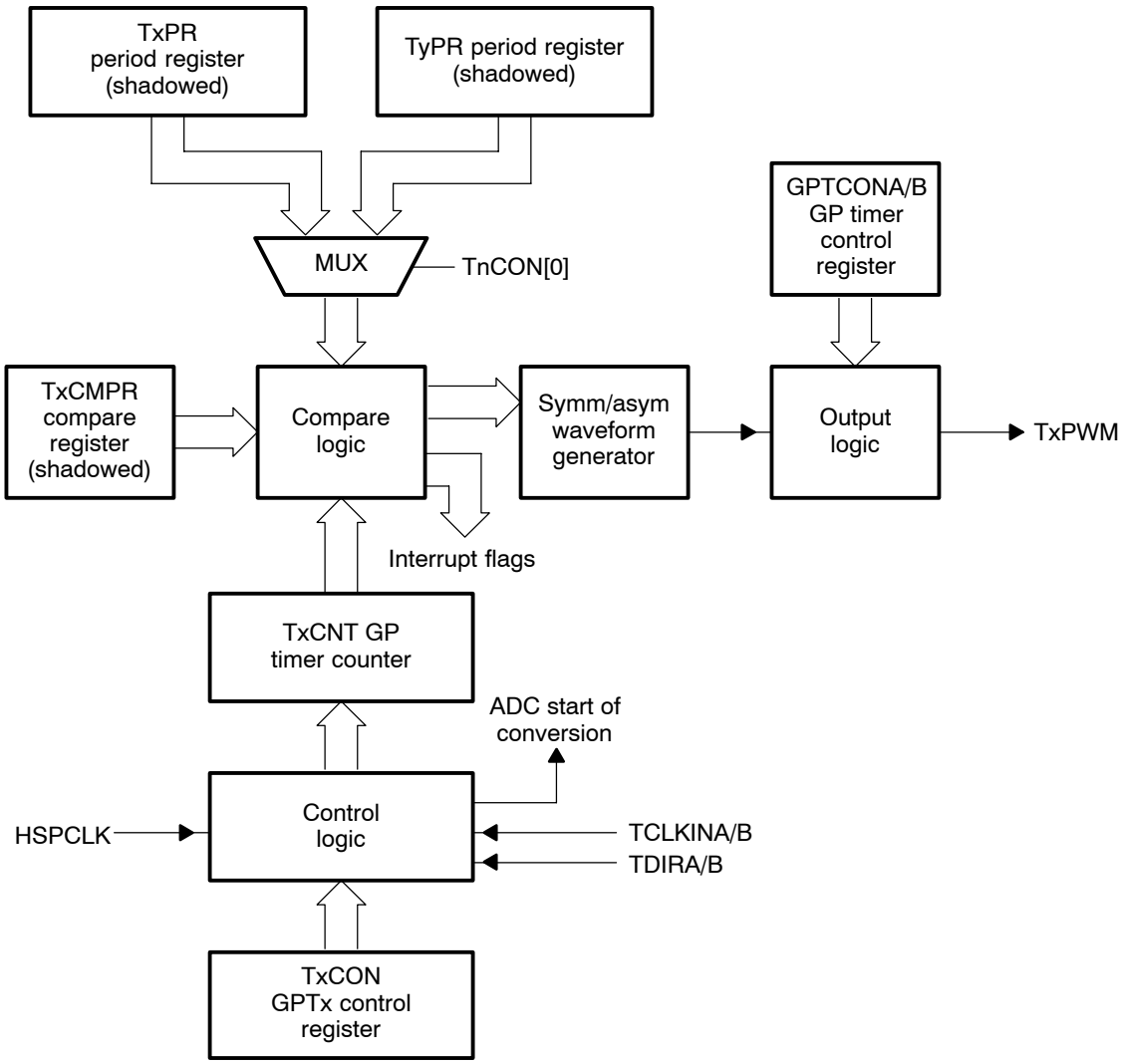
Another overall control register, GPTCONA/B, specifies the action to be taken by the timers on different timer events, and indicates the counting directions of the GP timers. GPTCONA/B is readable and writable, although writing to the status bits has no effect.

Note:

Timer 2 can select the period register of timer 1 as its period register. In Figure 1–3, the MUX is applicable only when the figure represents timer 2.

Timer 4 can select the period register of timer 3 as its period register. In Figure 1–3, the MUX is applicable only when the figure represents timer 4.

Figure 1–3. General-Purpose Timer Block Diagram (x = 2 or 4) [when x = 2: y = 1 and n = 2; when x = 4: y = 3 and n = 4]



1.4.2 GP Timer Inputs

The inputs to the GP timers are:

- The internal HSPCLK
- An external clock, TCLKINA/B, that has a maximum frequency of one-fourth that of the device clock
- Direction input, TDIRA/B, for use by the GP timers in directional up-/down-counting mode

- Reset signal, RESET

When a timer is used with the QEP circuit, the QEP circuit generates both the timer's clock and the counting direction.

1.4.3 GP Timer Outputs

The outputs of the timers are:

- GP timer compare outputs TxCMP, x = 1, 2, 3, 4
- ADC start-of-conversion signal to ADC module
- Underflow, overflow, compare match, and period match signals to its own compare logic and to the compare units
- Counting direction indication bits

1.4.4 Individual GP Timer Control Register (TxCON)

The operational mode of a timer is controlled by its individual control register TxCON. Bits in the TxCON register determine:

- Which of the four counting modes the timer is in
- Whether an internal or external clock is to be used by the GP timer
- Which of the eight input clock prescale factors (ranging from 1 to 1/128) is used
- On which condition the timer compare register is reloaded
- Whether the timer is enabled or disabled
- Whether the timer compare operation is enabled or disabled
- Which period register is used by timer 2, its own, or timer 1's period register (EVA)
  Which period register is used by timer 4, its own, or timer 3's period register (EVB)

1.4.5 Overall GP Timer Control Register (GPTCONA/B)

The control register GPTCONA/B specifies the action to be taken by the timers on different timer events and indicates their counting directions.

1.4.6 GP Timer Compare Registers

The compare register associated with a GP timer stores the value to be constantly compared with the counter of the GP timer. When a match happens, the following events occur:

- A transition occurs on the associated compare output according to the bit pattern in GPTCONA/B
- The corresponding interrupt flag is set
- A peripheral interrupt request is generated if the interrupt is unmasked

The compare operation of a GP timer can be enabled or disabled by the appropriate bit in TxCON.

The compare operation and outputs can be enabled in any of the timer modes, including QEP mode.

1.4.7 GP Timer Period Register

The value in the period register of a GP timer determines the period of the timer. A GP timer resets to 0, or starts counting downward when a match occurs between the period register and the timer counter, depending on which counting mode the timer is in.

1.4.8 Double Buffering of GP Timer Compare and Period Registers

The compare and period registers, TxCMPR and TxPR, of a GP timer are shadowed. A new value can be written to any of these registers at any time during a period. However, the new value is written to the associated shadow register. For the compare register, the content in the shadow register is loaded into the working (active) register only when a certain timer event specified by TxCON occurs. For the period register, the working register is reloaded with the value in its shadow register only when the value of the counter register TxCNT is 0. The condition on which a compare register is reloaded can be one of the following:

- Immediately after the shadow register is written
- On underflow; that is, when the GP timer counter value is 0
- On underflow or period match; that is, when the counter value is 0 or when the counter value equals the value of the period register

The double buffering feature of the period and compare registers allows the application code to update the period and compare registers at any time during a period in order to change the timer period and the width of the PWM pulse for the period that follows. On-the-fly change of the timer period value, in the case of PWM generation, means on-the-fly change of PWM carrier frequency.

Note: Period Register Initialization

The period register of a GP timer should be initialized before its counter is initialized to a non-zero value. Otherwise, the value of the period register will remain unchanged until the next underflow.

A compare register is transparent (the newly loaded value goes directly into the active register) when the associated compare operation is disabled. This applies to all Event Manager compare registers.

1.4.9 GP Timer Compare Output

The compare output of a GP timer can be specified active high, active low, forced high, or forced low, depending on how the GPTCONA/B bits are configured. It goes from low to high (high to low) on the first compare match when it is active high (low). It then goes from high to low (low to high) on the second compare match if the GP timer is in an up-/down-counting mode, or on period match if the GP timer is in up-counting mode. The timer compare output becomes high (low) right away when it is specified to be forced high (low).

1.4.10 Timer Counting Direction

The counting directions of the GP timers are reflected by their respective bits in GPTCONA/B during all timer operations as follows:

- 1 represents the up-counting direction
- 0 represents the down-counting direction

The input pin TDIRA/B determines the direction of counting when a GP timer is in directional up-/down-counting mode. When TDIRA/B is high, upward counting is specified; when TDIRA/B is low, downward counting is specified.

1.4.11 Timer Clock

The source of the GP timer clock can be the internal device clock or the external clock input, TCLKINA/B. The frequency of the external clock must be less than or equal to one-fourth of that of the device clock. GP timer 2 (EVA) and GP timer 4 (EVB) can be used with the QEP circuits, in directional up-/down-counting mode. In this case, the QEP circuits provide both the clock and direction inputs to the timer.

A wide range of prescale factors are provided for the clock input to each GP timer.

1.4.12 QEP-Based Clock Input

The quadrature encoder pulse (QEP) circuit, when selected, can generate the input clock and counting direction for GP timer 1/2/3/4 (QEPCLK is one of the clock sources for Timer 1) in the directional up/down-counting mode. This input clock cannot be scaled by GP timer prescaler circuits (that is, the prescaler

of the selected GP timer is always one if the QEP circuit is selected as the clock source). Furthermore, the frequency of the clock generated by the QEP circuits is four times that of the frequency of each QEP input channel because both the rising and falling edges of both QEP input channels are counted by the selected timer. The frequency of the QEP input must be less than or equal to one-fourth of that of the device clock.

1.4.13 GP Timer Synchronization

GP timer 2 can be synchronized with GP timer 1 (for EVA) and GP timer 4 can be synchronized with GP timer 3 (for EVB) by proper configuration of T2CON and T4CON, respectively, in the following ways:

- EVA:
  Set the T2SWT1 bit in T2CON to start GP timer 2 counting with the TENABLE bit in T1CON (thus, both timer counters start simultaneously)
- EVA:
  Initialize the timer counters in GP timers 1 and 2 with different values before starting synchronized operation
- EVA:
  Specify that GP timer 2 uses the period register of GP timer 1 as its period register (ignoring its own period register) by setting SELT1PR in T2CON
- EVB:
  Set the T4SWT3 bit in T4CON to start GP timer 4 counting with the TENABLE bit in T3CON (thus, both timer counters start simultaneously)
- EVB:
  Initialize the timer counters in GP timers 3 and 4 with different values before starting synchronized operation
- EVB:
  Specify that GP timer 4 uses the period register of GP timer 3 as its period register (ignoring its own period register) by setting SELT3PR in T4CON

This allows the desired synchronization between GP timer events. Since each GP timer starts the counting operation from its current value in the counter register, one GP timer can be programmed to start with a known delay after the other GP timer.

1.4.14 Starting the A/D Converter With a Timer Event

The bits in GPTCONA/B can specify that an ADC start signal be generated on a GP timer event such as underflow, compare match, or period match. This

feature provides synchronization between the GP timer event and the ADC start without any CPU intervention.

1.4.15 GP Timer in Emulation Suspend

The GP timer control register bits also define the operation of the GP timers during emulation suspend. These bits can be set to allow the operation of GP timers to continue when an emulation interrupt occurs making in-circuit emulation possible. They can also be set to specify that the operation of GP timers stops immediately, or after completion of the current counting period, when emulation interrupt occurs.

Emulation suspend occurs when the device clock is stopped by the emulator, for example, when the emulator encounters a break point.

1.4.16 GP Timer Interrupts

There are sixteen interrupt flags in the EVAIFRA, EVAIFRB, EVBIFRA, and EVBIFRB registers for the GP timers. Each of the four GP timers can generate four interrupts upon the following events:

- Overflow: TxOFINT (x = 1, 2, 3, or 4)
- Underflow: TxUFINT (x = 1, 2, 3, or 4)
- Compare match: TxCINT (x = 1, 2, 3, or 4)
- Period match: TxPINT (x = 1, 2, 3, or 4)

A timer compare event (match) happens when the content of a GP timer counter is the same as that of the compare register. The corresponding compare interrupt flag is set one clock cycle after the match if the compare operation is enabled.

An overflow event occurs when the value of the timer counter reaches FFFFh. An underflow event occurs when the timer counter reaches 0000h. Similarly, a period event happens when the value of the timer counter is the same as that of the period register. The overflow, underflow, and period interrupt flags of the timer are set one clock cycle after the occurrence of each individual event. Note that the definition of overflow and underflow is different from their conventional definitions.

1.4.17 GP Timer Counting Operation

Each GP timer has four possible modes of operation:

- Stop/Hold mode
- Continuous Up-Counting mode
- Directional Up-/Down-Counting mode
- Continuous Up-/Down-Counting mode

The bit pattern in the corresponding timer control register TxCON determines the counting mode of a GP timer. The timer enabling bit, TxCON[6], enables or disables the counting operation of a timer. When the timer is disabled, the counting operation of the timer stops and the prescaler of the timer is reset to x/1. When the timer is enabled, the timer starts counting according to the counting mode specified by other bits of TxCON.

1.4.18 Stop/Hold Mode

In this mode the GP timer stops and holds at its current state. The timer counter, the compare output, and the prescale counter all remain unchanged in this mode.

1.4.19 Continuous Up-Counting Mode

The GP timer in this mode counts up according to the scaled input clock until the value of the timer counter matches that of the period register. On the next rising edge of the input clock after the match, the GP timer resets to zero and starts counting up again.

The period interrupt flag of the timer is set one clock cycle after the match between the timer counter and period register. A peripheral interrupt request is generated if the flag is not masked. An ADC start is sent to the ADC module at the same time the flag is set, if the period interrupt of this timer has been selected by the appropriate bits in GPTCONA/B to start the ADC.

One clock cycle after the GP timer becomes 0, the underflow interrupt flag of the timer is set. A peripheral interrupt request is generated by the flag if it is unmasked. An ADC start is sent to the ADC module at the same time if the underflow interrupt flag of this timer has been selected by appropriate bits in GPTCONA/B to start ADC.

The overflow interrupt flag is set one clock cycle after the value in TxCNT matches FFFFh. A peripheral interrupt request is generated by the flag if it is unmasked.

The duration of the timer period is (TxPR) + 1 cycles of the scaled clock input except for the first period. The duration of the first period is the same if the timer counter is zero when counting starts.

The initial value of the GP timer can be any value between 0h and FFFFh inclusive. When the initial value is greater than the value in the period register, the timer counts up to FFFFh, resets to zero, and continues the operation as if the initial value was zero. When the initial value in the timer counter is the same as that of the period register, the timer sets the period interrupt flag, resets to

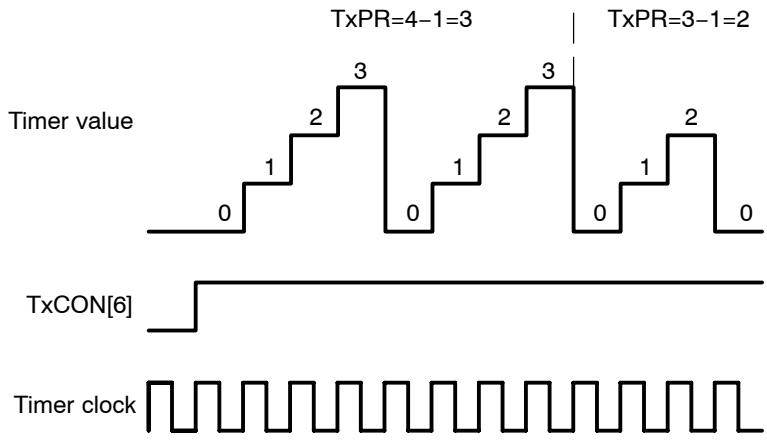
zero, sets the underflow interrupt flag, and then continues the operation again as if the initial value was zero. If the initial value of the timer is between zero and the contents of the period register, the timer counts up to the period value and continue to finish the period as if the initial counter value was the same as that of the period register.

The counting direction indication bit in GPTCONA/B is one for the timer in this mode. Either the external or internal device clock can be selected as the input clock to the timer. TDIRA/B input is ignored by the GP timer in this counting mode.

The continuous up-counting mode of the GP timer is particularly useful for the generation of edge-triggered or asynchronous PWM waveforms and sampling periods in many motor and motion control systems.

Figure 1−4 shows the continuous up-counting mode of the GP timer.

Figure 1−4. GP Timer Continuous Up-Counting Mode (TxPR = 3 or 2)



As shown in Figure 1−4, *GP Timer Continuous Up-Counting Mode (TxPR = 3 or 2)*, no clock cycle is missed from the time the counter reaches the period register value to the time it starts another counting cycle.

1.4.20 Directional Up-/Down-Counting Mode

The GP timer in directional up-/down-counting mode counts up or down according to the scaled clock and TDIRA/B inputs. The GP timer starts counting up until its value reaches that of the period register (or FFFFh if the initial count is greater than the period) when the TDIRA/B pin is held high. When the timer value equals that of its period register (or FFFFh) the timer resets to zero and continues counting up to the period again. When TDIRA/B is held low, the GP

timer counts down until its value becomes zero. When the value of the timer has counted down to zero, the timer reloads its counter with the value in the period register and starts counting down again.

The initial value of the timer can be any value between 0000h to FFFFh. When the initial value of the timer counter is greater than that of the period register, the timer counts up to FFFFh before resetting itself to zero and counting up to the period. If TDIRA/B is low when the timer starts with a value greater than the period register, it counts down to the value of the period register and continues counting down to zero, at which point the timer counter gets reloaded with the value from the period register as normal.

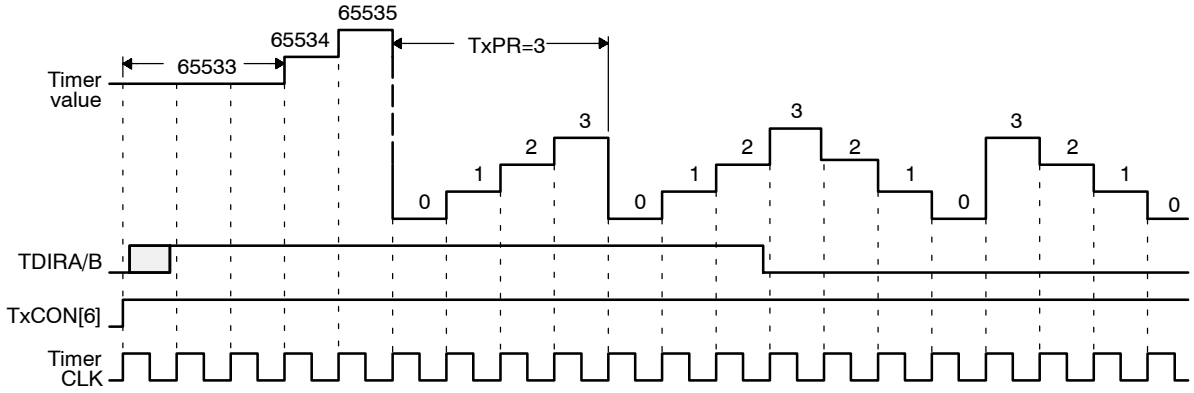
The period, underflow, and overflow interrupt flags, interrupts, and associated actions are generated on respective events in the same manner as they are generated in the continuous up-counting mode.

The latency from a change of TDIRA/B to a change of counting direction is one clock cycle after the end of the current count (that is, after the end of the current prescale counter period).

The direction of counting is indicated for the timer in this mode by the corresponding direction indication bit in GPTCONA/B: 1 means counting up; 0 means counting down. Either the external clock from the TCLKINA/B pin or the internal device clock can be used as the input clock for the timer in this mode.

Figure 1–5 shows the directional up-/down-counting mode of the GP timers.

Figure 1–5. GP Timer Directional Up-/Down-Counting Mode: Prescale Factor 1 and TxPR = 3



The directional up-/down-counting mode of GP timer 2/4 can be used with the quadrature encoder pulse (QEP) circuits in the EV module. The QEP circuits

provide both the counting clock and direction for GP timer 2/4 in this case. This mode of operation can also be used to time the occurrence of external events in motion/motor control and power electronics applications.

1.4.21 Continuous Up-/Down-Counting Mode

This mode of operation is the same as the directional up-/down-counting mode, but the TDIRA/B pin has no effect on the counting direction. The counting direction only changes from up to down when the timer reaches the period value (or FFFFh if the initial timer value is greater than the period). The timer direction only changes from down to up when the timer reaches zero.

The period of the timer in this mode is 2*(TxPR) cycles of the scaled clock input, except for the first period. The duration of the first counting period is the same if the timer counter is zero when counting starts.

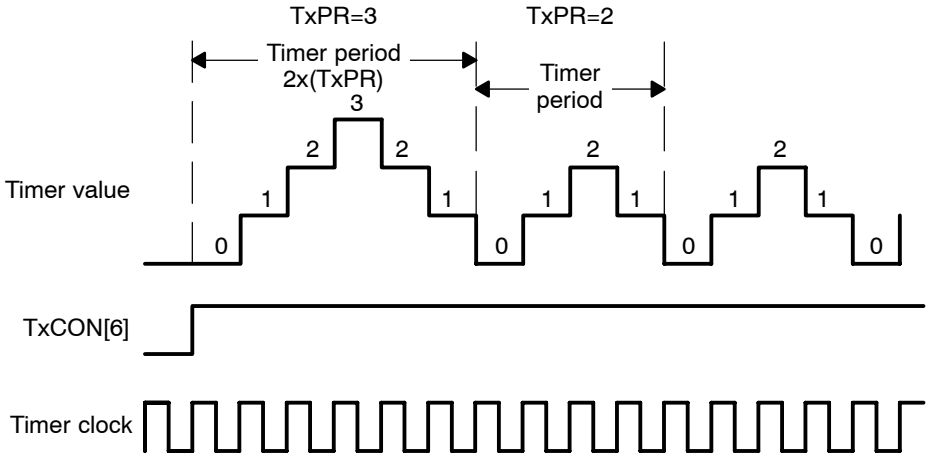
The initial value of the GP timer counter can be any value between 0h and FFFFh inclusive. When the initial value is greater than that of the period register, the timer counts up to FFFFh, resets to zero, and continues the operation as if the initial value was zero. When the initial value in the timer counter is the same as that of the period register, the timer counts down to zero and continues again as if the initial value was zero. If the initial value of the timer is between zero and the contents of the period register, the timer counts up to the period value and continues to finish the period as if the initial counter value was the same as that of the period register.

The period, underflow, and overflow interrupt flags, interrupts, and associated actions are generated on respective events in the same manner as they are generated in continuous up-counting mode.

The counting direction indication bit for this timer in GPTCONA/B is one when the timer counts upward and zero when the timer counts downward. Either the external clock from the TCLKINA/B pin or the internal device clock can be selected as the input clock. TDIRA/B input is ignored by the timer in this mode.

Figure 1−6 shows the continuous up-/down-counting mode of the GP timer.

Figure 1–6. GP Timer Continuous Up-/Down-Counting Mode (TxPR = 3 or 2)



Continuous up-/down-counting mode is particularly useful in generating centered or symmetric PWM waveforms found in a broad range of motor/motion control and power electronics applications.

1.4.22 GP Timer Compare Operation

Each GP timer has an associated compare register TxCMPR and a PWM output pin TxPWM. The value of a GP timer counter is constantly compared to that of its associated compare register. A compare match occurs when the value of the timer counter is the same as that of the compare register. Compare operation is enabled by setting TxCON[1] to one. If it is enabled, the following happens on a compare match:

- The compare interrupt flag of the timer is set one clock cycle after the match
- A transition occurs on the associated PWM output according to the bit configuration in GPTCONA/B, one device clock cycle after the match
- If the compare interrupt flag has been selected by the appropriate GPTCONA/B bits to start ADC, an ADC start signal is generated at the same time the compare interrupt flag is set

A peripheral interrupt request is generated by the compare interrupt flag if it is unmasked.

1.4.23 PWM Transition

The transition on the PWM output is controlled by an asymmetric and symmetric waveform generator and the associated output logic, and depends on the following:

- ❏ Bit definition in GPTCONA/B
- ❏ Counting mode the timer is in
- ❏ Counting direction when the counting mode is continuous-up/-down mode

1.4.24 Asymmetric/Symmetric Waveform Generator

The asymmetric/symmetric waveform generator generates an asymmetric or symmetric PWM waveform based on the counting mode the GP timer is in.

Asymmetric Waveform Generation

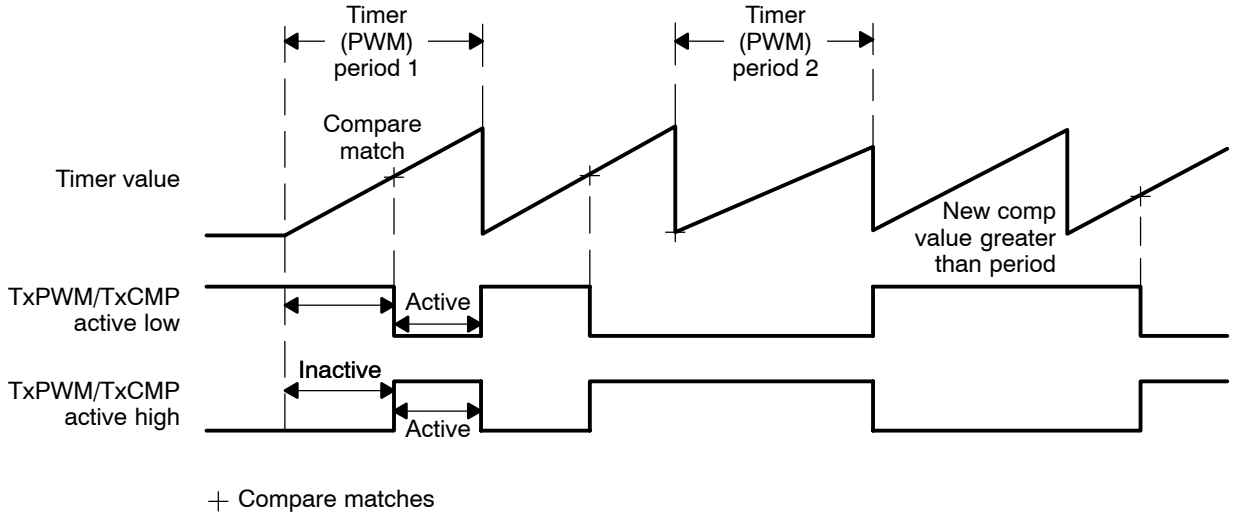
An asymmetric waveform (Figure 1–7) is generated when the GP timer is in continuous up-counting mode. When the GP timer is in this mode, the output of the waveform generator changes according to the following sequence:

- ❏ zero before the counting operation starts
- ❏ remains unchanged until the compare match happens
- ❏ toggles on compare match
- ❏ remains unchanged until the end of the period
- ❏ resets to zero at the end of a period on period match, if the new compare value for the following period is not zero

The output is one for the whole period, if the compare value is zero at the beginning of a period. The output does not reset to zero if the new compare value for the following period is zero. This is important because it allows the generation of PWM pulses of 0% to 100% duty cycle without glitches. The output is zero for the whole period if the compare value is greater than the value in the period register. The output is one for one cycle of the scaled clock input if the compare value is the same as that of the period register.

One characteristic of asymmetric PWM waveforms is that a change in the value of the compare register only affects one side of the PWM pulse.

Figure 1–7. GP Timer Compare/PWM Output in Up-Counting Mode



Symmetric Waveform Generation

A symmetric waveform (Figure 1–8) is generated when the GP timer is in continuous up-/down-counting modes. When the GP timer is in this mode, the state of the output of the waveform generator is determined by the following:

- ❏ Zero before the counting operation starts
- ❏ Remains unchanged until first compare match
- ❏ Toggles on the first compare match
- ❏ Remains unchanged until the second compare match
- ❏ Toggles on the second compare match
- ❏ Remains unchanged until the end of the period
- ❏ Resets to zero at the end of the period if there is no second compare match, and the new compare value for the following period is not zero

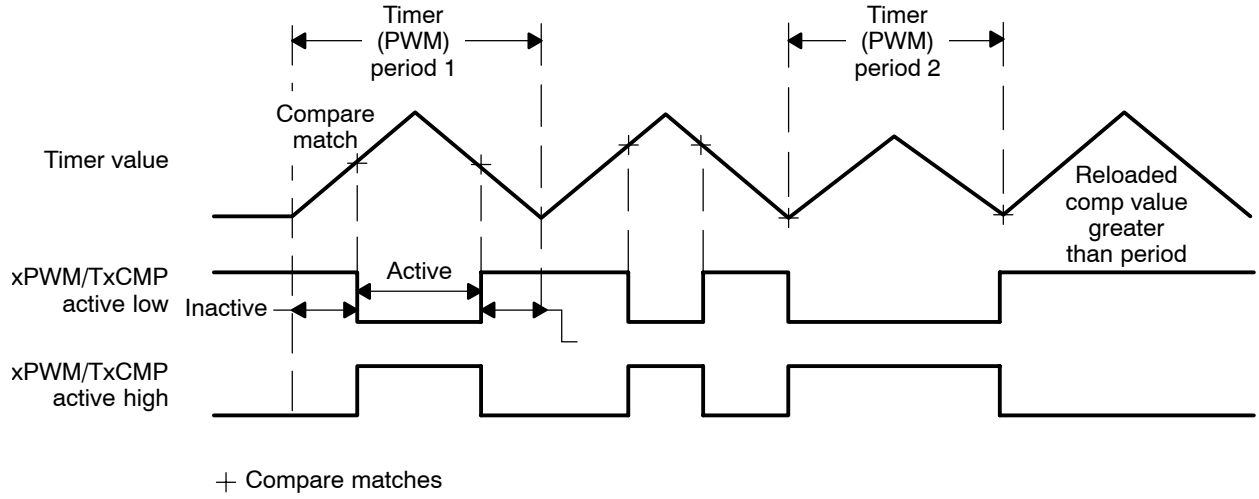
The output is set to one at the beginning of a period and remains one until the second compare match if the compare value is zero at the beginning of a period. After the first transition, the output remains one until the end of the period if the compare value is zero for the second half of the period. When this happens, the output does not reset to zero if the new compare value for the following period is still zero. This is done again to assure the generation of PWM pulses of 0% to 100% duty cycle without any glitches. The first transition does

not happen if the compare value is greater than or equal to that of the period register for the first half of the period. However, the output still toggles when a compare match happens in the second half of the period. This error in output transition, often as a result of calculation error in the application routine, is corrected at the end of the period because the output resets to zero, unless the new compare value for the following period is zero. In this case, the output remains one, which again puts the output of the waveform generator in the correct state.

Note:

The output logic determines what the active state is for all output pins.

Figure 1–8. GP Timer Compare/PWM Output in Up-/Down-Counting Modes



Output Logic

The output logic further conditions the output of the waveform generator to form the ultimate PWM output that controls different kinds of power devices. The PWM output can be specified active high, active low, forced low, and forced high by proper configuration of the appropriate GPTCONA/B bits.

The polarity of the PWM output is the same as that of the output of the associated asymmetric/symmetric waveform generator when the PWM output is specified active high.

The polarity of the PWM output is the opposite of that of the output of the associated asymmetric/symmetric waveform generator when the PWM output is specified active low.

The PWM output is set to one (or zero) immediately after the corresponding bits in GPTCONA/B are set, and the bit pattern specifies that the state of PWM output is forced high (or low).

In summary, during a normal counting mode, transitions on the GP timer PWM outputs happen according to Table 1–4 for the continuous up-counting mode and according to Table 1–5 for the continuous up-/down-counting mode, assuming compare is enabled.

Setting active means setting high for active high and setting low for active low. Setting inactive means the opposite.

The asymmetric/symmetric waveform generation, based on the timer counting mode and the output logic, is also applicable to the compare units.

Table 1–4. GP Timer Compare Output in Continuous Up-Counting Modes

Time in a Period	State of Compare Output
Before compare match	Inactive
On compare match	Set active
On period match	Set inactive

Table 1–5. GP Timer Compare Output in Continuous Up-/Down-Counting Modes

Time in a Period	State of Compare Output
Before 1st compare match	Inactive
On 1st compare match	Set active
On 2nd compare match	Set inactive
After 2nd compare match	Inactive

All GP timer PWM outputs are put in the high-impedance state when any of the following events occurs:

- GPTCONA/B[6] is set to zero by software
- $\overline{\text{PDPINTx}}$ is pulled low and is not masked
- Any reset event occurs
- TxCON[1] is set to zero by software

1.4.25 Active/Inactive Time Calculation

For the continuous up-counting mode, the value in the compare register represents the elapsed time between the beginning of a period and the occurrence of the first compare match (length of the inactive phase). This elapsed time is equal to the period of the scaled input clock multiplied by the value of TxCMPR. Therefore, the length of the active phase (the output pulse width) is given by (TxPR) − (TxCMPR) + 1 cycle of the scaled input clock.

For the continuous up-/down-counting mode, the compare register can have a different value while counting down from the value while counting up. The length of the active phase (output pulse width) for up-/down-counting modes is given by (TxPR) − $(TxCMPR)_{up}$ + (TxPR) − $(TxCMPR)_{dn}$ cycles of the scaled input clock, where $(TxCMPR)_{up}$ is the compare value on the way up and $(TxCMPR)_{dn}$ is the compare value on the way down.

When the value in TxCMPR is zero, the GP timer compare output is active for the whole period if the timer is in the up-counting mode. For the up-/down-counting mode, the compare output is active at the beginning of the period if $(TxCMPR)_{up}$ is zero. The output remains active until the end of the period if $(TxCMPR)_{dn}$ is also zero.

The length of the active phase (the output pulse width) is zero when the value of TxCMPR is greater than that of TxPR for up-counting modes. For the up-/down-counting mode, the first transition is lost when $(TxCMPR)_{up}$ is greater than or equal to (TxPR). Similarly, the second transition is lost when $(TxCMPR)_{dn}$ is greater than or equal to (TxPR). The GP timer compare output is inactive for the entire period if both $(TxCMPR)_{up}$ and $TxCMPR)_{dn}$ are greater than or equal to (TxPR) for the up-/down-counting mode.

Figure 1−7, *GP Timer Compare/PWM Output in Up-Counting Mode* (page 1-28) shows the compare operation of a GP timer in the up-counting mode. Figure 1−8, *GP Timer Compare/PWM Output in Up-/Down-Counting Modes* (page 1-29) shows the compare operation of a GP timer in the up-/down-counting mode.

1.5 Generation of PWM Outputs Using the GP Timers

Each GP timer can independently be used to provide a PWM output channel. Thus, up to two PWM outputs may be generated by the GP timers.

1.5.1 PWM Operation

To generate a PWM output with a GP timer, a continuous up- or up-/down-counting mode can be selected. Edge-triggered or asymmetric PWM waveforms are generated when a continuous-up count mode is selected. Centered or symmetric PWM waveforms are generated when a continuous-up/-down mode is selected. To set up the GP timer for the PWM operation, do the following:

- ❑ Set up TxPR according to the desired PWM (carrier) period
- ❑ Set up TxCON to specify the counting mode and clock source, and start the operation
- ❑ Load TxCMPR with values corresponding to the on-line calculated widths (duty cycles) of PWM pulses

The period value is obtained by dividing the desired PWM period by the period of the GP timer input clock, and subtracting one from the resulting number when the continuous up-counting mode is selected to generate asymmetric PWM waveforms. When the continuous up-/down-counting mode is selected to generate symmetric PWM waveforms, this value is obtained by dividing the desired PWM period by two times the period of the GP timer input clock.

The GP timer can be initialized the same way as in the previous example. During run time, the GP timer compare register is constantly updated with newly determined compare values corresponding to the newly determined duty cycles.

1.5.2 GP Timer Reset

When any RESET event occurs, the following happens:

- ❑ All GP timer register bits, except for the counting direction indication bits in GPTCONA/B, are reset to 0; thus, the operation of all GP timers is disabled. The counting direction indication bits are all set to 1
- ❑ All timer interrupt flags are reset to 0

- All timer interrupt mask bits are reset to 0, except for $\overline{\text{PDPINTx}}$; thus, all GP timer interrupts are masked except for $\overline{\text{PDPINTx}}$
- All GP timer compare outputs are put in the high-impedance state

1.6 Compare Units

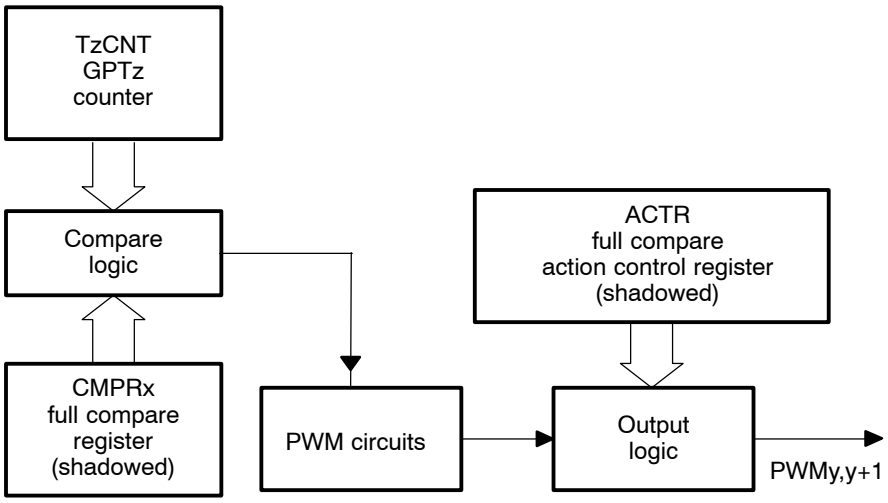
There are three (full) compare units (1, 2, and 3) in the EVA module and three (full) compare units (4, 5, and 6) in the EVB module. Each compare unit has two associated PWM outputs. The time base for the compare units is provided by GP timer 1 (for EVA) and by GP timer 3 (for EVB)

The compare units in each EV module include:

- Three 16-bit compare registers (CMPR1, CMPR2, and CMPR3 for EVA; and CMPR4, CMPR5, and CMPR6 for EVB), all with an associated shadow register, (RW)
- One 16-bit compare control register (COMCONA for EVA, and COMCONB for EVB), (RW)
- One 16-bit action control register (ACTRA for EVA, and ACTRB for EVB), with an associated shadow register, (RW)
- Six PWM (3-state) output (compare output) pins (PWMy, y = 1, 2, 3, 4, 5, 6 for EVA and PWMz, z = 7, 8, 9, 10, 11, 12 for EVB)
- Control and interrupt logic

The functional block diagram of a compare unit is shown in Figure 1–9.

Figure 1–9. Compare Unit Block Diagram
(For EVA: x = 1, 2, 3; y = 1, 3, 5; z = 1.
For EVB: x = 4, 5, 6; y = 7, 9, 11; z = 3.)



The time base for the compare units and the associated PWM circuits is provided by GP timer 1 (for EVA) or GP timer 3 (for EVB), which can be in any of

its counting modes when the compare operation is enabled. Transitions occur on the compare outputs.

Compare Inputs/Outputs

The inputs to a compare unit include:

- Control signals from control registers
- GP timer 1/3 (T1CNT/T3CNT) and its underflow and period match signals
- RESET

The output of a compare unit is a compare match signal. If the compare operation is enabled, this match signal sets the interrupt flag and causes transitions on the two output pins associated with the compare unit.

Compare Operation Modes

The operation mode of the compare units is determined by the bits in COMCONx. These bits determine:

- Whether the compare operation is enabled
- Whether the compare outputs are enabled
- The condition on which the compare registers are updated with the values in their shadow registers
- Whether space vector PWM mode is enabled

Operation

The following paragraph describes the operation of the EVA compare unit. The operation of the EVB compare unit is identical. For EVB, GP timer 3 and ACTRB are used.

The value of the GP timer 1 counter is continuously compared with that of the compare register. When a match is made, a transition appears on the two outputs of the compare unit according to the bits in the action control register (ACTRA). The bits in ACTRA can individually specify each output to be toggle active high or toggle active-low (if not forced high or low) on a compare match. The compare interrupt flag associated with a compare unit is set when a compare match is made between GP timer 1 and the compare register of this compare unit, if compare is enabled. A peripheral interrupt request is generated by the flag if the interrupt is unmasked. The timing of output transitions,

setting of interrupt flags, and generation of interrupt requests are the same as that of the GP timer compare operation. The outputs of the compare units in compare mode are subject to modification by the output logic, dead band units, and the space vector PWM logic.

1.6.1 Register Setup for Compare Unit Operation

The register setup sequence for compare unit operation requires:

For EVA	For EVB
Setting up T1PR	Setting up T3PR
Setting up ACTRA	Setting up ACTRB
Initializing CMPRx	Initializing CMPRx
Setting up COMCONA	Setting up COMCONB
Setting up T1CON	Setting up T3CON

1.6.2 Compare Units Registers

The addresses of registers associated with compare units and associated PWM circuits are shown in Table 1–6, *Addresses of EVA Compare Control Registers* on page 1-36, and in Table 1–7, *Addresses of EVB Compare Control Registers* on page 1-37. These registers are discussed in the subsections that follow.

Compare Control Registers (COMCONA and COMCONB)

The operation of the compare units is controlled by the compare control registers (COMCONA and COMCONB). The bit definition of COMCONA is summarized in Figure 5–7 and that of COMCONB is summarized in Figure 5–8. COMCONA and COMCONB are readable and writable.

Table 1–6. Addresses of EVA Compare Control Registers

Address	Register	Name
7411h	COMCONA	Compare control register
7413h	ACTRA	Compare action control register
7415h	DBTCONA	Dead-band timer control register
7417h	CMPR1	Compare register 1
7418h	CMPR2	Compare register 2
7419h	CMPR3	Compare register 3

Table 1−7. Addresses of EVB Compare Control Registers

Address	Register	Name
7511h	COMCONB	Compare control register
7513h	ACTRB	Compare action control register
7515h	DBTCONB	Dead-band timer control register
7517h	CMPR4	Compare register 4
7518h	CMPR5	Compare register 5
7519h	CMPR6	Compare register 6

1.6.3 Compare Unit Interrupts

There is a maskable interrupt flag in EVxIFRA and EVxIFRB for each compare unit. The interrupt flag of a compare unit is set one clock cycle after a compare match, if a compare operation is enabled. A peripheral interrupt request is generated by the flag if it is unmasked.

1.6.4 Compare Unit Reset

When any reset event occurs, all register bits associated with the compare units are reset to zero and all compare output pins are put in the high-impedance state.

Chapter 2

PWM Circuits

The pulse-width modulation (PWM) circuits associated with compare units make it possible to generate six PWM output channels (per EV) with programmable dead-band and output polarity.

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2.1 PWM Circuits Associated With Compare Units

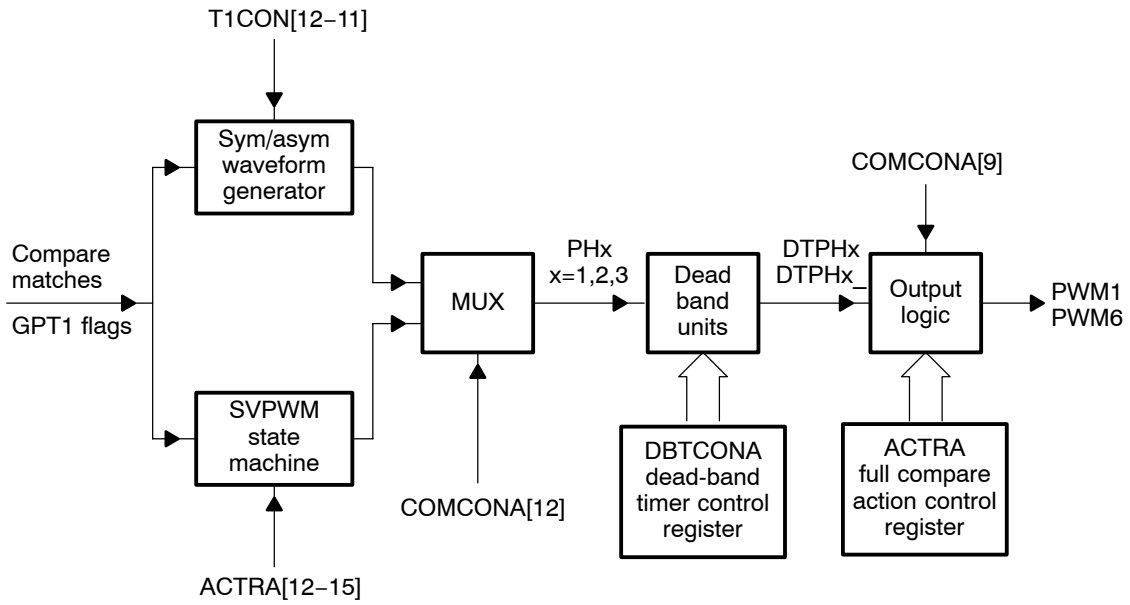
The EVA PWM circuits functional block diagram is shown in Figure 2−1. It includes the following functional units:

- Asymmetric/Symmetric Waveform Generators
- Programmable Dead-Band Unit (DBU)
- Output Logic
- Space Vector (SV) PWM State Machine

The EVB PWM circuits functional block diagram is identical to that of the EVA with the corresponding change of configuration registers.

The asymmetric/symmetric waveform generators are the same as those of the GP timers. The dead-band units and output logic are discussed in sections 2.1.2 and 2.1.5, respectively. The space vector PWM state machine and the space vector PWM technique are described later in this chapter.

Figure 2−1. PWM Circuits Block Diagram



The PWM circuits are designed to minimize CPU overhead and user intervention when generating pulse width modulated waveforms used in motor control and motion control applications. PWM generation with compare units and associated PWM circuits are controlled by the following control registers: T1CON, COMCONA, ACTRA, and DBTCONA (in case of EVA); and T3CON, COMCONB, ACTRB, and DBTCONB (in case of EVB).

2.1.1 PWM Generation Capability of Event Manager

The PWM waveform generation capability of each event manager module (A and B) is summarized as follows:

- ❏ Five independent PWM outputs, three of which are generated by the compare units; the other two are generated by the GP timer compares – plus three additional PWM outputs, dependent on the three compare unit PWM outputs
- ❏ Programmable dead-band for the PWM output pairs associated with the compare units
- ❏ Minimum dead-band duration of one device clock cycle
- ❏ Minimum PWM pulse width and pulse width increment/decrement of one clock cycle
- ❏ 16-bit maximum PWM resolution
- ❏ On-the-fly change of PWM carrier frequency (double buffered period registers)
- ❏ On-the-fly change of PWM pulse widths (double buffered compare registers)
- ❏ Power Drive Protection Interrupt
- ❏ Programmable generation of asymmetric, symmetric, and space vector PWM waveforms
- ❏ Minimum CPU overhead because of the auto-reloading of the compare and period registers

2.1.2 Programmable Dead-Band (Dead-Time) Unit

EVA and EVB have their own programmable dead-band units (DBTCONA and DBTCONB, respectively). The programmable dead-band unit features:

- One 16-bit dead-band control register, DBTCONx (RW)
- One input clock prescaler: x/1, x/2, x/4, etc., to x/32
- Device (CPU) clock input
- Three 4-bit down-counting timers
- Control logic

2.1.3 Dead-Band Timer Control Registers A and B (DBTCONA and DBTCONB)

The operation of the dead-band unit is controlled by the dead-band timer control registers (DBTCONA and DBTCONB). The bit description of DBTCONA is given in Figure 5−15 and that of DBTCONB is given in Figure 5−16.

2.1.4 Inputs and Outputs of Dead-Band Unit

The inputs to the dead-band unit are PH1, PH2, and PH3 from the asymmetric/ symmetric waveform generators of compare units 1, 2, and 3, respectively.

The outputs of the dead-band unit are DTPH1, DTPH1_, DTPH2, DTPH2_, DTPH3, and DTPH3_, corresponding to PH1, PH2, and PH3, respectively.

Dead Band Generation

For each input signal PHx, two output signals, DTPHx and DTPHx_, are generated. When dead-band is not enabled for the compare unit and its associated outputs, the two signals are exactly the same. When the dead-band unit is enabled for the compare unit, the transition edges of the two signals are separated by a time interval called dead-band. This time interval is determined by the DBTCONx bits. If you assume that the value in DBTCONx[11−8] is *m,* and that the value in DBTCONx[4−2] corresponds to prescaler *x/p,* then the dead-band value is (*p***m*) device clock cycles.

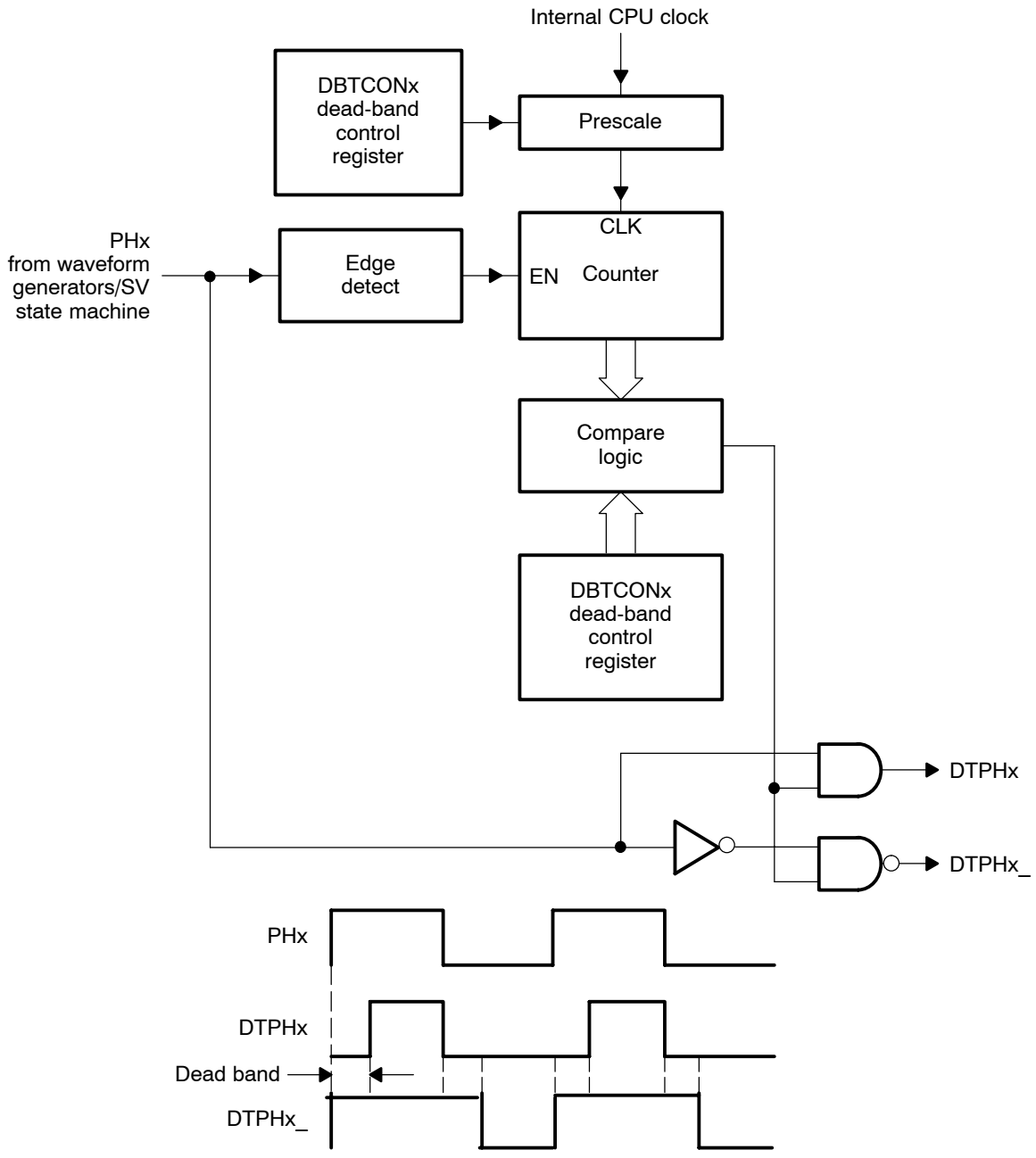
Table 2−1, on page 2-5, shows the dead-band generated by typical bit combinations in DBTCONx. The values are based on a 25-ns HSPCLK. Figure 2−2, on page 2-6, shows the block diagram of the dead-band logic for one compare unit.

Table 2–1. Dead-Band Generation Examples

DBT3–DBT0 (*m*) (DBTCONx[11–8])	DBTPS2–DBTPS0 (*p*) (DBTCONx[4–2])					
	110 and 1x1 (P=32)	100 (P=16)	011 (P=8)	010 (P=4)	001 (P=2)	000 (P=1)
0	0	0	0	0	0	0
1	0.8	0.4	0.2	0.1	0.05	0.025
2	1.6	0.8	0.4	0.2	0.1	0.05
3	2.4	1.2	0.6	0.3	0.15	0.075
4	3.2	1.6	0.8	0.4	0.2	0.1
5	4	2	1	0.5	0.25	0.125
6	4.8	2.4	1.2	0.6	0.3	0.15
7	5.6	2.8	1.4	0.7	0.35	0.175
8	6.4	3.2	1.6	0.8	0.4	0.2
9	7.2	3.6	1.8	0.9	0.45	0.225
A	8	4	2	1	0.5	0.25
B	8.8	4.4	2.2	1.1	0.55	0.275
C	9.6	4.8	2.4	1.2	0.6	0.3
D	10.4	5.2	2.6	1.3	0.65	0.325
E	11.2	5.6	2.8	1.4	0.7	0.35
F	12	6	3	1.5	0.75	0.375

Note: Table values are given in μs.

Figure 2–2. Dead-Band Unit Block Diagram (x = 1, 2, or 3)



Note: Signals such as PHx, DTPHx, and $\overline{\text{DTPHx}}$ are internal to the device, and as such, external monitoring/control of these signals is not possible.

Other Important Features of Dead-Band Units

The dead-band unit is designed to prevent an overlap under any operating situation between the turn-on period of the upper and lower devices controlled by the two PWM outputs associated with each compare unit. This includes those situations where you have loaded a dead-band value greater than that of the duty cycle, and when the duty cycle is 100% or 0%. As a result, the PWM outputs associated with a compare unit do not reset to an inactive state at the end of a period when dead band is enabled for the compare unit.

2.1.5 Output Logic

The output logic circuit determines the polarity and/or the action that must be taken on a compare match for outputs PWMx, for x = 1–6. The outputs associated with each compare unit can be specified active low, active high, forced low, or forced high. The polarity and/or the action of the PWM outputs can be programmed by proper configuration of bits in the ACTR register. The PWM output pins can all be put in the high-impedance state by any of the following:

- Software clearing the COMCONx[9] bit
- Hardware pulling $\overline{\text{PDPINTx}}$ low when $\overline{\text{PDPINTx}}$ is unmasked
- The occurrence of any reset event

Active $\overline{\text{PDPINTx}}$ (when enabled) and system reset override the bits in COMCONx and ACTRx

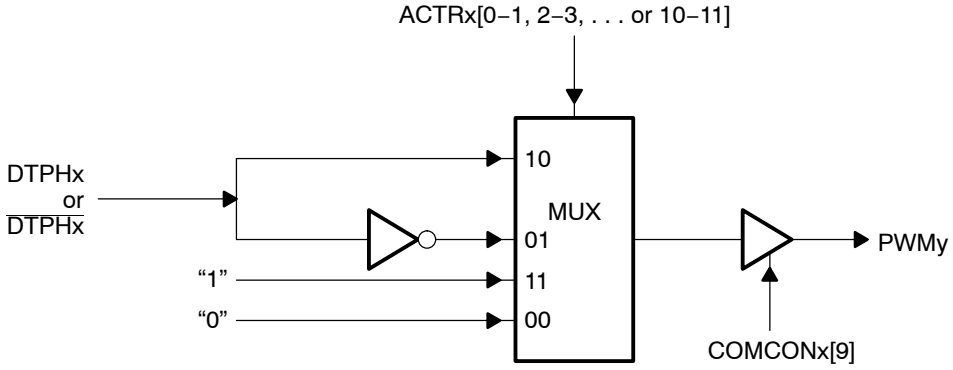
Figure 2–3, on page 2-8, shows a block diagram of the output logic circuit (OLC). The inputs of output logic for the compare units are:

- DTPH1, $\overline{\text{DTPH1}}$, DTPH2, $\overline{\text{DTPH2}}$, DTPH3, and $\overline{\text{DTPH3}}$ from the dead-band unit and compare match signals
- The control bits of ACTRx
- $\overline{\text{PDPINTx}}$ and RESET

The outputs of the Output Logic for the compare units are:

- PWMx, x = 1–6 (for EVA)
- PWMy, y = 7–12 (for EVB)

Figure 2–3. Output Logic Block Diagram (x = 1, 2, or 3; y = 1, 2, 3, 4, 5, or 6)



Output logic for PWM mode

2.2 PWM Waveform Generation

A PWM signal is a sequence of pulses with changing pulse widths. The pulses are spread over a number of fixed-length periods so that there is one pulse in each period. The fixed period is called the PWM (carrier) period and its inverse is called the PWM (carrier) frequency. The widths of the PWM pulses are determined, or modulated, from pulse to pulse according to another sequence of desired values, the modulating signal.

In a motor control system, PWM signals are used to control the on and off time of switching power devices that deliver the desired current and energy to the motor windings (see Figure 2–6 on page 2-14). The shape and frequency of the phase currents and the amount of energy delivered to the motor windings control the required speed and torque of the motor. In this case, the command voltage or current to be applied to the motor is the modulating signal. The frequency of the modulating signal is typically much lower than the PWM carrier frequency.

2.2.1 PWM Signal Generation

To generate a PWM signal, an appropriate timer is needed to repeat a counting period that is the same as the PWM period. A compare register is used to hold the modulating values. The value of the compare register is constantly compared with the value of the timer counter. When the values match, a transition (from low to high, or high to low) happens on the associated output. When a second match is made between the values, or when the end of a timer period is reached, another transition (from high to low, or low to high) happens on the associated output. In this way, an output pulse is generated whose on (or off) duration is proportional to the value in the compare register. This process is repeated for each timer period with different (modulating) values in the compare register. As a result, a PWM signal is generated at the associated output.

Dead Band

In many motion/motor and power electronics applications, two power devices, an upper and a lower, are placed in series on one power converter leg. The turn-on periods of the two devices must not overlap with each other in order to avoid a shoot-through fault. Thus, a pair of non-overlapping PWM outputs is often required to properly turn on and off the two devices. A dead time (deadband) is often inserted between the turning-off of one transistor and the turning-on of the other transistor. This delay allows complete turning-off of one transistor before the turning-on of the other transistor. The required time delay is specified by the turning-on and turning-off characteristics of the power transistors and the load characteristics in a specific application.

2.2.2 Generation of PWM Outputs With Event Manager

Each of the three compare units, together with GP timer 1 (in the case of EVA) or GP timer 3 (in the case of EVB), the dead-band unit, and the output logic in the event manager module, can be used to generate a pair of PWM outputs with programmable dead-band and output polarity on two dedicated device pins. There are six such dedicated PWM output pins associated with the three compare units in each EV module. These six dedicated output pins can be used to conveniently control 3-phase ac induction or brushless dc motors. The flexibility of output behavior control by the compare action control register (ACTRx) also makes it easy to control switched reluctance and synchronous reluctance motors in a wide range of applications. The PWM circuits can also be used to conveniently control other types of motors such as dc brush and stepper motors in single or multi-axis control applications. Each GP timer compare unit, if desired, can also generate a PWM output based on its own timer.

2.2.3 Asymmetric and Symmetric PWM Generation

Both asymmetric and symmetric PWM waveforms can be generated by every compare unit on the EV module. In addition, the three compare units together can be used to generate 3-phase symmetric space vector PWM outputs. PWM generation with GP timer compare units has been described in the GP timer sections. Generation of PWM outputs with the compare units is discussed in this section.

2.2.4 Register Setup for PWM Generation

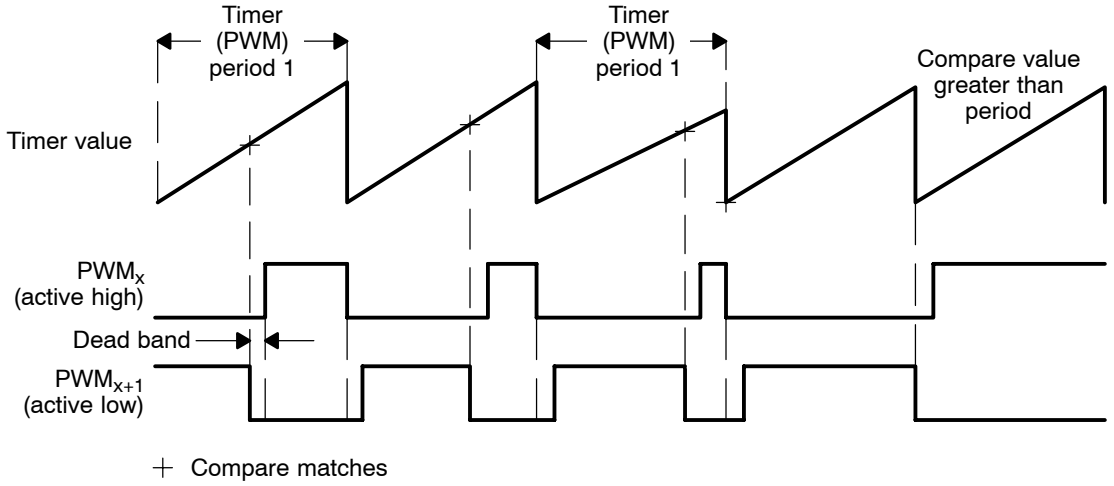
All three kinds of PWM waveform generations with compare units and associated circuits require configuration of the same Event Manager registers. The setup process for PWM generation includes the following steps:

- ❑ Setup and load ACTRx
- ❑ Setup and load DBTCONx, if dead-band is to be used
- ❑ Initialize CMPRx
- ❑ Setup and load COMCONx
- ❑ Setup and load T1CON (for EVA) or T3CON (for EVB) to start the operation
- ❑ Rewrite CMPRx with newly determined values

2.2.5 Asymmetric PWM Waveform Generation

The edge-triggered or asymmetric PWM signal is characterized by modulated pulses which are not centered with respect to the PWM period, as shown in Figure 2–4. The width of each pulse can only be changed from one side of the pulse.

Figure 2–4. Asymmetric PWM Waveform Generation With Compare Unit and PWM Circuits (x = 1, 3, or 5)



To generate an asymmetric PWM signal, GP timer 1 is put in the continuous up-counting mode and its period register is loaded with a value corresponding to the desired PWM carrier period. The COMCONx is configured to enable the compare operation, set the selected output pins to be PWM outputs, and enable the outputs. If dead-band is enabled, the value corresponding to the required dead-band time should be written by software into the DBT(3:0) bits in DBTCONx(11:8). This is the period for the 4-bit dead-band timers. One dead-band value is used for all PWM output channels.

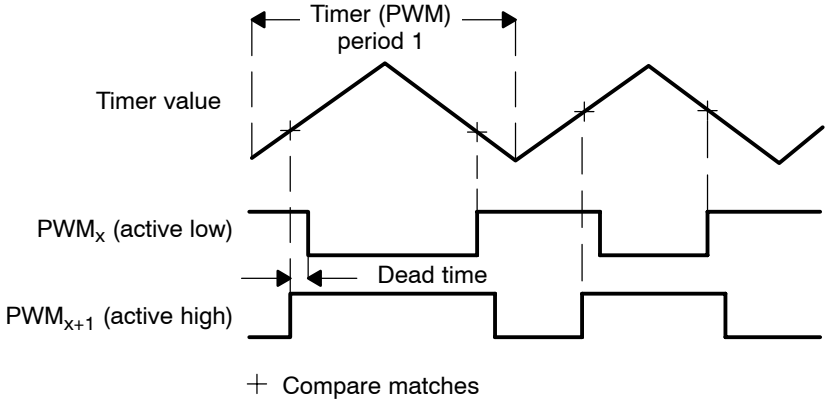
By proper configuration of ACTRx with software, a normal PWM signal can be generated on one output associated with a compare unit while the other is held low (or off) or high (or on), at the beginning, middle, or end of a PWM period. Such software controlled flexibility of PWM outputs is particularly useful in switched reluctance motor control applications.

After GP timer 1 (or GP timer 3) is started, the compare registers are rewritten every PWM period with newly determined compare values to adjust the width (the duty cycle) of PWM outputs that control the switch-on and -off duration of the power devices. Since the compare registers are shadowed, a new value can be written to them at any time during a period. For the same reason, new values can be written to the action and period registers at any time during a period to change the PWM period or to force changes in the PWM output definition.

2.2.6 Symmetric PWM Waveform Generation

A centered or symmetric PWM signal is characterized by modulated pulses which are centered with respect to each PWM period. The advantage of a symmetric PWM signal over an asymmetric PWM signal is that it has two inactive zones of the same duration: at the beginning and at the end of each PWM period. This symmetry has been shown to cause less harmonics than an asymmetric PWM signal in the phase currents of an ac motor, such as induction and dc brushless motors, when sinusoidal modulation is used. Figure 2–5 shows two examples of symmetric PWM waveforms.

Figure 2–5. Symmetric PWM Waveform Generation With Compare Units and PWM Circuits (x = 1, 3, or 5)



The generation of a symmetric PWM waveform with a compare unit is similar to the generation of an asymmetric PWM waveform. The only exception is that GP timer 1 (or GP timer 3) now needs to be put in continuous up-/down-counting mode.

There are usually two compare matches in a PWM period in symmetric PWM waveform generation, one during the upward counting before period match, and another during downward counting after period match. A new compare value becomes effective after the period match (reload on period) because it makes it possible to advance or delay the second edge of a PWM pulse. An application of this feature is when a PWM waveform modification compensates for current errors caused by the dead-band in ac motor control.

Because the compare registers are shadowed, a new value can be written to them at any time during a period. For the same reason, new values can be written to the action and period registers at any time during a period to change the PWM period or to force changes in the PWM output definition.

2.2.7 Double Update PWM Mode

The 28x Event Manager supports “Double Update PWM Mode.” This mode refers to a PWM operation mode in which the position of the leading edge and the position of the trailing edge of a PWM pulse are independently modifiable in each PWM period. To support this mode, the compare register that determines the position of the edges of a PWM pulse must allow (buffered) compare value update once at the beginning of a PWM period and another time in the middle of a PWM period.

The compare registers in 28x Event Managers are all buffered and support three compare value reload/update (value in buffer becoming active) modes. These modes have earlier been documented as compare value reload conditions. The reload condition that supports double update PWM mode is reloaded on Underflow (beginning of PWM period) OR Period (middle of PWM period). Double update PWM mode can be achieved by using this condition for compare value reload.

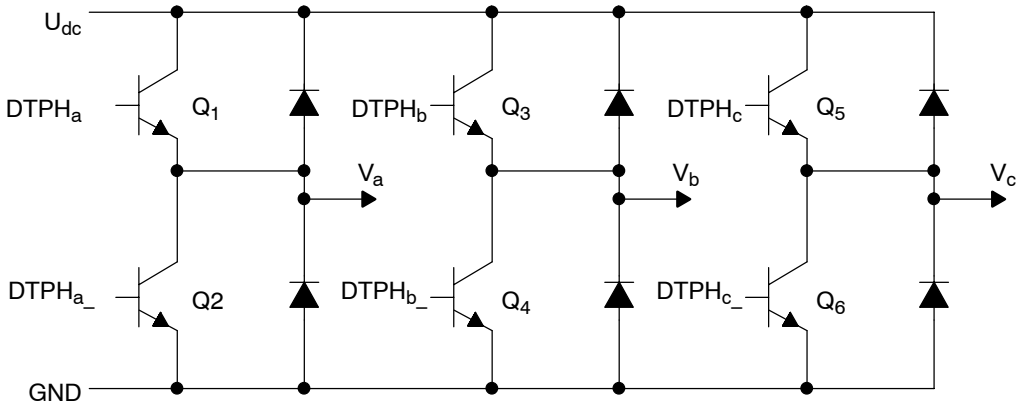
2.3 Space Vector PWM

Space vector PWM refers to a special switching scheme of the six power transistors of a 3-phase power converter. It generates minimum harmonic distortion to the currents in the windings of a 3-phase ac motor. It also provides more efficient use of supply voltage in comparison with the sinusoidal modulation method.

2.3.1 3-Phase Power Inverter

The structure of a typical 3-phase power inverter is shown in Figure 2–6, where V_a, V_b, and V_c are the voltages applied to the motor windings. The six power transistors are controlled by $DTPH_x$ and $DTPH_{x\_}$ (x = a, b, and c). When an upper transistor is switched on ($DTPH_x$ = 1), the lower transistor is switched off ($DTPH_{x\_}$ = 0). Thus, the on and off states of the upper transistors (Q1, Q3, and Q5) or, equivalently, the state of DTPHx (x = a, b, and c) are sufficient to evaluate the applied motor voltage U_{out}.

Figure 2–6. 3-Phase Power Inverter Schematic Diagram



Power Inverter Switching Patterns and the Basic Space Vectors

When an upper transistor of a leg is on, the voltage V_x (x = a, b, or c) applied by the leg to the corresponding motor winding is equal to the voltage supply U_{dc}. When it is off, the voltage applied is zero. The on and off switching of the upper transistors ($DTPH_x$, x = a, b, or c) have eight possible combinations. The eight combinations and the derived motor line-to-line and phase voltage in terms of dc supply voltage U_{dc} are shown in Table 2–2, on page 2-15, where a, b, and c represent the values of $DTPH_a$, $DTPH_b$, and $DTPH_c$, respectively.

Table 2–2. Switching Patterns of a 3-Phase Power Inverter

a	b	c	$V_{a0}(U_{dc})$	$V_{b0}(U_{dc})$	$V_{c0}(U_{dc})$	$V_{ab}(U_{dc})$	$V_{bc}(U_{dc})$	$V_{ca}(U_{dc})$
0	0	0	0	0	0	0	0	0
0	0	1	–1/3	–1/3	2/3	0	–1	1
0	1	0	–1/3	2/3	–1/3	–1	1	0
0	1	1	–2/3	1/3	1/3	–1	0	1
1	0	0	2/3	–1/3	–1/3	1	0	–1
1	0	1	1/3	–2/3	1/3	1	–1	0
1	1	0	1/3	1/3	–2/3	0	1	–1
1	1	1	0	0	0	0	0	0

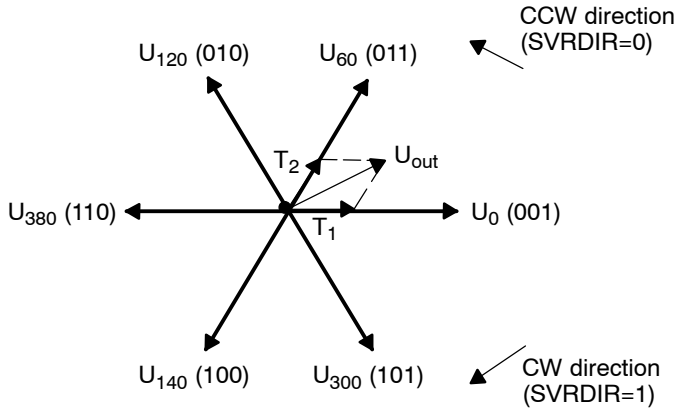
Note: 0 = off, 1 = on

Mapping the phase voltages corresponding to the eight combinations onto the d-q plane by performing a d-q transformation (which is equivalent to an orthogonal projection of the 3-vectors (a b c) onto the two dimensional plane perpendicular to the vector (1,1,1), the d-q plane), results in six nonzero vectors and two zero vectors. The nonzero vectors form the axes of a hexagonal. The angle between two adjacent vectors is 60 degrees. The two zero vectors are at the origin. These eight vectors are called the basic space vectors and are denoted by U_0, U_{60}, U_{120}, U_{180}, U_{240}, U_{300}, O_{000}, and O_{111}. The same transformation can be applied to the demanded voltage vector U_{out} to be applied to a motor. Figure 2–7 shows the projected vectors and the projected desired motor voltage vector U_{out}.

The d axis and q axis of a d-q plane correspond here to the horizontal and vertical geometrical axes of the stator of an ac machine.

The objective of the space vector PWM method is to approximate the motor voltage vector U_{out} by a combination of these eight switching patterns of the six power transistors.

Figure 2−7. Basic Space Vectors and Switching Patterns



The binary representations of two adjacent basic vectors are different in only one bit; that is, only one of the upper transistors switches when the switching pattern switches from U_x to U_{x+60} or from U_{x+60} to U_x. Also, the zero vectors O_{000} and O_{111} apply no voltage to the motor.

2.3.2 Approximation of Motor Voltage With Basic Space Vectors

The projected motor voltage vector U_{out}, at any given time, falls into one of the six sectors. Thus, for any PWM period, it can be approximated by the vector sum of two vector components lying on the two adjacent basic vectors:

$$U_{out} = T_1 U_x + T_2 U_{x+60} + T_0 (O_{000} \text{ or } O_{111})$$

where T_0 is given by $T_p - T_1 - T_2$ and T_p is the PWM carrier period. The third term on the right side of the equation does not affect the vector sum U_{out}. The generation of U_{out} is beyond the scope of this context. For more details on space vector PWM and motor control theory, see *The Field Orientation Principle in Control of Induction Motors* by Andrzej M. Trzynadlowski (The Kluwer International Series in Engineering and Computer Science, Vol. 258:Power).

The above approximation means that the upper transistors must have the on and off pattern corresponding to U_x and U_{x+60} for the time duration of T_1 and T_2, respectively, in order to apply voltage U_{out} to the motor. The inclusion of zero basic vectors helps to balance the turn on and off periods of the transistors, and thus their power dissipation.

2.3.3 Space Vector PWM Waveform Generation With Event Manager

The EV module has built-in hardware to greatly simplify the generation of symmetric space vector PWM waveforms. Software is used to generate space vector PWM outputs.

2.3.4 Software

To generate space vector PWM outputs, the user software must:

- ❑ Configure ACTRx to define the polarity of the compare output pins
- ❑ Configure COMCONx to enable compare operation and space vector PWM mode, and set the reload condition for CMPRx to be underflow
- ❑ Put GP timer 1 (or GP timer 3) in continuous up-/down-counting mode to start the operation

The user software then needs to determine the voltage U_{out} to be applied to the motor phases in the two dimensional d-q plane, decompose U_{out}, and perform the following for each PWM period:

- ❑ Determine the two adjacent vectors, U_x and U_{x+60}
- ❑ Determine the parameters T_1, T_2, and T_0
- ❑ Write the switching pattern corresponding to U_x in ACTRx[14–12] and 1 in ACTRx[15], or the switching pattern of U_{x+60} in ACTRx[14–12] and 0 in ACTRx[15]
- ❑ Put (1/2 T1) in CMPR1 and (1/2 T1 + 1/2 T2) in CMPR2

2.3.5 Space Vector PWM Hardware

The space vector PWM hardware in the EV module does the following to complete a space vector PWM period:

- ❑ At the beginning of each period, sets the PWM outputs to the (new) pattern U_y defined by ACTRx[14–12]
- ❑ On the first compare match during up-counting between CMPR1 and GP timer 1 at (1/2 T1), switches the PWM outputs to the pattern of U_{y+60} if ACTRx[15] is 1, or to the pattern of U_y if ACTRx[15] is 0 ($U_{0-60} = U_{300}$, $U_{360+60} = U_{60}$)
- ❑ On the second compare match during up-counting between CMPR2 and GP timer 1 at (1/2 T1 + 1/2 T2), switches the PWM outputs to the pattern (000) or (111), whichever differs from the second pattern by one bit
- ❑ On the first compare match during down-counting between CMPR2 and GP timer 1 at (1/2 T1 + 1/2 T2), switches the PWM outputs back to the second output pattern
- ❑ On the second compare match during down-counting between CMPR1 and GP timer 1 at (1/2 T1), switches the PWM outputs back to the first pattern

2.3.6 Space Vector PWM Waveforms

The space vector PWM waveforms generated are symmetric with respect to the middle of each PWM period; and for this reason, it is called the symmetric space vector PWM generation method. Figure 2–8 shows examples of the symmetric space vector PWM waveforms.

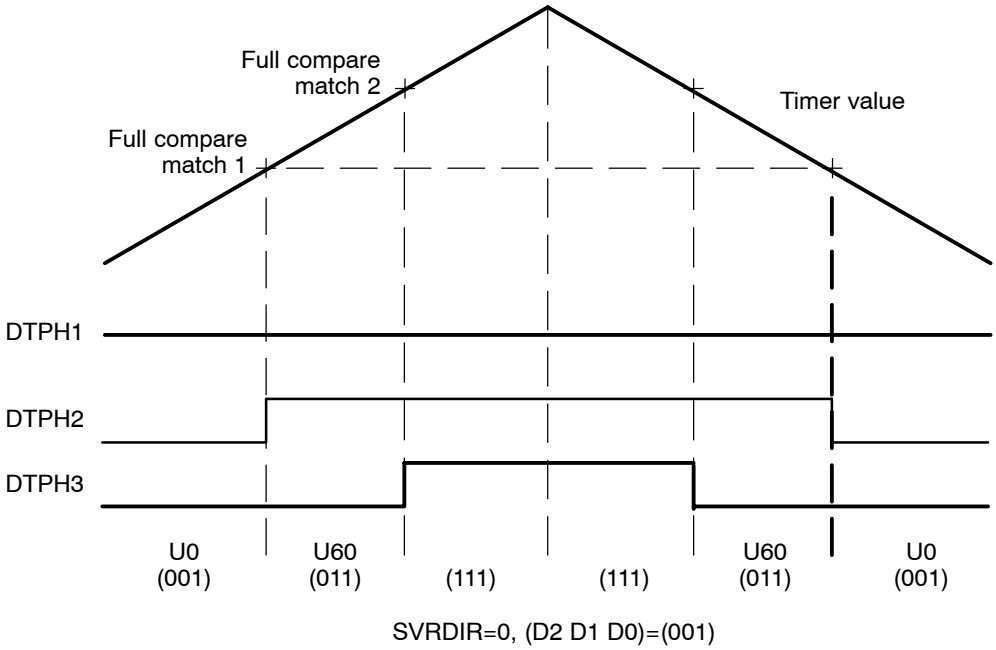
2.3.7 The Unused Compare Register

Only two compare registers are used in space vector PWM output generation. The third compare register, however, is still constantly compared with GP timer 1. When a compare match happens, the corresponding compare interrupt flag remains set and a peripheral interrupt request is generated, if the flag is unmasked. Therefore, the compare register that is not used in space vector PWM output generation can still be used to time events happening in a specific application. Also, because of the extra delay introduced by the state machine, the compare output transitions are delayed by one clock cycle in space vector PWM mode.

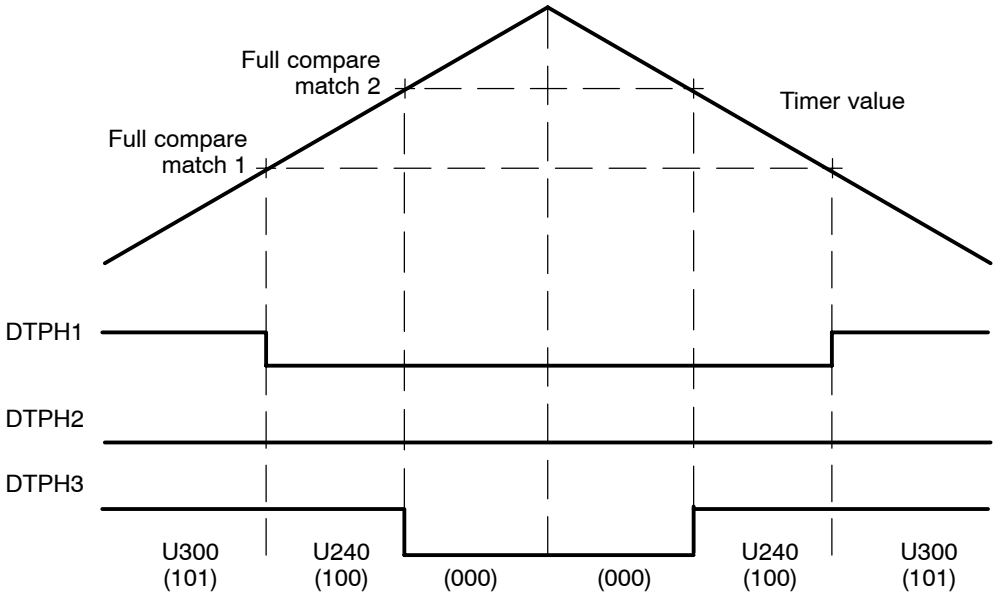
2.3.8 Space Vector PWM Boundary Conditions

All three compare outputs become inactive when both compare registers (CMPR1 and CMPR2) are loaded with a zero value in space vector PWM mode. It is the user's responsibility to assure that (CMPR1) $\leq$ (CMPR2) $\leq$ (T1PR) in the space vector PWM mode; otherwise, unpredictable behavior may result.

Figure 2–8. Symmetric Space Vector PWM Waveforms



SVRDIR=0, (D2 D1 D0)=(001)



SVRDIR=1, (D2 D1 D0)=(101)

Chapter 3

Capture Units

Capture units enable logging of transitions on capture input pins. There are six capture units, three in each EV module. Capture Units 1, 2, and 3 are associated with EVA and Capture Units 4, 5, and 6 are associated with EVB. Each capture unit is associated with a capture input pin.

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3.1 Capture Unit Overview

Each EVA capture unit can choose GP timer 2 or 1 as its time base; however, CAP1 and CAP2 cannot choose a different timer between themselves as their timebase. Each EVB capture unit can choose GP timer 4 or 3 as its time base; however, CAP4 and CAP5 cannot choose a different timer between themselves as their timebase.

The value of the GP timer is captured and stored in the corresponding 2-level-deep FIFO stack when a specified transition is detected on a capture input pin (CAPx). Figure 3–1 shows a block diagram of an EVA capture unit and Figure 3–2 shows a block diagram of an EVB capture unit.

3.1.1 Capture Unit Features

Capture units have the following features:

- One 16-bit capture control register (CAPCONA for EVA, CAPCONB for EVB), (RW)
- One 16-bit capture FIFO status register (CAPFIFOA for EVA, CAPFIFOB for EVB)
- Selection of GP timer 1 or 2 (for EVA) and GP timer 3 or 4 (for EVB) as the time base
- Three 16-bit 2-level-deep FIFO stacks, one for each capture unit
- Six Schmitt-triggered capture input pins, CAP1 through CAP6, one input pin for each capture unit. (All inputs are synchronized with the device/CPU clock: in order for a transition to be captured, the input must hold at its current level to meet the two rising edges of the device clock. If the input qualifier circuit is used, then the pulse width requirement warranted by the qualification circuitry must be met as well. Input pins CAP1 and CAP2 (CAP4 and CAP5 in case of EVB) can also be used as QEP inputs to QEP circuit).
- User-specified transition detection (rising edge, falling edge, or both edges)
- Six maskable interrupt flags, one for each capture unit

Figure 3–1. Capture Units Block Diagram (EVA)

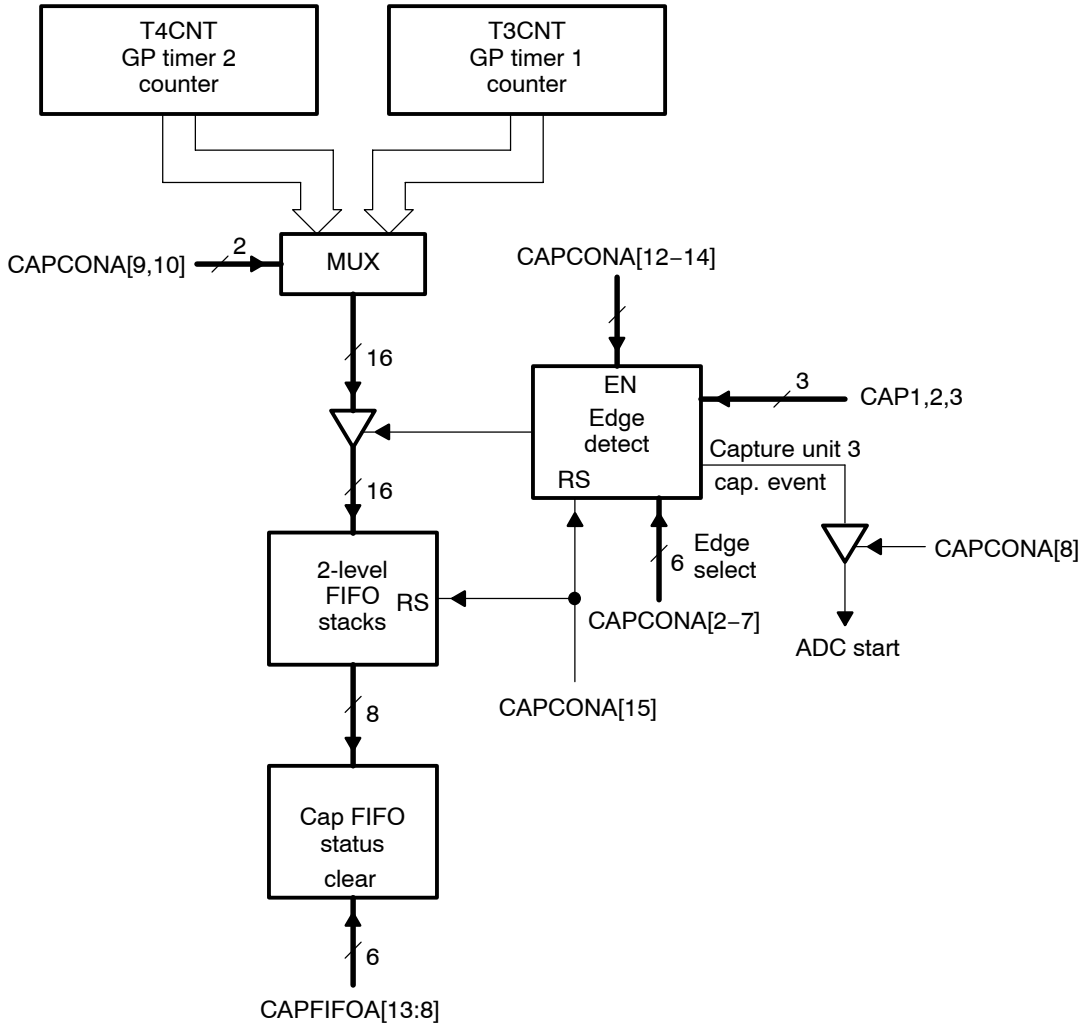
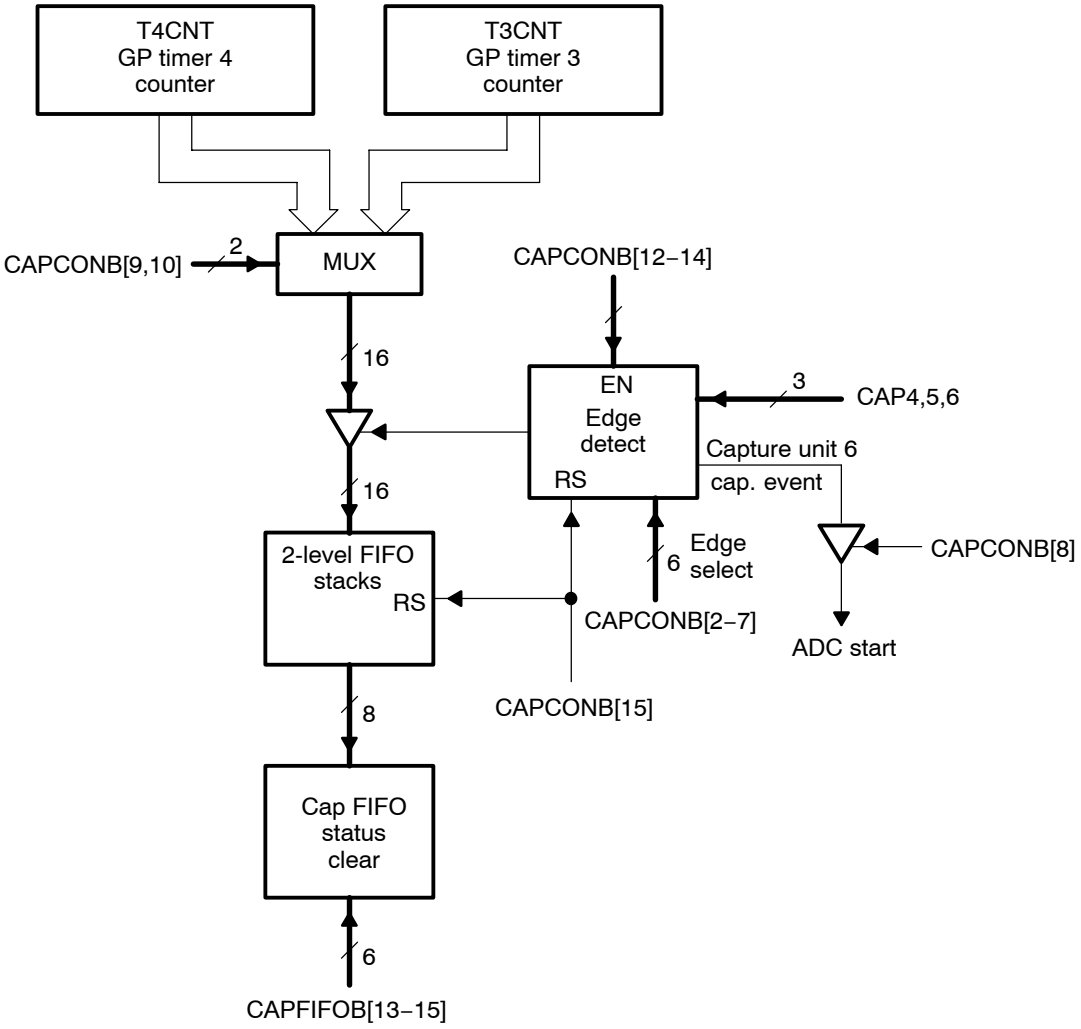


Figure 3–2. Capture Units Block Diagram (EVB)



3.2 Operation of Capture Units

After a capture unit is enabled, a specified transition on the associated input pin causes the counter value of the selected GP timer to be loaded into the corresponding FIFO stack. At the same time, if there are already one or more valid capture values stored in the FIFO stack (CAPxFIFO bits not equal to zero), the corresponding interrupt flag is set. If the flag is unmasked, a peripheral interrupt request is generated. The corresponding status bits in CAPFIFOx are adjusted to reflect the new status of the FIFO stack each time a new counter value is captured in a FIFO stack. The latency from the time a transition happens in a capture input to the time the counter value of the selected GP timer is locked is two clock cycles. This does not include any additional latency due to the input qualifier circuitry.

All capture unit registers are cleared to zero by a RESET condition.

3.2.1 Capture Unit Time Base Selection

For EVA, Capture Unit 3 has a separate time base selection bit from Capture Units 1 and 2. This allows the two GP timers to be used at the same time, one for Capture Units 1 and 2, and the other for Capture Unit 3. For EVB, Capture Unit 6 has a separate time-base selection bit.

Capture operation does not affect the operation of any GP timer or the compare/PWM operations associated with any GP timer.

3.2.2 Capture Unit Setup

For a capture unit to function properly, the following register setup must be performed:

1) Initialize the CAPFIFOx and clear the appropriate status bits.

2) Set the selected GP timer in one of its operating modes.

3) Set the associated GP timer compare register or GP timer period register, if necessary.

4) Set up CAPCONA or CAPCONB as appropriate.

3.3 Capture Unit FIFO Stacks

Each capture unit has a dedicated 2-level-deep FIFO stack. The top stack consists of CAP1FIFO, CAP2FIFO, and CAP3FIFO (in the case of EVA) or CAP4FIFO, CAP5FIFO, and CAP6FIFO (in the case of EVB). The bottom stack consists of CAP1FBOT, CAP2FBOT, and CAP3FBOT (in the case of EVA) or CAP4FBOT, CAP5FBOT, and CAP6FBOT (in the case of EVB). The top-level register of any of the FIFO stacks is a read-only register that always contains the oldest counter value captured by the corresponding capture unit. Therefore, a read access to the FIFO stack of a capture unit always returns the oldest counter value stored in the stack. When the oldest counter value in the top register of the FIFO stack is read, the newer counter value in the bottom register of the stack, if any, is pushed into the top register.

If desired, the bottom register of the FIFO stack can be read. Reading the bottom register of the FIFO stack causes the FIFO status bits to change to 01 (has one entry) if they were previously 10 or 11. If the FIFO status bits were previously 01 when the bottom FIFO register is read, they will change to 00 (empty).

3.3.1 First Capture

The counter value of the selected GP timer (captured by a capture unit when a specified transition happens on its input pin) is written into the top register of the FIFO stack, if the stack is empty. At the same time, the corresponding status bits are set to 01. The status bits are reset to 00 if a read access is made to the FIFO stack before another capture is made.

3.3.2 Second Capture

If another capture occurs before the previously captured counter value is read, the newly captured counter value goes to the bottom register. In the meantime, the corresponding status bits are set to 10. When the FIFO stack is read before another capture happens, the older counter value in the top register is read out, the newer counter value in the bottom register is pushed up into the top register, and the corresponding status bits are set to 01.

The appropriate capture interrupt flag is set by the second capture. A peripheral interrupt request is generated if the interrupt is not masked.

3.3.3 Third Capture

If a capture happens when there are already two counter values captured in the FIFO stack, the oldest counter value in the top register of the stack is pushed out and lost, the counter value in the bottom register of the stack is pushed up into the top register, the newly captured counter value is written into the bottom register, and the status bits are set to 11 to indicate that one or more older captured counter values have been lost.

The appropriate capture interrupt flag is also set by the third capture. A peripheral interrupt request is generated if the interrupt is not masked.

3.4 Capture Interrupt

When a capture is made by a capture unit and there is already at least one valid value in the FIFO (indicated by CAPxFIFO bits not equal to zero), the corresponding interrupt flag is set, and if unmasked, a peripheral interrupt request is generated. Thus, a pair of captured counter values can be read by an interrupt service routine if the interrupt is used. If an interrupt is not desired, either the interrupt flag or the status bits can be polled to determine if two captures have occurred allowing the captured counter values to be read.

3.5 Quadrature Encoder Pulse (QEP) Circuit

Each Event Manager module has a quadrature encoder pulse (QEP) circuit. The QEP circuit, when enabled, decodes and counts the quadrature encoded input pulses on pins CAP1/QEP1 and CAP2/QEP2 (in case of EVA) or CAP4/QEP3 and CAP5/QEP4 (in case of EVB). The QEP circuit can be used to interface with an optical encoder to get position and speed information from a rotating machine. When the QEP circuit is enabled, the capture function on CAP1/CAP2 and CAP4/CAP5 pins is disabled.

3.5.1 QEP Pins

The three QEP input pins are shared between capture units 1, 2, and 3 (or 3, 4, and 5, for EVB), and the QEP circuit.

3.5.2 QEP Circuit Time Base

The time base for the QEP circuit is provided by GP timer 2 (GP timer 4, in case of EVB). The GP timer must be put in directional-up/down count mode with the QEP circuit as the clock source. Figure 3–3 shows the block diagram of the QEP circuit for EVA and Figure 3–4 shows the block diagram of the QEP circuit for EVB.

Figure 3–3. Quadrature Encoder Pulse (QEP) Circuit Block Diagram for EVA

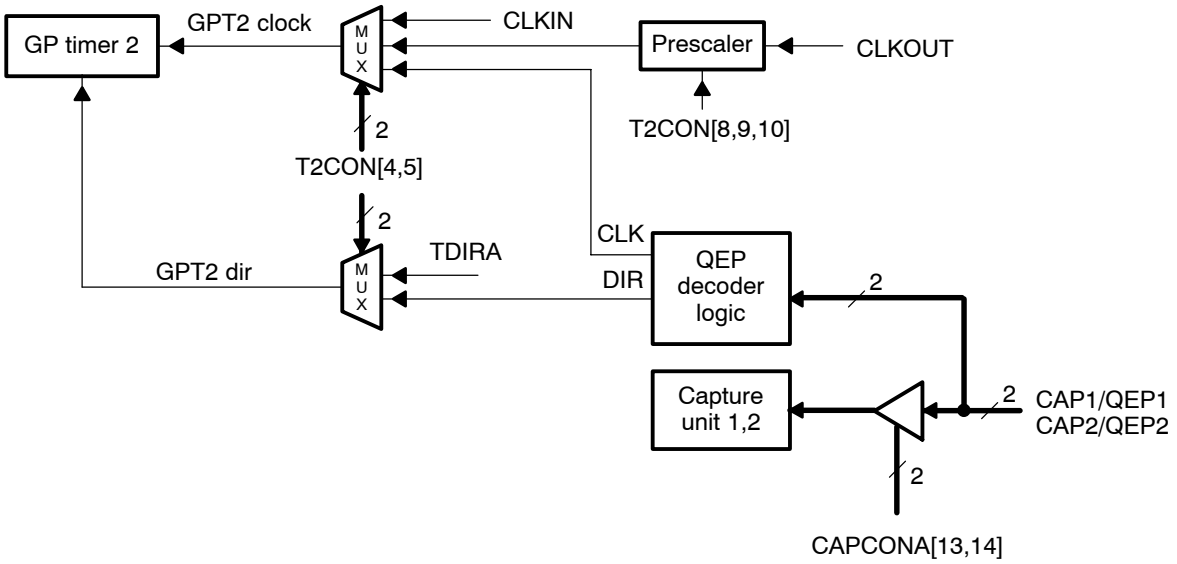
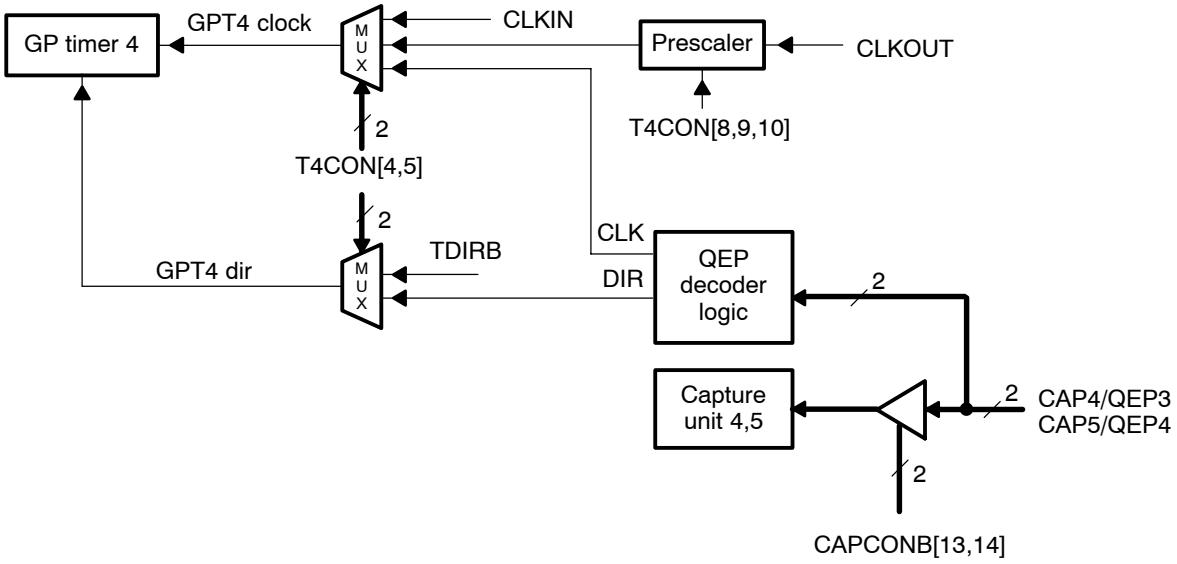


Figure 3–4. Quadrature Encoder Pulse (QEP) Circuit Block Diagram for EVB



3.5.3 Decoding

Quadrature encoded pulses are two sequences of pulses with a variable frequency and a fixed phase shift of a quarter of a period (90 degrees). When generated by an optical encoder on a motor shaft, the direction of rotation of the motor can be determined by detecting which of the two sequences is the leading sequence. The angular position and speed can be determined by the pulse count and pulse frequency.

QEP Circuit

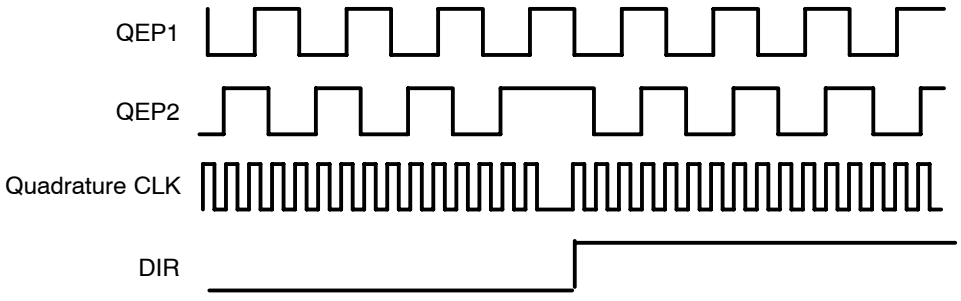
The direction detection logic of the QEP circuit in the EV module determines which one of the sequences is the leading sequence. It then generates a direction signal as the direction input to GP timer 2 (or 4). The timer counts up if CAP1/QEP1 (CAP4/QEP3 for EVB) input is the leading sequence, and counts down if CAP2/QEP2 (CAP5/QEP4 for EVB) is the leading sequence.

Both edges of the pulses of the two quadrature encoded inputs are counted by the QEP circuit. Therefore, the frequency of the clock generated by the QEP logic to GP timer 2 (or 4) is four times that of each input sequence. This quadrature clock is connected to the clock input of GP timer 2 (or 4).

Quadrature Encoded Pulse Decoding Example

Figure 3–5 shows an example of quadrature encoded pulses and the derived clock and counting direction.

Figure 3–5. Quadrature Encoded Pulses and Decoded Timer Clock and Direction



3.5.4 QEP Counting

GP timer 2 (or 4) always starts counting from its current value. A desired value can be loaded to the GP timer's counter prior to enabling the QEP mode. When the QEP circuit is selected as the clock source, the timer ignores the TDIRA/B and TCLKINA/B input pins.

GP Timer Interrupt and Associated Compare Outputs in QEP Operation

Period, underflow, overflow, and compare interrupt flags for a GP timer with a QEP circuit clock are generated on respective matches. A peripheral interrupt request can be generated by an interrupt flag, if the interrupt is unmasked.

3.5.5 Register Setup for the QEP Circuit

To start the operation of the QEP circuit in EVA:

1) Load GP timer 2's counter, period, and compare registers with desired values, if necessary

2) Configure T2CON to set GP timer 2 in directional-up/down mode with the QEP circuits as clock source, and enable the selected timer

To start the operation of the QEP circuit in EVB:

1) Load GP timer 4s counter, period, and compare registers with desired values, if necessary

2) Configure T4CON to set GP timer 4 in directional-up/down mode with the QEP circuits as clock source, and enable the selected timer

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Chapter 4

EV Interrupts

This chapter explains the organization of interrupts and describes how to request them.

Topic **Page**

4.1 Event Manager (EV) Interrupt Overview

EV interrupt events are organized into three groups: A, B, and C. Each group is associated with a different interrupt flag and interrupt enable register. There are several event manager peripheral interrupt requests in each EV interrupt group. Table 4−2 shows all EVA interrupts, their priority, and grouping; and Table 4−3 shows all EVB interrupts, their priority, and grouping. There is an interrupt flag register and a corresponding interrupt mask register for each EV interrupt group, as shown in Table 4−1. A flag in EVAIFRx (x = A, B, or C) is masked (will not generate a peripheral interrupt request) if the corresponding bit in EVAIMRx is zero.

Table 4−1. Interrupt Flag Register and Corresponding Interrupt Mask Register

Flag Register	Mask Register	EV Module
EVAIFRA	EVAIMRA	EVA
EVAIFRB	EVAIMRB	
EVAIFRC	EVAIMRC	
EVBIFRA	EVBIMRA	EVB
EVBIFRB	EVBIMRB	
EVBIFRC	EVBIMRC	

4.2 EV Interrupt Request and Service

When a peripheral interrupt request is acknowledged, the appropriate peripheral interrupt vector is loaded into the peripheral interrupt vector register (PIVR) by the PIE controller. The vector loaded into the PIVR is the vector for the highest priority pending enabled event. The vector register can be read by the interrupt service routine (ISR).

Table 4–2. Event Manager A (EVA) Interrupts

Group	Interrupt	Priority within group	Vector (ID)†	Description/Source	INT
A	$\overline{\text{PDPINTA}}$	1 (highest)	0020h	Power Drive Protection Interrupt A	1
A	CMP1INT	2	0021h	Compare Unit 1 compare interrupt	2
	CMP2INT	3	0022h	Compare Unit 2 compare interrupt	
	CMP3INT	4	0023h	Compare Unit 3 compare interrupt	
	T1PINT	5	0027h	GP timer 1 period interrupt	
	T1CINT	6	0028h	GP timer 1 compare interrupt	
	T1UFINT	7	0029h	GP timer 1 underflow interrupt	
	T1OFINT	8	002Ah	GP timer 1 overflow interrupt	
B	T2PINT	1	002Bh	GP timer 2 period interrupt	3
	T2CINT	2	002Ch	GP timer 2 compare interrupt	
	T2UFINT	3	002Dh	GP timer 2 underflow interrupt	
	T2OFINT	4	002Eh	GP timer 2 overflow interrupt	
C	CAP1INT	1	0033h	Capture Unit 1 interrupt	3
	CAP2INT	2	0034h	Capture Unit 2 interrupt	
	CAP3INT	3 (lowest)	0035h	Capture Unit 3 interrupt	

† The Vector ID is used by DSP/BIOS.

Table 4−3. Event Manager B (EVB) Interrupts

Group	Interrupt	Priority within group	Vector (ID)†	Description/Source	INT
A	PDPINTB	1 (highest)	0019h	Power Drive Protection Interrupt B	1
A	CMP4INT	2	0024h	Compare Unit 4 compare interrupt	
	CMP5INT	3	0025h	Compare Unit 5 compare interrupt	
	CMP6INT	4	0026h	Compare Unit 6 compare interrupt	
	T3PINT	5	002Fh	GP timer 3 period interrupt	4
	T3CINT	6	0030h	GP timer 3 compare interrupt	
	T3UFINT	7	0031h	GP timer 3 underflow interrupt	
	T3OFINT	8	0032h	GP timer 3 overflow interrupt	
B	T4PINT	1	0039h	GP timer 4 period interrupt	
	T4CINT	2	003Ah	GP timer 4 compare interrupt	5
	T4UFINT	3	003Bh	GP timer 4 underflow interrupt	
	T4OFINT	4	003Ch	GP timer 4 overflow interrupt	
C	CAP4INT	1	0036h	Capture Unit 4 interrupt	
	CAP5INT	2	0037h	Capture Unit 5 interrupt	5
	CAP6INT	3 (lowest)	0038h	Capture Unit 6 interrupt	

† The Vector ID is used by DSP/BIOS.

Table 4−4. Conditions for Interrupt Generation

Interrupt	Condition For Generation
Underflow	When the counter reaches 0000h
Overflow	When the counter reaches FFFFh
Compare	When the counter register contents match that of the compare register
Period	When the counter register contents match that of the period register

4.2.1 Interrupt Generation

When an interrupt event occurs in the EV module, the corresponding interrupt flag in one of the EV interrupt flag registers is set to one. A peripheral interrupt request is generated to the Peripheral Interrupt Expansion controller, if the flag is locally unmasked (the corresponding bit in EVAIMRx is set to one).

4.2.2 Interrupt Vector

The peripheral interrupt vector corresponding to the interrupt flag that has the highest priority among the flags that are set and enabled is loaded into the PIVR when an interrupt request is acknowledged (this is all done in the peripheral interrupt controller, external to the event manager peripheral).

Note: Failure to Clear the Interrupt Flag Bit

The interrupt flag bit in the peripheral register must be cleared by software writing a 1 to the bit in the ISR. Failure to clear this bit will prevent future interrupt requests by that source.

Chapter 5

EV Registers

This chapter includes all of the event manager (EV) registers, grouped by function.

Topic **Page**

5.1 Register Overview

All EV-A registers are listed in Table 1–2 and EV-B registers are listed in Table 1–3.

5.2 Timer Registers

The timer registers include the following:

- Timer 1 Counter Register (T1CNT) — Address 7401h
- Timer 1 Compare Register (T1CMPR) — Address 7402h
- Timer 1 Period Register (T1PR) — Address 7403h
- Timer 2 Counter Register (T2CNT) — Address 7405h
- Timer 2 Compare Register (T2CMPR) — Address 7406h
- Timer 2 Period Register (T2PR) — Address 7407h
- Timer 3 Counter Register (T3CNT) — Address 7501h
- Timer 3 Compare Register (T3CMPR) — Address 7502h
- Timer 3 Period Register (T3PR) — Address 7503h
- Timer 4 Counter Register (T4CNT) — Address 7505h
- Timer 4 Compare Register (T4CMPR) — Address 7506h
- Timer 4 Period Register (T4PR) — Address 7507h
- Timer 1 Control Register (T1CON) — Address 7404h
- Timer 2 Control Register (T2CON) — Address 7408h
- Timer 3 Control Register (T3CON) — Address 7504h
- Timer 4 Control Register (T4CON) — Address 7508h

Note:

All of these registers are separate and, therefore, independently configurable.

The generic form of each of these registers is shown in Figure 5–1 through Figure 5–6.

Figure 5–1. Timer x Counter Register (TxCNT, where x = 1, 2, 3, or 4)

15	0
T1CNT	
R/W-x	

Legend: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15:0	T1CNT	Holds the instantaneous value of Timer 1 counter

Figure 5–2. Timer x Compare Register (TxCMPR, where x = 1, 2, 3, or 4)

15	0
T1CMPR	
R/W-x	

Legend: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15:0	T1CMPR	Holds the compare value of Timer 1 counter

Figure 5–3. Timer x Period Register (TxPR, where x = 1, 2, 3, or 4)

15	0
T1PR	
R/W-x	

Legend: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15:0	T1PR	Holds the period value of Timer 1 counter

The bit definition of the individual GP timer control registers, TxCON, is shown in Figure 5–4. The bit definition of the overall GP timer control registers, GPTCONA and GPTCONB, are shown in Figure 5–5 (on page 5-5) and Figure 5–6 (on page 5-8), respectively.

Note:

Each Timer Control Register (TxCON) is independently configurable.

Figure 5–4. Timer x Control Register (TxCON; x = 1, 2, 3, or 4)

15	14	13	12	11	10	9	8
Free	Soft	Reserved	TMODE1	TMODE0	TPS2	TPS1	TPS0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

7	6	5	4	3	2	1	0
T2SWT1/ T4SWT3†	TENABLE	TCLKS1	TCLKS0	TCLD1	TCLD0	TECMPR	SELT1PR/ SELT3PR†
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

Legend: R = Read access, W = Write access, -0 = value after reset
† Reserved in T1CON and in T3CON

Figure 5−4. Timer x Control Register (TxCON; x = 1, 2, 3, or 4) (Continued)

Bit(s)	Name	Description
15:14	FREE, SOFT	Emulation control bits 00 Stop immediately on emulation suspend 01 Stop after current timer period is complete on emulation suspend 10 Operation is not affected by emulation suspend 11 Operation is not affected by emulation suspend
13	Reserved	Reads return zero, writes have no effect.
12−11	TMODE1−TMODE0	Count mode selection 00 Stop/Hold 01 Continuous-Up/-Down Count Mode 10 Continuous-Up Count Mode 11 Directional-Up/-Down Count Mode
10−8	TPS2−TPS0	Input clock prescaler 000 x/1 001 x/2 010 x/4 011 x/8 100 x/16 101 x/32 110 x/64 111 x/128 (x = HSPCLK)
7	T2SWT1 T4SWT3	T2SWT1. For EVA, this bit is T2SWT1. (GP timer 2 starts with GP timer 1.) Start GP timer 2 with GP timer 1's timer enable bit. This bit is reserved in T1CON. T4SWT3. For EVB, this bit is T4SWT3. (GP timer 4 starts with GP timer 3.) Start GP timer 4 with GP timer 3's timer-enable bit. This bit is reserved in T3CON. 0 Use own TENABLE bit 1 Use TENABLE bit of T1CON (in case of EVA) or T3CON (in case of EVB) to enable and disable operation ignoring own TENABLE bit
6	TENABLE	Timer enable 0 Disable timer operation (the timer is put in hold and the prescaler counter is reset) 1 Enable timer operations

Figure 5–4. Timer x Control Register (TxCON; x = 1, 2, 3, or 4) (Continued)

Bit(s)	Name	Description
5–4	TCLKS(1,0)	Clock source 00 Internal (i.e., HSPCLK) 01 External (i.e., TCLKINx) 10 Reserved 11 QEP circuit
3–2	TCLD(1,0)	Timer compare register reload condition 00 When counter is 0 01 When counter value is 0 or equals period register value 10 Immediately 11 Reserved
1	TECMPR	Timer compare enable 0 Disable timer compare operation 1 Enable timer compare operation
0	SELT1PR, SELT3PR	SELT1PR. In the case of EVA, this bit is SELT1PR (Period register select). When set to 1 in T2CON, the period register of Timer 1 is chosen for Timer 2 also, ignoring the period register of Timer 2. This bit is a reserved bit in T1CON. SELT3PR. In the case of EVB, this bit is SELT3PR (Period register select). When set to 1 in T4CON, the period register of Timer 3 is chosen for Timer 4 also, ignoring the period register of Timer 4. This bit is a reserved bit in T3CON. 0 Use own period register 1 Use T1PR (in case of EVA) or T3PR (in case of EVB) as period register ignoring own period register

Figure 5–5. GP Timer Control Register A (GPTCONA) — Address 7400h

15	14	13	12	11	10	9	8
Reserved	T2STAT	T1STAT	T2CTRIPE	T1CTRIPE	T2TOADC		T1TOADC
R-0	R-1	R-1	R/W-1	R/W-1	R/W-0		R/W-0

7	6	5	4	3	2	1	0
T1TOADC	TCMPOE	T2CMPOE	T1CMPOE	T2PIN		T1PIN	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	

Note: R = Read access, W = Write access, -n = value after reset

Figure 5−5.GP Timer Control Register A (GPTCONA) — Address 7400h (Continued)

Bit(s)	Name	Description
15	Reserved	Reads return zero; writes have no effect.
14	T2STAT	GP timer 2 Status. Read only 0 Counting downward 1 Counting upward
13	T1STAT	GP timer 1 Status. Read only 0 Counting downward 1 Counting upward
12	T2CTRIPE	T2CTRIP Enable. This bit, when active, enables and disables Timer 2 Compare Trip (T2CTRIP). This bit is active only when EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. 0 T2CTRIP is disabled. T2CTRIP does not affect Timer 2 compare output, GPTCON(5), or PDPINT flag (EVIFRA(0)). 1 T2CTRIP is enabled. When T2CTRIP is low, Timer 2 compare output goes into HI-Z state, GPTCON(5) is reset to zero, and PDPINT flag [EVIFRA(0)] is set to one.
11	T1CTRIPE	T1CTRIP Enable. This bit, when active, enables and disables Timer 1 Compare Trip (T1CTRIP) input. This bit is active only when EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. 0 T1CTRIP is disabled. T1CTRIP does not affect Timer 1 compare output, GPTCON(4), or PDPINT flag (EVIFRA(0)). 1 T1CTRIP is enabled. When T1CTRIP is low, Timer 1 compare output goes into HI-Z state, GPTCON(4) is reset to zero, and PDPINT flag (EVIFRA(0)) is set to one.
10−9	T2TOADC	Start ADC with timer 2 event 00 No event starts ADC 01 Setting of underflow interrupt flag starts ADC 10 Setting of period interrupt flag starts ADC 11 Setting of compare interrupt flag starts ADC

Notes: 1) Both GPTCON[12] and GPTCON[11] default to 1 when EXTCON[0] is first set to 1.

2) MUXs replace GPTCON[6] and (EVIMRA(0) | PDPINT) to drive the enabling and disabling of T1PWM_T1CMP and T2PWM_T2CMP outputs separately. Both MUXs are controlled by EXTCON(0):
− When EXTCON(0) = 0, both MUXs select GPTCON(6) and (!EVIMRA(0) | PDPINT).
− When EXTCON(1) = 1, the MUX for T1PWM_T1CMP selects GPTCON(4), and the MUX for T2PWM_T2CMP selects GPTCON(5).

3) (!EVIMRA(0) | PDPINT) represents the asynchronous path of PDPINT pin to the compare output buffers existing in the 240x™ design.

Figure 5−5.GP Timer Control Register A (GPTCONA) — Address 7400h (Continued)

Bit(s)	Name	Description
8−7	T1TOADC	Start ADC with timer 1 event 00 No event starts ADC 01 Setting of underflow interrupt flag starts ADC 10 Setting of period interrupt flag starts ADC 11 Setting of compare interrupt flag starts ADC
6	TCMPOE	Timer compare output enable. This bit, when active, enables and disables timer compare outputs. This bit is active only if EXTCON(0) = 0. This bit is reserved when EXTCON(0) = 1. This bit, when active, is reset to zero when both PDPINT/T1CTRIP are low and EVIMRA(0) = 1. 0 Timer compare outputs, T1/2PWM_T1/2CMP, are in high-impedance state. 1 Timer compare outputs, T1/2PWM_T1/2CMP, are driven by individual timer compare logic.
5	T2CMPOE	Timer 2 compare output enable. This bit, when active, enables and disables EV Timer 2 compare output, T2PWM_T1CMP. This bit is active only if EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. This bit, when active, is reset to zero when T2CTRIP is low and is also enabled. 0 Timer 2 compare output, T2PWM_T2CMP, is in high-impedance state. 1 Timer 2 compare outputs T2PWM_T2CMP, is driven by individual timer 2 compare logic.
4	T1CMPOE	Timer 1 Compare Output Enable. This bit, when active, enables or disables EV Timer 1 compare output T1PWM_T1CMP. This bit is active only when EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. This bit, when active is reset to zero when T1CTRIP is low and is also enabled. 0 Timer 1 compare output, T1PWM_T1CMP, is in HI−z state. 1 Timer 1 compare output, T1PWM_T1CMP, is driven by Timer 1 compare logic.
3−2	T2PIN	Polarity of GP timer 2 compare output 00 Forced low 01 Active low 10 Active high 11 Forced high

Notes: 1) Both GPTCON[12] and GPTCON[11] default to 1 when EXTCON[0] is first set to 1.

2) MUXs replace GPTCON[6] and (EVIMRA(0) | PDPINT) to drive the enabling and disabling of T1PWM_T1CMP and T2PWM_T2CMP outputs separately. Both MUXs are controlled by EXTCON(0):
− When EXTCON(0) = 0, both MUXs select GPTCON(6) and (!EVIMRA(0) | PDPINT).
− When EXTCON(1) = 1, the MUX for T1PWM_T1CMP selects GPTCON(4), and the MUX for T2PWM_T2CMP selects GPTCON(5).

3) (!EVIMRA(0) | PDPINT) represents the asynchronous path of PDPINT pin to the compare output buffers existing in the 240x™ design.

Figure 5−5.GP Timer Control Register A (GPTCONA) — Address 7400h (Continued)

Bit(s)	Name	Description
1−0	T1PIN	Polarity of GP timer 1 compare output 00 Forced low 01 Active low 10 Active high 11 Forced high

Notes: 1) Both GPTCON[12] and GPTCON[11] default to 1 when EXTCON[0] is first set to 1.

2) MUXs replace GPTCON[6] and (EVIMRA(0) | PDPINT) to drive the enabling and disabling of T1PWM_T1CMP and T2PWM_T2CMP outputs separately. Both MUXs are controlled by EXTCON(0):
− When EXTCON(0) = 0, both MUXs select GPTCON(6) and (!EVIMRA(0) | PDPINT).
− When EXTCON(1) = 1, the MUX for T1PWM_T1CMP selects GPTCON(4), and the MUX for T2PWM_T2CMP selects GPTCON(5).

3) (!EVIMRA(0) | PDPINT) represents the asynchronous path of PDPINT pin to the compare output buffers existing in the 240x™ design.

Figure 5−6. GP Timer Control Register B (GPTCONB) — Address 7500h

15	14	13	12	11	10	9	8
Reserved	T4STAT	T3STAT	T4CTRIPE	T3CTRIPE	T4TOADC		T3TOADC
R/W-0	R-1	R-1	R/W-1	R/W-1	R/W-0		R/W-0

7	6	5	4	3	2	1	0
T3TOADC	TCMPOE	T4CMPOE	T3CMPOE	T4PIN		T3PIN	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	

Note: R = Read access, W = Write access, -n = value after reset

Bit(s)	Name	Description
15	Reserved	Reads return zero; writes have no effect.
14	T4STAT	GP timer 4 Status. Read only 0 Counting downward 1 Counting upward
13	T3STAT	GP timer 3 Status. Read only 0 Counting downward 1 Counting upward
12	T4CTRIPE	T4CTRIP Enable. This bit, when active, enables and disables Timer 4 Compare Trip (T4CTRIP). This bit is active only when EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. 0 T4CTRIP is disabled. T4CTRIP does not affect Timer 4 compare output, GPTCON(5), or PDPINT flag (EVIFRA(0)). 1 T4CTRIP is enabled. When T4CTRIP is low, Timer 4 compare output goes into HI-Z state, GPTCON(5) is reset to zero, and PDPINT flag [EVIFRA(0)] is set to one.

Figure 5−6.GP Timer Control Register B (GPTCONB) — Address 7500h (Continued)

Bit(s)	Name	Description
11	T3CTRIPE	T3CTRIP Enable. This bit, when active, enables and disables Timer 3 Compare Trip (T3CTRIP) input. This bit is active only when EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. 0 T3CTRIP is disabled. T3CTRIP does not affect Timer 3 compare output, GPTCON(4), or PDPINT flag (EVIFRA(0)). 1 T3CTRIP is enabled. When T3CTRIP is low, Timer 3 compare output goes into HI-Z state, GPTCON(4) is reset to zero, and PDPINT flag (EVIFRA(0)) is set to one.
10−9	T4TOADC	Start ADC with timer 4 event 00 No event starts ADC 01 Setting of underflow interrupt flag starts ADC 10 Setting of period interrupt flag starts ADC 11 Setting of compare interrupt flag starts ADC
8−7	T3TOADC	Start ADC with timer 3 event 00 No event starts ADC 01 Setting of underflow interrupt flag starts ADC 10 Setting of period interrupt flag starts ADC 11 Setting of compare interrupt flag starts ADC
6	TCMPOE	Compare output enable. If $\overline{\text{PDPINTx}}$ is active, this bit it set to zero. 0 Disable all GP timer compare outputs (all compare outputs are put in the high-impedance state) 1 Enable all GP timer compare outputs
5	T4CMPOE	Timer 4 compare output enable. This bit, when active, enables and disables EV Timer 4 compare output, T4PWM_T4CMP. This bit is active only if EXTCON(0) = 0. This bit is reserved when EXTCON(0) = 1. This bit, when active, is reset to zero when T4CTRIP is low and is also enabled. 0 Timer 4 compare output, T4PWM_T4CMP, is in high-impedance state. 1 Timer 4 compare outputs T4PWM_T4CMP, is driven by individual timer 4 compare logic.
4	T3CMPOE	Timer 3 Compare Output Enable. This bit, when active, enables or disables EV Timer 1 compare output T3PWM_T3CMP. This bit is active only when EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. This bit, when active is reset to zero when T3CTRIP is low and is also enabled. 0 Timer 3 compare output, T3PWM_T3CMP, is in HI−z state. 1 Timer 3 compare output, T3PWM_T3CMP, is driven by Timer 3 compare logic.

Figure 5−6.GP Timer Control Register B (GPTCONB) — Address 7500h (Continued)

Bit(s)	Name	Description
3−2	T4PIN	Polarity of GP timer 4 compare output
		00 Forced low
		01 Active low
		10 Active high
		11 Forced high
1−0	T3PIN	Polarity of GP timer 3 compare output
		00 Forced low
		01 Active low
		10 Active high
		11 Forced high

5.3 Compare Control Register

Figure 5–7. Compare Control A (COMCONA) Register — Address 7411h

15	14	13	12	11	10	9	8
CENABLE	CLD1	CLD0	SVENABLE	ACTRLD1	ACTRLD0	FCMPOE	$\overline{\text{PDPINTA}}$ Status
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

7	6	5	4	3	2	1	0
FCMP3OE	FCMP2OE	FCMP1OE	Reserved		C3TRIPE	C2TRIPE	C1TRIPE
R/W-0	R/W-0	R/W-0	R-0		R/W-1	R/W-1	R/W -1

Legend: R = Read, W = Write, -n = reset value

Note: Shaded areas indicate that the bit is active only when the EXTCONA bit 0 = 1.

Bit(s)	Name	Description
15	CENABLE	Compare enable
		0 Disables compare operation. All shadowed registers (CMPRx, ACTRB) become transparent
		1 Enables compare operation
14–13	CLD1, CLD0	
		00 When T3CNT = 0 (that is, underflow)
		01 When T3CNT = 0 or T3CNT = T3PR (that is, on underflow or period match)
		10 Immediately
		11 Reserved; result is unpredictable
12	SVENABLE	Space vector PWM mode enable
		0 Disables space vector PWM mode
		1 Enables space vector PWM mode
11–10	ACTRLD1, ACTRLD0	Action control register reload condition
		00 When T3CNT = 0 (that is, underflow)
		01 When T3CNT = 0 or T3CNT = T3PR (that is, on underflow or period match)
		10 Immediately
		11 Reserved; result is unpredictable
9	FCMPOE	Full Compare Output Enable: This bit, when active, enables and disables all full compare outputs at the same time. This bit is active only if EXTCONA(0) = 0. This bit is reserved when EXTCONA(0) = 1. This bit, when active, is reset to zero when both PDPINTA/T1CTRIP is low and EVAIFRA(0) = 1.
		0 Full compare outputs, PWM1/2/3/4/5/6, are in Hi-Z state.
		1 Full compare outputs, PWM1/2/3/4/5/6, are driven by corresponding compare logic.
8	$\overline{\text{PDPINTA}}$ Status	This bit reflects the current status of the $\overline{\text{PDPINTA}}$ pin.

Figure 5−7. Compare Control A — Address 7411h (COMCONA) Register (Continued)

Bit(s)	Name	Description
7	FCMP3OE	Full Compare 3 Output Enable: This bit, when active, enables or disables Full Compare 3 outputs, PWM5/6. This bit is active only if EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0. This bit, when active, is reset to zero when C3TRIP is low and is also enabled. 0 Full Compare 3 outputs, PWM5/6, are in high-impedance state. 1 Full Compare 3 outputs, PWM5/6, are driven by Full Compare 3 logic.
6	FCMP2OE	Full Compare 2 Output Enable: This bit, when active, enables or disables Full Compare 2 outputs, PWM3/4. This bit is active only if EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0. This bit, when active, is reset to zero when C2TRIP is low and is also enabled. 0 Full Compare 2 outputs, PWM3/4, are in high-impedance state. 1 Full Compare 2 outputs, PWM3/4, are driven by Full Compare 2 logic.
5	FCMP1OE	Full Compare 1 Output Enable: This bit, when active, enables or disables Full Compare 1 outputs, PWM1/2. This bit is active only if EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0. This bit, when active, is reset to zero when C1TRIP is low and is also enabled. 0 Full Compare 1 outputs, PWM1/2, are in high-impedance state. 1 Full Compare 1 outputs, PWM1/2, are driven by Full Compare 1 logic.
4−3	Reserved	
2	C3TRIPE	C3TRIP Enable: This bit, when active, enables or disables Full Compare 3 trip (C3TRIP). This bit is active only if EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0. 0 C3TRIP is disabled. C3TRIP does not affect Full Compare 3 outputs, COMCONA(8), or PDPINT flag (EVAIFRA(0)). 1 C3TRIP is enabled. When C3TRIP is low, both Full Compare 3 outputs go into high-impedance state, COMCONA(8) is reset to zero, and PDPINTA flag (EVAIFRA(0)) is set to one.
1	C2TRIPE	C2TRIP Enable: This bit, when active, enables or disables Full Compare 2 trip (C2TRIP). This bit is active only if EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0. 0 C2TRIP is disabled. C2TRIP does not affect Full Compare 2 outputs, COMCONA(7), or PDPINTA flag (EVAIFRA(0)). 1 C2TRIP is enabled. When C2TRIP is low, both Full Compare 2 outputs go into high-impedance state, COMCONA(7) is reset to zero, and PDPINTA flag (EVAIFRA(0)) is set to one.

Figure 5–7. Compare Control A — Address 7411h (COMCONA) Register (Continued)

Bit(s)	Name	Description
0	C1TRIPE	C1TRIP Enable: This bit, when active, enables or disables Full Compare 1 trip (C1TRIP). This bit is active only if EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0. 0 C1TRIP is disabled. C1TRIP does not affect Full Compare 1 outputs, COMCONA(6), or PDPINTA flag (EVAIFRA(0)). 1 C1TRIP is enabled. When C1TRIP is low, both Full Compare 1 outputs go into high-impedance state, COMCONA(6) is reset to zero, and PDPINTA flag (EVAIFRA(0)) is set to one.

Figure 5–8. Compare Control B (COMCONB) Register — Address 7511h

15	14	13	12	11	10	9	8
CENABLE	CLD1	CLD0	SVENABLE	ACTRLD1	ACTRLD0	FCMPOE	$\overline{\text{PDPINTB}}$ Status
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0
7	6	5	4	3	2	1	0
FCMP6OE	FCMP5OE	FCMP4OE	Reserved		C6TRIPE	C5TRIPE	C4TRIPE
R/W-0	R/W-0	R/W-0	R-0		R/W-1	R/W-1	R/W -1

Legend: R = Read, W = Write, -n = reset value

Note: Shaded areas indicate that the bit is active only when the EXTCONA bit 0 = 1.

Bit(s)	Name	Description
15	CENABLE	Compare enable 0 Disables compare operation. All shadowed registers (CMPRx, ACTRB) become transparent 1 Enables compare operation
14–13	CLD1, CLD0	 00 When T3CNT = 0 (that is, underflow) 01 When T3CNT = 0 or T3CNT = T3PR (that is, on underflow or period match) 10 Immediately 11 Reserved; result is unpredictable
12	SVENABLE	Space vector PWM mode enable 0 Disables space vector PWM mode 1 Enables space vector PWM mode
11–10	ACTRLD1, ACTRLD0	Action control register reload condition 00 When T3CNT = 0 (that is, underflow) 01 When T3CNT = 0 or T3CNT = T3PR (that is, on underflow or period match) 10 Immediately 11 Reserved; result is unpredictable

Figure 5–8.Compare Control B (COMCONB) Register — Address 7511h (Continued)

9	FCMPOE	Full Compare Output Enable: This bit, when active, enables and disables all full compare outputs at the same time. This bit is active only if EXTCONB(0) = 0. This bit is reserved when EXTCONB(0) = 1. This bit, when active, is reset to zero when both PDPINTB/T3CTRIP is low and EVBIFRA(0) = 1. 0 Full compare outputs, PWM7/8/9/10/11/12, are in high-impedance state. 1 Full compare outputs, PWM7/8/9/10/11/12, are driven by corresponding compare logic.
8	$\overline{\text{PDPINTB}}$ Status	This bit reflects the current status of the $\overline{\text{PDPINTB}}$ pin.
7	FCMP6OE	Full Compare 6 Output Enable: This bit, when active, enables or disables Full Compare 6 outputs, PWM11/12. This bit is active only if EXTCONB(0) = 1. This bit is reserved when EXTCONB(0) = 0. This bit, when active, is reset to zero when C6TRIP is low and is also enabled. 0 Full Compare 6 outputs, PWM11/12, are in high-impedance state. 1 Full Compare 6 outputs, PWM11/12, are driven by Full Compare 6 logic.
6	FCMP5OE	Full Compare 5 Output Enable: This bit, when active, enables or disables Full Compare 5 outputs, PWM9/10. This bit is active only if EXTCONB(0) = 1. This bit is reserved when EXTCONB(0) = 0. This bit, when active, is reset to zero when C5TRIP is low and is also enabled. 0 Full Compare 5 outputs, PWM9/10, are in high-impedance state. 1 Full Compare 5 outputs, PWM9/10, are driven by Full Compare 2 logic.
5	FCMP4OE	Full Compare 4 Output Enable: This bit, when active, enables or disables Full Compare 4 outputs, PWM7/8. This bit is active only if EXTCONB(0) = 1. This bit is reserved when EXTCONB(0) = 0. This bit, when active, is reset to zero when C4TRIP is low and is also enabled. 0 Full Compare 4 outputs, PWM7/8, are in high-impedance state. 1 Full Compare 4 outputs, PWM7/8, are driven by Full Compare 4 logic.
4–3	Reserved	
2	C6TRIPE	C6TRIP Enable: This bit, when active, enables or disables Full Compare 6 trip (C6TRIP). This bit is active only if EXTCONB(0) = 1. This bit is reserved when EXTCONB(0) = 0. 0 C6TRIP is disabled. C6TRIP does not affect Full Compare 6 outputs, COMCON(8), or PDPINTB flag (EVBIFRA(0)). 1 C6TRIP is enabled. When C6TRIP is low, both Full Compare 6 outputs go into high-impedance state, COMCONB(8) is reset to zero, and PDPINTB flag (EVBIFRA(0)) is set to one.

Figure 5–8.Compare Control B (COMCONB) Register — Address 7511h *(Continued)*

Bit(s)	Name	Description
1	C5TRIPE	C5TRIP Enable: This bit, when active, enables or disables Full Compare 5 trip (C5TRIP). This bit is active only if EXTCONB(0) = 1. This bit is reserved when EXTCONB(0) = 0. 0 C5TRIP is disabled. C5TRIP does not affect Full Compare 5 outputs, COMCON(7), or PDPINT flag (EVBIFRA(0)). 1 C5TRIP is enabled. When C5TRIP is low, both Full Compare 5 outputs go into high-impedance state, COMCONB(7) is reset to 0, and PDPINTB flag (EVBIFRA(0)) is set to 1.
0	C4TRIPE	C4TRIP Enable: This bit, when active, enables or disables Full Compare 4 trip (C4TRIP). This bit is active only if EXTCONB(0) = 1. This bit is reserved when EXTCONB(0) = 0. 0 C4TRIP is disabled. C4TRIP does not affect Full Compare 4 outputs, COMCONB(6), or PDPINTB flag (EVBIFRA(0)). 1 C4TRIP is enabled. When C4TRIP is low, both Full Compare 4 outputs go into high-impedance state, COMCONB(6) is reset to zero, and PDPINTB flag (EVBIFRA(0)) is set to one.

Note:

If the CxTRIPE bits are used as GPIO bits, then the compare-trip functionality must be disabled in the COMCONx registers. Otherwise, the corresponding PWM pin(s) might be inadvertently driven into high impedance, when the CxTRIPE/GPIO bit is driven low.

5.4 Compare Action Control Registers

The compare action control registers (ACTRA and ACTRB) control the action that takes place on each of the six compare output pins (PWMx, where x = 1–6 for ACTRA, and x = 7–12 for ACTRB) on a compare event, if the compare operation is enabled by COMCONx[15]. ACTRA and ACTRB are double-buffered. The condition on which ACTRA and ACTRB is reloaded is defined by bits in COMCONx. ACTRA and ACTRB also contain the SVRDIR, D2, D1, and D0 bits needed for space vector PWM operation. The bit configuration of ACTRA is described in Figure 5–9 and that of ACTRB is described in Figure 5–10.

Figure 5–9. Compare Action Control Register A (ACTRA) — Address 7413h

15	14	13	12	11	10	9	8
SVRDIR	D2	D1	D0	CMP6ACT1	CMP6ACT0	CMP5ACT1	CMP5ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

7	6	5	4	3	2	1	0
CMP4ACT1	CMP4ACT0	CMP3ACT1	CMP3ACT0	CMP2ACT1	CMP2ACT0	CMP1ACT1	CMP1ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15	SVRDIR	Space vector PWM rotation direction. Used only in space vector PWM output generation. 0 Positive (CCW) 1 Negative (CW)
14–12	D2–D0	Basic space vector bits. Used only in space vector PWM output generation.
11–10	CMP6ACT1–0	Action on compare output pin 6, CMP6. 00 Forced low 01 Active low 10 Active high 11 Forced high
9–8	CMP5ACT1–0	Action on compare output pin 5, CMP5. 00 Forced low 01 Active low 10 Active high 11 Forced high

Figure 5−9.Compare Action Control Register A (ACTRA) — Address 7413h (Continued)

Bit(s)	Name	Description
7−6	CMP4ACT1−0	Action on compare output pin 4, CMP4. 00 Forced low 01 Active low 10 Active high 11 Forced high
5−4	CMP3ACT1−0	Action on compare output pin 3, CMP3 00 Forced low 01 Active low 10 Active high 11 Forced high
3−2	CMP2ACT1−0	Action on compare output pin 2, CMP2 00 Forced low 01 Active low 10 Active high 11 Forced high
1−0	CMP1ACT1−0	Action on compare output pin 1, CMP1 00 Forced low 01 Active low 10 Active high 11 Forced high

Figure 5−10. Compare Action Control Register B (ACTRB) — Address 7513h

15	14	13	12	11	10	9	8
SVRDIR	D2	D1	D0	CMP12ACT1	CMP12ACT0	CMP11ACT1	CMP11ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

7	6	5	4	3	2	1	0
CMP10ACT1	CMP10ACT0	CMP9ACT1	CMP9ACT0	CMP8ACT1	CMP8ACT0	CMP7ACT1	CMP7ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15	SVRDIR	Space vector PWM rotation direction. Used only in space vector PWM output generation. 0 Positive (CCW) 1 Negative (CW)
14−12	D2−D0	Basic space vector bits. Used only in space vector PWM output generation.

Figure 5−10. Compare Action Control Register B (ACTRB) — Address 7513h (Continued)

Bit(s)	Name	Description
11−10	CMP12ACT1−0	Action on compare output pin 12, CMP12.
		00 Forced low
		01 Active low
		10 Active high
		11 Forced high
9−8	CMP11ACT1−0	Action on compare output pin 11, CMP11.
		00 Forced low
		01 Active low
		10 Active high
		11 Forced high
7−6	CMP10ACT1−0	Action on compare output pin 10, CMP10.
		00 Forced low
		01 Active low
		10 Active high
		11 Forced high
5−4	CMP9ACT1−0	Action on compare output pin 9, CMP9
		00 Forced low
		01 Active low
		10 Active high
		11 Forced high
3−2	CMP8ACT1−0	Action on compare output pin 8, CMP8
		00 Forced low
		01 Active low
		10 Active high
		11 Forced high
1−0	CMP7ACT1−0	Action on compare output pin 7, CMP7
		00 Forced low
		01 Active low
		10 Active high
		11 Forced high

5.5 Capture Unit Registers

The operation of the capture units is controlled by four 16-bit control registers, CAPCONA/B and CAPFIFOA/B. TxCON (x = 1, 2, 3, or 4) registers are also used to control the operation of the capture units since the time base for capture circuits can be provided by any of these timers.

Figure 5–11. Capture Control Register A (CAPCONA) — Address 7420h

15	14	13	12	11	10	9	8
CAPRES	CAP12EN		CAP3EN	Reserved	CAP3TSEL	CAP12TSEL	CAP3TOADC
RW-0	RW-0		RW-0	RW-0	RW-0	RW-0	RW-0

7	6	5	4	3	2	1	0
CAP1EDGE		CAP2EDGE		CAP3EDGE		Reserved	
RW-0		RW-0		RW-0		RW-0	

Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15	CAPRES	Capture reset. Always reads zero.
		0 Clear all registers of capture units to 0
		1 No action
14–13	CAP12EN	Captures 1 and 2 Enable:
		00 Disable captures 1 and 2. FIFO stacks retain their contents.
		01 Enable captures 1 and 2.
		10 Reserved
		11 Reserved
12	CAP3EN	Capture 3 Enable:
		0 Disables Capture Unit 3; FIFO stack of Capture Unit 3 retains its contents
		1 Enable capture 3.
11	Reserved	Reads return zero; writes have no effect.
10	CAP3TSEL	GP timer selection for capture unit 3.
		0 Selects GP timer 2
		1 Selects GP timer 1
9	CAP12TSEL	GP timer selection for capture units 1 and 2.
		0 Selects GP timer 2
		1 Selects GP timer 1
8	CAP3TOADC	Capture unit 3 event starts ADC.
		0 No action
		1 Starts ADC when the CAP3INT flag is set

Figure 5−11. Capture Control Register A (CAPCONA) — Address 7420h (Continued)

Bit(s)	Name	Description
7−6	CAP1EDGE	Edge detection control for Capture Unit 1.
		00 No detection
		01 Detects rising edge
		10 Detects falling edge
		11 Detects both edges
5−4	CAP2EDGE	Edge detection control for Capture Unit 2.
		00 No detection
		01 Detects rising edge
		10 Detects falling edge
		11 Detects both edges
3−2	CAP3EDGE	Edge detection control for Capture Unit 3.
		00 No detection
		01 Detects rising edge
		10 Detects falling edge
		11 Detects both edges
1−0	Reserved	Reads return zero; writes have no effect.

Figure 5−12. Capture Control Register B (CAPCONB) — Address 7520h

15	14	13	12	11	10	9	8
CAPRES	CAP45EN		CAP6EN	Reserved	CAP6TSEL	CAP45TSEL	CAP6TOADC
R/W-0	R/W-0		R/W-0	R-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CAP4EDGE		CAP5EDGE		CAP6EDGE		Reserved	
R/W-0		R/W-0		R/W-0		R/W-0	

Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15	CAPRES	This bit is not implemented as a register bit. Writing a 0 simply clears the capture registers.
		0 Clear all registers of capture units and QEP circuit to 0
		1 No action
14−13	CAP45EN	Capture Units 4 and 5 and QEP circuit control.
		00 Disables Capture Units 4 and 5. FIFO stacks retain their contents
		01 Enables Capture Units 4 and 5
		10 Reserved
		11 Reserved

Figure 5−12. Capture Control Register B (CAPCONB) — Address 7520h (Continued)

12	CAP6EN	Capture unit 6 control
		0 Disables Capture Unit 6; FIFO stack of Capture Unit 6 retains its contents
		1 Enables Capture Unit 6
11	Reserved	Reads return zero; writes have no effect.
10	CAP6TSEL	GP timer selection for Capture Unit 6
		0 Selects GP timer 4
		1 Selects GP timer 3
9	CAP45TSEL	GP timer selection for Capture Units 4 and 5
		0 Selects GP timer 4
		1 Selects GP timer 3
8	CAP6TOADC	Capture Unit 6 event starts ADC.
		0 No action
		1 Starts ADC when the CAP6INT flag is set.
7−6	CAP4EDGE	Edge detection control for Capture Unit 4.
		00 No detection
		01 Detects rising edge
		10 Detects falling edge
		11 Detects both edges
5−4	CAP5EDGE	Edge detection control for Capture Unit 5.
		00 No detection
		01 Detects rising edge
		10 Detects falling edge
		11 Detects both edges
3−2	CAP6EDGE	Edge detection control for Capture Unit 6.
		00 No detection
		01 Detects rising edge
		10 Detects falling edge
		11 Detects both edges
1−0	Reserved	

5.5.1 Capture FIFO Status Register A (CAPFIFOA)

CAPFIFOA contains the status bits for each of the three FIFO stacks of the capture units. The bit description of CAPFIFOA is given in Figure 5−13. If a write occurs to the CAPnFIFOA status bits at the same time as they are being updated (because of a capture event), the write data takes precedence.

The write operation to the CAPFIFOx registers can be used as a programming advantage. For example, if 01 is written into the CAPnFIFO bits, the EV module is led to “believe” that there is already an entry in the FIFO. Subsequently, every time the FIFO gets a new value, a capture interrupt will be generated.

Figure 5−13. Capture FIFO Status Register A (CAPFIFOA) — Address 7422h

15 14	13 12	11 10	9 8	7 0
Reserved	CAP3FIFO	CAP2FIFO	CAP1FIFO	Reserved
R-0	R/W-0	R/W-0	R/W-0	R-0

Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15−14	Reserved	Reads return zero; writes have no effect.
13−12	CAP3FIFO	CAP3FIFO status
		00 Empty
		01 Has one entry
		10 Has two entries
		11 Had two entries and captured another one; first entry has been lost
11−10	CAP2FIFO	CAP2FIFO status
		00 Empty
		01 Has one entry
		10 Has two entries
		11 Had two entries and captured another one; first entry has been lost
9−8	CAP1FIFO	CAP1FIFO status
		00 Empty
		01 Has one entry
		10 Has two entries
		11 Had two entries and captured another one; first entry has been lost
7−0	Reserved	Reads return zero; writes have no effect.

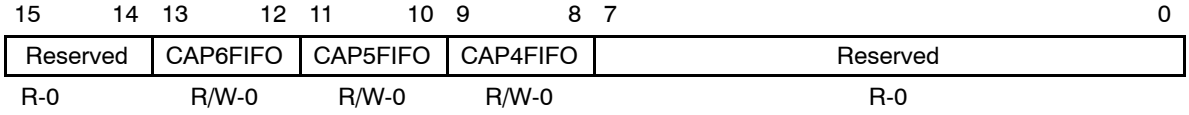
5.5.2 Capture FIFO Status Register B (CAPFIFOB)

CAPFIFOB contains the status bits for each of the three FIFO stacks of the capture units. The bit description of CAPFIFOB is given in Figure 5−14. If a

write occurs to the CAPnFIFOB status bits at the same time as they are being updated (because of a capture event), the write data takes precedence.

The write operation to the CAPFIFOx registers can be used as a programming advantage. For example, if 01 is written into the CAPnFIFO bits, the EV module is led to “believe” that there is already an entry in the FIFO. Subsequently, every time the FIFO gets a new value, a capture interrupt is generated.

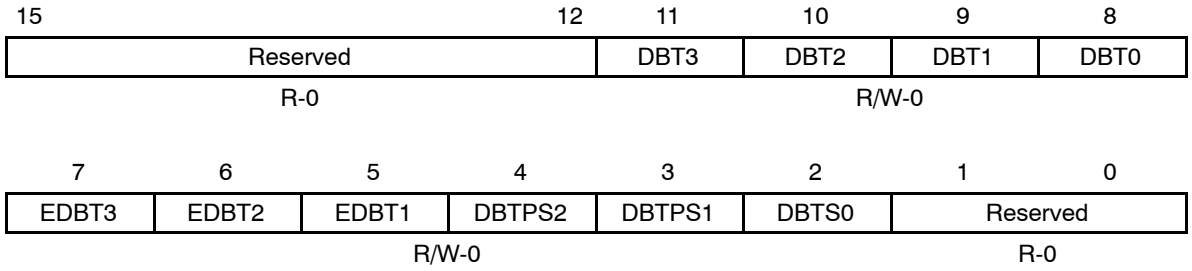
Figure 5−14. Capture FIFO Status Register B (CAPFIFOB) — Address 7522h



Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15−14	Reserved	Reads return zero; writes have no effect.
13−12	CAP6FIFO	CAP6FIFO Status
		00 Empty
		01 Has one entry
		10 Has two entries
		11 Had two entries and captured another one; first entry has been lost
11−10	CAP5FIFO	CAP5FIFO Status
		00 Empty
		01 Has one entry
		10 Has two entries
		11 Had two entries and captured another one; first entry has been lost
9−8	CAP4FIFO	CAP4FIFO Status
		00 Empty
		01 Has one entry
		10 Has two entries
		11 Had two entries and captured another one; first entry has been lost
7−0	Reserved	Reads return zero; writes have no effect.

Figure 5−15. Dead-Band Timer Control Register A (DBTCONA) — Address xx15h



Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15−12	Reserved	
11−8	DBT3 (MSB) − DBT0 (LSB)	Dead-band timer period. These bits define the period value of the three 4-bit dead-band timers.
7	EDBT3	Dead-band timer 3 enable (for pins PWM5 and PWM6 of Compare Unit 3). 0 Disable 1 Enable
6	EDBT2	Dead-band timer 2 enable (for pins PWM3 and PWM4 of Compare Unit 2). 0 Disable 1 Enable
5	EDBT1	Dead-band timer 1 enable (for pins PWM1 and PWM2 of Compare Unit 1). 0 Disable 1 Enable
4−2	DBTPS2 − DBTPS0	Dead-band timer prescaler 000 x/1 001 x/2 010 x/4 011 x/8 100 x/16 101 x/32 110 x/32 111 x/32 111 x = Device (CPU) clock frequency
1−0	Reserved	

Figure 5−16. Dead-Band Timer Control Register B (DBTCONB) — Address xx15h

15	14	13	12	11	10	9	8
Reserved				DBT3	DBT2	DBT1	DBT0
R-0				R/W-0			

7	6	5	4	3	2	1	0
EDBT3	EDBT2	EDBT1	DBTPS2	DBTPS1	DBTS0	Reserved	
R/W-0						R-0	

Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15−12	Reserved	
11−8	DBT3 (MSB) − DBT0 (LSB)	Dead-band timer period. These bits define the period value of the three 4-bit dead-band timers.
7	EDBT3	Dead-band timer 3 enable (for pins PWM11 and PWM12 of Compare Unit 3). 0 Disable 1 Enable
6	EDBT2	Dead-band timer 2 enable (for pins PWM9 and PWM10 of Compare Unit 2). 0 Disable 1 Enable
5	EDBT1	Dead-band timer 1 enable (for pins PWM7 and PWM8 of Compare Unit 1). 0 Disable 1 Enable
4−2	DBTPS2 − DBTPS0	Dead-band timer prescaler 000 x/1 001 x/2 010 x/4 011 x/8 100 x/16 101 x/32 110 x/32 111 x/32 111 x = Device (CPU) clock frequency
1−0	Reserved	

5.6 EV Interrupt Flag Registers

The registers are all treated as 16-bit memory mapped registers. The unused bits all return zero when read by software. Writing to unused bits has no effect. Since EVxIFRx are readable registers, occurrence of an interrupt event can be monitored by software polling the appropriate bit in EVxIFRx when the interrupt is masked.

Figure 5–17. EVA Interrupt Flag Register A (EVAIFRA) — Address 742Fh

15						10	9	8
Reserved						TIOFINT FLAG	T1UFINT FLAG	T1CINT FLAG
R-0						R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0	
T1PINT FLAG	Reserved			CMP3INT FLAG	CMP2INT FLAG	CMP1INT FLAG	PDPINTA FLAG	
R/W-0	R-0			R/W-0	R/W-0	R/W-0	R/W-0	

Note: R = Read access, W = Write access, -n = value after reset

Bit(s)	Name	Description
15–11	Reserved	Reserved. Reads return 0; writes have no effect.
10	T1OFINT FLAG	GP timer 1 overflow interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag
9	T1UFINT FLAG	GP timer 1 underflow interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag
8	T1CINT FLAG	GP timer 1 compare interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag

Figure 5−17. EVA Interrupt Flag Register A (EVAIFRA) — Address 742Fh (Continued)

7	T1PINT FLAG	GP timer 1 compare interrupt		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag
6−4	Reserved	Reads return zero; writes have no effect		
3	CMP3INT FLAG	Compare 3 interrupt		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag
2	CMP2INT FLAG	Compare 2 interrupt		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag
1	CMP1INT FLAG	Compare 1 interrupt		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag
0	PDPINTA FLAG	Power Drive Protection Interrupt Flag: The definition of this bit depends on EXTCONA(0). When EXTCONA(0) = 0, the definition remains the same as 240x. When EXTCONA(0) = 1, this bit is set when any compare trip is low and is also enabled.		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag

Figure 5−18. EVA Interrupt Flag Register B (EVAIFRB) — Address 7430h

15	14	13	12	11	10	9	8
Reserved							
R/W-0							

7	6	5	4	3	2	1	0
Reserved				T2OFINT FLAG	T2UFINT FLAG	T2CINT FLAG	T2PINT FLAG
R-0				RW1C-0	RW1C-0	RW1C-0	RW1C-0

Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

Bit(s)	Name	Description
15−14	Reserved	Reads return 0; writes have no effect.
3	T2OFINT FLAG	GP timer 2 overflow interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag
2	T2UFINT FLAG	GP timer 2 underflow interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag
1	T2CINT FLAG	GP timer 2 compare interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag
0	T2PINT FLAG	GP timer 2 period interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag

Figure 5−19. EVA Interrupt Flag Register C (EVAIFRC) — Address 7431h

15	8
Reserved	
R-0	

7	3	2	1	0
Reserved		CAP3FINT FLAG	CAP2FINT FLAG	CAP1FINT FLAG
R-0		RW1C-0	RW1C-0	RW1C-0

Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

Bit(s)	Name	Description
15−3	Reserved	Reads return 0; writes have no effect.
2	CAP3FINT FLAG	Capture 3 interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag
1	CAP2FINT FLAG	Capture 2 interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag
0	CAP1FINT FLAG	Capture 1 interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag

Figure 5−20. EVA Interrupt Mask Register A (EVAIMRA) — Address 742Ch

15	11	10	9	8
Reserved		T1OFINT	T1UFINT	T1CINT
R-0		R/W-0	R/W-0	R/W-0

7	6	4	3	2	1	0
T1PINT	Reserved		CMP3INT	CMP2INT	CMP1INT	PDPINTA
R/W-0	R-0		R/W-0	R/W-0	R/W-0	R/W-1

Note: R = Read access, W = write access, -n = value after reset

Bit(s)	Name	Description
15−11	Reserved	
10	T1OFINT	T1OFINT enable
		0 Disable
		1 Enable
9	T1UFINT	T1UFINT enable
		0 Disable
		1 Enable
8	T1CINT	T1CINT enable
		0 Disable
		1 Enable
7	T1PINT	T1PINT enable
		0 Disable
		1 Enable
6−4	Reserved	
3	CMP3INT	CMP3INT enable
		0 Disable
		1 Enable
2	CMP2INT	CMP2INT enable
		0 Disable
		1 Enable

Figure 5−20. EVA Interrupt Mask Register A (EVAIMRA) — Address 742Ch (Continued)

Bit(s)	Name	Description
1	CMP1INT	CMP1INT enable 0 Disable 1 Enable
0	PDPINTA	PDPINTA ENABLE. The definition of this bit depends on EXTCONA(0). When EXTCONA(0) = 0, the definition remains the same as 240x, i.e., this bit enables and disables both PDP interrupt and the direct path of PDPINT pin to compare output buffers. When EXTCONA(0) = 1, this bit becomes just a PDP interrupt enable and disable bit. 0 Disable 1 Enable

Figure 5−21. EVA Interrupt Mask Register B (EVAIMRB) — Address 742Dh

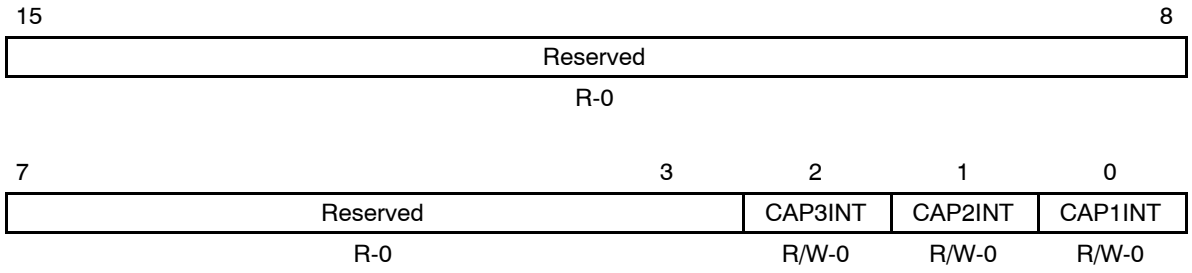
15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved		T2OFINT	T2UFINT	T2CINT	T2PINT
R-0		R/W-0	R/W-0	R/W-0	R/W-0

Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15−4	Reserved	
3	T2OFINT	T2OFINT enable 0 Disable 1 Enable
2	T2UFINT	T2UFINT enable 0 Disable 1 Enable
1	T2CINT	T2CINT enable 0 Disable 1 Enable
0	T2PINT	T2PINT enable 0 Disable 1 Enable

Figure 5−22. EVA Interrupt Mask Register C (EVAIMRC) — Address 742Eh



Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description
15−3	Reserved	
2	CAP3INT ENABLE	CAP3INT Enable 0 Disable 1 Enable
1	CAP2INT ENABLE	CAP2INT Enable 0 Disable 1 Enable
0	CAP1INT ENABLE	CAP1INT Enable 0 Disable 1 Enable

Figure 5−23. EVB Interrupt Flag Register A (EVBIFRA) — Address 752Fh

15	11	10	9	8
Reserved		T3OFINT FLAG	T3UFINT FLAG	T3CINT FLAG
R-0		RW1C-0	RW1C-0	RW1C-0

7	6	4	3	2	1	0
T3PINT FLAG	Reserved		CMP6INT	CMP5INT	CMP4INT	PDPINTB
RW1C-0	R-0		RW1C-0	RW1C-0	RW1C-0	RW1C-0

Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

Bit(s)	Name	Description
15−11	Reserved	Reads return 0; writes have no effect.
10	T3OFINT	T3OFINT FLAG. GP timer 3 overflow interrupt.
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag
9	T3UFINT	T3UFINT FLAG. GP timer 3 underflow interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag
8	T3CINT	T3CINT FLAG. GP timer 3 compare interrupt
		Read: 0 Flag is reset
		1 Flag is set
		Write: 0 No effect
		1 Resets flag

Figure 5−23. EVB Interrupt Flag Register A (EVBIFRA) — Address 752Fh (Continued)

7	T3PINT	T3PINT FLAG. GP timer 3 period interrupt		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag
6−4	Reserved			
3	CMP6INT	CMP6INT FLAG. Compare 6 interrupt.		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag
2	CMP5INT	CMP6INT FLAG. Compare 5 interrupt.		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag
1	CMP4INT	CMP6INT FLAG. Compare 4 interrupt.		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag
0	PDPINTB	PDPINTB FLAG. Power drive protection interrupt.		
		Read:	0	Flag is reset
			1	Flag is set
		Write:	0	No effect
			1	Resets flag

Figure 5–24. EVB Interrupt Flag Register B (EVBIFRB) — Address 7530h

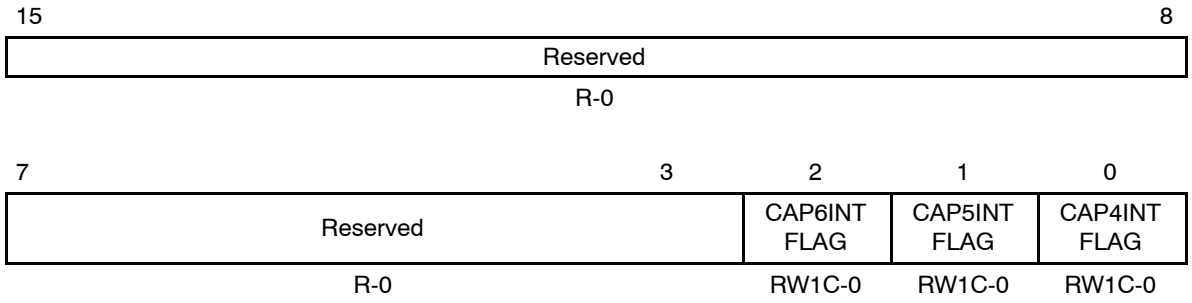
15	14	13	12	11	10	9	8
Reserved							
R-0							

7	6	5	4	3	2	1	0
Reserved				T4OFINT FLAG	T4UFINT FLAG	T4CINT FLAG	T4PINT FLAG
R-0				RW1C-0	RW1C-0	RW1C-0	RW1C-0

Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

Bit(s)	Name	Description
15–4	Reserved	
3	T4OFINT FLAG	GP timer 4 overflow interrupt Read: 0 Flag is reset 1 Flag is set Write: 0 No effect 1 Resets flag
2	T4UFINT FLAG	GP timer 4 underflow interrupt Read: 0 Flag is reset 1 Flag is set Write: 0 No effect 1 Resets flag
1	T4CINT FLAG	GP timer 4 compare interrupt Read: 0 Flag is reset 1 Flag is set Write: 0 No effect 1 Resets flag
0	T4PINT FLAG	GP timer 4 period interrupt Read: 0 Flag is reset 1 Flag is set Write: 0 No effect 1 Resets flag

Figure 5−25. EVB Interrupt Flag Register C (EVBIFRC) — Address 7531h



Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

Bit(s)	Name	Description
15−3	Reserved	
2	CAP6INT FLAG	GP timer 4 overflow interrupt. Read: 0 Flag is reset 1 Flag is set Write: 0 No effect 1 Resets flag
1	CAP5INT FLAG	GP timer 4 overflow interrupt. Read: 0 Flag is reset 1 Flag is set Write: 0 No effect 1 Resets flag
0	CAP4INT FLAG	GP timer 4 overflow interrupt. Read: 0 Flag is reset 1 Flag is set Write: 0 No effect 1 Resets flag

Figure 5–26. EVB Interrupt Mask Register A (EVBIMRA) — Address 752Ch

15	11	10	9	8
Reserved		T3OFINT ENABLE	T3UFINT ENABLE	T3CINT ENABLE
R/W-0		R/W-0	R/W-0	R/W-0

7	6	4	3	2	1	0
T3PINT ENABLE	Reserved		CMP6INT ENABLE	CMP5INT ENABLE	CMP4INT ENABLE	PDPINTB ENABLE
R/W-0	R-0		R/W-0	R/W-0	R/W-0	R/W-1

Note: R = Read access, W = Write access, -n = value after reset

Bit(s)	Name	Description
15–11	Reserved	
10	T3OFINT ENABLE	T3OFINT Enable 0 Disable 1 Enable
9	T3UFINT ENABLE	T3UFINT Enable 0 Disable 1 Enable
8	T3CINT ENABLE	T3CINT Enable 0 Disable 1 Enable
7	T3PINT ENABLE	T3PINT Enable 0 Disable 1 Enable
6–4	Reserved	
3	CMP6INT ENABLE	CMP6INT Enable 0 Disable 1 Enable
2	CMP5INT ENABLE	CMP5INT Enable 0 Disable 1 Enable
1	CMP4INT ENABLE	CMP4INT Enable 0 Disable 1 Enable
0	PDPINTB ENABLE	PDPINTB Enable. This is enabled (set to 1) following reset 0 Disable 1 Enable

Figure 5–27. EVB Interrupt Mask Register B (EVBIMRB) — Address 752Dh

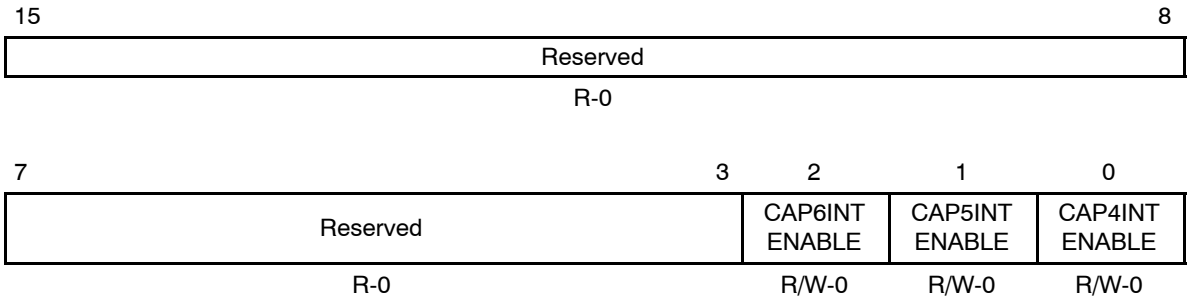
15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved		T4OFINT ENABLE	T4UFINT ENABLE	T4CINT ENABLE	T4PINT ENABLE
R-0		RW-0	RW-0	RW-0	RW-0

Note: R = Read access, W = Write access, -0 = value after reset

Bit(s)	Name	Description	
15–4	Reserved		
3	T4OFINT ENABLE		
		0	Disable
		1	Enable
2	T4UFINT ENABLE		
		0	Disable
		1	Enable
1	T4CINT ENABLE		
		0	Disable
		1	Enable
0	T4PINT ENABLE		
		0	Disable
		1	Enable

Figure 5–28. EVB Interrupt Mask Register C (EVBIMRC) — Address 752Eh



Note: R = Read access, W = Write access, -n = value after reset

Bit(s)	Name	Description	
15–3	Reserved		
2	CAP6INT ENABLE		
		0	Disable
		1	Enable
1	CAP5INT ENABLE		
		0	Disable
		1	Enable
0	CAP4INT ENABLE		
		0	Disable
		1	Enable

5.7 EV Control Registers

EXTCONA and EXTCONB are added control registers to enable and disable the added/modified features. The EXTCONx registers are required for compatibility with 240x EV. EXTCONx enables and disables the additions and modifications in features. All additions and modifications are disabled by default to keep compatibility with 240x EV. The description applies to EXTCONA. EXTCONB is identical to this register except that it controls the EVB register set.

Figure 5–29. EV Extension Control Register A (EXTCONA) — Address 7409h

15	14	13	12	11	10	9	8
Reserved							
R-0							

7	6	5	4	3	2	1	0
Reserved				EVSOCE	QEPIE	QEPIQUAL	INDCOE
R-0				R/W-0	R/W-0	R/W-0	R/W-0

Bit(s)	Name	Description
15:4	Reserved	
3	EVSOCE	EV Start-of-Conversion Output Enable. This bit enables and disables the ADC start-of-conversion output of EV (i.e., EVASOCn for EVA and EVBSOCn for EVB). When enabled, a negative (active-low) pulse of 32 x HSPCLK is generated on selected EV ADC start-of-conversion event. This bit does not affect the EVTOADC signal routed to the ADC module as optional SOC trigger. 0 Disables $\overline{\text{EVSOC}}$ output. $\overline{\text{EVSOC}}$ is in high-impedance state. 1 Enables $\overline{\text{EVSOC}}$ output.
2	QEPIE	QEP Index Enable. This bit enables and disables the CAP3_QEPI1 as index input. CAP3_QEPII, when enabled as index input, can cause the timer configured as the QEP counter to reset. 0 Disables CAP3_QEPI1 as index input. Transitions on CAP3_QEPI1 do not affect the timer configured as the QEP counter. 1 Enables CAP3_QPII as index input. Either a zero-to-one transition on CAP3_QEPI1 alone (when EXTCONA[1] = 0), or a zero-to-one transition plus CAP1_QEP1 and CAP2_QEP2 are both high (when EXTCON[1] = 1), causes the timer configured as QEP counter to reset to zero.
1	QEPIQUAL	CAP3_QEPI1 Index Qualification Mode. This bit turns on and off QEP index qualifier. 0 CAP3_QEPI1 qualification mode is off. CAP3_QEPI1 is allowed to pass the qualifier unaffected. 1 CAP3_QEPI1 qualification mode is on. A zero-to-one transition is allowed to pass the qualifier only when both CAP1_QEP1 and CAP2_QEP2 are high. Otherwise the output of the qualifier stays low.

Figure 5−29. EV Control Register (EXTCONA) — Address 7409h *(Continued)*

Bit(s)	Name	Description
0	INDCOE	Independent compare output enable mode. This bit, when set to one, allows compare outputs to be enabled and disabled independently. 0 Independent compare output enable mode is disabled. Time 1 and 2 compare outputs are enabled and disabled at the same time by GPTCONA(6). Full Compare 1, 2, and 3 outputs are enabled and disabled at the same time by COMCONA(9). GPTCONA(12,11,5,4) and COMCONA(7:5, 2:0) are reserved. EVIFRA(0) enables and disables all the compare outputs at the same time. EVIMR(0) enables and disables PDP interrupt and the direct path of $\overline{\text{PDPINT}}$ signal at the same time. 1 Independent compare output enable mode is enabled. Compare outputs are enabled and disabled respectively by GPTCON(5,4) and COMCON(7:5). Compare trips are enabled and disabled respectively by GPTCON(12,11) and COMCON(2:0). GPTCON(6) and COMCON(9) are reserved. EVIFRA[0] is set to one when any trip input is low and is also enabled. EVIMRA(0) functions only as interrupt enable and disable.

5.8 Differences in Register Bit Definitions

The changes described here are for one EV. The same changes must be implemented in both EVA and EVB. This includes the addition of the EXTCONx control register, i.e., an EXTCONx register is added to each EV instance, one in EVA, and another in EVB.

Changes are introduced to registers as shown in Table 5−1. Only the bits that changed are shown; all others are the same as they were in the 240x EV. See the individual registers in this chapter for complete bit descriptions.

Table 5−1. Register Bit Changes

Bit(s)	Name	Description
TXCON Register Bit Changes		
5,4	TCLKS(1,0)	Timer 2 Clock Source 00 Internal, i.e., HSPCLK 01 External, i.e., TCLKIN 10 Reserved 11 QEP circuit After the change, both Timers 1 and 2 (and, similarly, both Timers 3 and 4) are allowed to use QEP circuit as clock source.
GPTCON Register Bit Changes		
12	T2CTRIPE	T2CTRIP Enable: This bit, when active, enables and disables Timer 2 Compare Trip (T2CTRIP). This bit is active only when EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0: 0 T2CTRIP is disabled. T2CTRIP does not affect Timer 2 compare output, GPTCON(5), or PDPINT flag (EVIFRA(0)). 1 T2CTRIP is enabled. When T2CTRIP is low, Timer 2 compare output goes into high-impedance state, GPTCON(5) is reset to zero, and PDPINT flag (EVIFRA(0)) is set to one.
11	T1CTRIPE	T1CTRIP Enable: This bit, when active, enables and disables Timer 1 Compare Trip (T1CTRIP) input. This bit is active only when EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0: 0 T1CTRIP is disabled. T1CTRIP does not affect Timer 1 compare output, GPTCON(4), or PDPINT flag (EVIFRA(0)). 1 T1CTRIP is enabled. When T1CTRIP is low, Timer 1 compare output goes into high-impedance state, GPTCON(4) is reset to zero, and PDPINT flag (EVIFRA(0)) is set to one.

Table 5–1. Register Bit Changes (Continued)

Bit(s)	Name	Description
6	TCMPOE	Timer Compare Output Enable: This bit, when active, enables and disables timer compare outputs. This bit is active only if EXTCONA(0) = 0. This bit is reserved when EXTCONA(0) = 1. This bit, when active, is reset to zero when both PDPINT/T1CTRIP is low and EVIMRA(0) = 1 are true: 0 Timer compare outputs, T1/2PWM_T1/2CMP, are in high-impedance state. 1 Timer compare outputs, T1/2PWM_T1/2CMP, are driven by individual timer compare logic.
5	T2CMPOE	Timer 2 Compare Output Enable: This bit, when active, enables or disables EV Timer 2 compare output, T2PWM_T2CMP. This bit is active only if EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0. This bit, when active, is reset to zero when T2CTRIP is low and is also enabled: 0 Timer 2 compare output, T2PWM_T2CMP, is in high-impedance state. 1 Timer 2 compare output, T2PWM_T2CMP, is driven by Timer 2 compare logic.
4	T1CMPOE	Timer 1 Compare Output Enable: This bit, when active, enables or disables EV Timer 1 compare output, T1PWM_T1CMP. This bit is active only EXTCONA(0) = 1. This bit is reserved when EXTCONA(0) = 0. This bit, when active, is reset to zero when T1CTRIP is low and is also enabled: 0 Timer 1 compare output, T1PWM_T1CMP, is in high-impedance state. 1 Timer 1 compare output, T1PWM_T1CMP, is driven by Timer 1 compare logic.
		COMCON Register Bit Changes
9	FCMPOE	Full Compare Output Enable: This bit, when active, enables and disables all full compare outputs at the same time. This bit is active only if EXTCONA(0) = 0. This bit is reserved when EXTCONA(0) = 1. This bit, when active is reset to zero when both PDPINT/T1CTRIP is low and EVIFRA(0) = 1: 0 Full compare outputs, PWM1/2/3/4/5/6, are in high-impedance state. 1 Full compare outputs, PWM1/2/3/4/5/6, are driven by corresponding compare logic.
8	PDPINT	Status of $\overline{\text{PDPINT}}$ pin

Table 5−1. Register Bit Changes (Continued)

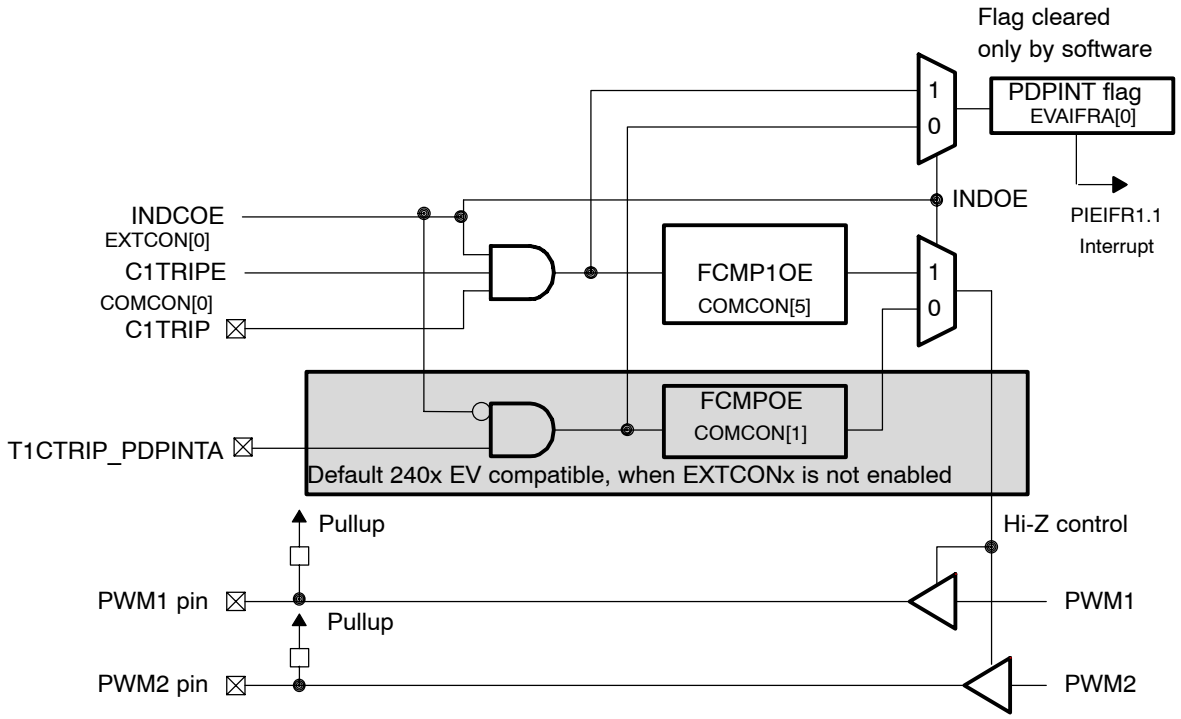
Bit(s)	Name	Description
7	FCMP3OE	Full Compare 3 Output Enable: This bit, when active, enables or disables Full Compare 3 outputs, PWM5/6. This bit is active only if EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. This bit, when active, is reset to zero when C3TRIP is low and is also enabled: 0 Full Compare 3 outputs, PWM5/6, are in high-impedance state. 1 Full Compare 3 outputs, PWM5/6, are driven by Full Compare 3 logic.
6	FCMP2OE	Full Compare 2 Output Enable: This bit, when active, enables or disables Full Compare 2 outputs, PWM4/5. This bit is active only if EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. This bit, when active, is reset to zero when C2TRIP is low and is also enabled: 0 Full Compare 2 outputs, PWM4/5, are in high-impedance state. 1 Full Compare 2 outputs, PWM4/5, are driven by Full Compare 2 logic.
5	FCMP1OE	Full Compare 1 Output Enable: This bit, when active, enables or disables Full Compare 1 outputs, PWM1/2. This bit is active only if EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0. This bit, when active, is reset to zero when C1TRIP is low and is also enabled: 0 Full Compare 1 outputs, PWM1/2, are in high-impedance state. 1 Full Compare 1 outputs, PWM1/2, are driven by Full Compare 1 logic.
4:3	reserved	
2	C3TRIPE	C3TRIP Enable: This bit, when active, enables or disables Full Compare 3 trip (C3TRIP). This bit is active only if EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0: 0 C3TRIP is disabled. C3TRIP does not affect Full Compare 3 outputs, COMCON(8), or PDPINT flag (EVIFRA(0)). 1 C3TRIP is enabled. When C3TRIP is low, both Full Compare 3 outputs go into high-impedance state, COMCON(8) is reset to zero, and PDPINT flag (EVIFRA(0)) is set to one.
1	C2TRIPE	C2TRIP Enable: This bit, when active, enables or disables Full Compare 2 trip (C2TRIP). This bit is active only if EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0: 0 C2TRIP is disabled. C2TRIP does not affect Full Compare 2 outputs, COMCON(7), or PDPINT flag (EVIFRA(0)). 1 C2TRIP is enabled. When C2TRIP is low, both Full Compare 2 outputs go into high-impedance state, COMCON(7) is reset to zero, and PDPINT flag (EVIFRA(0)) is set to one.

Table 5−1. Register Bit Changes (Continued)

Bit(s)	Name	Description
0	C1TRIPE	C1TRIP Enable: This bit, when active, enables or disables Full Compare 1 trip (C1TRIP). This bit is active only if EXTCON(0) = 1. This bit is reserved when EXTCON(0) = 0: 0 C1TRIP is disabled. C1TRIP does not affect Full Compare 1 outputs, COMCON(6), or PDPINT flag (EVIFRA(0)). 1 C1TRIP is enabled. When C1TRIP is low, both Full Compare 1 outputs go into high-impedance state, COMCON(6) is reset to zero, and PDPINT flag (EVIFRA(0)) is set to one.
CAPCON Register Bit Changes		
13:14	CAP12EN	Captures 1 and 2 Enable: 00 Disable Captures 1 and 2. FIFO stacks retain their contents. 01 Enable Captures 1 and 2 10 Reserved 11 Reserved An early version of the 240x User's Guide wrongly assumed that CAPCON(13:14) also controls the enabling and disabling of QEP circuit.
EVIFRA Register Bit Changes		
0	PDPINT	Power Drive Protection Interrupt Flag: The definition of this bit depends on EXTCON(0). When EXTCON(0) = 0, the definition remains the same as '240x. When EXTCON(0) = 1, this bit is set when any compare trip is low and is also enabled.
EVIMRA Register Bit Changes		
0	PDPINT	PDPINT Enable: The definition of this bit depends on EXTCON(0). When EXTCON(0) = 0, the definition remains the same as 240x, i.e., this bit enables and disables both PDP interrupt and the direct path of PDPINT pin to compare output buffers. When EXTCON(0) = 1, this bit becomes just a PDP interrupt enable and disable bit.

EXTCONx is an added control register to enable and disable the added/modified features; therefore, the entire set of bit descriptions is new. See the register in Figure 5−29 on page 5-40 for the descriptions. Figure 5−30 and Figure 5−31 show the Hi-Z control using the EXTCONx register.

Figure 5−30. EXTCONx Register Bit Controls for PWM Hi-Z Control



Note: This diagram is a logical representation of Hi-Z control and does not reflect the actual circuit in a specific device.

Control Sequence	INDOE	C1TRIPE	C1TRIP Pin	FCMP1OE Bit	PDPINT Flag Only	Hi-Z Control	PWMs
EXTCONx bits enabled for individual PWMs control	1	1	1	1	0	1	PWM signal
Low pulse on the C1TRIP pin†	1	1	⊓				
FCMP1OE is cleared for Hi-Z enable	1	1	1	0	1	0	Hi-Z
Set FCMP1OE = 1 to remove Hi-Z control	1	1	1	1	0	1	PWM signal

Notes: 1) The shaded cells in the table show the changes affected due to low pulse on the T1CTRIP pin.

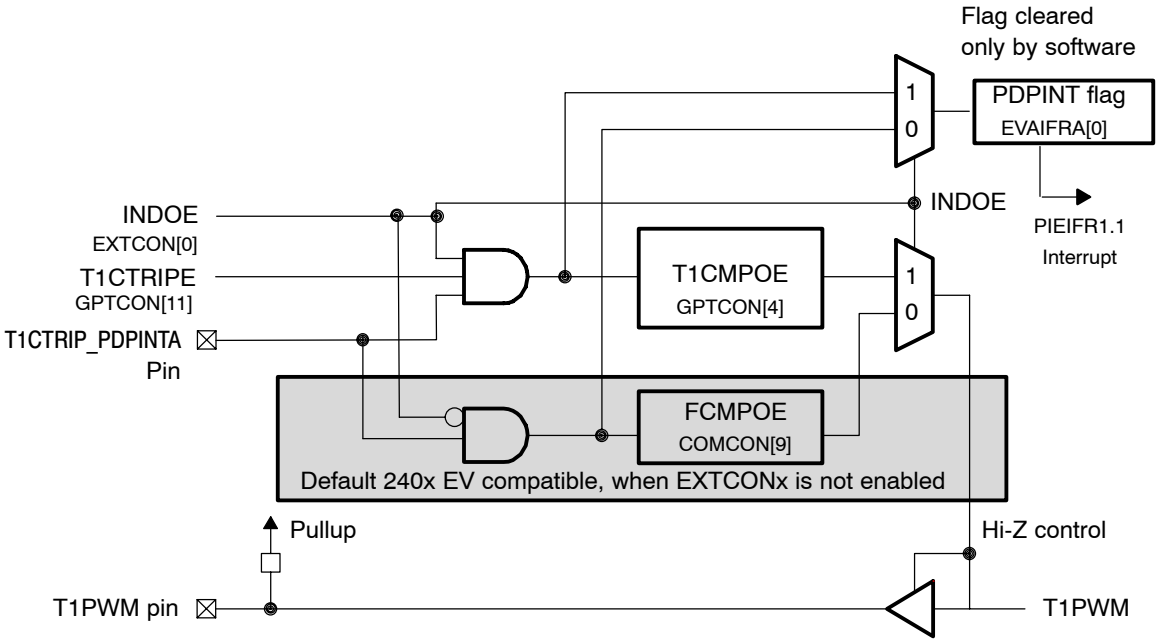
2) FCMPOE This is active in 240x EV-compatible mode when EXTCON_bit0_INDOE = 0
This is a single bit that controls high-impedance (Hi-Z) mode for all the PWM pairs:
EVA − PWM1/2, PWM 3/4, PWM 5/6, T1/T2 PWM.

3) FCMP1OE This is active in the enhanced mode for the EV when EXTCON_bit0_INDOE = 1
This bit controls high-impedance mode only for the PWM 1/2 pair
FCMP2OE, FCMP3OE control PWM 3/4, PWM 5/6 pairs
EVB has similar independent PWM high-impedance mode control in its register set.

4) T1CTRIP_PDPINTA trip control alone has the direct control path to PWM Hi-Z control buffers and the FCMPOE bit control logic. C1TRIP/C2TRIP/C3TRIP pins do not have direct control path to the Hi-Z buffers. They all go through to their respective FCMPxOE bits.

† Pulse width is based on the input qualifier on this pin.

Figure 5–31. EXTCONx Register Bit Controls for T1/T2 PWM Hi-Z Control



Note: This diagram is a logical representation of Hi-Z control and does not reflect the actual circuit in a specific device.

Control Sequence	INDOE	T1CTRIPE	T1CTRIP Pin	T1CMPOE Bit	PDPINT Flag Only	Hi-Z Control	PWMs
EXTCONx bits enabled for individual PWMs control	1	1	1	1	0	1	T1PWM signal
Low pulse on the T1CTRIP pin†	1	1	⊓				
T1CMPOE is cleared for high'-impedance (Hi-Z) enable	1	1	1	0	1	0	Hi-Z
Set T1CMPOE = 1 to remove Hi-Z control	1	1	1	1	0	1	T1PWM signal

Notes: 1) The shaded cells in the table show the changes affected due to low pulse on the T1CTRIP pin.

2) FCMPOE This is active in 240x™ EV-compatible mode when EXTCON_bit0_INDOE = 0
This is a single bit that controls high-impedance mode for all the PWM pairs:
EVA – PWM1/2, PWM 3/4, PWM 5/6, T1/T2 PWM.

3) T1CMPOE This is active in the enhanced mode for the EV when EXTCON_bit0_INDOE = 1
This bit controls high-impedance mode only for the T1PWM pin
T1CMPOE, T2CMPOE control T1PWM, T2PWM pins
EVB has similar independent T3PWM/T4PWM high-impedance mode control in its register set.

† Pulse width is based on the input qualifier on this pin.

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Appendix A

Revision History

This document was revised to SPRU065B from SPRU065A, which was released in July 2003. The scope of the revisions was limited to technical changes as described in A.1. This appendix lists only revisions made in the most recent version.

A.1 Changes Made in This Revision

The following changes were made in this revision:

Page	Additions/Modifications/Deletions
1-34	Changed T2PR and T2CON to 3 for EVB in Section 1.6.
5-12	Changed definition of bit 6 of the Compare Control A Register (Figure 5−7)
5-20	Changed name of bits 14−13 in the CAPCONB Register (Figure 5−12)
B-1	Updated Registers in the register layout summary in Appendix B

Appendix B

EV Register Summary

Figure B–1. Timer x Counter Register (TxCNT, where x = 1, 2, 3, or 4)

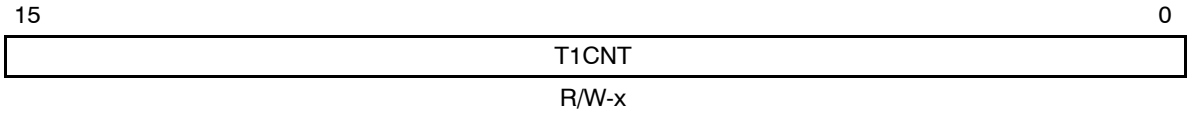


Figure B–2. Timer x Compare Register (TxCMPR, where x = 1, 2, 3, or 4)

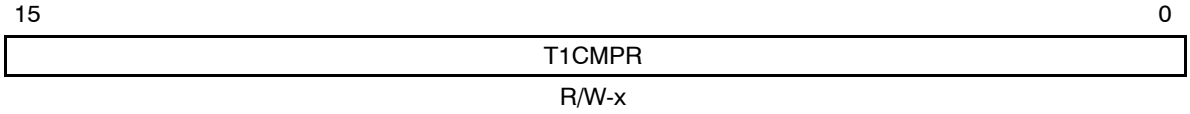


Figure B–3. Timer x Period Register (TxPR, where x = 1, 2, 3, or 4)

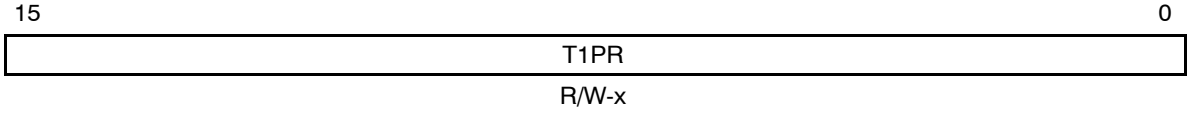


Figure B–4. Timer x Control Register (TxCON; x = 1, 2, 3, or 4)

15	14	13	12	11	10	9	8
Free	Soft	Reserved	TMODE1	TMODE0	TPS2	TPS1	TPS0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

7	6	5	4	3	2	1	0
T2SWT1/ T4SWT3†	TENABLE	TCLKS1	TCLKS0	TCLD1	TCLD0	TECMPR	SELT1PR/ SELT3PR†
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

Legend: R = Read access, W = Write access, -0 = value after reset
† Reserved in T1CON and in T3CON

Figure B–5. GP Timer Control Register A (GPTCONA) — Address 7400h

15	14	13	12	11	10	9	8
Reserved	T2STAT	T1STAT	T2CTRIPE	T1CTRIPE	T2TOADC		T1TOADC
R-0	R-1	R-1	R/W-1	R/W-1	R/W-0		R/W-0

7	6	5	4	3	2	1	0
T1TOADC	TCMPOE	T2CMPOE	T1CMPOE	T2PIN		T1PIN	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	

Note: R = Read access, W = Write access, -n = value after reset

Figure B–6. GP Timer Control Register B (GPTCONB) — Address 7500h

15	14	13	12	11	10	9	8
Reserved	T4STAT	T3STAT	T4CTRIPE	T3CTRIPE	T4TOADC		T3TOADC
R/W-0	R-1	R-1	R/W-1	R/W-1	R/W-0		R/W-0

7	6	5	4	3	2	1	0
T3TOADC	TCMPOE	T4CMPOE	T3CMPOE	T4PIN		T3PIN	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0	

Figure B–7. Compare Control A (COMCONA) Register — Address 7411h

15	14	13	12	11	10	9	8
CENABLE	CLD1	CLD0	SVENABLE	ACTRLD1	ACTRLD0	FCMPOE	$\overline{\text{PDPINTA}}$ Status
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

7	6	5	4	3	2	1	0
FCMP3OE	FCMP2OE	FCMP1OE	Reserved		C3TRIPE	C2TRIPE	C1TRIPE
R/W-0	R/W-0	R/W-0	R-0		R/W-1	R/W-1	R/W -1

Figure B–8. Compare Control B (COMCONB) Register — Address 7511h

15	14	13	12	11	10	9	8
CENABLE	CLD1	CLD0	SVENABLE	ACTRLD1	ACTRLD0	FCMPOE	$\overline{\text{PDPINTB}}$ Status
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

7	6	5	4	3	2	1	0
FCMP6OE	FCMP5OE	FCMP4OE	Reserved		C6TRIPE	C5TRIPE	C4TRIPE
R/W-0	R/W-0	R/W-0	R-0		R/W-1	R/W-1	R/W -1

Legend: R = Read, W = Write, -n = reset value

Note: Shaded areas indicate that the bit is active only when the EXTCONA bit 0 = 1.

Figure B–9. Compare Action Control Register A (ACTRA) — Address 7413h

15	14	13	12	11	10	9	8
SVRDIR	D2	D1	D0	CMP6ACT1	CMP6ACT0	CMP5ACT1	CMP5ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

7	6	5	4	3	2	1	0
CMP4ACT1	CMP4ACT0	CMP3ACT1	CMP3ACT0	CMP2ACT1	CMP2ACT0	CMP1ACT1	CMP1ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

Figure B–10. Compare Action Control Register B (ACTRB) — Address 7513h

15	14	13	12	11	10	9	8
SVRDIR	D2	D1	D0	CMP12ACT1	CMP12ACT0	CMP11ACT1	CMP11ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

7	6	5	4	3	2	1	0
CMP10ACT1	CMP10ACT0	CMP9ACT1	CMP9ACT0	CMP8ACT1	CMP8ACT0	CMP7ACT1	CMP7ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

Note: R = Read access, W = Write access, -0 = value after reset

Figure B–11. Capture Control Register A (CAPCONA) — Address 7420h

15	14	13	12	11	10	9	8
CAPRES	CAP12EN		CAP3EN	Reserved	CAP3TSEL	CAP12TSEL	CAP3TOADC
RW-0	RW-0		RW-0	RW-0	RW-0	RW-0	RW-0

7	6	5	4	3	2	1	0
CAP1EDGE		CAP2EDGE		CAP3EDGE		Reserved	
RW-0		RW-0		RW-0		RW-0	

Note: R = Read access, W = Write access, -0 = value after reset

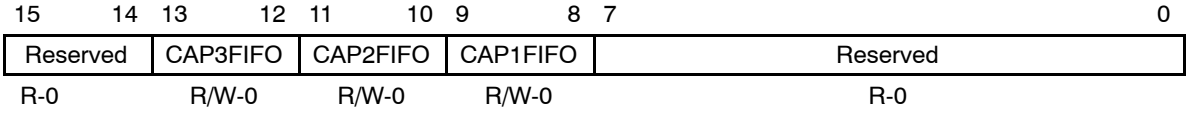
Figure B–12. Capture Control Register B (CAPCONB) — Address 7520h

15	14	13	12	11	10	9	8
CAPRES	CAP45EN		CAP6EN	Reserved	CAP6TSEL	CAP45TSEL	CAP6TOADC
R/W-0	R/W-0		R/W-0	R-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
CAP4EDGE		CAP5EDGE		CAP6EDGE		Reserved	
R/W-0		R/W-0		R/W-0		R/W-0	

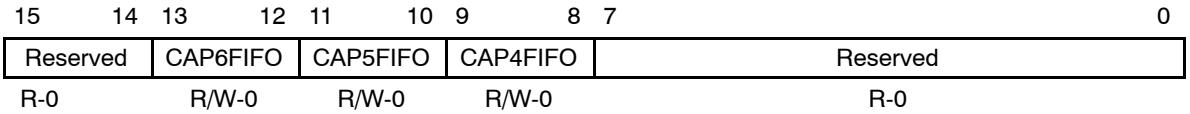
Note: R = Read access, W = Write access, -0 = value after reset

Figure B−13. Capture FIFO Status Register A (CAPFIFOA) — Address 7422h



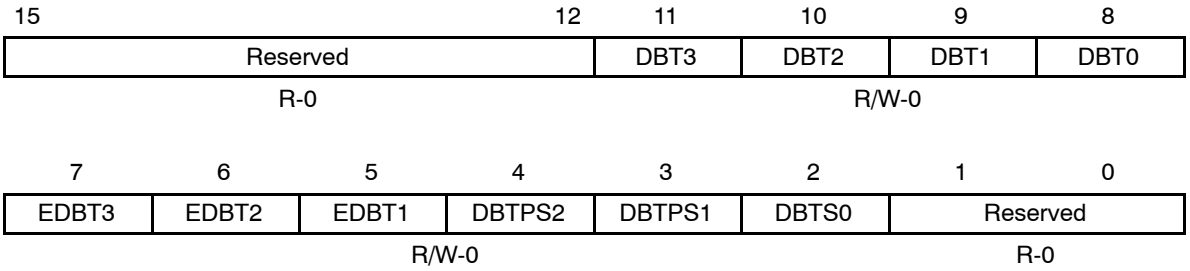
Note: R = Read access, W = Write access, -0 = value after reset

Figure B−14. Capture FIFO Status Register B (CAPFIFOB) — Address 7522h



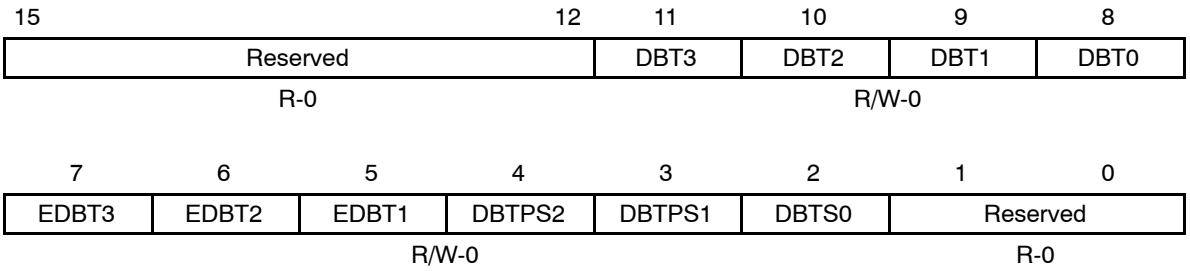
Note: R = Read access, W = Write access, -0 = value after reset

Figure B−15. Dead-Band Timer Control Register A (DBTCONA) — Address xx15h



Note: R = Read access, W = Write access, -0 = value after reset

Figure B−16. Dead-Band Timer Control Register B (DBTCONB) — Address xx15h



Note: R = Read access, W = Write access, -0 = value after reset

Figure B–17. EVA Interrupt Flag Register A (EVAIFRA) — Address 742Fh

15					10	9	8
Reserved					TIOFINT FLAG	T1UFINT FLAG	T1CINT FLAG
R-0					R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
T1PINT FLAG	Reserved			CMP3INT FLAG	CMP2INT FLAG	CMP1INT FLAG	PDPINTA FLAG
R/W-0	R-0			R/W-0	R/W-0	R/W-0	R/W-0

Note: R = Read access, W = Write access, -n = value after reset

Figure B–18. EVA Interrupt Flag Register B (EVAIFRB) — Address 7430h

15							8
Reserved							
R/W-0							

7			4	3	2	1	0
Reserved				T2OFINT FLAG	T2UFINT FLAG	T2CINT FLAG	T2PINT FLAG
R-0				RW1C-0	RW1C-0	RW1C-0	RW1C-0

Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

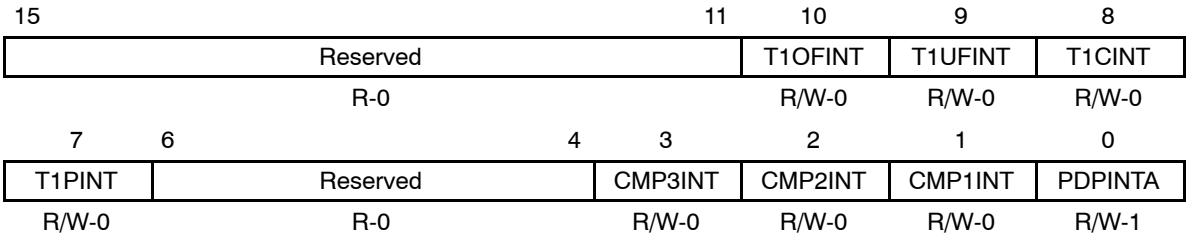
Figure B–19. EVA Interrupt Flag Register C (EVAIFRC) — Address 7431h

15							8
Reserved							
R-0							

7				3	2	1	0
Reserved					CAP3FINT FLAG	CAP2FINT FLAG	CAP1FINT FLAG
R-0					RW1C-0	RW1C-0	RW1C-0

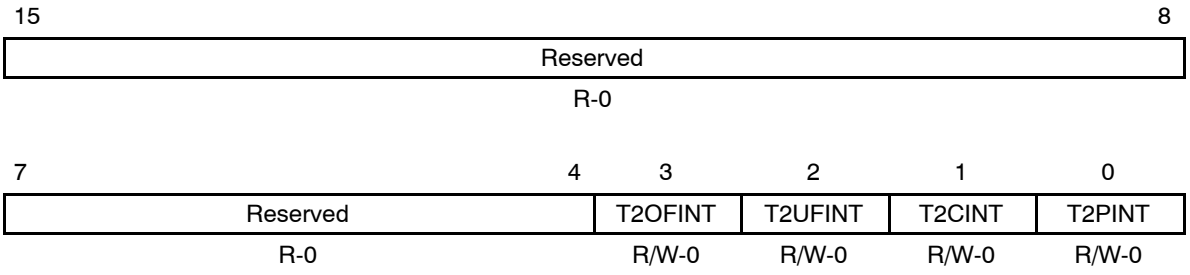
Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

Figure B–20. EVA Interrupt Mask Register A (EVAIMRA) — Address 742Ch



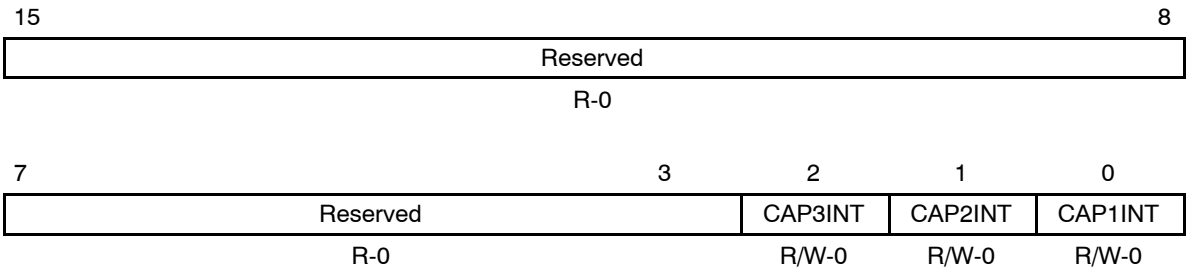
Note: R = Read access, W = write access, -n = value after reset

Figure B–21. EVA Interrupt Mask Register B (EVAIMRB) — Address 742Dh



Note: R = Read access, W = Write access, -0 = value after reset

Figure B–22. EVA Interrupt Mask Register C (EVAIMRC) — Address 742Eh



Note: R = Read access, W = Write access, -0 = value after reset

Figure B–23. EVB Interrupt Flag Register A (EVBIFRA) — Address 752Fh

15 – 11	10	9	8
Reserved	T3OFINT FLAG	T3UFINT FLAG	T3CINT FLAG
R-0	RW1C-0	RW1C-0	RW1C-0

7	6 – 4	3	2	1	0
T3PINT FLAG	Reserved	CMP6INT	CMP5INT	CMP4INT	PDPINTB
RW1C-0	R-0	RW1C-0	RW1C-0	RW1C-0	RW1C-0

Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

Figure B–24. EVB Interrupt Flag Register B (EVBIFRB) — Address 7530h

15 – 8
Reserved
R-0

7 – 4	3	2	1	0
Reserved	T4OFINT FLAG	T4UFINT FLAG	T4CINT FLAG	T4PINT FLAG
R-0	RW1C-0	RW1C-0	RW1C-0	RW1C-0

Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

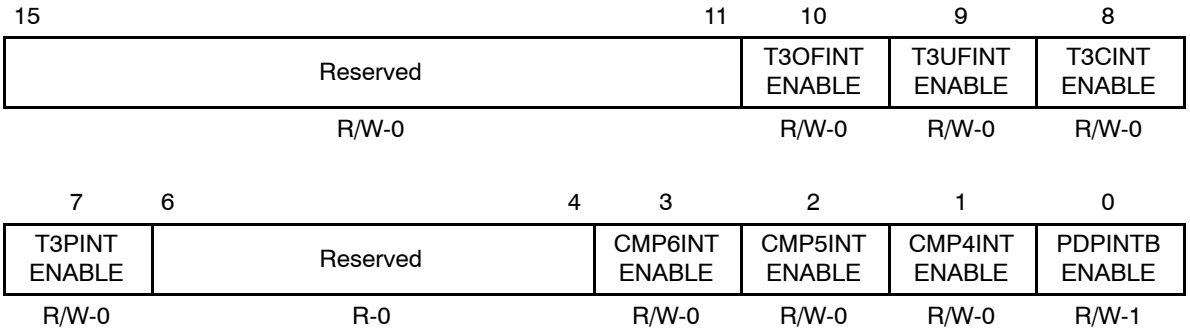
Figure B–25. EVB Interrupt Flag Register C (EVBIFRC) — Address 7531h

15 – 8
Reserved
R-0

7 – 3	2	1	0
Reserved	CAP6INT FLAG	CAP5INT FLAG	CAP4INT FLAG
R-0	RW1C-0	RW1C-0	RW1C-0

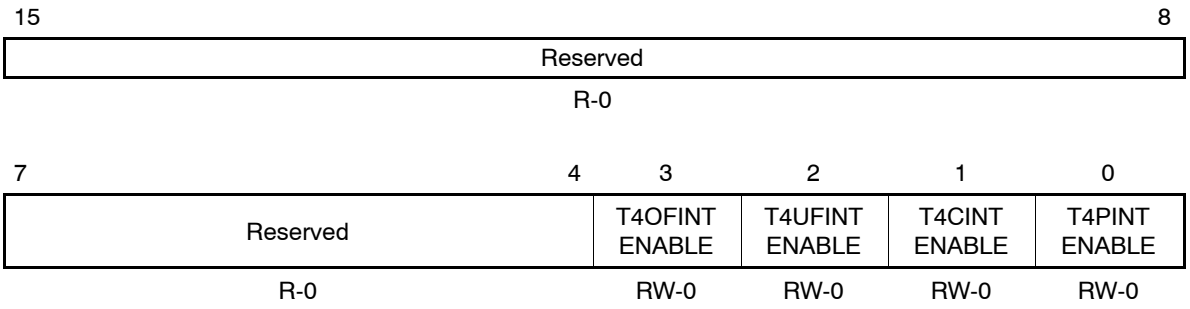
Note: R = Read access, W1C = Write 1 to clear, -0 = value after reset

Figure B–26. EVB Interrupt Mask Register A (EVBIMRA) — Address 752Ch



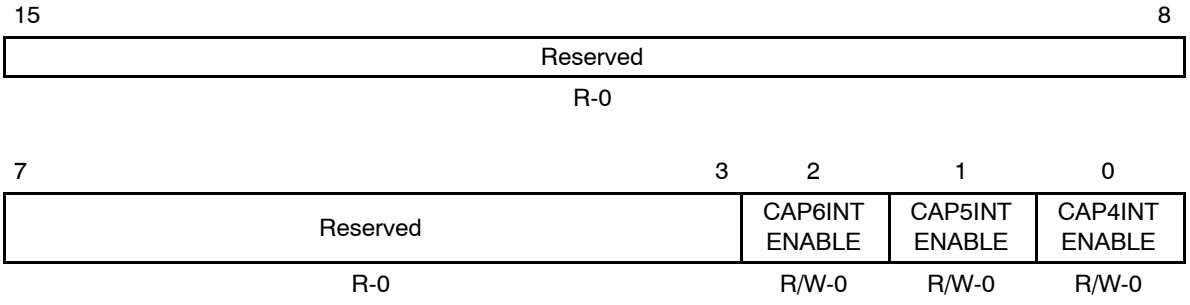
Note: R = Read access, W = Write access, -n = value after reset

Figure B–27. EVB Interrupt Mask Register B (EVBIMRB) — Address 752Dh



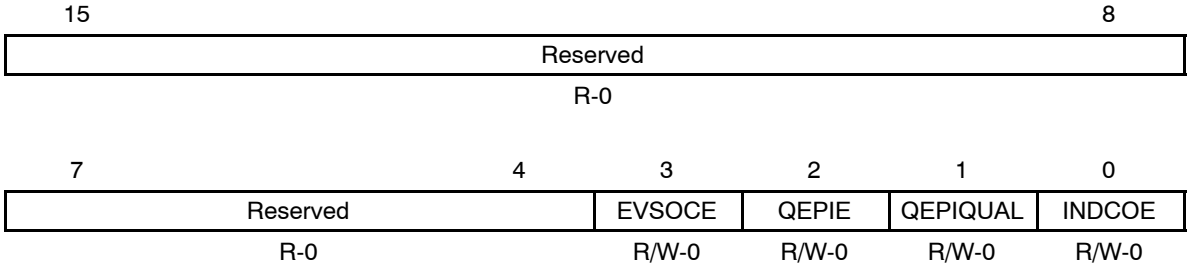
Note: R = Read access, W = Write access, -0 = value after reset

Figure B–28. EVB Interrupt Mask Register C (EVBIMRC) — Address 752Eh



Note: R = Read access, W = Write access, -n = value after reset

Figure B–29. EV Extension Control Register A (EXTCONA) — Address 7409h



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