

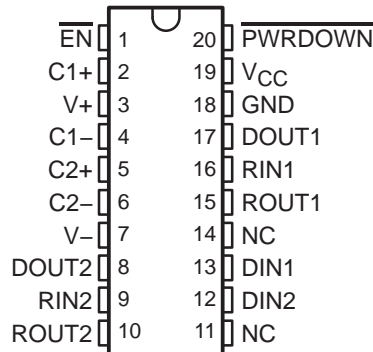
MAX3222

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ± 15 -kV ESD PROTECTION

SLLS408G – JANUARY 2000 – REVISED MARCH 2004

- RS-232 Bus-Pin ESD Protection Exceeds ± 15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates Up To 250 kbit/s
- Two Drivers and Two Receivers
- Low Standby Current . . . 1 μ A Typical
- External Capacitors . . . $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbit/s)
 - SNx5C3222
- Applications
 - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The MAX3222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–0°C to 70°C	SOIC (DW)	Tube of 25	MAX3222CDW	MAX3222C
		Reel of 2000	MAX3222CDWR	
	SSOP (DB)	Tube of 70	MAX3222CDB	MA3222C
		Reel of 2000	MAX3222CDBR	
	TSSOP (PW)	Tube of 70	MAX3222CPW	MA3222C
		Reel of 2000	MAX3222CPWR	
–40°C to 85°C	SOIC (DW)	Tube of 25	MAX3222IDW	MAX3222I
		Reel of 2000	MAX3222IDWR	
	SSOP (DB)	Tube of 70	MAX3222IDB	MB3222I
		Reel of 2000	MAX3222IDBR	
	TSSOP (PW)	Tube of 70	MAX3222IPW	MB3222I
		Reel of 2000	MAX3222IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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MAX3222
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
WITH ±15-kV ESD PROTECTION
SLLS408G – JANUARY 2000 – REVISED MARCH 2004

description/ordering information (continued)

The MAX3222 can be placed in the power-down mode by setting $\overline{\text{PWRDOWN}}$ low, which draws only 1 μA from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled; V_+ is lowered to V_{CC} , and V_- is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting $\overline{\text{EN}}$ high.

Function Tables

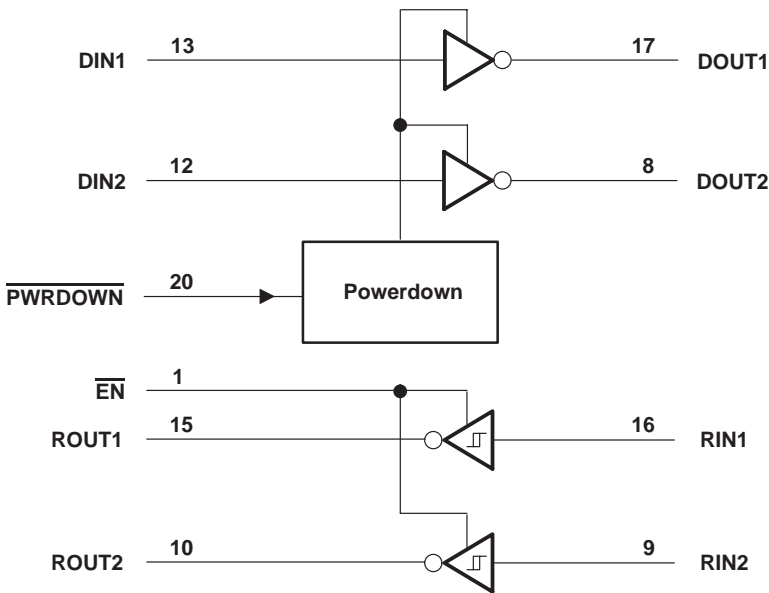
EACH DRIVER		
INPUTS		OUTPUT DOUT
DIN	$\overline{\text{PWRDOWN}}$	
X	L	Z
L	H	H
H	H	L

H = high level, L = low level, X = irrelevant,
Z = high impedance

EACH RECEIVER		
INPUTS		OUTPUT ROUT
RIN	$\overline{\text{EN}}$	
L	L	H
H	L	L
X	H	Z
Open	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), Open = input
disconnected or connected driver off

logic diagram (positive logic)



MAX3222

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ± 15 -kV ESD PROTECTION

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, $V+$ (see Note 1)	–0.3 V to 7 V
Negative output supply voltage range, $V-$ (see Note 1)	0.3 V to –7 V
Supply voltage difference, $V+ - V-$ (see Note 1)	13 V
Input voltage range, V_I : Drivers, \overline{EN} , $\overline{PWRDOWN}$	–0.3 V to 6 V
Receivers	–25 V to 25 V
Output voltage range, V_O : Drivers	–13.2 V to 13.2 V
Receivers	–0.3 V to $V_{CC} + 0.3$ V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package	70°C/W
DW package	58°C/W
PW package	83°C/W
Operating virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 4 and Figure 5)

				MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3$ V		3	3.3	3.6	V
		$V_{CC} = 5$ V		4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	$DIN, \overline{EN}, \overline{PWRDOWN}$	$V_{CC} = 3.3$ V	2			V
			$V_{CC} = 5$ V	2.4			
V_{IL}	Driver and control low-level input voltage	$DIN, \overline{EN}, \overline{PWRDOWN}$				0.8	V
V_I	Driver and control input voltage	$DIN, \overline{EN}, \overline{PWRDOWN}$		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature	MAX3222C		0		70	°C
		MAX3222I		–40		85	

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
I_I	Input leakage current ($\overline{EN}, \overline{PWRDOWN}$)			± 0.01	± 1	μ A
I_{CC}	Supply current	No load, $\overline{PWRDOWN}$ at V_{CC}		0.3	1	mA
	Supply current (powered off)	No load, $\overline{PWRDOWN}$ at GND		1	10	μ A

[‡] All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

NOTE 4: Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.



DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH} High-level output voltage	DOOUT at $R_L = 3\text{ k}\Omega$ to GND, DIN = GND	5	5.4		V
V_{OL} Low-level output voltage	DOOUT at $R_L = 3\text{ k}\Omega$ to GND, DIN = V_{CC}	–5	–5.4		V
I_{IH} High-level input current	$V_I = V_{CC}$		± 0.01	± 1	μA
I_{IL} Low-level input current	V_I at GND		± 0.01	± 1	μA
I_{OS} Short-circuit output current‡	$V_{CC} = 3.6\text{ V}$, $V_O = 0\text{ V}$		± 35	± 60	mA
	$V_{CC} = 5.5\text{ V}$, $V_O = 0\text{ V}$				
r_o Output resistance	V_{CC} , V_+ , and $V_- = 0\text{ V}$, $V_O = \pm 2\text{ V}$	300	10M		Ω
I_{off} Output leakage current	$\overline{\text{PWRDOWN}} = \text{GND}$, $V_{CC} = 3\text{ V to } 3.6\text{ V}$, $V_O = \pm 12\text{ V}$			± 25	μA
	$\overline{\text{PWRDOWN}} = \text{GND}$, $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $V_O = \pm 10\text{ V}$			± 25	

† All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Maximum data rate	$C_L = 1000\text{ pF}$, $R_L = 3\text{ k}\Omega$, One DOOUT switching, See Figure 1	150	250		kbit/s
$t_{sk(p)}$ Pulse skew§	$C_L = 150\text{ pF to } 2500\text{ pF}$, $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, See Figure 2		300		ns
$SR(tr)$ Slew rate, transition region (See Figure 1)	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, $V_{CC} = 3.3\text{ V}$		$C_L = 150\text{ pF to } 1000\text{ pF}$	6	V/ μs
			$C_L = 150\text{ pF to } 2500\text{ pF}$	4	

† All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

§ Pulse skew is defined as $|t_{pLH} - t_{pHL}|$ of each channel of the same device.

NOTE 4: Test conditions are $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\text{ }\mu\text{F}$, $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6 V	V _{CC} - 0.1 V		V
V _{OL} Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+} Positive-going input threshold voltage	V _{CC} = 3.3 V		1.5	2.4	V
	V _{CC} = 5 V		1.8	2.4	
V _{IT-} Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.2		V
	V _{CC} = 5 V	0.8	1.5		
V _{hys} Input hysteresis (V _{IT+} - V _{IT-})			0.3		V
I _{off} Output leakage current	$\overline{\text{EN}} = V_{\text{CC}}$		± 0.05	± 10	μA
r _i Input resistance	V _I = ± 3 V to ± 25 V	3	5	7	k Ω

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V \pm 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

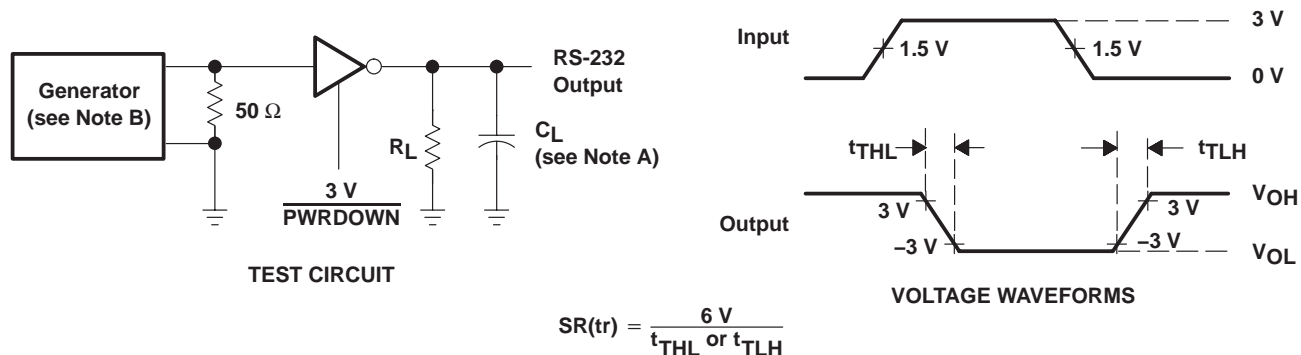
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t _{PLH} Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 3		300		ns
t _{PHL} Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 3		300		ns
t _{en} Output enable time	C _L = 150 pF, R _L = 3 k Ω , See Figure 4		200		ns
t _{dis} Output disable time	C _L = 150 pF, R _L = 3 k Ω , See Figure 4		200		ns
t _{sk(p)} Pulse skew‡	See Figure 3		300		ns

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

‡ Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μF , C2–C4 = 0.33 μF at V_{CC} = 5 V \pm 0.5 V.

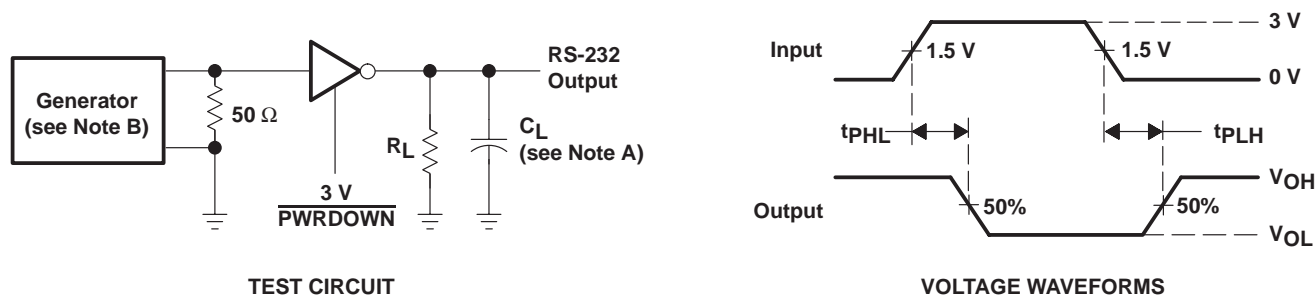
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

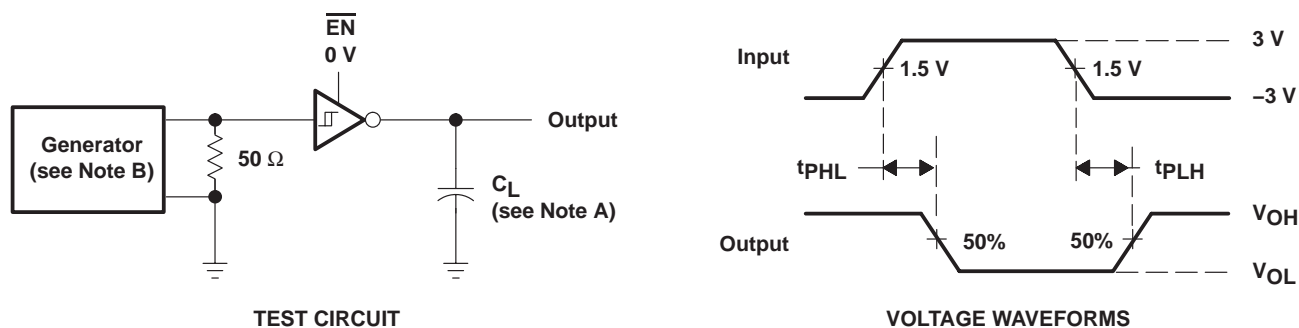
Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 2. Driver Pulse Skew

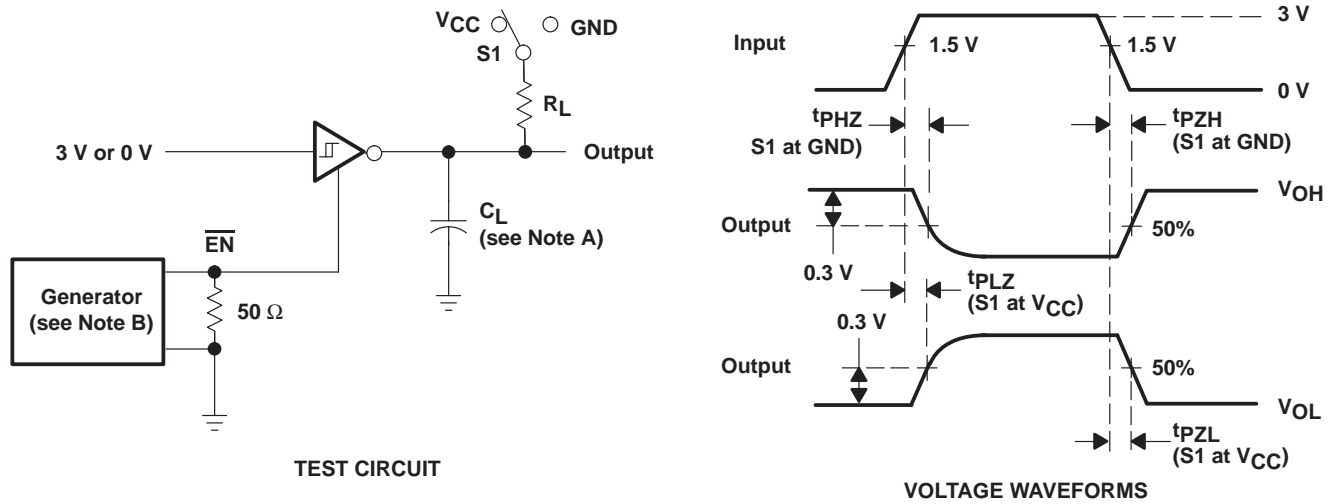


NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Receiver Propagation Delay Times

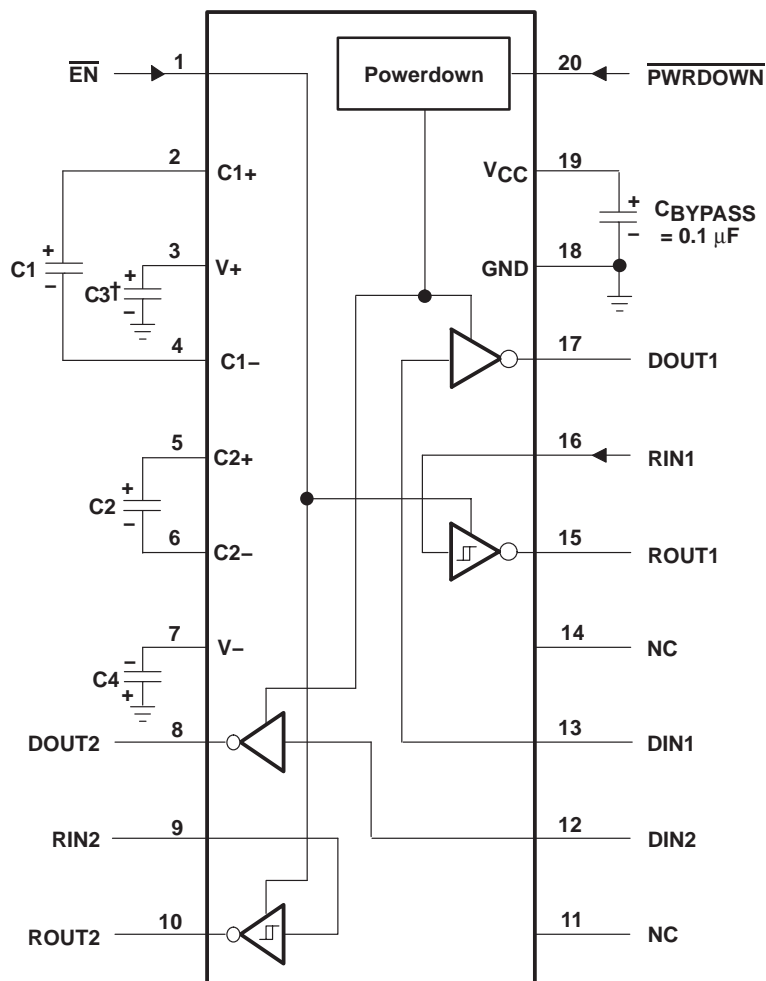
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 4. Receiver Enable and Disable Times

APPLICATION INFORMATION



† C3 can be connected to VCC or GND.

NOTES: A. Resistor values shown are nominal.

B. NC – No internal connection

C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

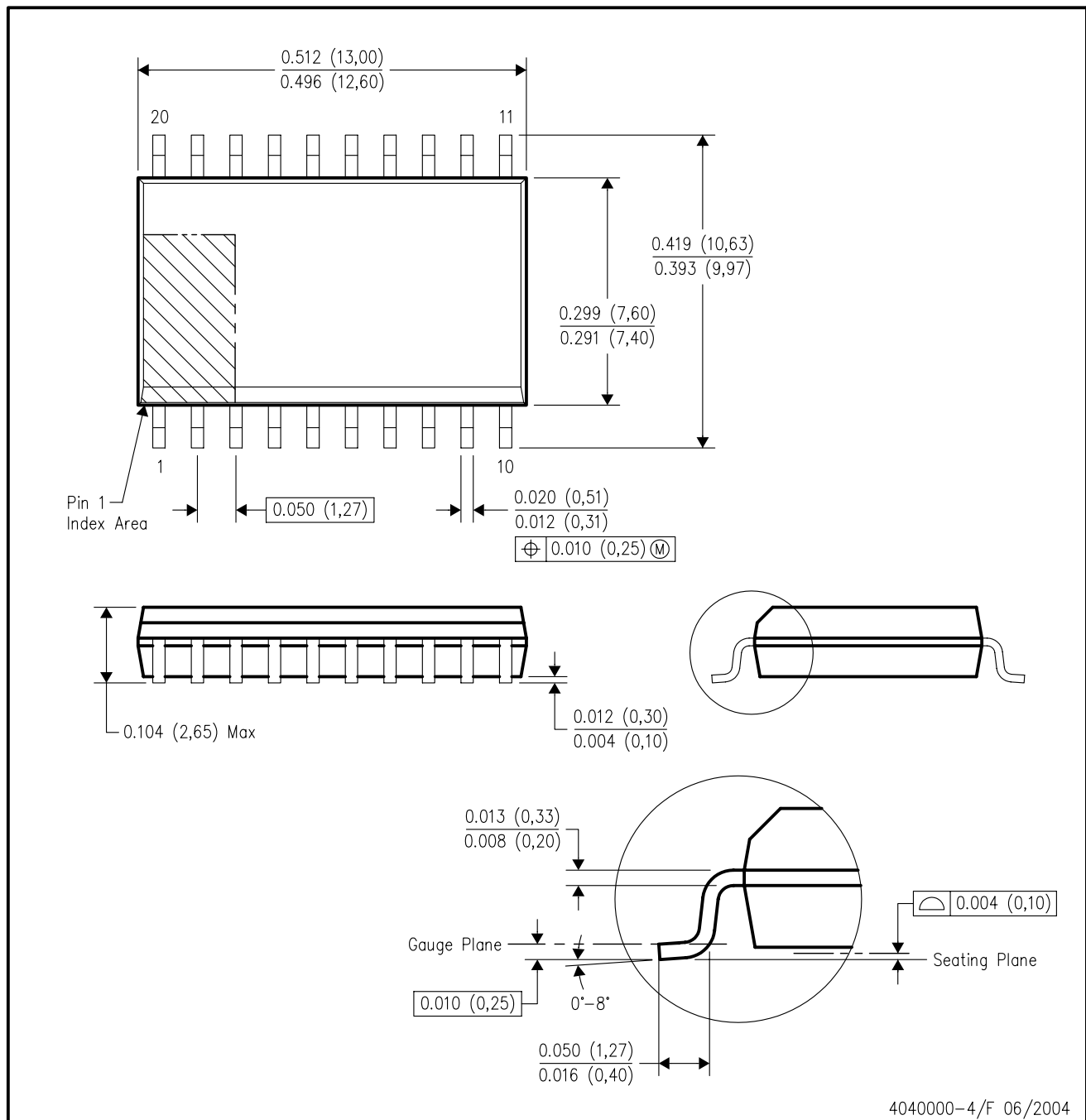
VCC vs CAPACITOR VALUES

VCC	C1	C2, C3, and C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

Figure 5. Typical Operating Circuit and Capacitor Values

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

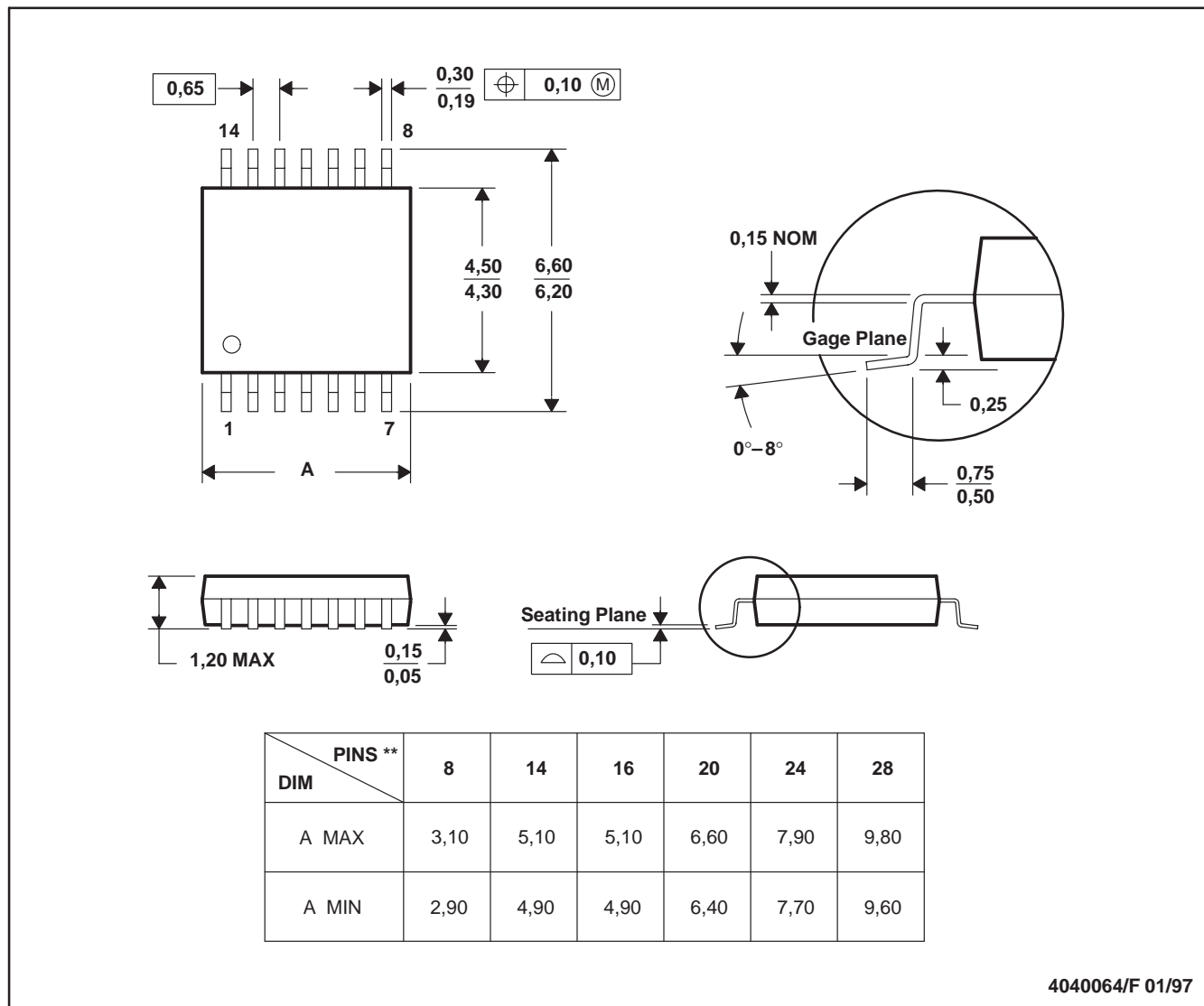


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

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