TMS320F28x DSP Peripherals Reference Guide

Literature Number: SPRU566A
June 2003

Texas Instruments

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Contents

1.1 System Control and Interrupts (literature number SPRU078) 2
1.1.1 Code Security Module (CSM) 2
1.1.2 Peripheral Clocking 2
1.1.3 General-Purpose Input/Output (GPIO) Multiplexer 3
1.1.4 Peripheral Frames 3
1.1.5 Peripheral Interrupt Expansion (PIE) Block 3
1.2 External Interface (XINTF) (SPRU067) 3
1.3 Enhanced Controller Area Network (eCAN) (SPRU074) 3
1.4 Event Manager (EV) (SPRU065) 3
1.5 Analog-to-Digital Converter (ADC) (SPRU060) 4
1.6 Multichannel Buffered Serial Port (McBSP) (SPRU061) 4
1.7 Serial Communications Interface (SCI) (SPRU051) 4
1.8 Serial Port Interface (SPI) (SPRU059) 4
1.9 Boot ROM (SPRU095) 4

TMS320F28x DSP Peripherals

This overview guide includes all the peripherals available for TMS320F28x™ devices. Table 1 shows the peripherals used by each TMS320F28x device. You can download the peripheral guide by clicking on the literature number, which is linked to the portable document format (pdf) file.

Table 1. Peripheral Selection Guide

Peripheral	Lit. No.	F2810™ Device	F2812™ Device
System Control and Interrupts	SPRU078	✓	✓
External Interface (XINTF)	SPRU067		✓
Enhanced Controller Area Network (eCAN)	SPRU074	✓	✓
Event Manager (EV)	SPRU065	✓	✓
Analog-to-Digital Converter (ADC)	SPRU060	✓	✓
Multichannel Buffered Serial Port (McBSP)	SPRU061	✓	✓
Serial Communications Interface (SCI)	SPRU051	✓	✓
Serial Peripheral Interface (SPI)	SPRU059	✓	✓
Boot ROM	SPRU095	✓	✓

Note:

The EV, SCI, and SPI peripherals are almost identical to those available on the 240x™ devices; however, these modules have enhanced features. See the respective documents for details.

Descriptions of the peripherals are included in the following sections.

1.1 System Control and Interrupts (literature number SPRU078)

- The *System Control and Interrupts Peripheral Guide* (SPRU078) includes information on the following modules:
- Memory, including Flash and OTP configuration
- Code security module (CSM)
- Clocking, low power modes, watchdog, and CPU-timers
- General-purpose inputs/outputs (GPIO)
- Peripheral frames
- Peripheral interrupt expansion (PIE)

1.1.1 Code Security Module (CSM)

Security is defined with respect to the access of the on-chip program memory and prevents unauthorized copying of proprietary code. The code security module (CSM) blocks access to several on-chip program memory blocks.

1.1.2 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled so as to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports and the event managers, CAP and QEP blocks can be scaled relative to the CPU clock. This enables the timing of peripherals to be decoupled from increasing CPU clock speeds.

1.1.2.1 CPU-Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timers 1 and 2 are reserved for Real-Time OS (RTOS) applications. CPU-Timer 2 is connected to INT14 of the CPU. CPU-Timer 1 can be connected to INT13 of the CPU. CPU-Timer 0 is for general use and is connected to the PIE block.

1.1.2.2 Watchdog Timer

The F2810 and F2812 support a watchdog timer. The user software must regularly reset the watchdog counter within a certain time frame; otherwise,

the watchdog generates a reset to the processor. The watchdog can be disabled if necessary.

1.1.3 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose I/O (GPIO) signals. This enables you to use a pin as GPIO if the peripheral signal or function is not used. On reset, all GPIO pins are configured as inputs. You can then individually program each pin for GPIO mode or Peripheral Signal mode. For specific inputs, you can also select the number of input qualification cycles to filter unwanted noise glitches.

1.1.4 Peripheral Frames

The F2810 and F2812 contain three peripheral register spaces. Some registers within these frames can be protected from CPU writes by the EALLOW protection mechanism.

1.1.5 Peripheral Interrupt Expansion (PIE) Block

The PIE block multiplexes numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F2810/F2812, 45 of the possible 96 interrupts are used by peripherals. The interrupts are grouped into blocks of eight and each group is fed into one of 12 CPU interrupt lines ($\overline{\text{INT1}}$ to $\overline{\text{INT12}}$). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes nine CPU clock cycles to fetch the vector and save critical CPU registers. Therefore, the CPU can respond quickly to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

1.2 External Interface (XINTF) (SPRU067)

The external interface (XINTF) on the F2812 device is a nonmultiplexed asynchronous bus that is used to interface to external devices and memory.

1.3 Enhanced Controller Area Network (eCAN) (SPRU074)

This is the enhanced version of the CAN peripheral. It supports 32 mailboxes, time stamping of messages, and is CAN 2.0B-compliant.

1.4 Event Manager (EV) (SPRU065)

The event manager module includes general-purpose timers, full-compare/pulse-width modulation (PWM) units, capture inputs (CAP) and

quadrature-encoder pulse (QEP) circuits. Two such event managers are provided, which enable two three-phase motors to be driven or four two-phase motors. The event managers on the F2810 and F2812 are compatible to the event managers on the 240x devices (with some minor enhancements).

1.5 Analog-to-Digital Converter (ADC) (SPRU060)

The ADC block is a 12-bit converter, single ended, 16-channels. It contains two sample-and-hold units for simultaneous sampling.

1.6 Multichannel Buffered Serial Port (McBSP) (SPRU061)

The McBSP is used to connect to E1/T1 lines, phone-quality codecs for modem applications or high-quality stereo-quality Audio DAC devices. The McBSP receive and transmit registers are supported by a 16-level FIFO. This significantly reduces the overhead for servicing this peripheral.

1.7 Serial Communications Interface (SCI) (SPRU051)

The SCI is a two-wire asynchronous serial port, commonly known as UART. On the F2810 and the F2812, the port supports a 16-level, receive and transmit FIFO for reducing servicing overhead.

1.8 Serial Port Interface (SPI) (SPRU059)

The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. On the F2810 and the F2812, the port supports a 16-level, receive and transmit FIFO for reducing servicing overhead.

1.9 Boot ROM (SPRU095)

The boot ROM is factory-programmable with boot-loading software. Boot-mode signals (general-purpose I/Os) are used to tell the bootloader software which mode to use. The F2810 and F2812 Boot ROM also contains standard math tables such as SIN/COS for use in IQ math related algorithms.