Makerere University

College of Engineering Design, Art and Technology

Department of Electrical and Computer Engineering

CMP1203: Computer Organization and Architecture
Continuous Assessment Test1

Date; 22nd March 2019 Time: 8:00 to 9:30 a.m.

INSTRUCTIONS: ANSWER **ALL** QUESTIONS

Note: It is not enough to arrive at the correct answer. You are required to justify ALL your solutions.

Question 1 [20 marks]

a) Indicate whether the following statement are **TRUE** or **FALSE** and explain your choice.

i) Is it impossible to define a single value as an optimum cache size**? [4 marks]**
ii) Set-associative cache mapping is a compromise between direct and fully associative cache mapping. **[4 marks]**
iii) when using direct cache mapping, if the cache is full, a replacement algorithm is required to determine which block must be replaced. **[4 marks]**
iv) An i7 quad core processor that runs at 3 GHz can execute 3 billion instructions per second. **[3 marks]**

b) Two manufacturers are selling hard disk drives. A is selling an array of 12 212.5GB disks for Shs. 200,000 and B is selling an array of 12 212.5GB disk for Shs. 210,000. Assume that manufacturer A is specifying the disk capacity in unformatted decimal BG, whereas manufacturer B is specifying the disk capacity in formatted binary GB. Which manufacture's disk has a smaller, cost per GB? Assume that the disk capacity reduces by 15% after formatting. Explain your answer. [**7 marks]**

Question 2[30 marks]

a) Express **79** and **89** in8-bit binary and add then using;

i) Signed-magnitude representation **[4 marks]**
ii) 2's complement representation **[4 marks]**
iii) Do your answers differ? Lf so, why? **[2 marks]**

b) Modern computer systems can be viewed to be organized in a hierarchy of levels. Each level performs a specific function and exists as a distinct virtual machine. Briefly explain these levels. **[12 marks]**

c) Consider an 8-way high order interleaved memory whose memory capacity is 512 words.

i) How many unique addresses are required for each word in memory? **[2 marks]**
ii) How many addresses are required for each memory module? **[2 marks]**
iii) Hence draw the address structure**. [4 marks]**