Module: Logic Design Lab
Name: …….....
University no:……..
Group no: ……
Lab Partner Name: *Mr. Mohamed El-Said*

Experiment 10: Multiplexers

Objective: To realize and implement

- Two-to-one-line multiplexer using logic gates by on a breadboard.
- Eight-to-one-line Multiplexer Using IC 4051.

Components Required:

- Mini Digital Training and Digital Electronic Sets.
- IC 7404, IC 7408, IC 7432, IC 74153, IC 4051.

Theory:

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is contro1led by a set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

Two-to-One-line Multiplexer (2x1 MUX): A two-to-one-line multiplexer connects one of two 1-bit sources to a common destination, as shown in Fig 1. The circuit has two data input lines, one output line, and one selection line S.

When S = 0, the upper AND gate is enabled and I_0 has a path to the output.

When S = 1, the lower AND gate is enabled and I_1 has a path to the output.

Multiplexer is often labeled as MUX in the block diagram

Truth table for 2x1 MUX

S	Y
0	I_0
1	I_1

$$Y = S'I_0 + SI_1$$

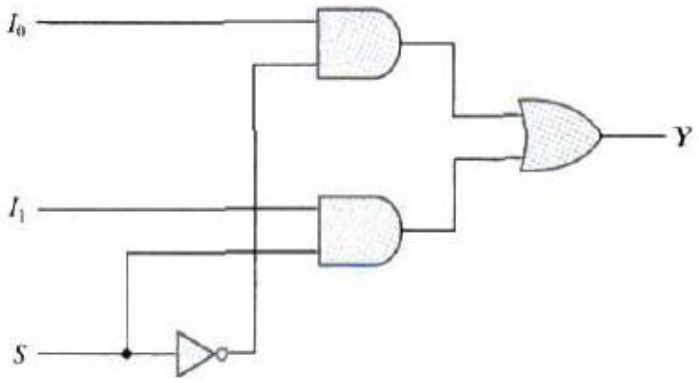


Fig1: Logic diagram of 2x1 MUX

Eight-to-one-line multiplexer (8x1 MUX): An eight-to-one-line multiplexer is a combinational circuit where one of the eight inputs is connected to one output. D_0, D_1, D_2… D_7 are the eight inputs. There are three select lines S_0, S_1, and S_2 to select input.

Truth table for 8-1 multiplexer:

S2	S1	S0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

$$\mathbf{Y = S_2'S_1'S_0'\,D_0 + S_2'S_1'S_0\,D_1 + S_2'S_1S0'\,D_2 + S_2'S_1S_0\,D_3 + S2S1'S0'\,D_4 + S_2S_1'S_0\,D_5 + S_2S_1S_0'\,D_6 + S_2S_1S_0\,D_7}$$

Each of the eight inputs, D_0 through D_7 is applied to one input of an AND gate. Selection lines S_0, S_1, and S_2 are decoded to select a particular AND gate.

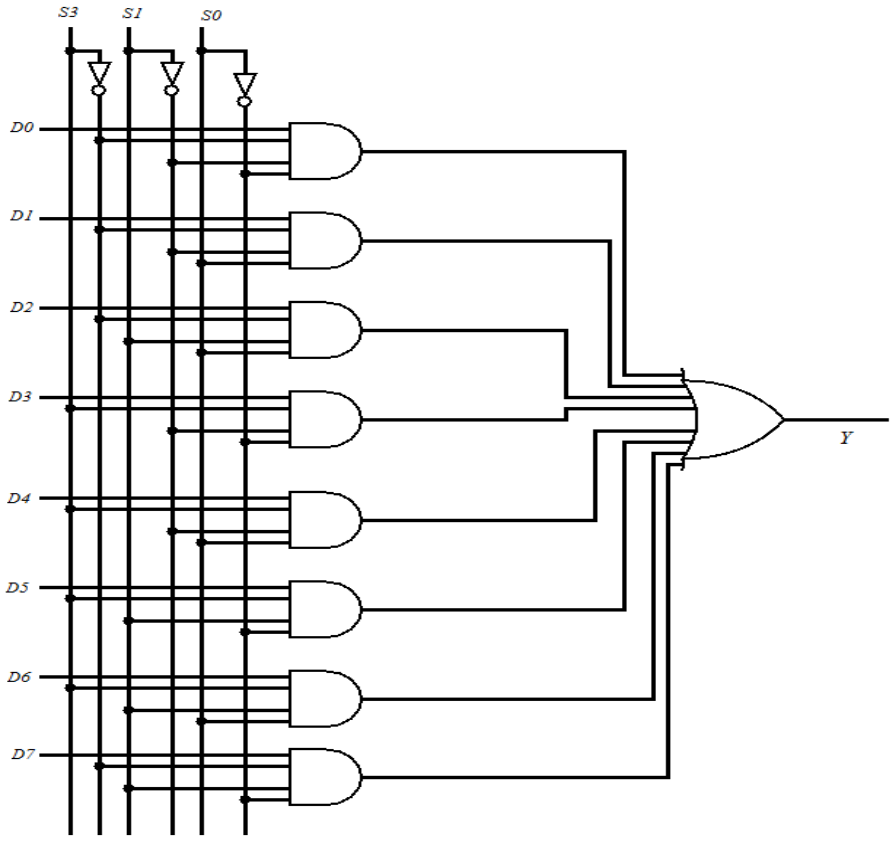


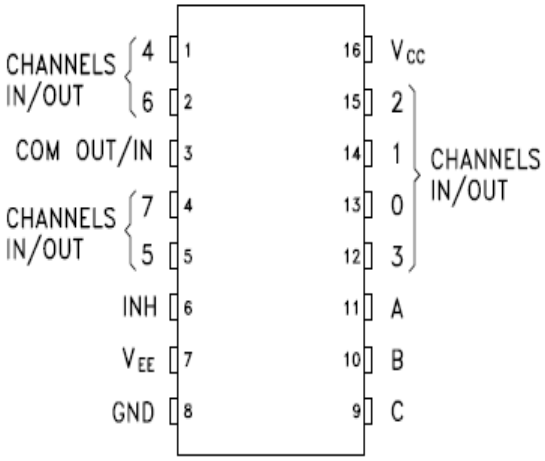
Fig: Logic diagram of 8-1 multiplexer

IC 4051 (Eight-to-One-line Mu1tiplexer):

IC **4051** is single 8-channel analog multiplexers/demultiplexers for application as digitally–controlled analog switches. It contains 8 bidirectional and digitally controlled analog switches. A built-in level shifting is included to allow an input range up to ±6 V (peak) for an analog signal with digital control signal of 0 to 6 V.

The VEE supply pin is provided for analog input signals. It has an inhibit (INH) input terminal to disable all the switches when is at high level. For operation as a digital multiplexer/demultiplexer, VEE is connected to GND. A, B and C control inputs select one channel out of eight

Pin diagram of IC 4051:



Pin description of IC 4051:

Pin number	Symbol	Name and function
3	COM OUT/IN	Common output/input
6	INH	Inhibit input
7	V_{EE}	Negative supply voltage
11, 10, 9	A, B, C	Select inputs
13, 14, 15, 12, 1, 5, 2, 4	X_0 to X_7	Independent input/outputs
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

Part A: Practice Procedure:

1. Implement 2x1 multiplexer using logic gates and breadboard, and verify the truth table.
2. Implement 8x1 multiplexer using IC 4051.

Conclusions: Thus Multiplexer is studied.

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<u>Part B:</u> Lab. Exercise:
Students are directed to do the following exercise.

Q1. Implement 8x1 line multiplexer using basic logic gates.
Draw the truth table of the circuit.
Write the Boolean expression for the output function.

Q2. Show how to implement full-adder circuit using two 4x1 line multiplexer.

Hint: $S(x,y,z) = \Sigma m(1,2,4,7)$, $C(x,y,z) = \Sigma m(3,5,6,7)$

Q3. Implement the function $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$ using a multiplexer.