Experiment # 7

Multiplexers & Demultiplexers

Objectives:

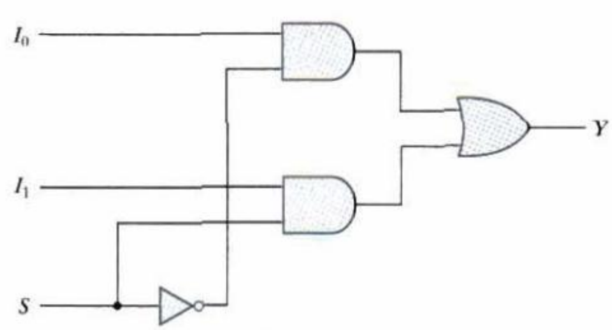
1. Understanding how to implement functions using multiplexers.
2. To study demultiplexer.

Theory:

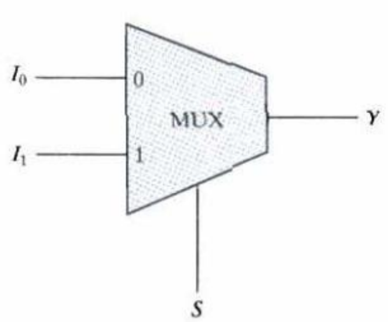
Multiplexers:

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2n input lines and n selection lines whose bit combinations determine which input is selected.

Two-to-one-line multiplexer:



(a) Logic diagram

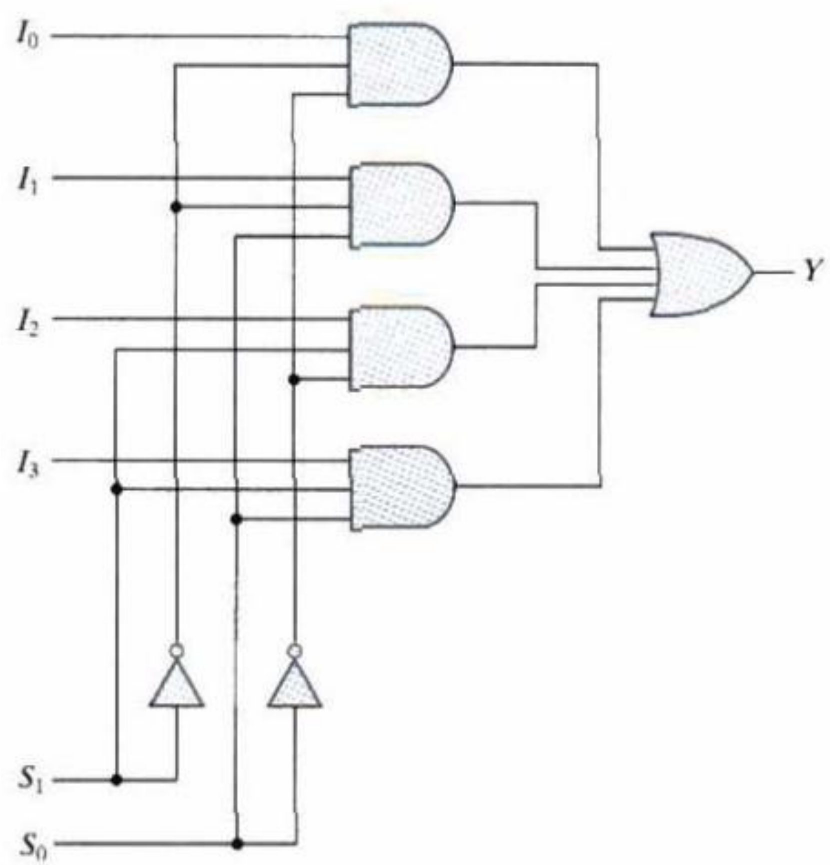


(b) Block diagram

$$Y = S' I_0 + S I_1$$

The circuit has two data input lines, one output line, and one selection line S. When S = 0, the upper AND gate is enabled and I_0 has a path to the output. When S =1, the lower AND gate is enabled and I_1 has a path to the output.

Four-to-one-line multiplexer:



(a) Logic diagram

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

$Y = S1'\ S0'\ I_0 + S1'\ S0\ I_1 + S1\ S0'\ I_2 + S1\ S0\ I_3$

Implementing a Boolean function using multiplexer:

For a function of n variables follow these steps:

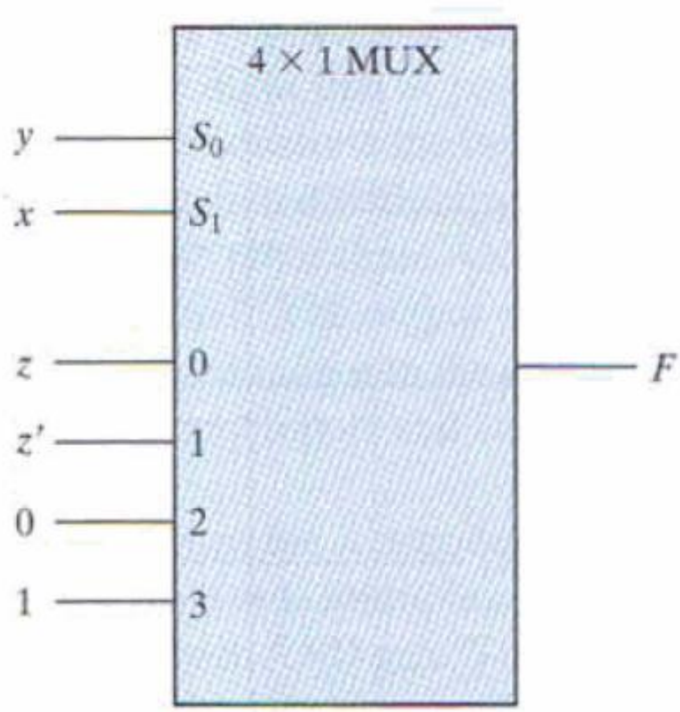
1. Select the type of Mux [2^{n-1}-to-1].
2. Select (n-1) as selection line.
3. The other input connects as input.

Example 1: F(x, y, z) = Σ (1, 2, 6, 7)

1. The type of Mux [2^2-to-1] == 4-to-1 mux.
2. Select (2) as selection line. == For example (x and y).
3. The other input connects as input. == (z).

x	y	z	F	
0	0	0	0	$F = z$
0	0	1	1	
0	1	0	1	$F = z'$
0	1	1	0	
1	0	0	0	$F = 0$
1	0	1	0	
1	1	0	1	$F = 1$
1	1	1	1	

(a) Truth table

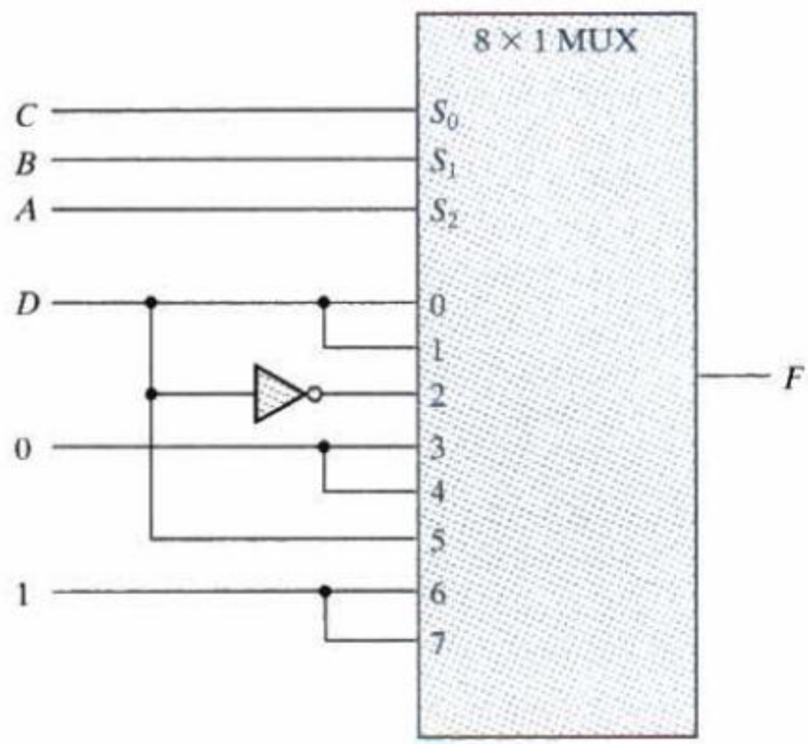


(b) Multiplexer implementation

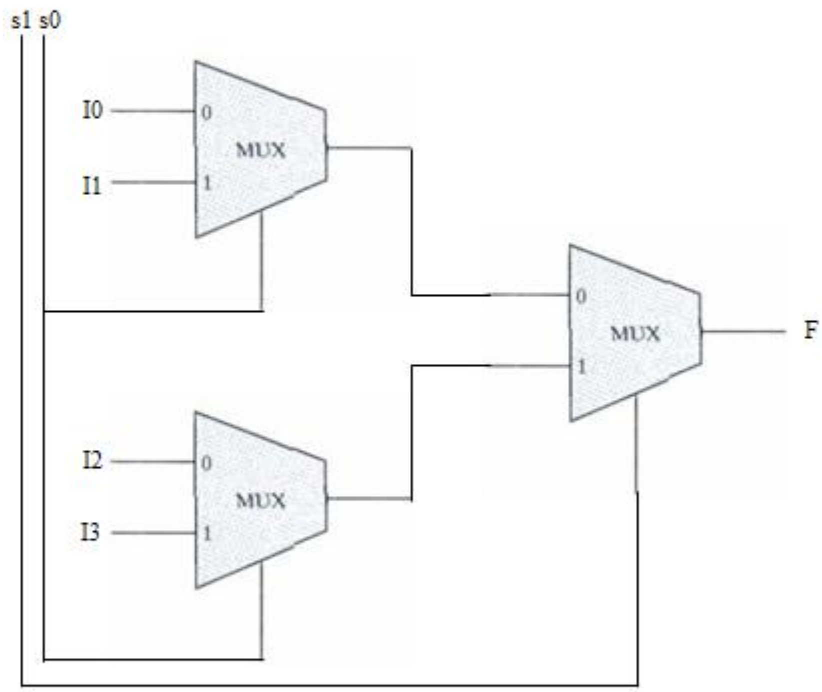
Example 2: F (A, B, C, D) = $\sum$ (1, 3, 4, 11, 12, 13, 14, 15)

1. The type of Mux [2^3-to-1] == 8-to-1 mux.
2. Select (3) as selection line. == For example (A, B and C).
3. The other input connects as input. == (D).

A	B	C	D	F	
0	0	0	0	0	$F = D$
0	0	0	1	1	
0	0	1	0	0	$F = D$
0	0	1	1	1	
0	1	0	0	1	$F = D'$
0	1	0	1	0	
0	1	1	0	0	$F = 0$
0	1	1	1	0	
1	0	0	0	0	$F = 0$
1	0	0	1	0	
1	0	1	0	0	$F = D$
1	0	1	1	1	
1	1	0	0	1	$F = 1$
1	1	0	1	1	
1	1	1	0	1	$F = 1$
1	1	1	1	1	



Building 4-to-1 mux using 2-to-1 mux:



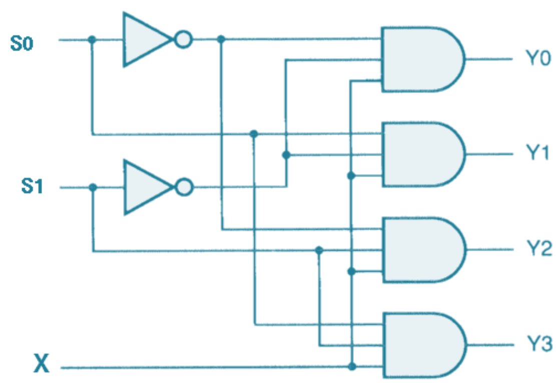
Demultiplexers:

Demultiplexer is a circuit that receives information from a single Line and directs it to one of 2^n possible output lines, the selection of a specific output is controlled by the bit combination of n selection lines.

One-to-four-line demultiplexer:

The following figure shows the block diagram and the truth table for 1x4 Demultiplexer.

By applying logic '1' to the input, the circuit will do the same function of the typical 2-to-4 Decoder.

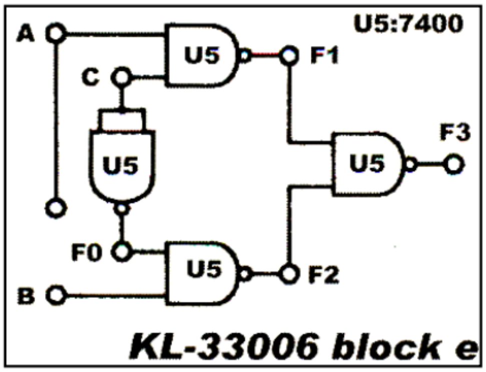


s_1	s_0	x	y_3	y_2	y_1	y_0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Lab Work:

Part 1: 2-to-1 Mux

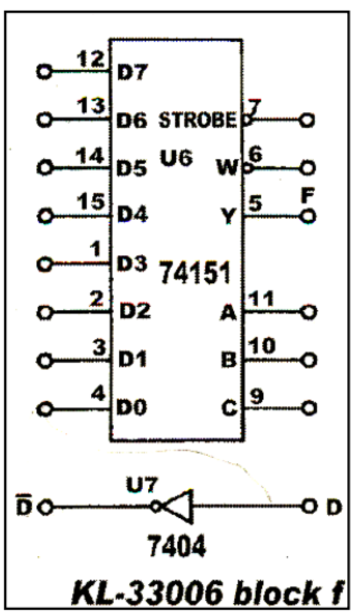
Construct 2-to-1 Mux using KL-33006 block e. (A, B as inputs, C selection line).Connect inputs A, B to SW0 and SW1. Connect input C to SW3.



C	B	A	F3
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Part 2: 8-to-1 Mux

Using Mux KL-33006 block f connect inputs D0-D7 to DIP1 Switch 0-7; inputs C, B, A to DATA Switches SW2, SW1, SW0 respectively, strobe to 0, Y and W to L0, L1 respectively then complete this table.



D7	D6	D5	D4	D3	D2	D1	D0	C	B	A	Y
0	0	0	0	0	0	1	1	0	0	0	
0	0	0	0	0	0	1	0	0	0	1	
0	0	0	1	0	1	0	1	0	1	0	
0	0	0	0	1	0	0	0	0	1	1	
1	0	0	1	0	0	0	0	1	0	0	
0	0	1	0	0	0	0	0	1	0	1	
0	1	1	0	0	0	0	0	1	1	0	
0	0	0	0	0	0	0	0	1	1	1	

Exercises:

a) Implement the following function using mux.

1- F (A, B, C, D) = $\prod$ (3, 8, 12).

2- F (A, B, C) = $\sum$ (0, 1, 6, 7).

b) Build 8-to-1 mux using two 4-to-1 mux and one 2-to-1 mux.