

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

B.Sc COMPUTER ENGINEERING

CMP 2203: DIGITAL LOGIC

SECOND YEAR, SEMESTER 2, 2015/2016

CAT 2

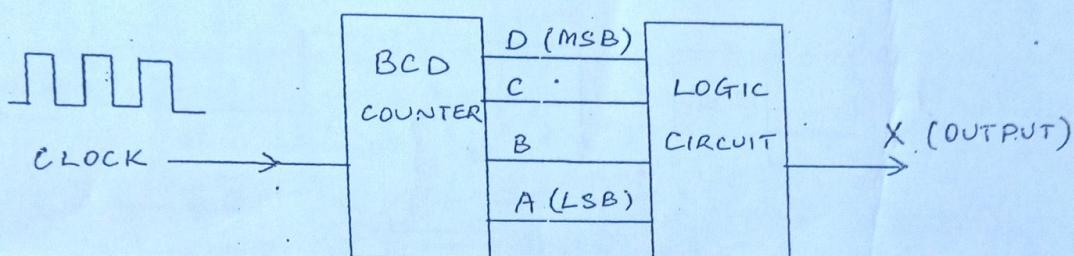
DATE: 26<sup>th</sup> APRIL, 2016

TIME: 10:00-12:00 NOON

INSTRUCTIONS: Answer ALL the FOUR Questions.

QUESTION 1

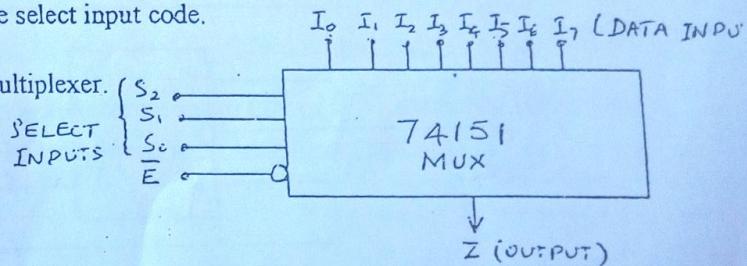
- a) The diagram, below shows a BCD Counter that produces an output code representing the number of Clock pulses applied to the counter.



Use the Karnaugh map and design a minimum Logic circuit that produces a HIGH output whenever the count is 2, 3 or 9

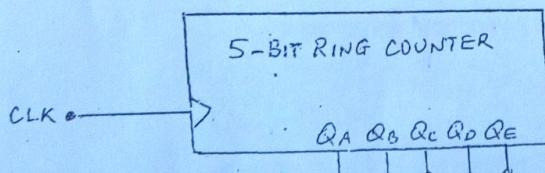
- b) The diagram below is a Logic symbol of the IC 74151 Multiplexer. The Enable input  $\bar{E}$  functions in such a way that when  $\bar{E} = 0$  the select Inputs will give passage of one Data Input to the output and when  $\bar{E} = 1$ , the Multiplexer output is 0 regardless of the select input code.

Draw the Logic circuit of the IC 74151 Multiplexer.



QUESTION 2

- a) The Logic Symbol of a 5-bit Ring Counter shown below:



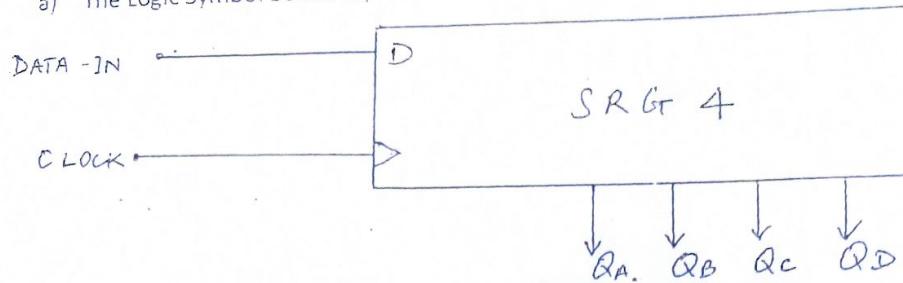
Draw a Logic Circuit of the 5-bit Ring counter using J-K Flip-Flops and a PGT clock.

- b) Assuming that  $Q_A = 1$  initially, show the following for the counter

- Timing diagram for 8 clock pulses.
- Sequence table
- State transition diagram
- Determine modulus of the counter

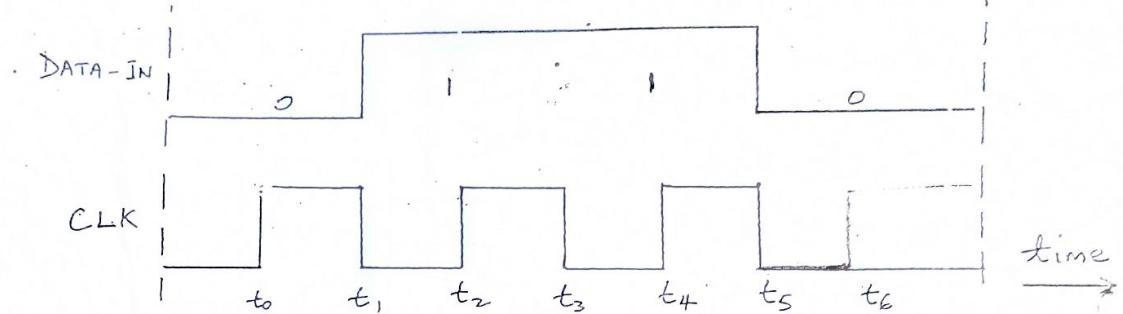
### QUESTION 3

- a) The Logic Symbol below represents a Serial in – Parallel out (SISO) Shift Register using D-type Flip-flops.



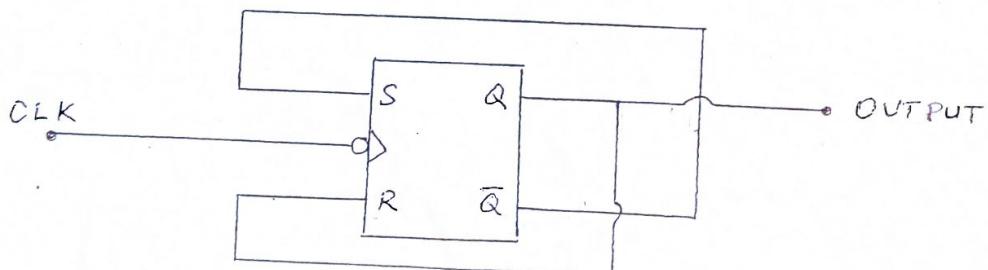
Draw a Logic Circuit of the Shift Register represented by the symbol. Use D type Flip-Flops.

- b) Show the states of the register in (a) above for the Data input and clock waveforms shown below. Assume that all Flip-Flops of the register contain binary 1's initially.



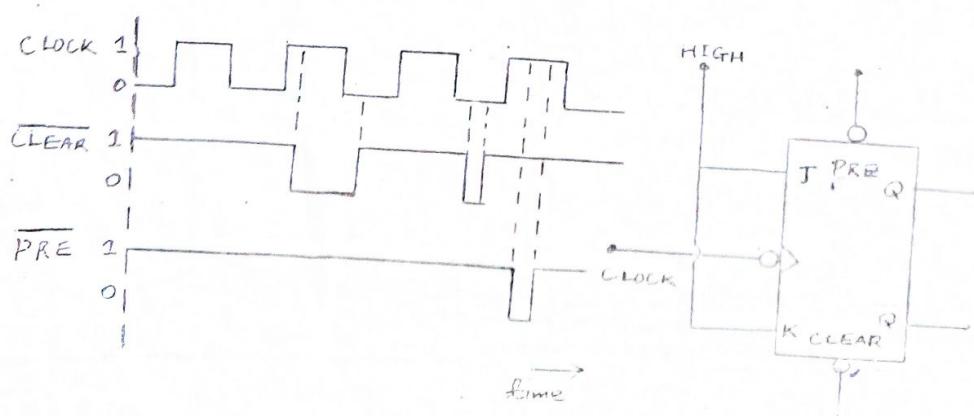
### QUESTION 4

- a) An S-R Flip-Flop is wired as shown in the diagram below:



The Flip-Flop is triggered by a 1 KHZ Clock Signal. Sketch the Q-output wave form for 10 clock pulses and determine the operating mode of the Flip-Flop. Assume the Flip-Flop is initially in the LOW state.

- b) Determine the Q-waveform of the Flop-Flop below, for the given input waveforms.



DATE: 13<sup>TH</sup> MAY, 2016.

TIME: 2.00 – 5.00 PM

**INSTRUCTIONS:**

This paper contains **FIVE** questions. Attempt **FOUR** questions only.  
Each question carries a total of 25 marks.

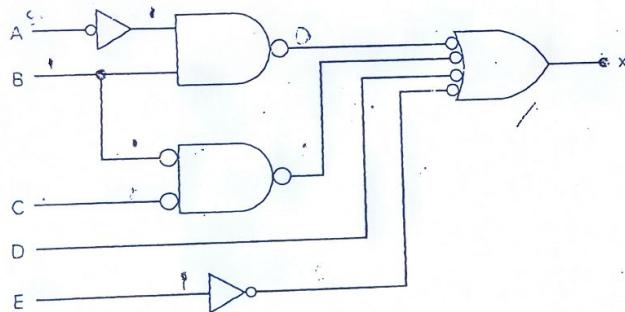
**QUESTION 1**

- a) Simplify the following logic expression using a Karnaugh map and draw the simplified logic function.

$$Y = \overline{(C+D)} + \overline{AC}\bar{D} + \overline{ABC} + \overline{AB}\overline{CD} + A\overline{CD}$$

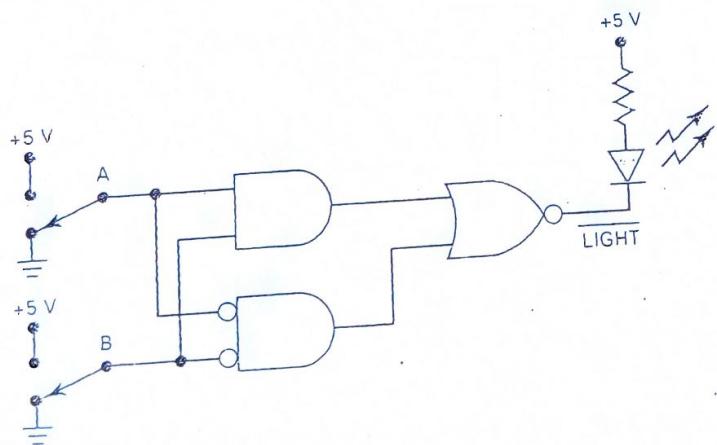
(8 marks)

- b) Determine the input conditions needed to cause the output in the Logic circuit below to go to it's ACTIVE HIGH state and write a complete truth table for the circuit.



(10 marks)

- c) The logic circuit below simulates a two-way switch to turn a lamp ON or OFF from two different switches. Here the lamp is an LED which will be on when the NOR gate output is LOW.

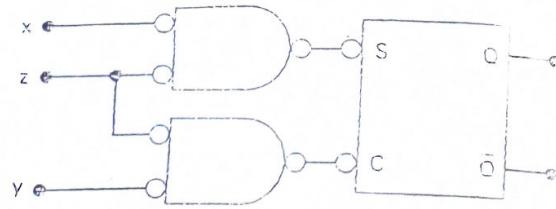
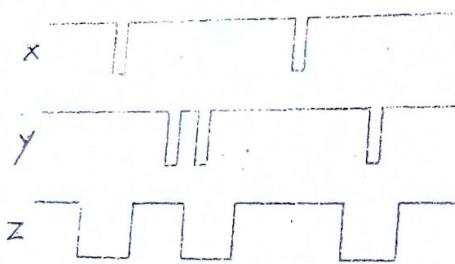


- i) Determine the input conditions needed to turn ON the LED.  
ii) Verify that the circuit operates as a two-way switch.

(7 marks)

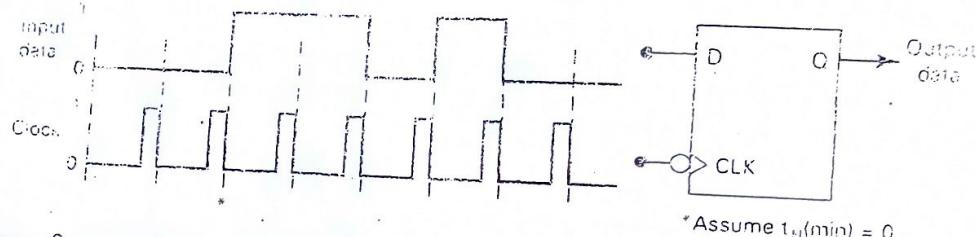
**QUESTION 2**

✓ a) The waveforms x, y and z are connected to the logic circuit shown.



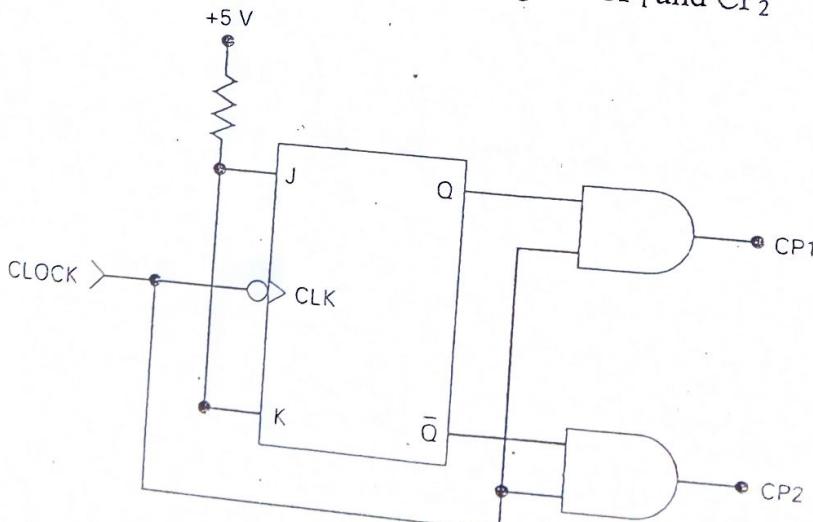
Assuming Q = 0 initially, Sketch the Q - waveform

- b) The DATA and Clock waveforms are applied to the edge-triggered D-type Flip-flop as shown below. (7 marks)



Sketch the Q - waveform and on this waveform and briefly comment on this waveform in comparison with the input Data waveform.

- c) The logic circuit below is used to generate two signals CP<sub>1</sub> and CP<sub>2</sub> (8 marks)

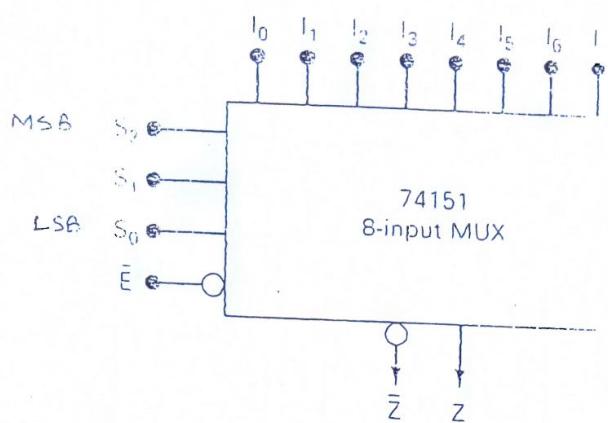


- i) Sketch CP<sub>1</sub> and CP<sub>2</sub> waveforms for five input clock pulses. Assume Q = 0 initially and zero propagation delay.  
 ii) Determine the frequency of CP<sub>1</sub> and CP<sub>2</sub> signals.

(10 marks)

### QUESTION 3

- a) The logic symbol of the 74151 IC, 8-input multiplexer is shown below:



- i) Draw the logic circuit of the 74151 MUX.
- ii) Construct a truth table of the MUX.

(10 Ma)

- b) Two 74151 ICs, an Inverter and an OR-gate are used to implement a 16-input multiplexer.

Using the logic symbol of the 74151 MUX, implement the 16-input MUX and describe the circuit operation.

(10 ma)

- c) The 74151 MUX is used to generate a logic function represented by the truth table below:

Inputs C B A	Output Z
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	0
1 0 1	0
1 1 0	0
1 1 1	1

Show the wiring of the 74151 MUX required to generate the logic function, Z as a Sum of Products.

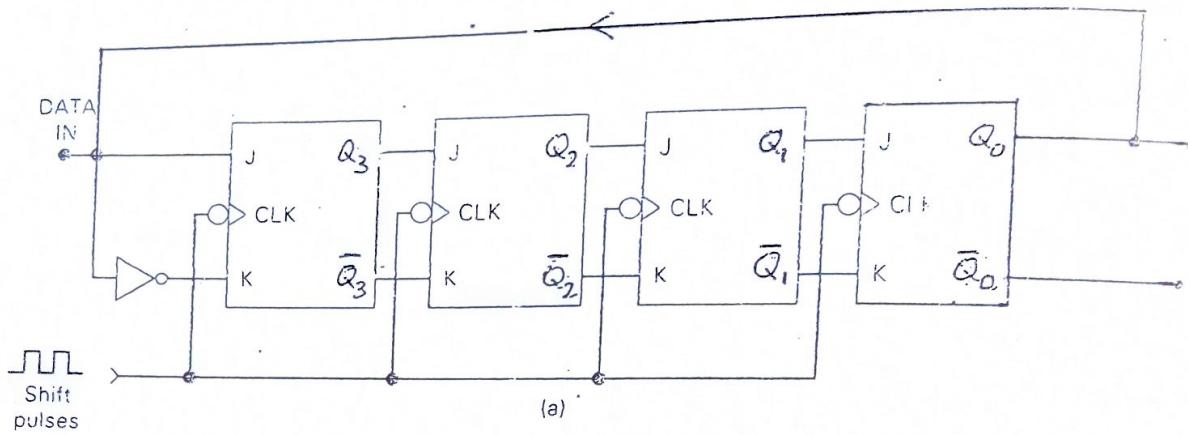
(5 n)

## QUESTION 4

- a) Draw a logic circuit showing synchronous parallel transfer of DATA from one 3-bit register to another using JK -flip flops.

(8 marks)

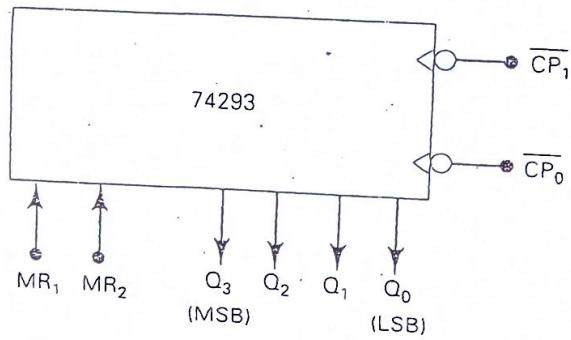
- b) The logic circuit below shows a circulating shift register.



Assume that the register starts with  $Q_3 Q_2 Q_1 Q_0 = 1 0 1 1$  stored in it, construct a sequence table of the register for 9 clock pulses.

(8 marks)

- c) The logic symbol of the 74293 IC asynchronous counter is shown below:



Show how two 74293 ICs can be connected such that a MOD-15 counter drives a MOD-4 counter to implement a MOD-60 counter.

## QUESTION 5

(9 marks)

- a) Draw the logic circuit of a MOD-6 asynchronous counter formed from a MOD-3 counter and a MOD-2 counter. Use JK type Flip-flops.

(8 marks)

- b) Sketch the waveforms at the Flip-flop outputs for 12 Clock pulses.  
Assume all Flip-flops are initially in the low state.

- c) Construct the state transition diagram of the MOD-6 counter.

(12 marks)

(5 marks)

MAKERERE UNIVERSITY  
COLLEGE OF ENGINEERING, DESIGN, ART AND TECHNOLOGY  
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING  
SECOND YEAR, SECOND SEMESTER EXAMINATIONS.2015/2016

CMP 2203: DIGITAL LOGIC

DATE: 17<sup>TH</sup> MAY, 2016.

TIME: 9.00 – 12.00 NOON

**INSTRUCTIONS:**

This paper contains **FIVE** questions. Attempt **FOUR** questions only.  
Each question carries a total of 25 marks.

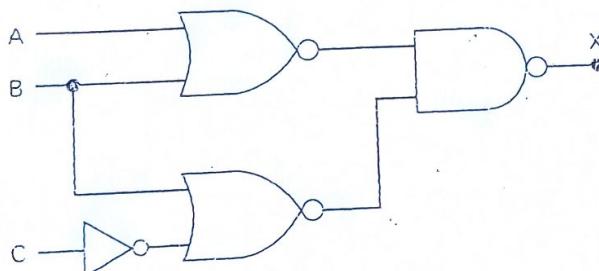
**QUESTION 1**

- a) Use a Karnaugh map to simplify the Logic function below and draw the simplified Logic circuit using NAND gates only.

$$Y = \bar{A} \bar{B} \bar{C} + \bar{B}C + \bar{A}B$$

(9 marks)

- b) Determine the truth table for the Logic circuit below:



*Spares*

- Synthesis & analysis
- Switch modeling
- Block diagram
- Minimization
- Gate

(8 marks)

- c) The circuit in part (b) above operates with an active-LOW output and turns ON an indicator lamp under the following input conditions:

A = B = LOW (LOGIC 0)

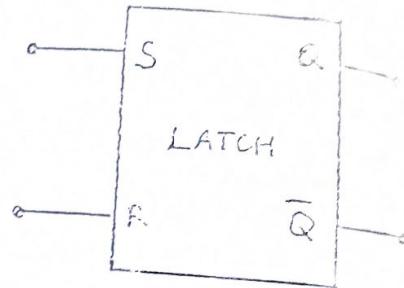
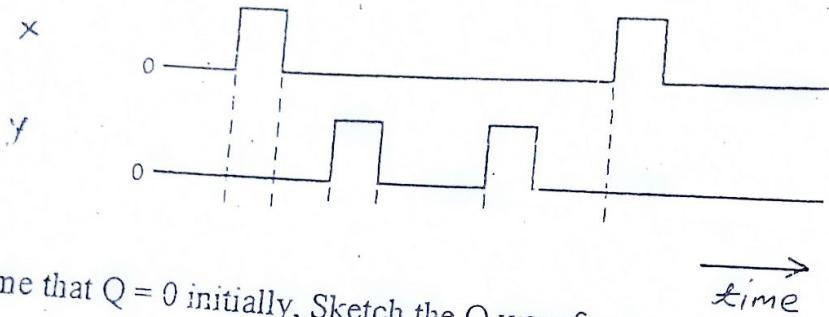
C = HIGH (LOGIC 1)

Draw a modified Logic circuit to represent this mode of operation.

(8 marks)

QUESTION 2

- a) Using appropriate Logic circuits and Truth tables briefly explain how the following latches are conditioned to operate in a digital system design.
- SR-NOR Latch
  - SR-NAND Latch
- b) i) The x and y waveforms below are applied to the S and R inputs of a NOR latch. (8 marks)

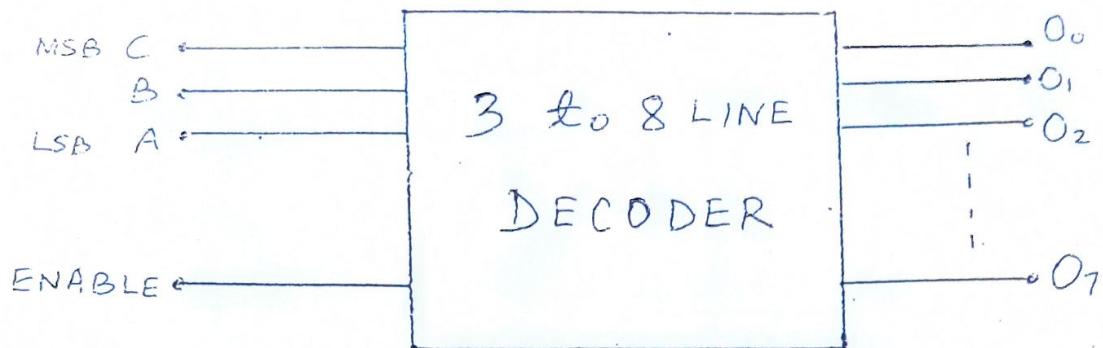


Assume that  $Q = 0$  initially, Sketch the  $Q$  waveform.

- ii) Invert the x and y waveforms and apply them to the SET and RESET inputs of a NAND Latch, determine the  $Q$  waveform. Assume  $Q = 0$  initially.
- c) i) Draw a Logic circuit used for serial transfer of a DATA word  $X_2 X_1 X_0$ <sub>LSB</sub> = 1 0 1 from one register X to another register Y leaving register X with a DATA word  $X_2 X_1 X_0$  = 0 0 0 at the end of the transfer operation. Use D-type Flip-flops. (8 marks)
- iii) Modify the Logic circuit in part (i) above so that the original DATA word stored in register X is present in both registers at the end of the transfer operation. (9 marks)

### QUESTION 3

The block symbol below represents a 3 to 8 line Decoder.



$S_2 S_1 S_0$
0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0

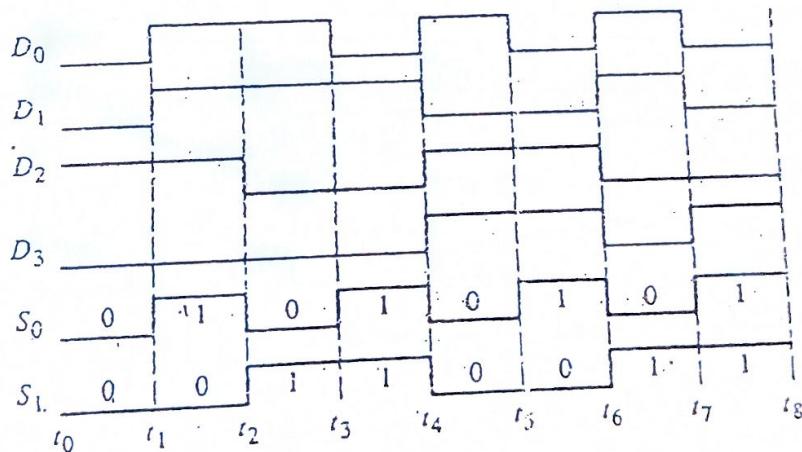
- a) Draw a Logic circuit of the Decoder and construct its truth table

(1)

- b) Show how a 1 to 8 line Demultiplexer can be implemented using the Decoder circuit in part (a) above

(1)

- c) The following Data and select waveforms are applied to 1 of 8 multiplexer.

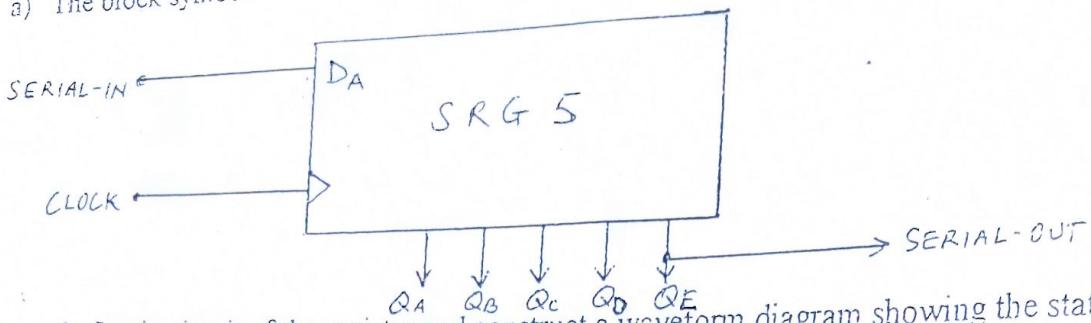


Determine the output waveform.

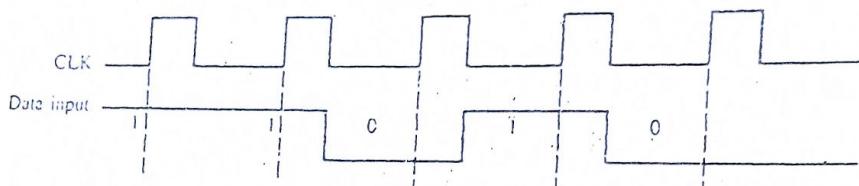
#### QUESTION 4

The block symbol of a 5-bit SISO type register using D-type Flip-flops is shown below:

- a) The block symbol of a 5-bit SISO type register using D-type Flip-flops is shown below:

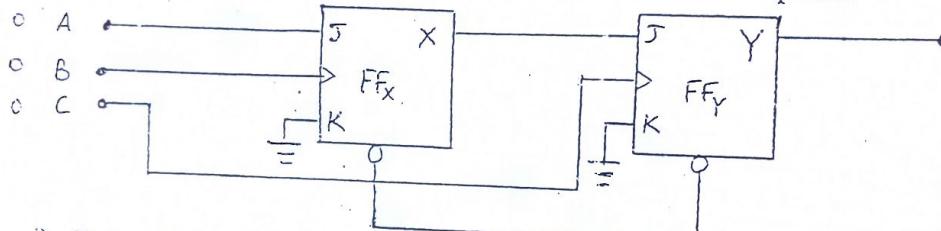


Draw the Logic circuit of the register and construct a waveform diagram showing the states of the register for the following specified Data input and Clock waveforms. Assume that the register is initially cleared



(10 marks)

- b) In the Logic circuit below the inputs A, B and C are all initially LOW, output Y is supposed to go HIGH only when the inputs(HIGH or LOW) change in a certain sequence

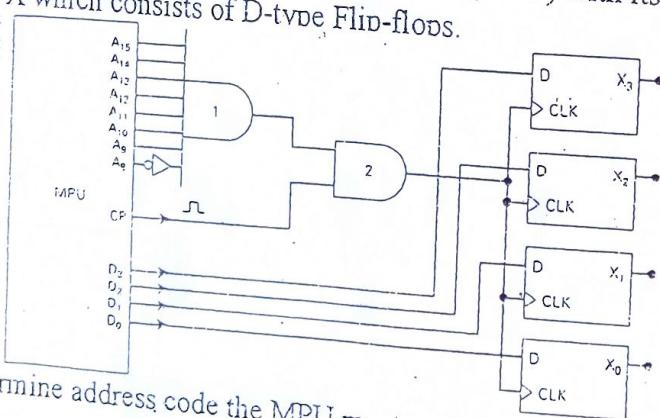


START

- i) Determine the sequence that will make Y go HIGH.  
ii) Explain why a START pulse is needed.

(6 marks)

- c) The figure below shows a microprocessor unit (MPU) with its outputs used to transfer Binary data to register X which consists of D-type Flip-flops.

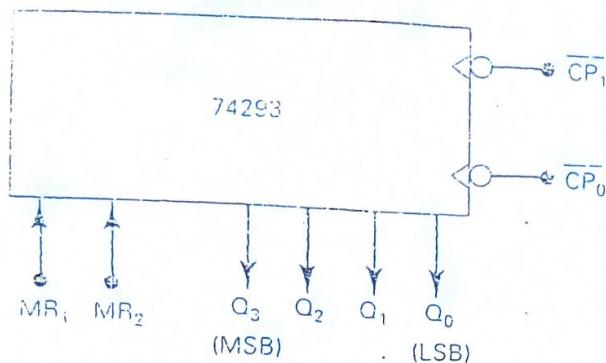


- i)  
ii) Determine address code the MPU must generate for the Data to be transferred into register X  
Assume that  $X_3 - X_0 = 0110$ ,  $A_{15} - A_8 = 11111111$ ,  $D_3 - D_0 = 1011$ . Determine the contents in register X after the clock pulse occurs.  
iii) Modify the circuit above so that only the presence of address code 10110110 will allow Data to be transferred to register X.

(9 Marks)

## QUESTION 5

The Logic symbol of the 74293 IC asynchronous counter is shown below:



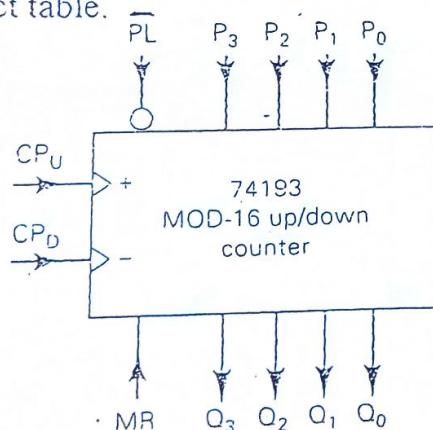
- a) Draw the Logic circuit of the 74293 IC asynchronous counter

(8 marks)

- b) Use the Logic symbol of the 74293 IC counter and show how it can be wired to produce 1.2kpps output from 18kpps clock input.

(8 marks)

- c) The figure below is a Logic symbol of the 74193 IC MOD -16 presetable UP/DOWN counter and its Mode select table.



Mode Select				
MR	PL	CP <sub>U</sub>	CP <sub>D</sub>	Mode
H	X	X	X	Asynch. reset
L	L	X	X	Asynch. preset
L	H	H	H	No change
L	H	↑	H	Count up
L	H	H	↑	Count down

H = HIGH; L = LOW  
X = Don't care; ↑ = PGT

With the clock wired at CP<sub>D</sub> terminal, MR at ground potential and CP<sub>U</sub> terminal maintained in the HIGH state, draw the state transition diagram of the counter

(9 marks)

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

B.Sc ELECTRICAL AND B.Sc TELECOMMUNICATIONS ENGINEERING

ELE 1201: INTRODUCTION TO DIGITAL ELECTRONICS

FIRST YEAR, SEMESTER 2, 2015/2016

CAT 2

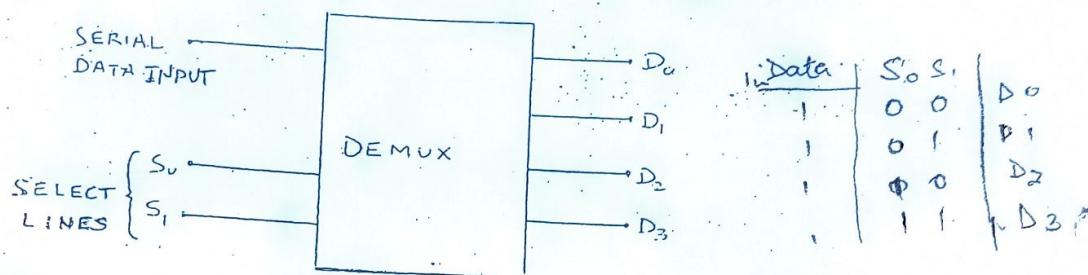
DATE: 25<sup>th</sup> APRIL, 2016

TIME 10:00 – 12:00 NOON

INSTRUCTIONS: ANSWER ALL THE FOUR QUESTIONS

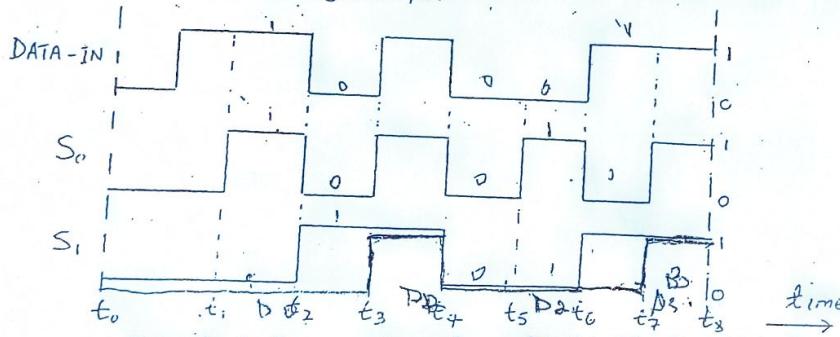
QUESTION 1

- a) The Logic Symbol below represents a 1 to 4 line Demultiplexer.



Synthesize a Logic circuit of the Demultiplexer and briefly explain its operation.

- b) The Serial data-input waveform and select inputs to the Demultiplexer in part (a) are shown in the figure below:

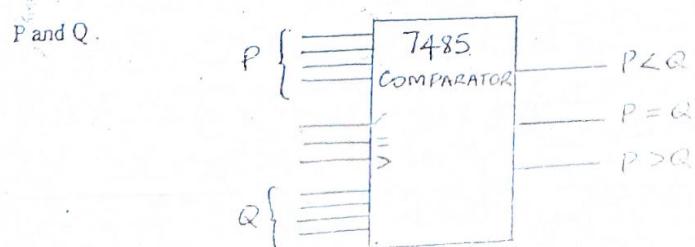


Determine the Data output waveforms of the 1 to 4 line Demultiplexer.

QUESTION 2

- a) Briefly explain how the EXCLUSIVE-NOR gate functions as a basic digital magnitude comparator and design a logic circuit that determines the equality of two binary numbers each having 4 bits.

- b) The figure below is a logic symbol for a 4-bit IC 7485 magnitude comparator for two binary numbers P and Q.



Using two 7485, draw a waveform diagram showing all necessary inputs and outputs of the comparators.

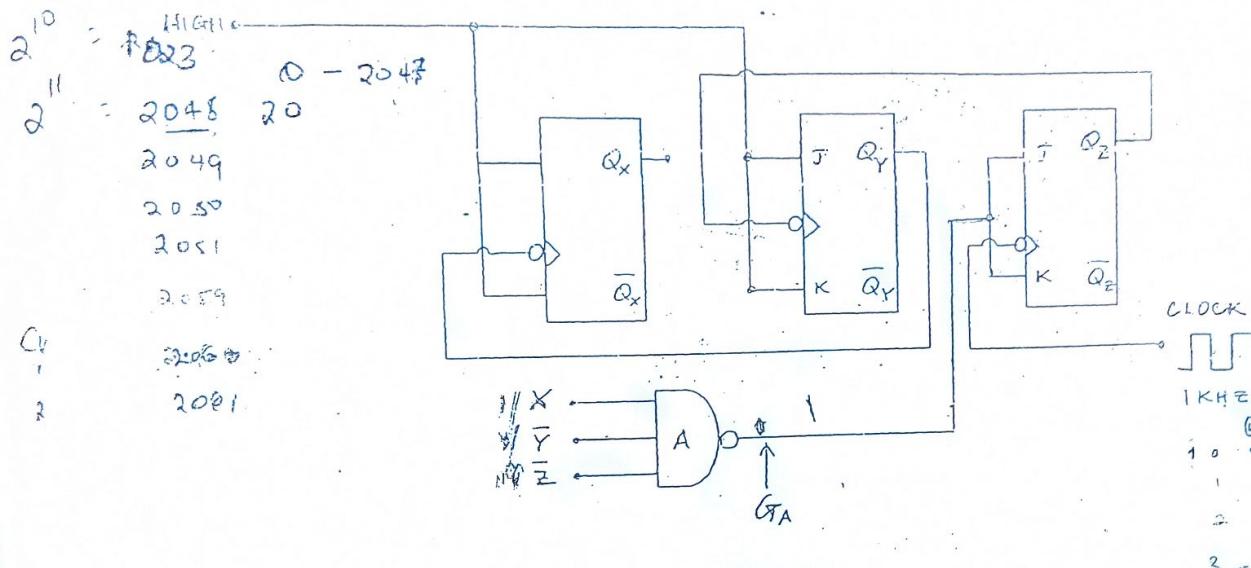
a) An asynchronous binary counter is designed to give a decimal counting range from 0 to 1011. Determine the following specifications of the counter:

- Number of Flip-Flops required to build the counter
- Frequency of the output waveform at the last Flip-Flop in the cascade
- Modulus of the counter
- Decimal count after 2060 clock pulses.

b) The diagram in the Figure below is a counter with all the Flip-Flops existing in the LOW state before the application of the clock pulses.

$$2^{11} = \underline{2048}$$

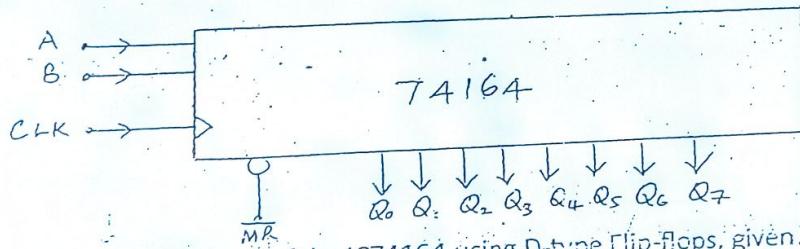
1	1	1	1
2	2	2	2
4	4	4	4
8	8	8	8
16	16	16	16
32	32	32	32
64	64	64	64
128	128	128	128
256	256	256	256
512	512	512	512
1024	1024	1024	1024



Sketch, on the same time scale, the Voltage waveforms  $Q_2$ ,  $Q_3$ ,  $Q_x$  and  $G_A$  for eight clock pulses and comment on the operation of the counter.

#### QUESTION 4

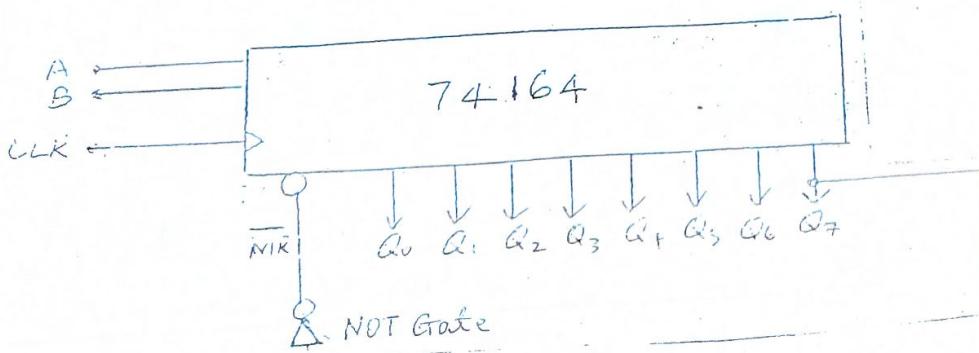
a) The logic symbol for the IC 74164 SIPO Register is shown below:



A, B are inputs to an AND gate within the IC, whose out. is the SERIAL input to the Register

Draw the circuit diagram of the IC74164 using D-type Flip-flops, given that an AND gate combines inputs A, B to produce the serial input to FF<sub>0</sub>

b) The IC74164 is wired as shown below. Assuming all the Flip-flops are initially cleared with A and B inputs maintained in the HIGH state, Construct a sequence table of the register for 9 clock pulses.



FIRST YEAR, SEMESTER 2, 2015 / 2016

## CAT 1

Date: 14<sup>th</sup> MARCH, 2016

TIME: 10.00 - 12.00 NOON

INSTRUCTIONS: Answer ALL the FOUR questions

Question 1

- a) Use Boolean algebra and verify that the following Logic function:

$$F = (\bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D})$$

Reduces to :

$$F = (\bar{A} \oplus C) + (\bar{B} \oplus \bar{D})$$

- b) (i) Verify, by giving relevant Logic expressions, that a two input AND gate can be realized using two input NOR gates.
- (ii) Draw the AND gate equivalent Logic circuit
- c) Design a logic circuit having input signal A, control input B and outputs X and Y to operate as follows:
1. When B = 1, output X will follow input A and output Y will be 0
  2. When B= 0, output X will be 0 and output Y will follow input A.

Question 2

- a) Given the Logic functions:  $F = \bar{A}C + \bar{A}B + A\bar{B}C + BC$

- i) Express it as a sum of minterms
- ii) Using Karnaugh map, deduce the minimal sum of products expression.

- b) Write a truth table for the following Logic function:

$$F(x,y,z) = \sum(0,6)$$

Synthesize a Logic circuit using two input and three input NAND gates exclusively

- c) Using a Karnaugh map derive the minimum logic circuit of figure 2 below.

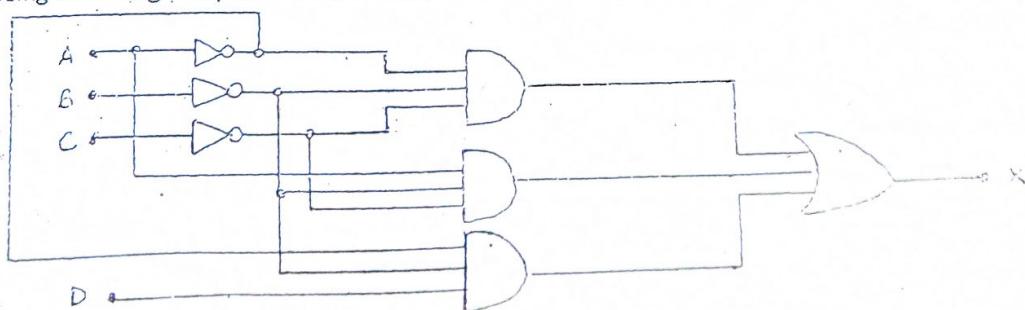
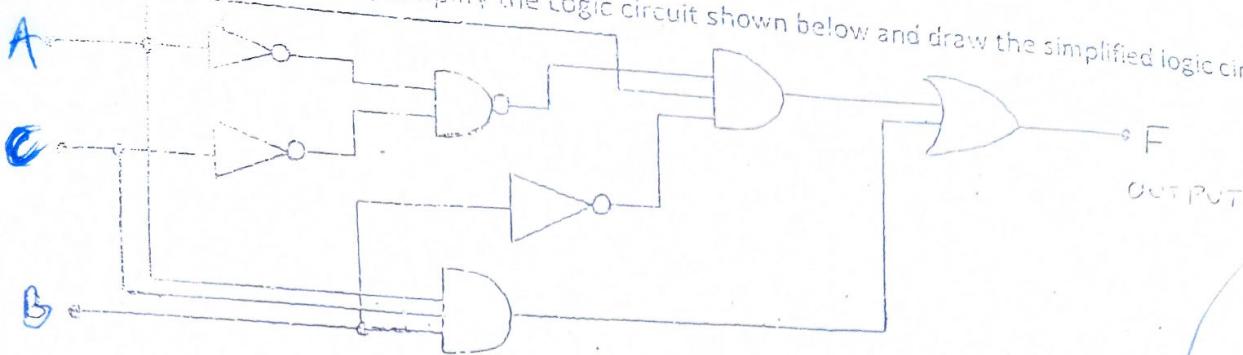
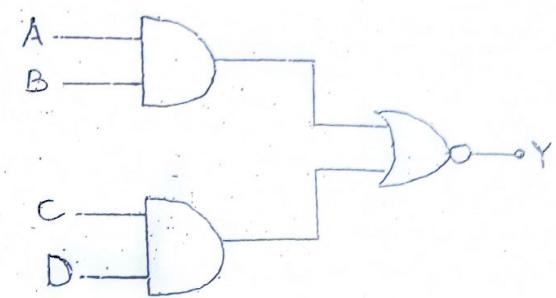
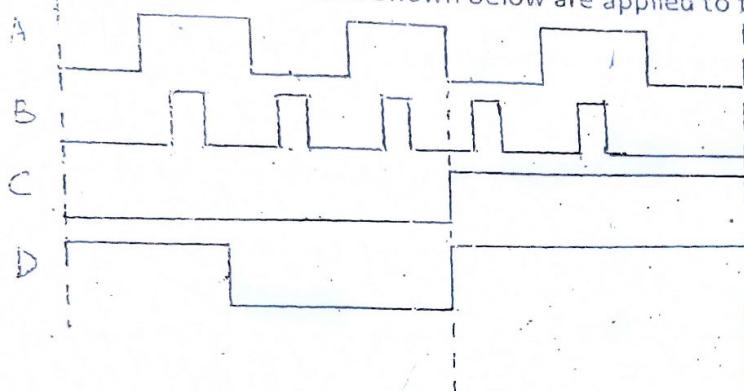


FIGURE 2



b) Using a Karnaugh map, verify that the logic function  $F = \bar{C}(\bar{A}\bar{B}\bar{D} + D) + \bar{A}\bar{B}C + \bar{D}$  reduces to  $F = \bar{C} + \bar{D} + A\bar{B}$

c) The pulse waveforms shown below are applied to the logic circuit shown. Sketch the waveform Y.



#### Question 4

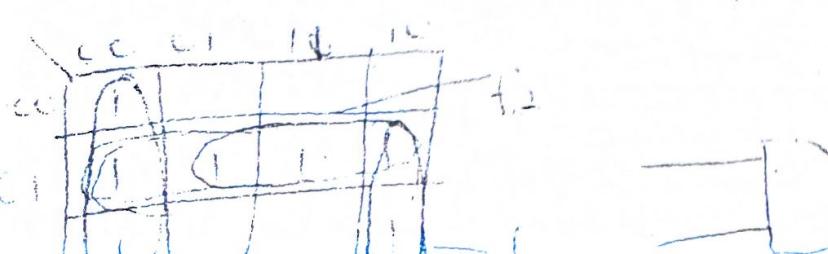
A Logic circuit that controls a LIFT door in a three-storey building has four inputs:

- M is a logic signal that indicates when the LIFT is moving ( $M=1$ ) or stopped ( $M=0$ )
- $F_1, F_2, F_3$  are floor indicator signals that are normally LOW and they go HIGH only when the LIFT is positioned at the particular floor. For example when the LIFT is lined up with the second floor  $F_2 = 1$  and  $F_1 = F_3 = 0$

The Logic Circuit output is the OPEN signal which is normally LOW and will go HIGH when the LIFT door is to be opened.

- Fill-in the truth table for the control logic circuit, taking into consideration all the don't care conditions.
- Using a Karnaugh map deduce a minimum Logic function for the OPEN output
- Implement the minimum control Logic circuit for the LIFT.

for  $f_1 = \begin{array}{c|ccccc} & A & B & C & D \\ \hline 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 \end{array} \quad f_2 = \begin{array}{c|ccccc} & A & B & C & D \\ \hline 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{array} \quad f_3 = \begin{array}{c|ccccc} & A & B & C & D \\ \hline 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{array}$



A	B	C	D	OPEN
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0

$$F = (\bar{A} + \bar{B}) = (\bar{A}\bar{B})$$

$$F = (\bar{A} + \bar{B})(\bar{A}\bar{B})$$

$$\begin{aligned} F &= \bar{A}\bar{A} + \bar{A}\bar{B} + \bar{B}\bar{A} \\ &= \bar{A}\bar{B} + \bar{B}\bar{A} \end{aligned}$$

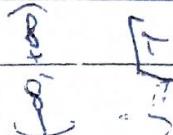
Date: 27<sup>th</sup> MARCH, 2015

TIME: 10.00 - 12.00NOON

CAT 1

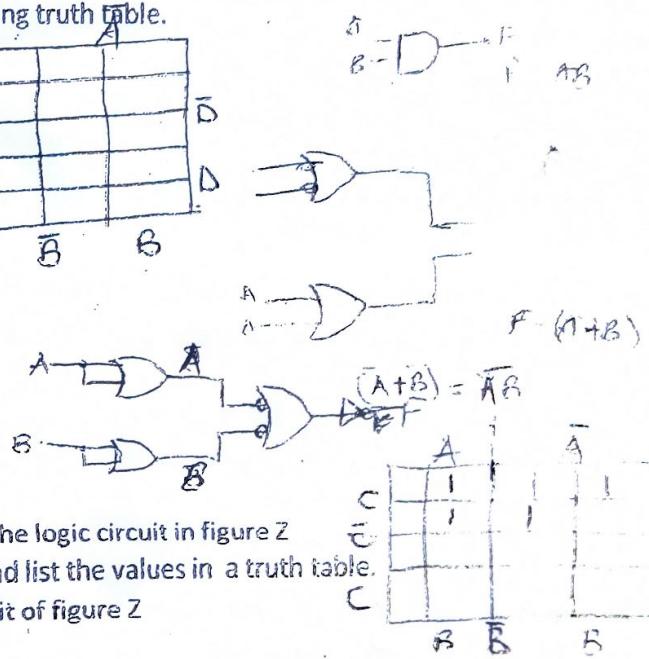
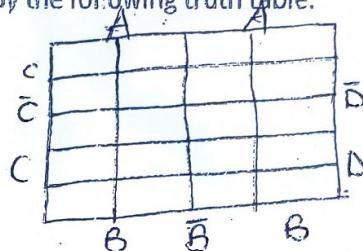
**INSTRUCTIONS:** Answer ALL the FOUR Questions

Question 1



- a) Verify that a two input AND- gate can be implemented using two input NOR- gates. Draw the implemented AND-gate logic circuit.
- b) Using a Karnaugh map, reduce the following logic function to its minimum sum of products form.  
 $F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}CD + A\bar{B}\bar{C}D$
- c) Synthesize a minimum logic circuit specified by the following truth table.

Inputs			Output
A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



Question 2

- a) (i) Write the Boolean expression for the output X of the logic circuit in figure Z  
(ii) Determine the value of X for all input conditions and list the values in a truth table.
- b) Using a Karnaugh map derive the minimum logic circuit of figure Z

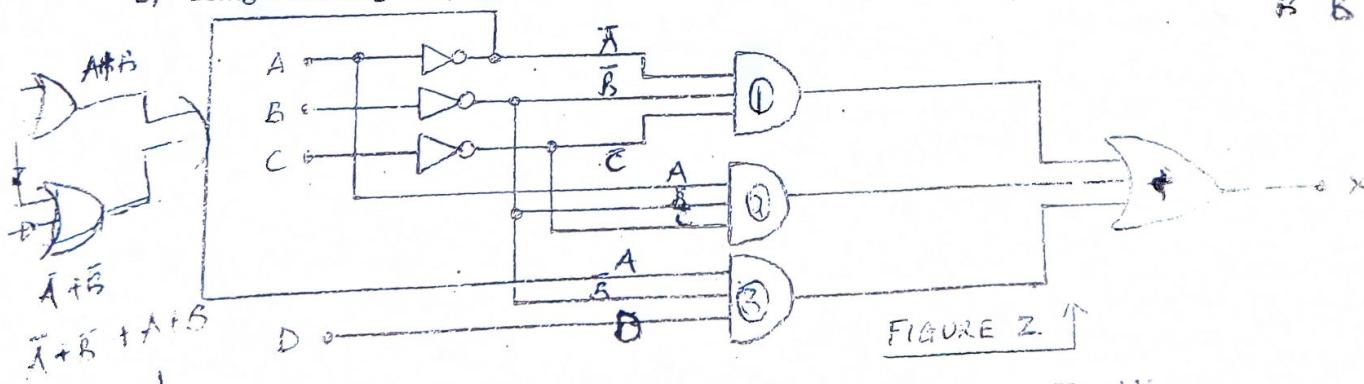


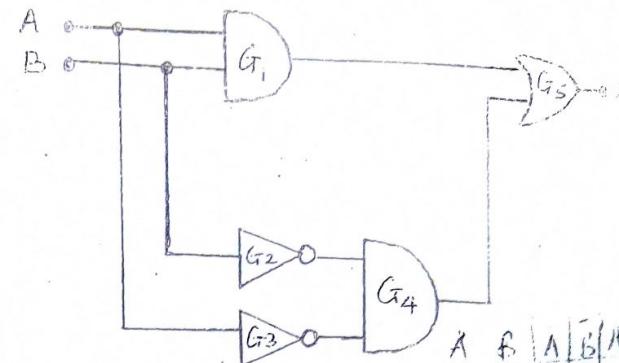
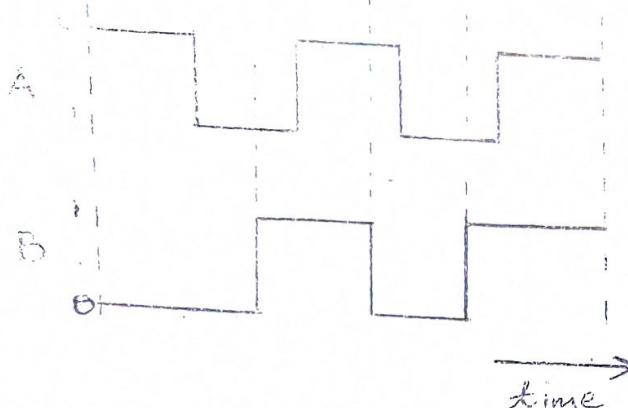
FIGURE Z.

- c) Design a logic circuit having input signal A, control input B and outputs X and Y to operate as follows:

1. When  $B = 1$ , output X will follow input A and output Y will be 0
2. When  $B = 0$ , output X will be 0 and output Y will follow input A.

### Question 3

- a) The logic circuit below has binary inputs varying according to the waveforms indicated, sketch the output waveform X.



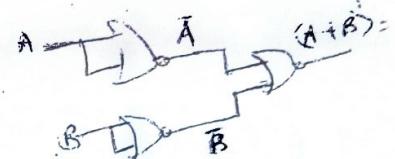
A	B	$A \oplus B$	$\bar{A}B$	$\bar{A}\bar{B}$	$\bar{B}$
0	0	0	0	1	1
0	1	1	0	0	0
1	0	1	1	0	1

- b) Two binary numbers A and B each has two digits and a digital comparator is required to compare the magnitude of the two numbers. The comparator gives outputs L, M and N such that:

$$L = \text{LOGIC 1, if } A < B; \quad M = \text{LOGIC 1, if } A = B; \quad N = \text{LOGIC 1, if } A > B$$

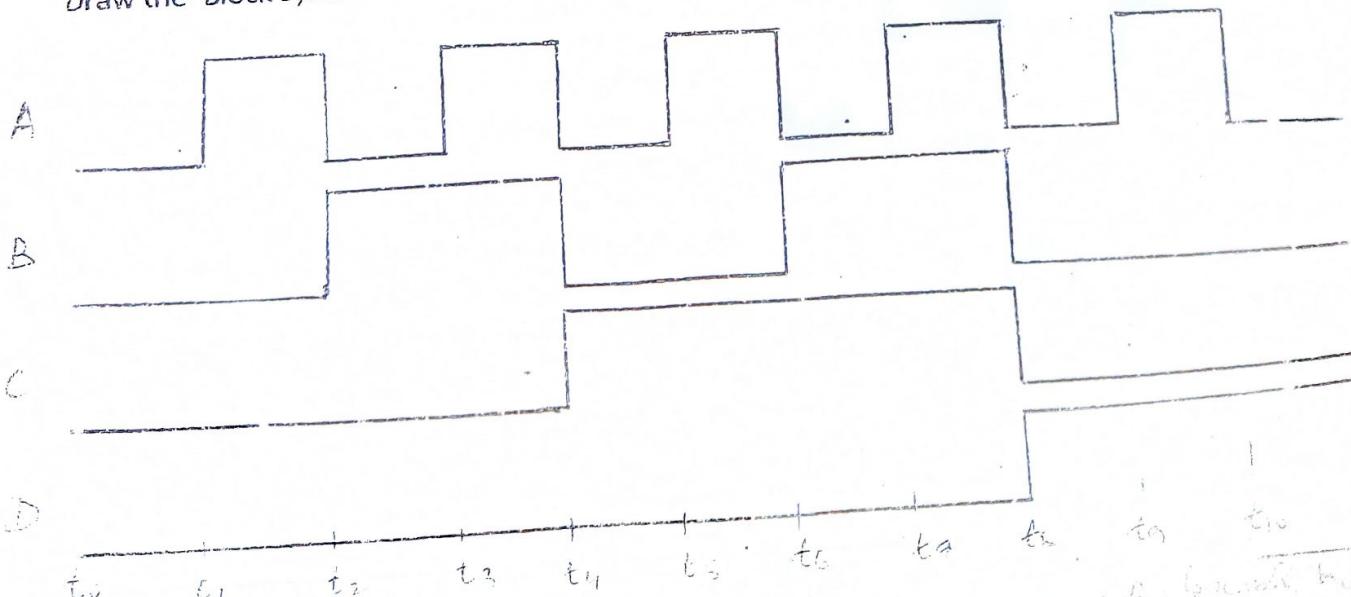
Construct a truth table for the comparator and use a Karnaugh map to derive a minimum Boolean expression for each output.

- c) Implement the minimum Digital Comparator circuit in (b) above.



### Question 4

- a) A BCD code is being transmitted to a remote receiver. The bits are  $A_3A_2A_1$  and  $A_0$  with  $A_3$  as the MSB. The receiver includes a BCD error detector circuit that examines the received code to verify if it is a legal BCD code. Design a minimum error detector circuit that produces a HIGH for any error condition.
- b) Implement a Logic Circuit required to decode the Binary number  $DCBA=1011_2$  by producing a Logic HIGH at the output.
- c) The 7442A IC is a BCD to Decimal Decoder producing ACTIVE-LOW outputs. Draw the Block Symbol for the 7442A IC and sketch the output wave forms for the given BCD inputs.



# DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

## B.Sc ELECTRICAL/TELECOMMUNICATIONS ENGINEERING

FIRST YEAR, SECOND SEMESTER 2014/2015

### ELE 1201: INTRODUCTION TO DIGITAL ELECTRONICS

DATE: 15<sup>TH</sup> MAY, 2015

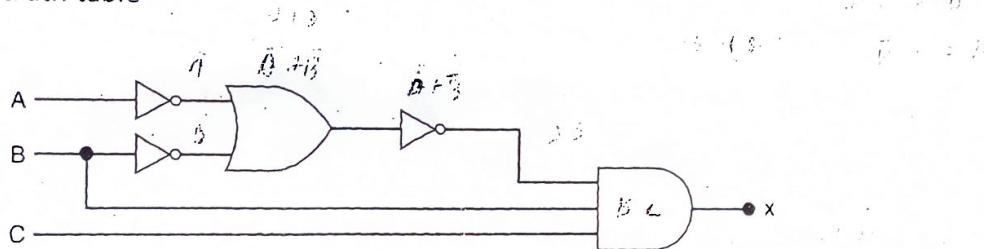
TIME: 2.00 – 5.00 PM

#### INSTRUCTIONS:

This paper contains FIVE Questions. Attempt FOUR Questions only. Each Question carries a total of 25 Marks.

#### QUESTION 1

- a) Implement the following two-input Boolean functions using exclusively NAND gates  
(i)  $F = A+B$       (ii)  $F = A \cdot B$       [6 Marks]
- b) Write the Boolean expression for the output X in the figure below and list the value of X for all possible input conditions in a truth table



[7 Marks]

- c) In a certain manufacturing process, the conveyor belt will shut down whenever specific conditions occur. These conditions are monitored and reflected by the states of four logic signals as follows:

- Signal A will be HIGH (LOGIC 1) whenever the conveyor belt speed is too fast. ✓
- Signal B will be HIGH whenever the collection bin at the end of the belt is full. ✓
- Signal C will be HIGH when the belt tension is too tight.
- Signal D will be HIGH when the manual override is off.

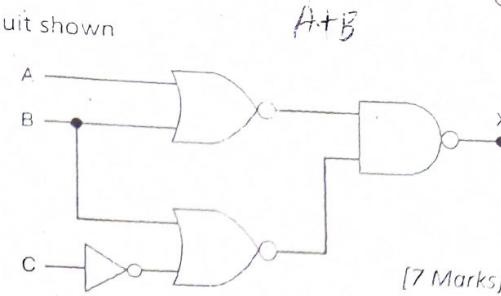
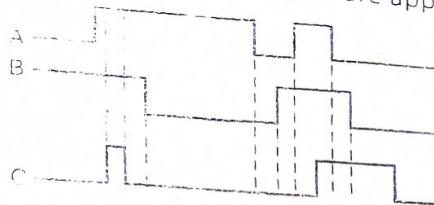
A logic circuit is needed to generate signal X that will go HIGH whenever conditions A and B exist simultaneously or whenever conditions C and D exist simultaneously.

- (i) Write a Logic expression for X and implement it using standard Logic gates      [5 Marks]

- (ii) Using the 74LS50 IC below show how it can be wired to implement the Logic expression X      [7 Marks]

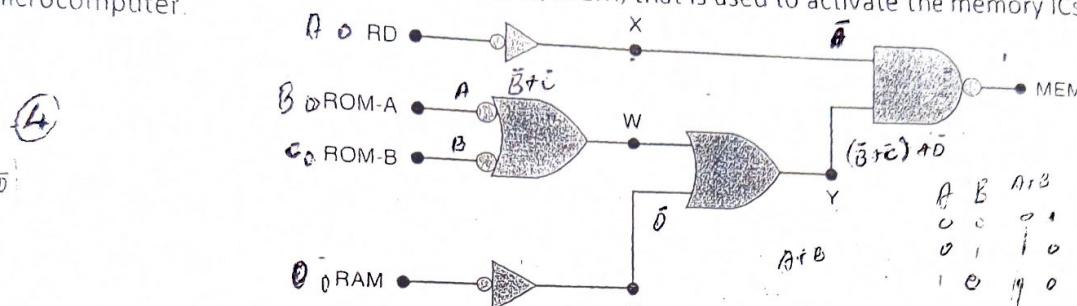
14 pin 2nd Mund IC

The following digital waveforms are applied to the logic circuit shown



Draw the resulting output waveform X.

- b) The Logic Circuit below generates an output, MEM, that is used to activate the memory ICs in a microcomputer.



Determine the input conditions necessary to activate MEM.

- c) In a photocopy machine, a stop Signal, S, is to be generated to stop the machine operation and energize an indicator lamp whenever either of the following conditions exists:

(1) There is no paper in the paper feeder tray

Or (2) The two microswitches in the paper path are activated indicating a paper jam.

The microswitches produce signals Q and R that go HIGH whenever paper is passing over the switch to activate it.

Design the Logic Circuit to produce a HIGH at the output signal for the stated Conditions and implement the circuit using two-input NAND gates.

### QUESTION 3'

- a) Show how a Full-Adder can be implemented using two Half-Adders when adding two binary digits A and B [8 Marks]
- b) Using the Logic symbol for a Full-Adder, show how a 4-bit parallel-adder can be implemented. [5 Marks]
- c) In a computer, the 4-bit binary numbers to be added are fetched from the memory and stored in Flip-Flop registers. Addition is then executed using a 4-bit parallel adder. The Augend bits  $A_3A_2A_1A_0$  are stored in the A register (Accumulator) while the Addend bits  $B_3B_2B_1B_0$  are stored in the B register. Each of these registers is made up of D-type Flip-Flops.

Draw a complete Logic circuit of the 4-bit parallel adder including the registers. By using LOAD, CLEAR and TRANSFER Signal Lines, describe the sequence of operations by which the Logic circuit will add binary numbers  $1001_{LSB}$  and  $0101_{LSB}$ . [12 Marks]



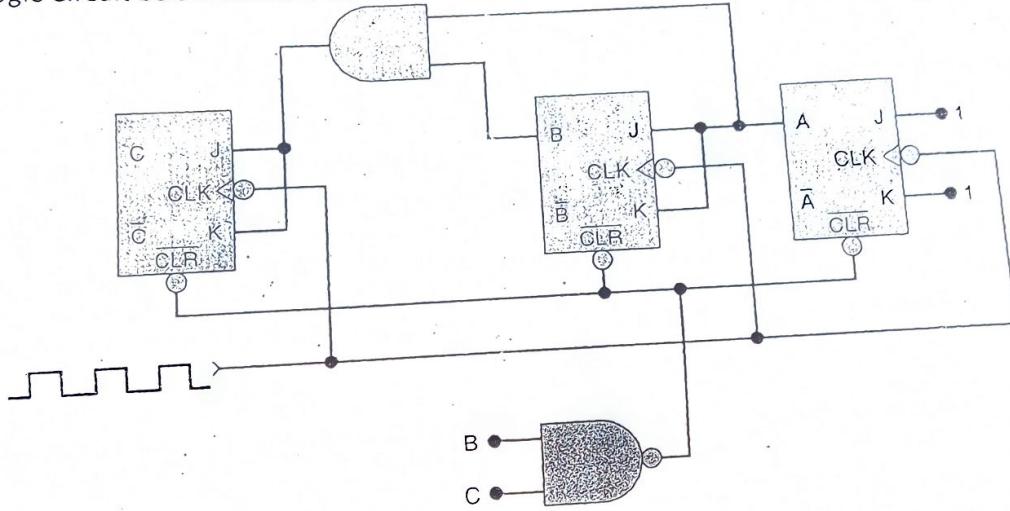
#### QUESTION 4

A digital system stores an 8-bit binary word  $X_7X_6X_5X_4X_3X_2X_1X_0$  LSB = 10110101<sub>LSB</sub> in a SIPO register. The binary word which is available in parallel form is to be transmitted to a remote destination in serial form by making use of an 8-input multiplexer (74HC 151 IC) with the LSB transmitted first and the MSB transmitted last. A MOD-8 synchronous counter is used to provide the select code bits  $S_2S_1S_0$  LSB as PGT Clock pulses are applied.

- a) Using Logic Symbols for the Register, Multiplexer and the Counter, draw a complete Block diagram of the digital system. [6 Marks]
- b) Design a Logic Circuit for each block used in the Digital System.  
Use D-Type Flip Flops for the Register and J-K Flip-Flops for the counter. [14 Marks]
- c) By denoting the MUX output terminal as Z, draw the Z waveform for 8 clock pulses. [5 Marks]

#### QUESTION 5

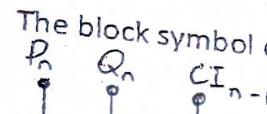
- a) The Logic Circuit below shows a Counter



- (i) Sketch the timing diagram, showing all the Flip-Flop outputs for 12 clock pulses. Assume an initial LOW state for each the Flip-Flop. [6 Marks]  
Determine the Modulus of the Counter. [4 Marks]
- (ii) The propagation delay ( $t_{pd}$ ) for each JK Flip-Flop is 50nS while  $t_{pd}$  for each logic gate used in the design of the counter is 20nS. Determine the maximum clock frequency ( $f_{max}$ ) for the Counter and compare this value with  $f_{max}$  for a Ripple counter of the same modulus. [7 Marks]
- (iii) Draw an upgraded Logic Circuit of the counter having a visual display of the counter states as the clock pulses are applied. Include a +5Vd.c power supply, current limiting resistors, LEDs and Inverter gates in the upgraded circuit. Each LED turns on when the Flip-Flop is HIGH. [8 Marks]

Question 2

a)



The block symbol of a binary Full-Adder is shown in the diagram below:

$P_n, Q_n$  :  $n^{\text{th}}$  digits of multidigit binary numbers to be added

$CI_{n-1}$  : Carry-Input digit

$CO_n$  : Carry - Output digit

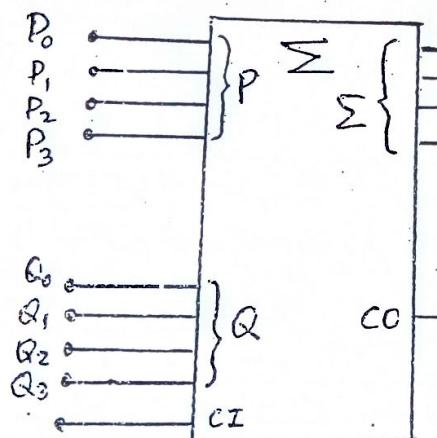
$S_n$  : Sum digit

Synthesize a minimum Full-Adder Logic Circuit using Standard Logic gates.

(3 Marks)

b)

The Logic Symbol of the 7483A IC which is a four-bit parallel adder is shown in the diagram below



$P, Q$  : Binary numbers to be added

$\Sigma_n$  : Partial Sums

$CI$  : Carry - Input to LSB adder

$CO$  : Sum digit

Draw a labeled block diagram of the four-bit parallel adder.

c)

Show how two 7483A ICs can be connected to form an 8-bit parallel adder. Draw block diagram and output values for

$$P = \text{MSB } 10111001_{\text{LSB}}$$

$$\text{and } Q = \text{MSB } 10011110_{\text{LSB}}$$

# MAKERERE UNIVERSITY

## COLLEGE OF ENGINEERING, DESIGN, ART & TECHNOLOGY DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING B.Sc ELECTRICAL/TELECOMMUNICATIONS PROGRAMME FIRST YEAR, SECOND SEMESTER EXAMINATIONS 2013/2014 ELE 1201: INTRODUCTION TO DIGITAL ELECTRONICS

DATE: 23rd MAY, 2014

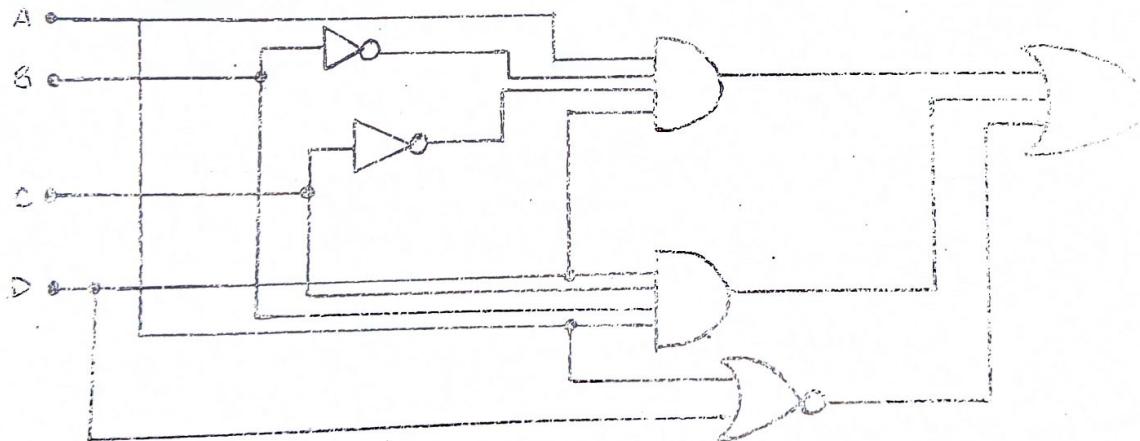
TIME: 2.00 - 3.30 P.M.

### INSTRUCTIONS:

This paper contains SIX Questions, Attempt FIVE Questions Only. Each Question carries a total of 20 marks

#### Question 1

- a) Using Boolean Algebra, Simplify the Logic Circuit shown in the diagram below and draw the Simplified Logic Circuit.



- b) Represent the Boolean function :

$$F(A, B, C) = \Sigma(0, 2, 4, 5, 6)$$
 on a Karnaugh map and express the function as a Sum of minterms

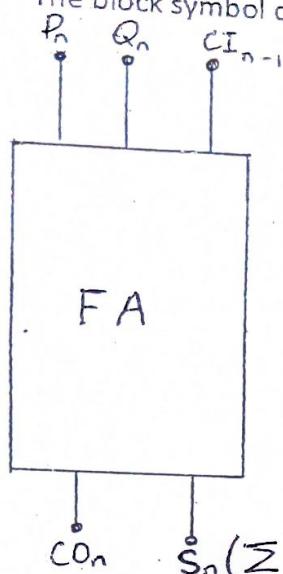
{ 7 MARKS }

- c) Synthesize a minimum Logic Circuit represented by the Boolean expression (b) above

{ 12 MARKS }

Question 2

- a) The block symbol of a binary Full-Adder is shown in the diagram below:



$P_n, Q_n$  :  $n^{\text{th}}$  digits of multidigit binary numbers to be added

$CI_{n-1}$  : Carry-Input digit

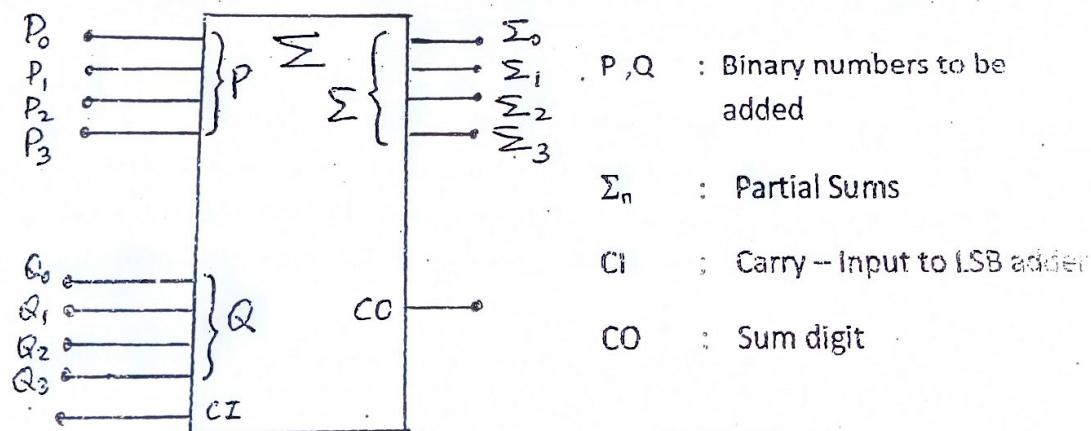
$CO_n$  : Carry - Output digit

$S_n$  : Sum digit

Synthesize a minimum Full-Adder Logic Circuit using Standard Logic gates.

(3 Marks)

- b) The Logic Symbol of the 7483A IC which is a four-bit parallel adder is shown in the diagram below



Draw a labeled block diagram of the four-bit parallel adder.

- c) Show how two 7483A ICs can be connected to form an 8-bit parallel adder. Give value of all output values for

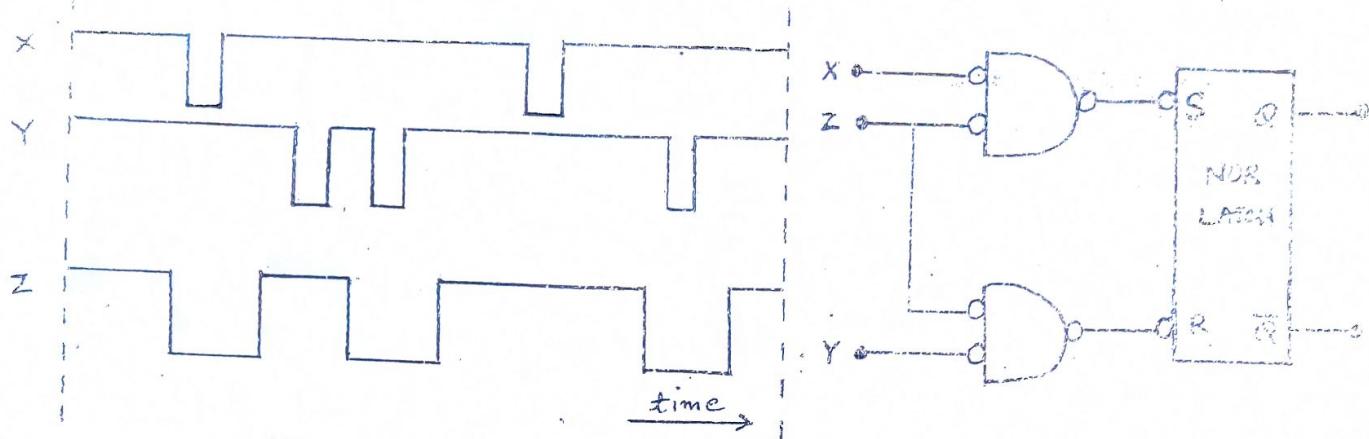
$$P = \text{MSB } 10111001_{\text{LSB}}$$

$$\text{and } Q = \text{MSB } 10011110_{\text{LSB}}$$

5

**Question 3**

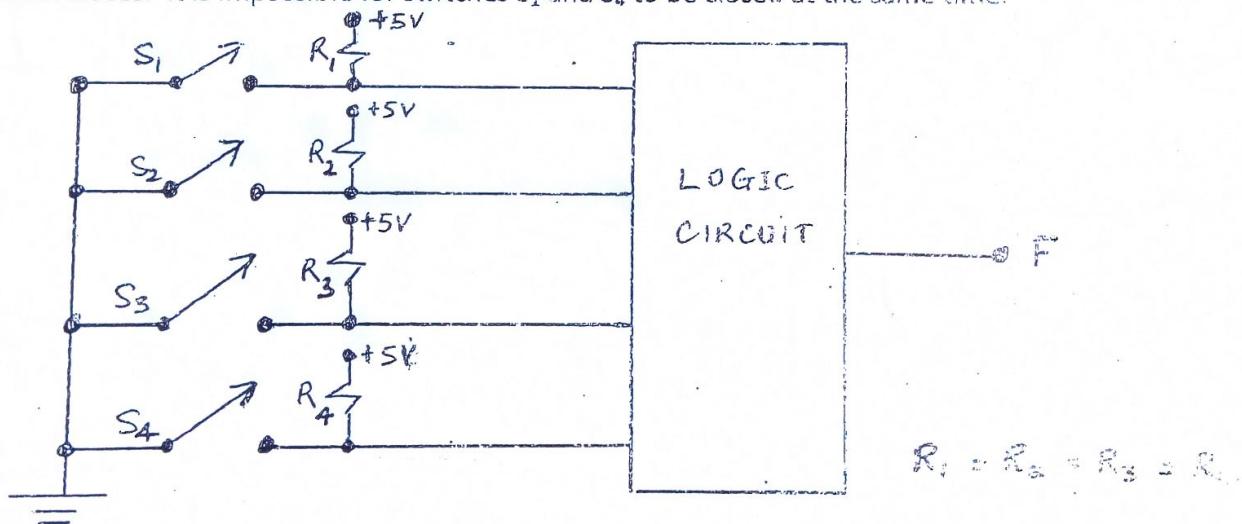
- a) The waveforms X, Y, and Z are connected to the circuit shown below.



Assuming that  $Q = 0$  initially, Sketch the Q waveform.

(6 MARKS)

- b) The diagram below shows four switches that are part of the control circuitry in a photocopying machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open and as the paper passes over the switch, the switch closes. It is impossible for switches  $S_1$  and  $S_4$  to be closed at the same time.



$$R_1 = R_2 = R_3 = R_4$$

By assigning logic values such that LOGIC 1 (HIGH) = +5v and LOGIC 0 (LOW) = 0v, Construct a truth table that produces a HIGH output whenever two or more switches are closed at the same time.

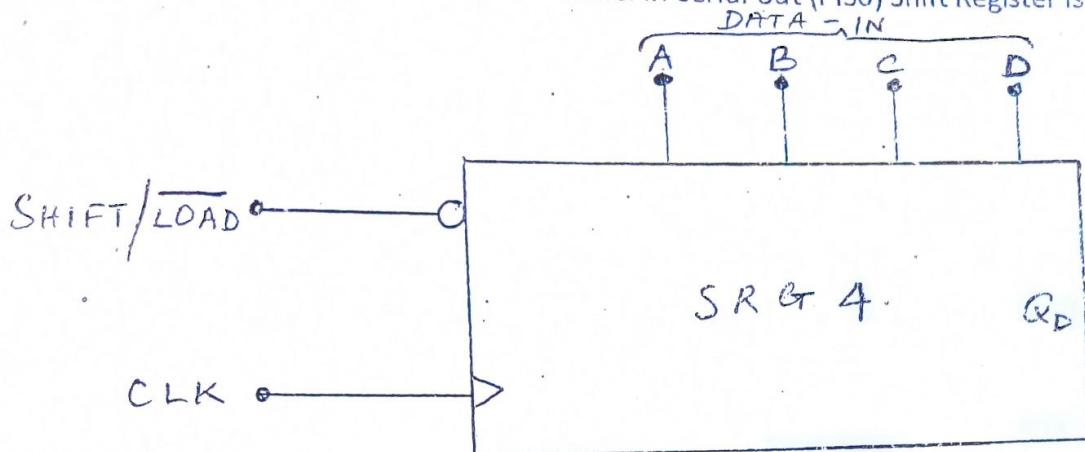
(8 MARKS)

- c) By making use of the Karnaugh map and taking advantage of don't care conditions, Design a minimum photocopier Logic Control circuit.

(6 MARKS)

#### Question 4

The Logic Symbol of a 4-bit Parallel in-serial out (PISO) Shift Register is shown below:

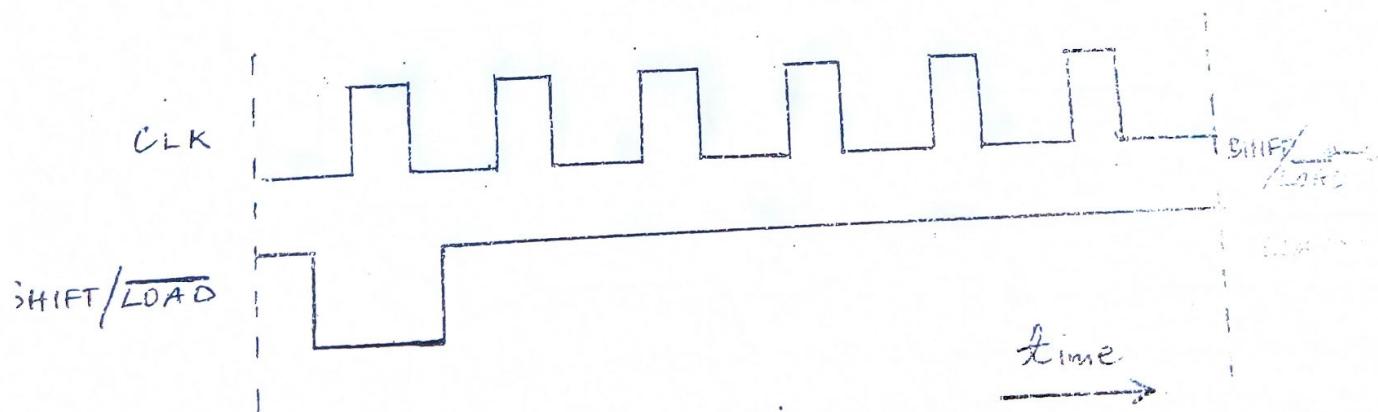


a) Draw the Logic Circuit of the 4-bit Shift-Register(SRG 4) using D-type Flip-Flops.

b) By referring to the Logic Circuit drawn in (a) above, explain how:

- i) DATA is loaded into the register
- ii) DATA is shifted through the register

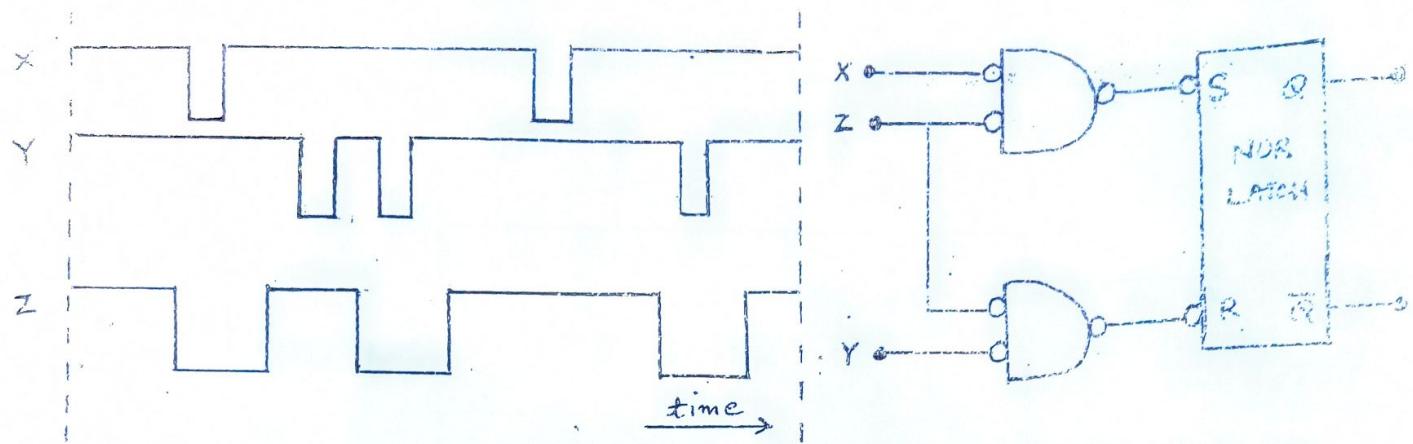
c) The SRG 4 with the indicated parallel input DATA, Clock and SHIFT/LOAD wave forms are shown below:



Show the Data Output Waveform for six clock pulses.

Question 3

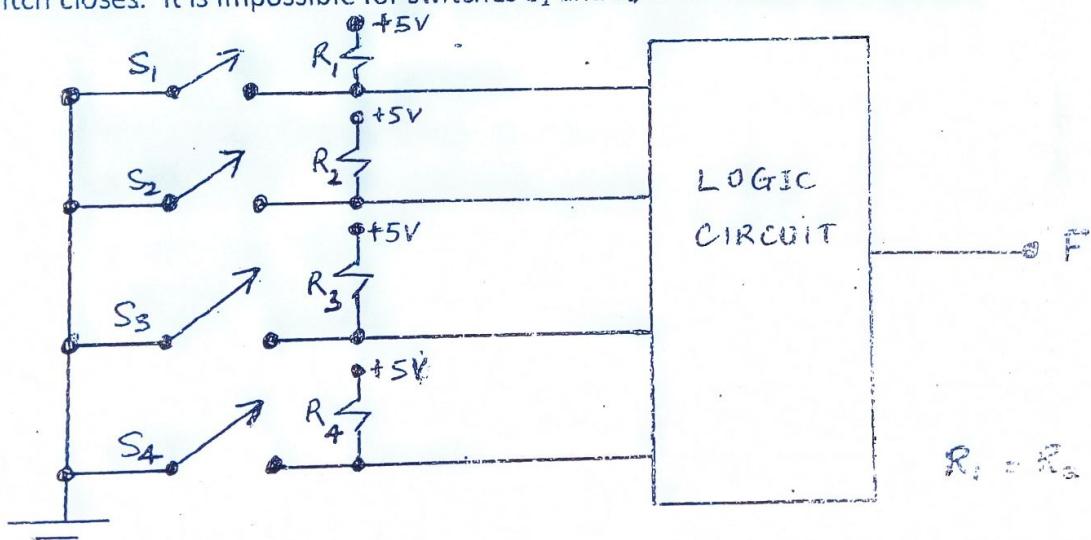
- a) The waveforms X, Y, and Z are connected to the circuit shown below.



Assuming that  $Q = 0$  initially, Sketch the Q waveform.

(6 MARKS)

- b) The diagram below shows four switches that are part of the control circuitry in a photocopying machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open and as the paper passes over the switch, the switch closes. It is impossible for switches  $S_1$  and  $S_4$  to be closed at the same time.



$$R_1 = R_2 = R_3 = R_4$$

By assigning logic values such that LOGIC 1 (HIGH) = +5v and LOGIC 0 (LOW) = 0v, Construct a truth table that produces a HIGH output whenever two or more switches are closed at the same time.

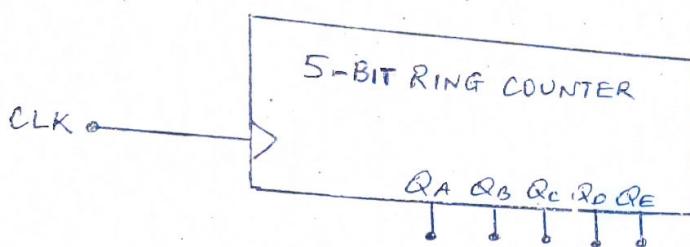
(8 MARKS)

- c) By making use of the Karnaugh map and taking advantage of don't care conditions, Design a minimum photocopier Logic Control circuit.

(6 MARKS)

Question 6

- a) The Logic Symbol of a 5-bit Ring Counter shown below:



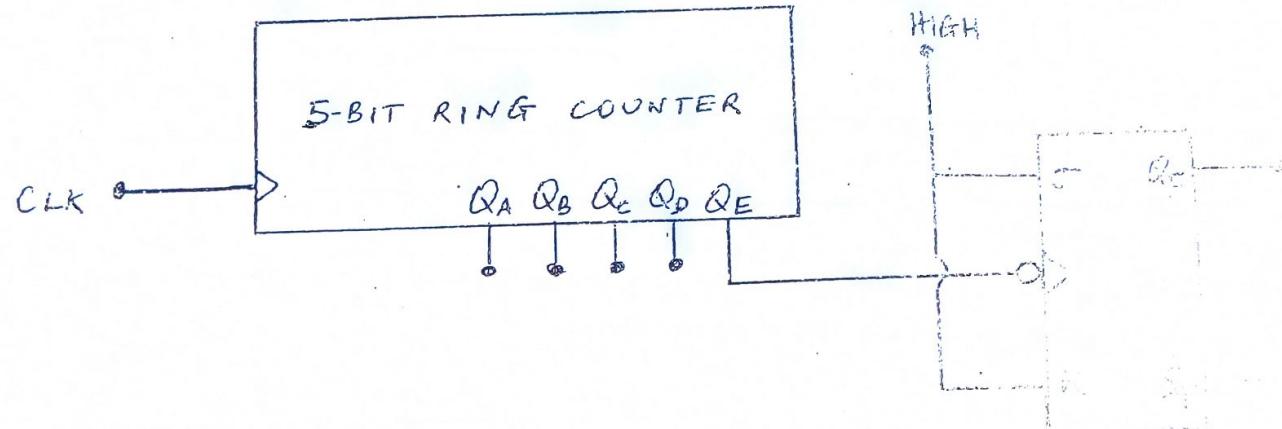
Draw a Logic Circuit of the 5-bit Ring counter using J-K Flip-Flops and a PGT clock.

(5 MARKS)

- b) Assuming that  $Q_A = 1$  initially, show the following for the counter
- Timing diagram
  - Sequence table
  - State transition diagram
  - Determine modulus of the counter

(3 MARKS)

- c) The 5-bit Ring counter is combined with a single J-K Flip-Flop as shown in the diagram below:



Determine the sequence of states  $(Q_A, Q_B, Q_C, Q_D, Q_E, Q_F)$  for the modified counter and its modulus.

(10 MARKS)

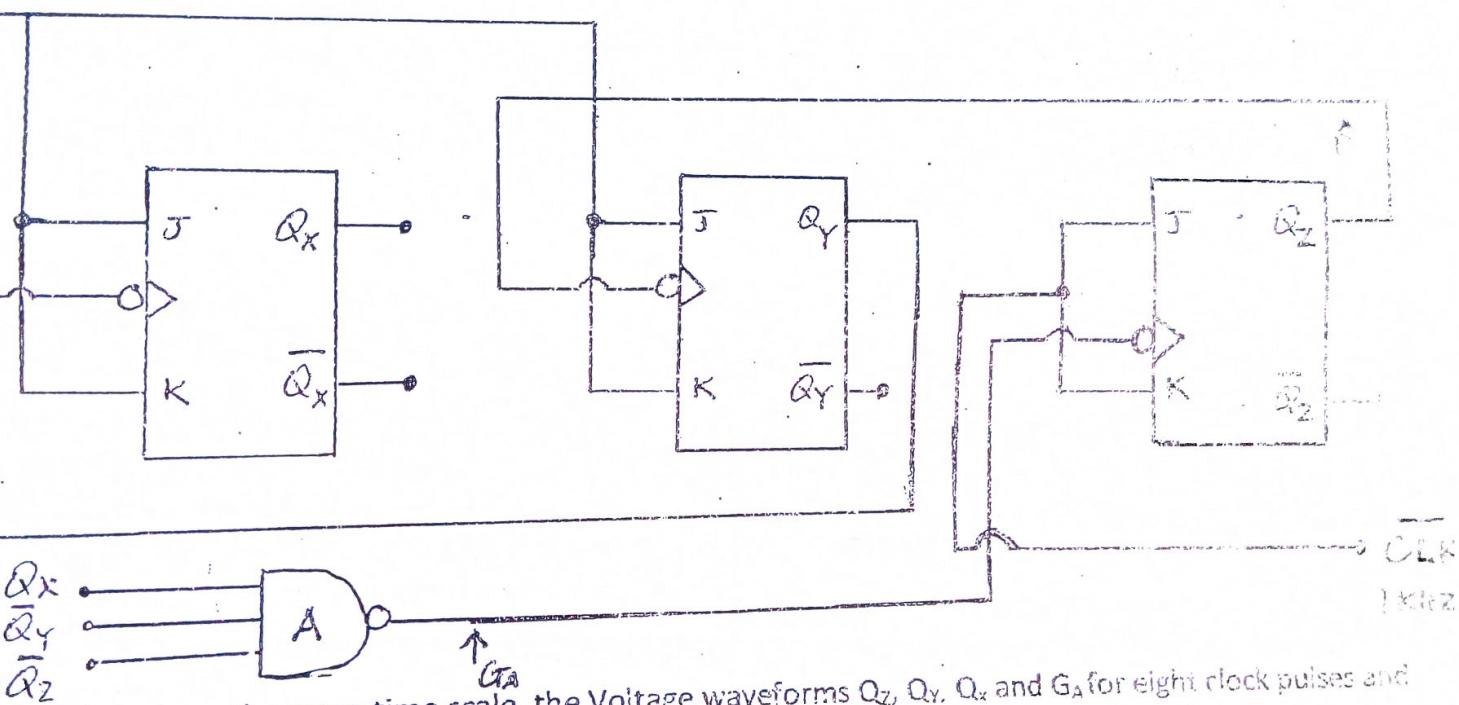
### Question 5

- a) An asynchronous binary counter is designed to give a decimal counting range from 0 to 1023. Determine the following specifications of the counter:

- i) Number of Flip-Flops required to build the counter
- ii) Frequency of the output waveform at the last Flip-Flop in the cascade
- iii) Modulus of the counter
- iv) Decimal count after 2060 clock pulses.

(8 MARKS)

- b) The diagram below is a counter with all the Flip-Flops existing in the LOW state before the application of the clock pulses.



Sketch on the same time scale, the Voltage waveforms  $Q_z$ ,  $Q_y$ ,  $Q_x$  and  $G_A$  for eight clock pulses and comment on the operation of the counter.

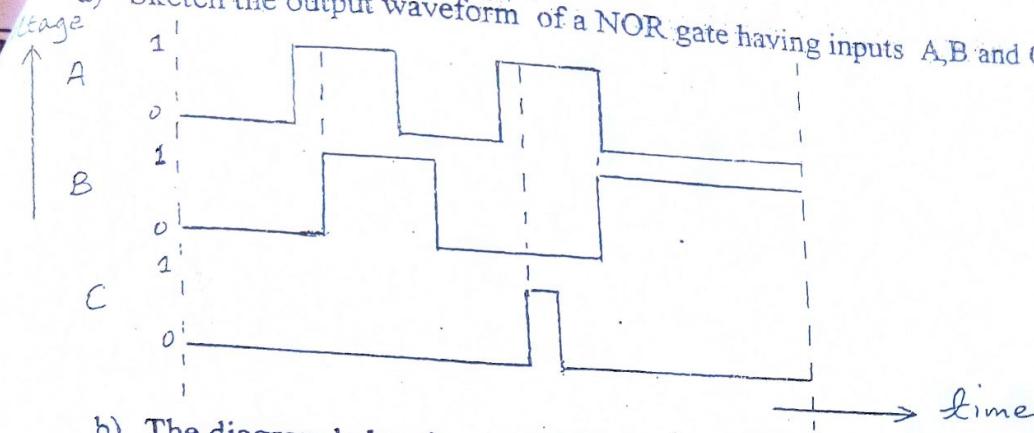
(7 MARKS)

- c) Design a decoding network for the counter in part (b) above using ACTIVE-HIGH decoding.

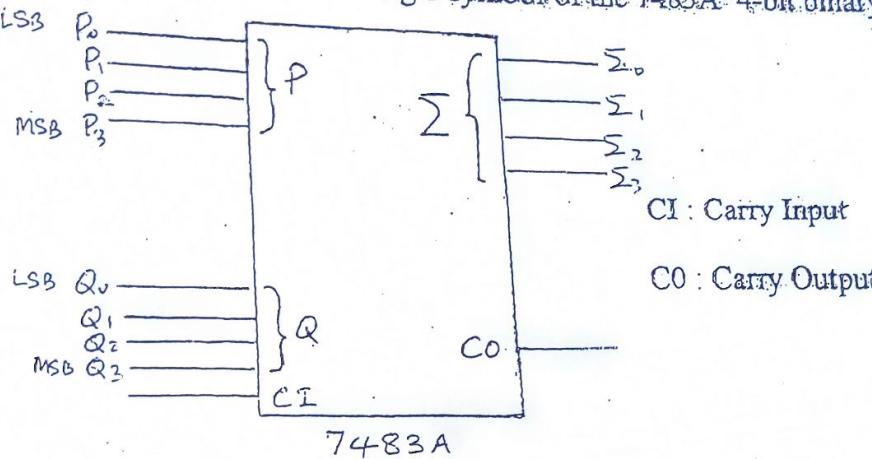
(5 MARKS)

### QUESTION 3

- a) Sketch the output waveform of a NOR gate having inputs A, B and C that vary as shown below.



- b) The diagram below is a Logic symbol of the 7483A 4-bit binary parallel adder.

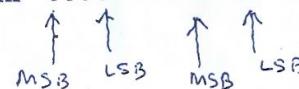


Draw a block diagram showing the Internal wiring of the 4-bit parallel adder.

### QUESTION 4

- a) Draw a diagram showing the Logic Symbol of a BCD to Decimal Decoder having active LOW Outputs.

- b) Sketch the input and output waveforms, on the same time scale, over 10 equal time intervals given that the BCD count increases sequentially from 0000 to 1001 with each BCD code lasting one time interval.



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MAKERERE UNIVERSITY

COLLEGE OF ENGINEERING, DESIGN, ART & TECHNOLOGY  
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

B.Sc ELECTRICAL ENGINEERING AND B.Sc  
TELECOMMUNICATION ENGINEERING

ELE 1201: INTRODUCTION TO DIGITAL ELECTRONICS

SEMESTER 2 (2010/2011) CAT 1

TIME: 10:00 AM - 12:00 NOON

DATE: 07-04-2011

INSTRUCTIONS: ANSWER ALL THE FOUR QUESTIONS

QUESTION 1

- a) Use Boolean algebra and verify that the following Logic function

$$F = \overline{(A\bar{B}CD + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D})}$$

Reduces to :

$$F = (\overline{A \oplus C}) + (\overline{B \oplus D})$$

- (i) Verify, by giving relevant Logic expressions, that a two input AND gate can be realized using two input NOR gates.
- (ii) Draw the AND gate equivalent Logic circuit

QUESTION 2

- i) Given the Logic functions:  $F = \bar{A}C + \bar{A}B + ABC + BC$

ii) Express it as a sum of minterms

iii) Using Karnaugh map, deduce the minimal sum of products expression.

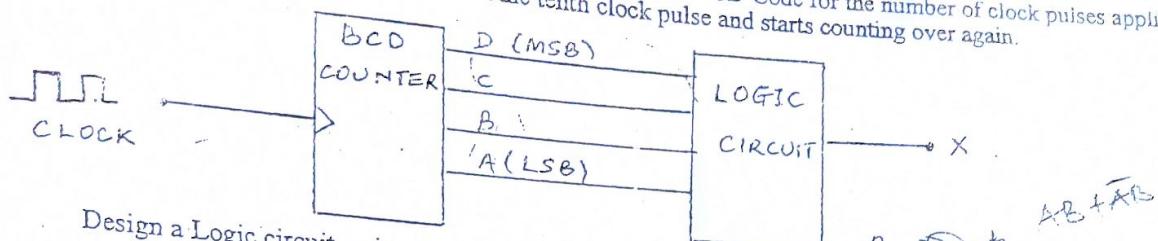
Write a truth table for the following Logic function:

$$F(A, B, C) = \sum(0, 0)$$

Synthesize a Logic circuit using two input and three input NOR gates exclusively.

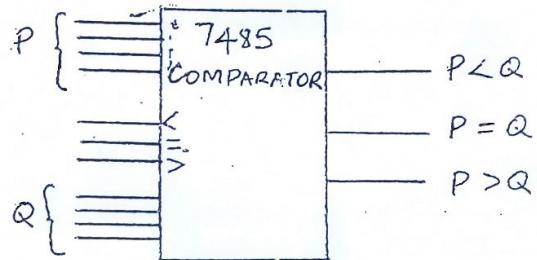
### QUESTION 2

- a) The figure below shows a BCD counter that produces a BCD Code for the number of clock pulses applied to the input. The counter resets to 0000 on the tenth clock pulse and starts counting over again.



- b) Briefly explain how the EXCLUSIVE-NOR gate functions as a basic digital magnitude comparator. and design a logic circuit that determines the equality of two binary numbers each having 4 bits. [6 Marks]

- c) The figure below is a logic symbol for a 4-bit IC 7485 magnitude comparator for two binary numbers P and Q. [4 bits]



$P_0, P_1, P_2, P_3$   
 $Q_0, Q_1, Q_2, Q_3$

Using two 7485 ICs draw a wiring diagram showing all necessary interconnections to compare the magnitudes of two 8-bit binary numbers [7 Marks]

### QUESTION 3

- a) A BCD - to - 7 segment Decoder/driver (7446 IC) takes a BCD input and provides outputs that pass a current through the appropriate LED segments to display the decimal digit. The anodes of the LEDs are all tied to +5V and the cathodes are connected through current-limiting resistors to the appropriate outputs of the Decoder/Driver active-LOW outputs.

Draw a wiring diagram showing the connection of the Decoder/driver IC and the 7-Segment display. [7 Marks]



- b) Each Segment of the 7-segment Display unit is rated to operate at 10mA at 2.7V for normal brightness. Calculate the value of the current-limiting resistor needed to produce 10mA per segment. [5 Marks]

- c) Design a minimum logic circuit for decoding segment 'a'. Make use of the Karnaugh map and take advantage of the 'don't care' conditions. [8 Marks]

✓ ✗  
200  
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DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING  
B.Sc ELECTRICAL / TELECOMMUNICATIONS ENGINEERING  
FIRST YER, SECOND SEMESTER EXAMINATIONS 2012/2013

ELE 1201: INTRODUCTION TO DIGITAL ELECTRONICS

DATE: 10<sup>TH</sup> MAY, 2013

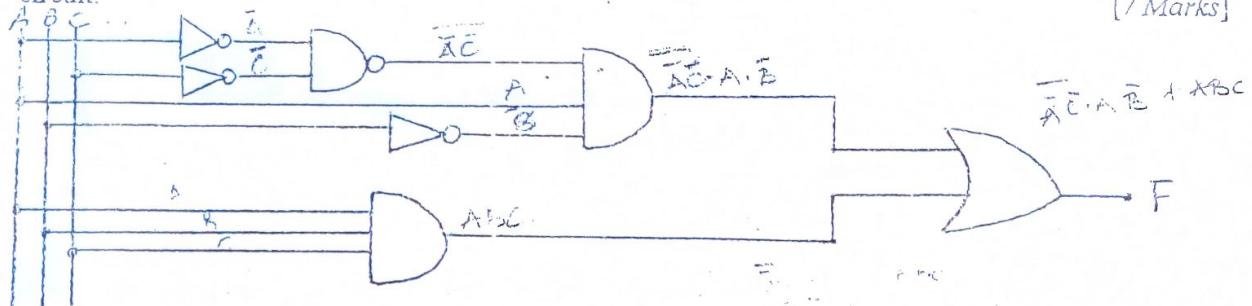
TIME : 2.00-5.00 PM

**INSTRUCTIONS:**

This paper contains SIX Questions. Attempt FIVE Questions only. Each Question carries a total of 20 marks

**QUESTION 1**

- a) Using Boolean Algebra, simplify the Logic Circuit shown in the figure below and draw the simplified Logic circuit. [7 Marks]



- b) i) Use the Karnaugh map to minimize the following Logic function [5 Marks]

$$F = ABC + BC + AB$$

- ii) Implement the minimum logic function using standard logic gates [3Marks]

- c) Design a logic circuit having input signal A, control input B and outputs X and Y to operate as follows:

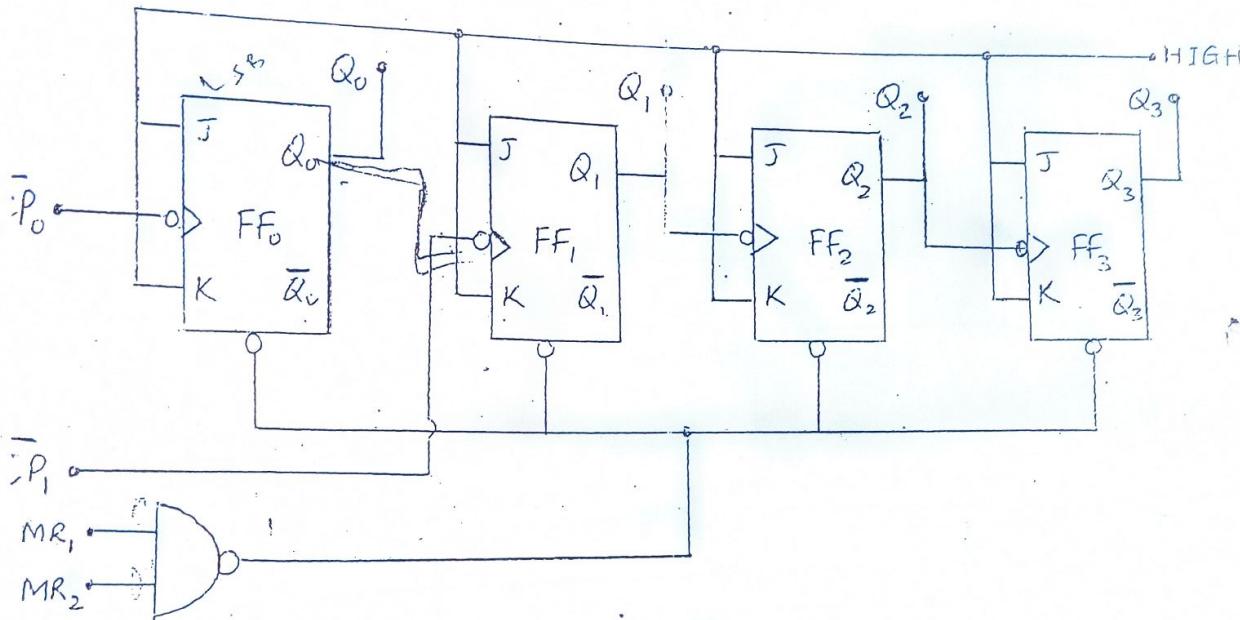
1. When B = 1, output X will follow input A and output Y will be 0

2. When B= 0, output X will be 0 and output Y will follow input A.

[5 Marks]

**QUESTION 5**

- a) i) Using simple illustrations, describe how an asynchronous counter differs from the synchronous counter, and give one major disadvantage of asynchronous counters in many applications. [6 Marks]
- ii) An 8 MHZ Square-wave clocks a 5-bit asynchronous counter. Determine the frequency of the output voltage waveform at  $FF_5$  given that the clock is connected to  $FF_0$ . [3 Marks]
- b) The Logic circuit in figure below shows the 74293 IC Asynchronous counter.



Draw the simplified Logic Symbol of the 742931C and show how it can be wired to implement a

MODULO-10 counter.

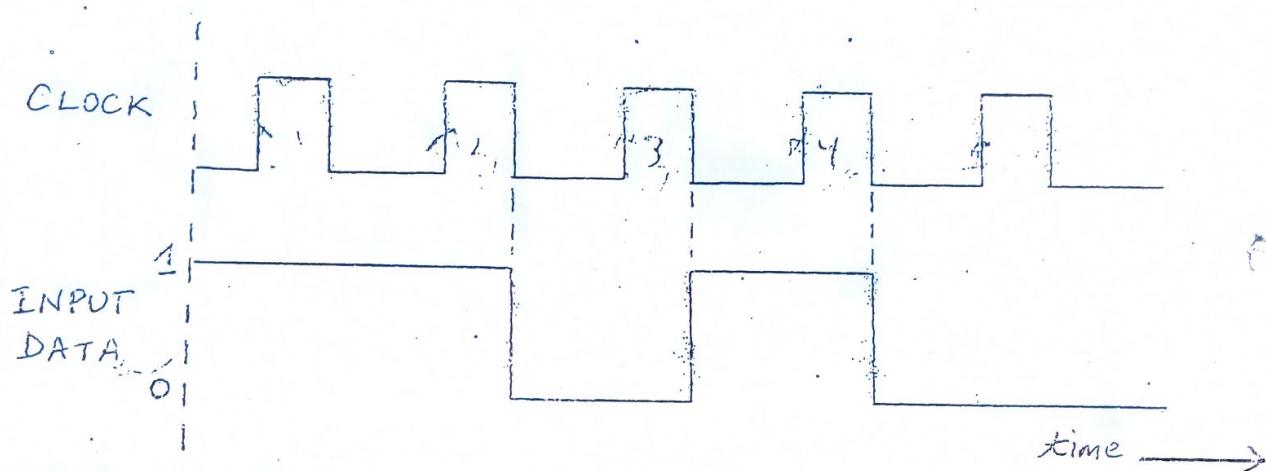
[5 Marks]

- c) Using the MODULO-10 Counter in part (a) above and a second 74293 1C based counter, show the wiring needed to provide frequency division of the input clock signal by 60. [6 Marks]

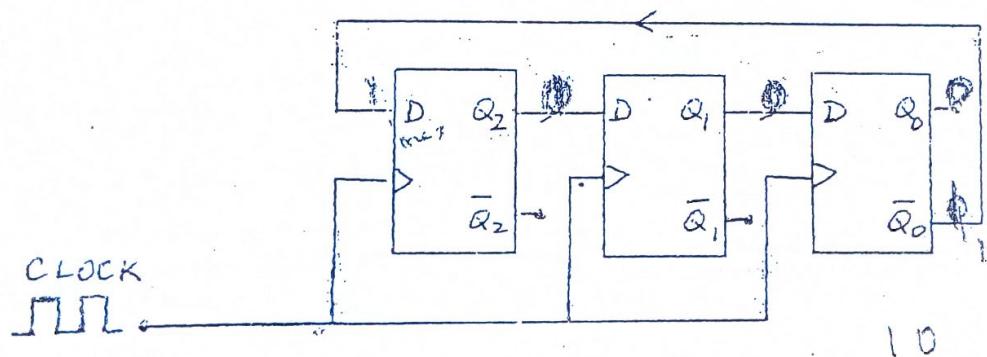
✓

#### QUESTION 4

- a) Draw a circuit diagram of a 5-bit SISO type register using D-type Flip-Flops, triggered by the positive edge of the clock pulse. [5A]
- b) Show the states of the register in part (a) above for the following specified Input Data and Clock waveform. [10A]



- c) The diagram below shows a Twisted-Ring Shift register counter.



Determine the following for the counter:

$$Q_2 = \frac{f_C}{6}$$

- State transition diagram
- Modulus of the counter
- Waveform diagram for seven input clock pulses
- Frequency of each Flip-Flop output waveform in terms of the clock frequency.

(19 Marks)

FIRST YEAR: SECOND SEMESTER 2012/2013

ELE 1201: INTRODUCTION TO DIGITAL ELECTRONICS

CAT2

DATE: 25<sup>TH</sup> APRIL, 2013

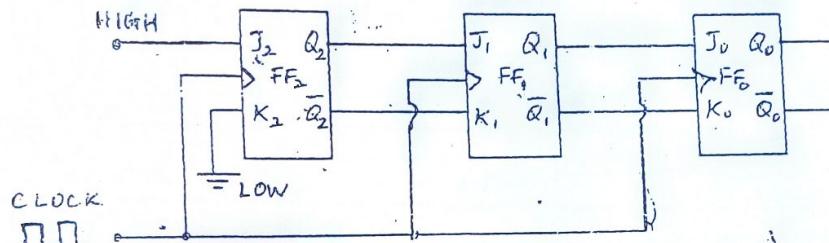
TIME: 10:00 – 12:00NOON

**INSTRUCTIONS: ANSWER ALL THE FOUR QUESTIONS**

## QUESTION 1

- (a) Draw a logic circuit for the R-S latch implemented by using two NAND gates. Show how the R-S latch can be modified to implement the RS flip-flop.

(b) The diagram in figure below shows a 3-bit register using J-K flip-flops. Explain the operation of the circuit and construct a sequence table for eight clock pulses. Assume that all flip-flops are RESET before arrival of the first clock pulse. 101

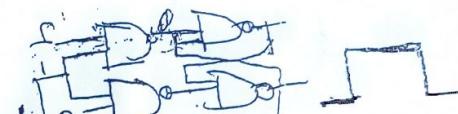
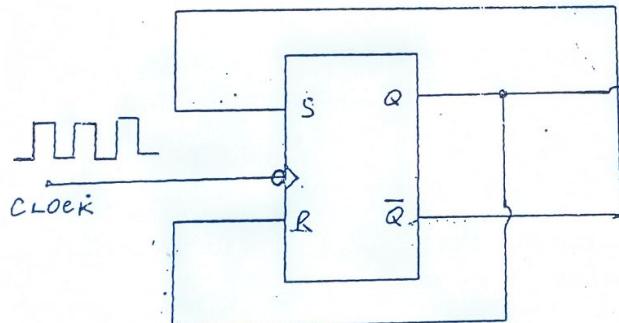


$Q_2$	$Q_1$	$Q_0$
0	0	0
0	0	1
0	1	1
0	1	0
1	1	0
1	0	0
1	0	1
1	1	0

107  
  
 Q<sub>2</sub> 1  
 J, I, J<sub>2</sub> Q, Q, Q, Q  
 000 0 0 0  
 100 1 1 1  
 200 2 2 2  
 300 3 3 3  
 400 4 4 4

## QUESTION 2

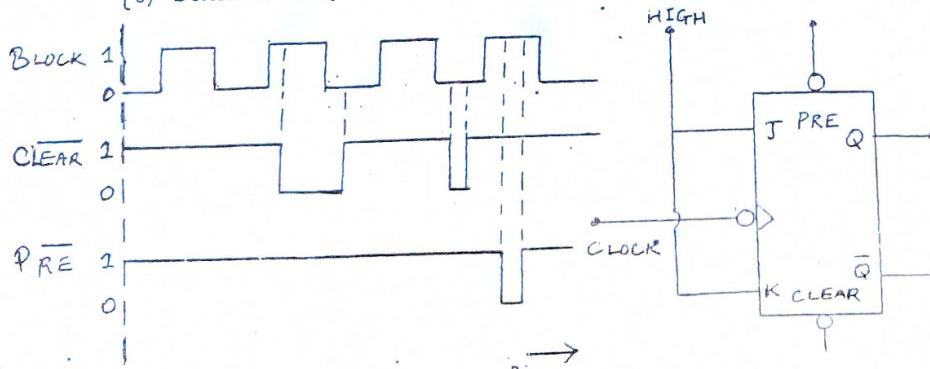
- (a) An S-R Flip-Flop is wired as shown in the diagram below:



UT.PUT		-	
R	S	Q	Q
O	I	I	O
I	O	O	I
O	O	female	

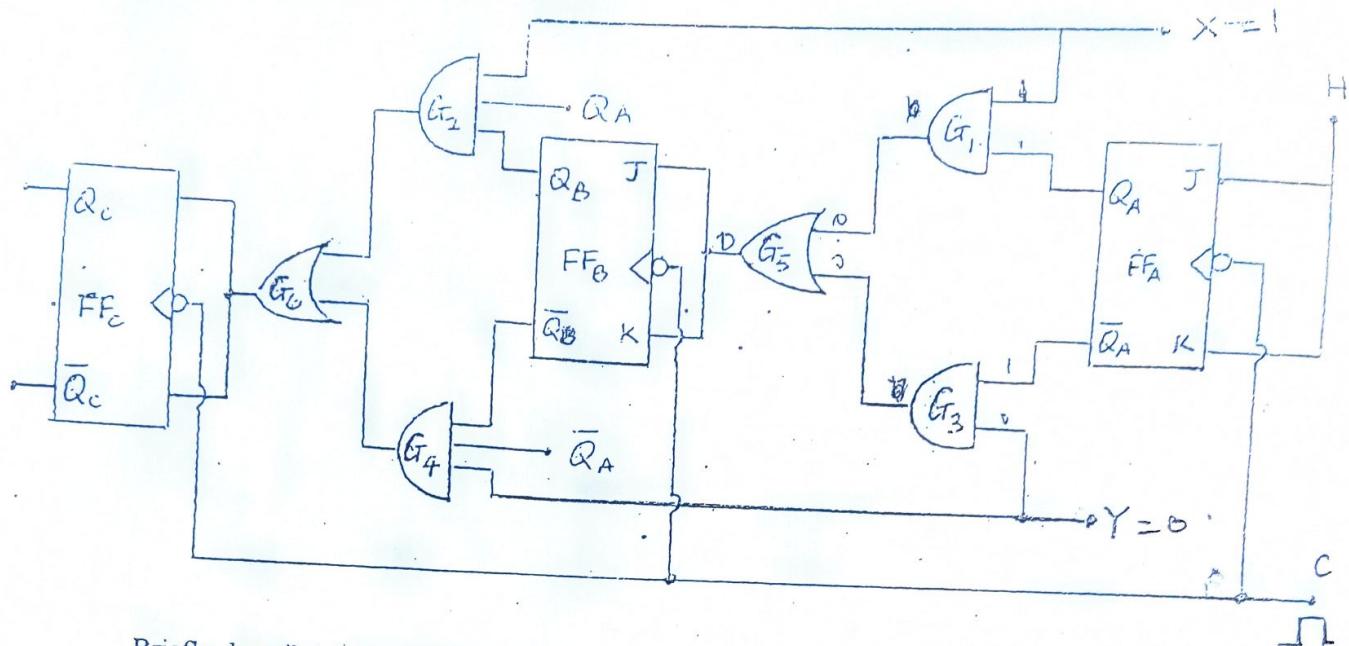
The Flip-Flop is triggered by a 1 KHZ Clock Signal, sketch the Q-output waveform for 10 clock pulses and determine the operating mode of the Flip-Flop. Assume the Flip-Flop is initially in the LOW state.

- (b) Determine the Q- waveform of the Flip-Flop below, for the given input waveforms.



QUESTION 6

- a) The Logic Circuit in figure below shows a synchronous reversible counter.



Briefly describe the operation of the circuit when:

- i)  $X$  and  $Y$  are both LOW
- ii)  $X$  and  $Y$  are both HIGH

[6 Marks]

- b) Write a state table of the counter when

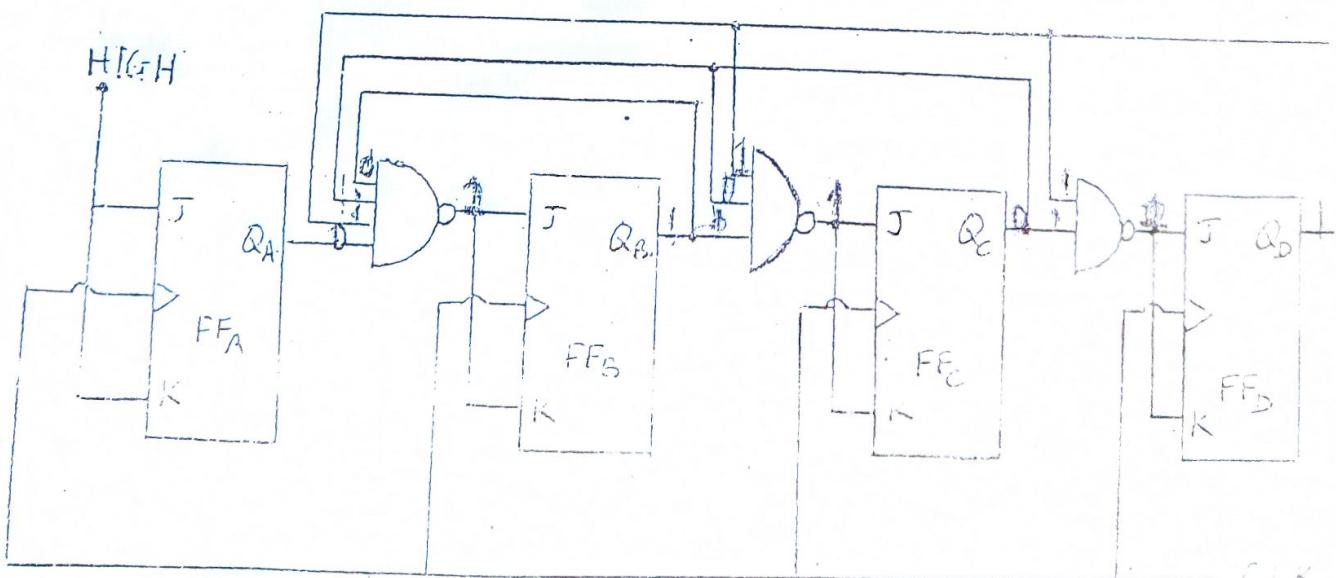
- i)  $X = 1$  and  $Y = 0$
- ii)  $X = 0$  and  $Y = 1$

Assume  $Q_A = Q_B = Q_C = 0$  initially.

[8 Marks]

- c) Write a Sequence table of the counter shown in the figure below for seven clock pulses and comment on the operation of the counter after the fourth clock pulse.

[6 Marks]



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**DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING**  
**B.Sc ELECTRICAL ENGINEERING AND B.Sc**  
**TELECOMMUNICATION ENGINEERING**  
**ELE 1201: INTRODUCTION TO DIGITAL ELECTRONICS**

**SEMESTER 2 (2012/2013) CAT 1**

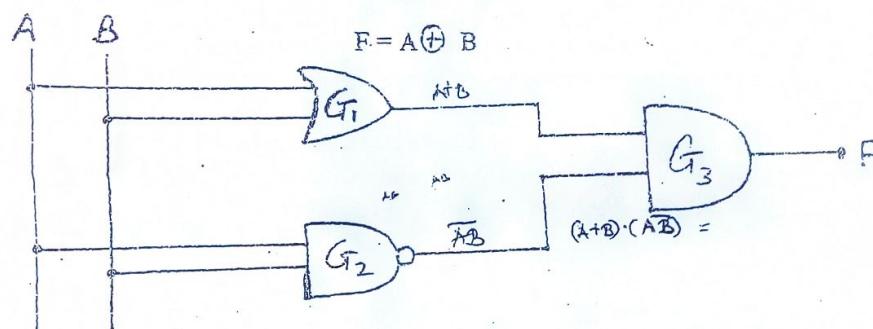
**TIME: 10:00 AM – 12:00 NOON**

**DATE: 28 MARCH, 2013**

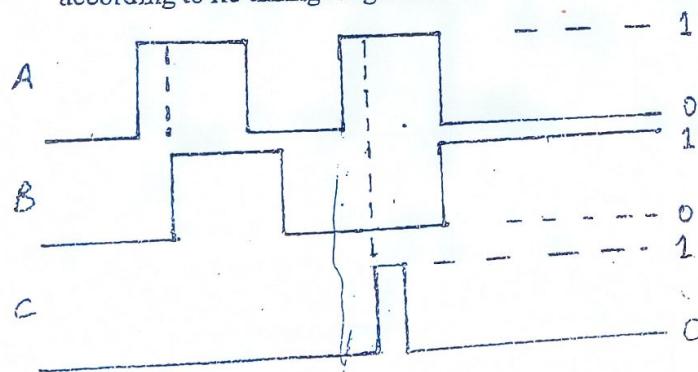
**INSTRUCTIONS:** Answer all the FOUR Questions.

**QUESTION 1**

- (a) Show by using a truth table that the Logic circuit below implements the function



- (b) Determine the NOR gate output waveform having inputs A, B and C that vary according to the timing diagram below:



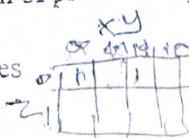
**QUESTION 2**

- (a) Given the Boolean function:  $F = \bar{A}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{B}\bar{C} + \bar{B}\bar{C}$

- (i) Express it as a sum of minterms.  
(ii) Using Karnaugh map, derive the minimal sum of products expression

- (b) Implement the following function with NAND gates

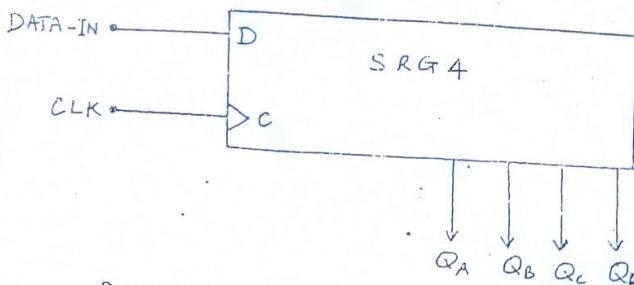
$$F(x,y,z) = \sum(0, 6)$$



$$\begin{array}{|c|c|c|} \hline A & B & C \\ \hline 0 & 0 & 0 \\ \hline 0 & 0 & 1 \\ \hline 0 & 1 & 0 \\ \hline 0 & 1 & 1 \\ \hline 1 & 0 & 0 \\ \hline 1 & 0 & 1 \\ \hline 1 & 1 & 0 \\ \hline 1 & 1 & 1 \\ \hline \end{array}$$

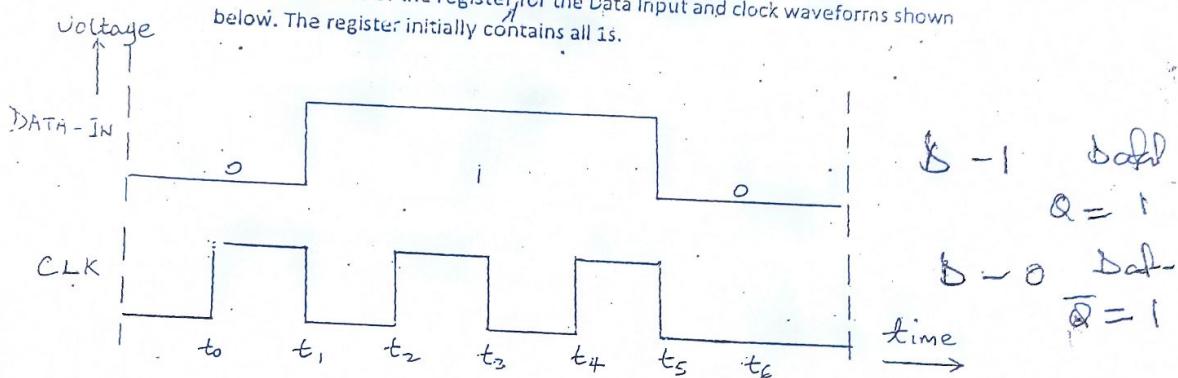
## QUESTION 3

- (a) The Logic Symbol below represents a Serial in - Parallel out (SISO) shift Register.



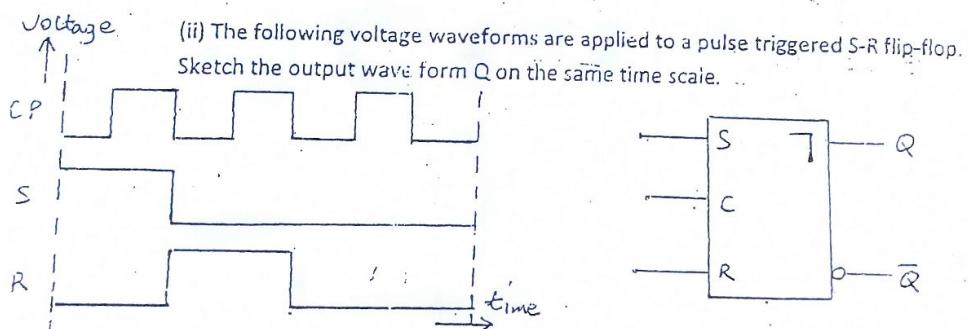
Draw a Logic Circuit of the Shift Register represented by the symbol.

- (b) Show the states of the register for the Data Input and clock waveforms shown below. The register initially contains all 1s.

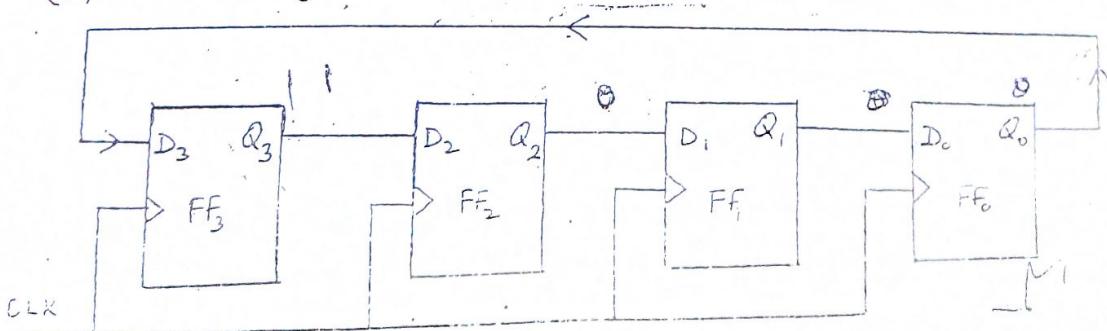


## QUESTION 4

- (a) (i) Using appropriate logic circuit illustrations, distinguish between edge-triggered and pulse-triggered types of flip-flops.



- (b) The Logic Circuit below shows a 4-bit Ring Counter



Assuming an initial count state  $Q_3 = 1$ ,  $Q_2 = Q_1 = Q_0 = 0$   
 Construct the timing diagram for 8 clock pulses and determine the Modulus of  
 the counter.

~~1<sup>st</sup> HYDRINE~~

MAHERERE UNIVERSITY  
FACULTY OF TECHNOLOGY  
DEPARTMENT OF ELECTRICAL ENGINEERING  
ECE (201) FIRST YEAR, SECOND SEMESTER 2004/2005 EXAMINATIONS

ECE 1206: INTRODUCTION TO DIGITAL ELECTRONICS

DATE: 21st June 2005

TIME: 2:00 - 5:00 P.M.

**INSTRUCTIONS**

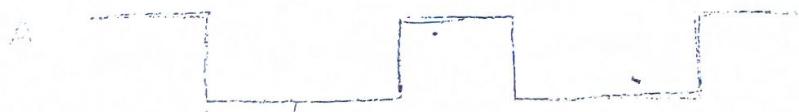
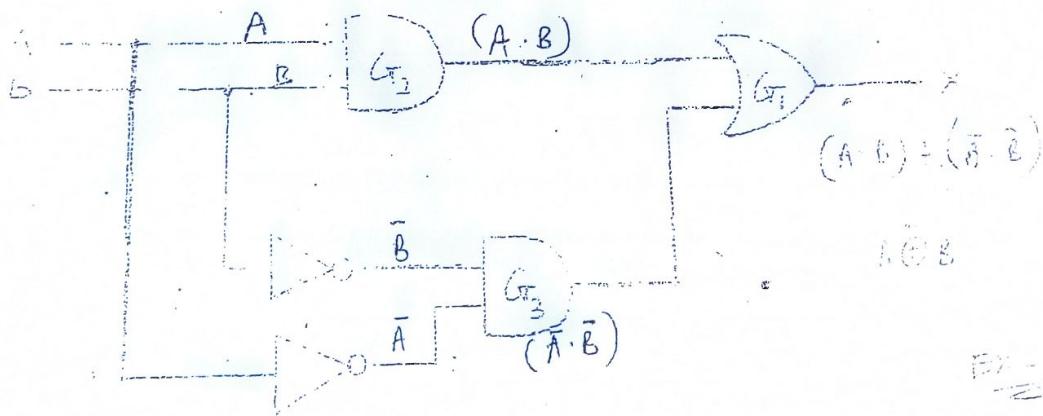
This paper contains FIVE questions. Attempt FOUR questions only.  
All questions carry equal marks.

**QUESTION 1:**

(a) Using the Karnaugh map, simplify the following Boolean function :

$$F(A,B,C,D) = \Sigma(0,1,2,5,8,9,10)$$

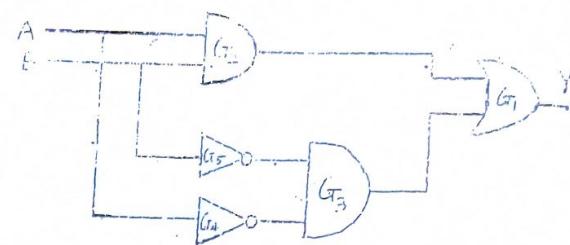
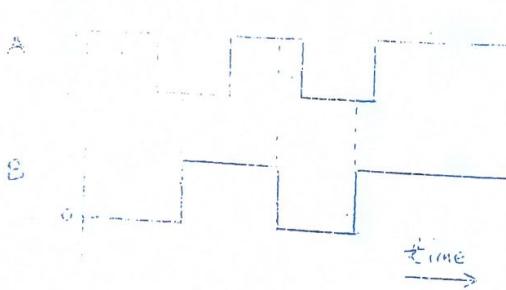
- (i) is sum of products (SOP)
- (ii) is product of sums (POS)
- (iii) Give the logic circuit implementation of the simplified expressions in part (a) above.
- (iv) Determine the output waveform for the circuit below, given the input waveforms as indicated.



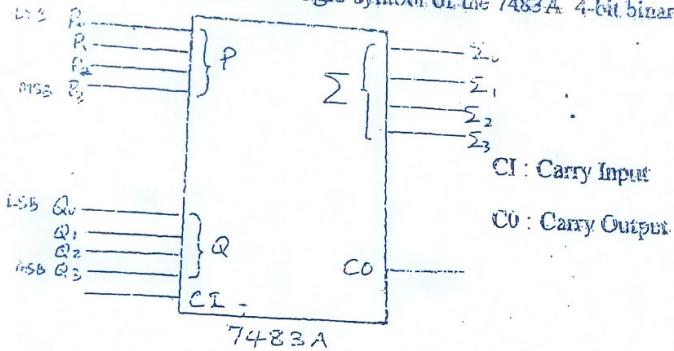
WAVEFORM ANSWERS

### QUESTION 3

- (a) The Logic circuit below has binary inputs varying according to the waveforms shown. Sketch the output waveform Y.



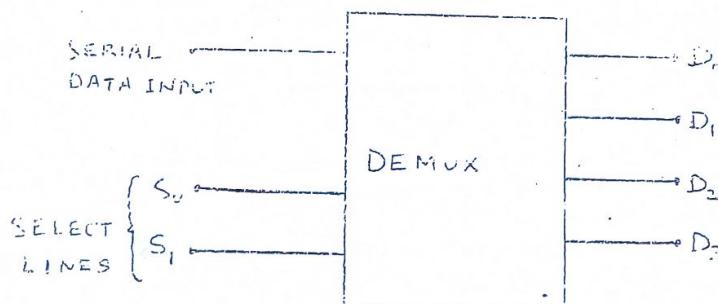
- (b) The diagram below is a Logic symbol of the 7483A 4-bit binary parallel adder.



Draw a block diagram showing the Internal wiring of the 4-bit parallel adder.

### QUESTION 4

- (a) The Logic Symbol below represents a 1 to 4 line Demultiplexer.

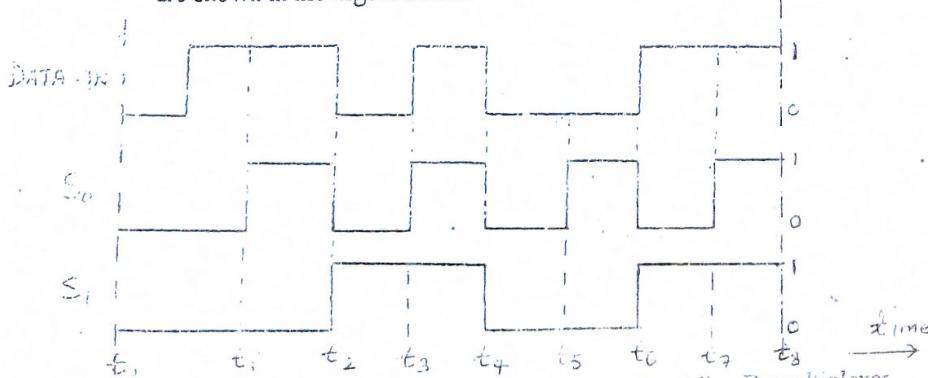


$$Y = \bar{D}_0 \bar{S}_0 \bar{S}_1 + \bar{D}_1 \bar{S}_0 S_1 + \bar{D}_2 S_0 \bar{S}_1 + \bar{D}_3 S_0 S_1$$

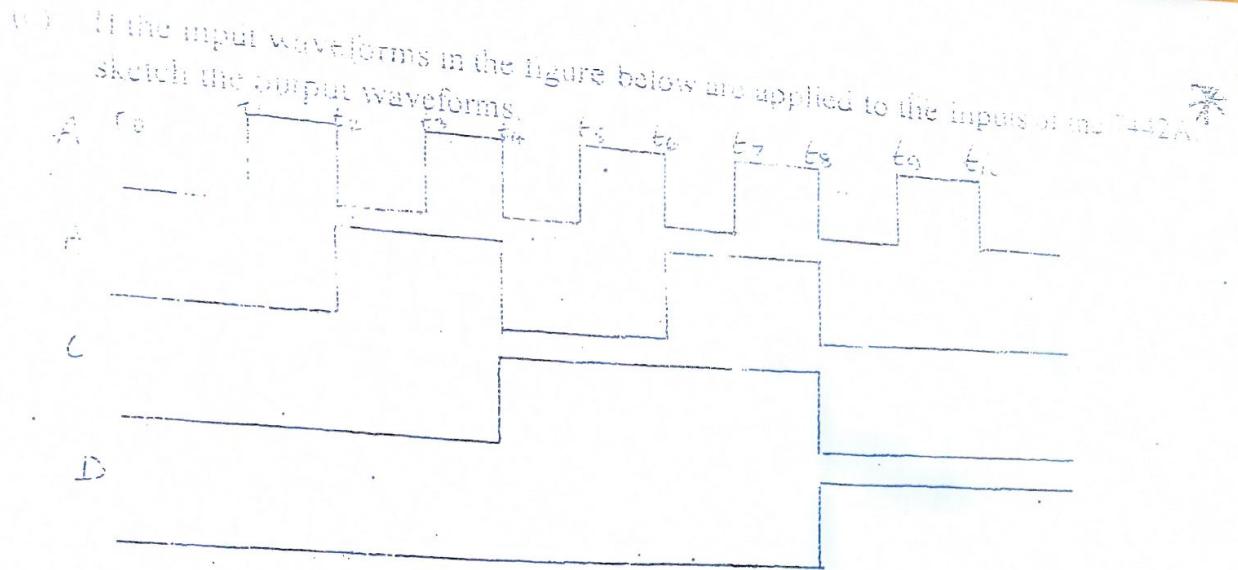
$D_0$	$D_1$	$D_2$	$D_3$
00	00	10	10
01	10	01	10

Synthesize a Logic circuit of the Demultiplexer and briefly explain its operation.

- (b) The Serial data-input waveform and select inputs to the Demultiplexer in part (a) are shown in the figure below:

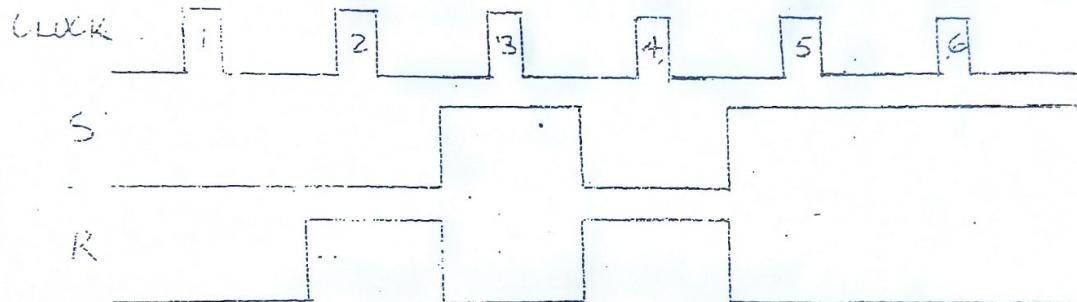


Determine the Data output waveforms of the 1 to 4 line Demultiplexer.

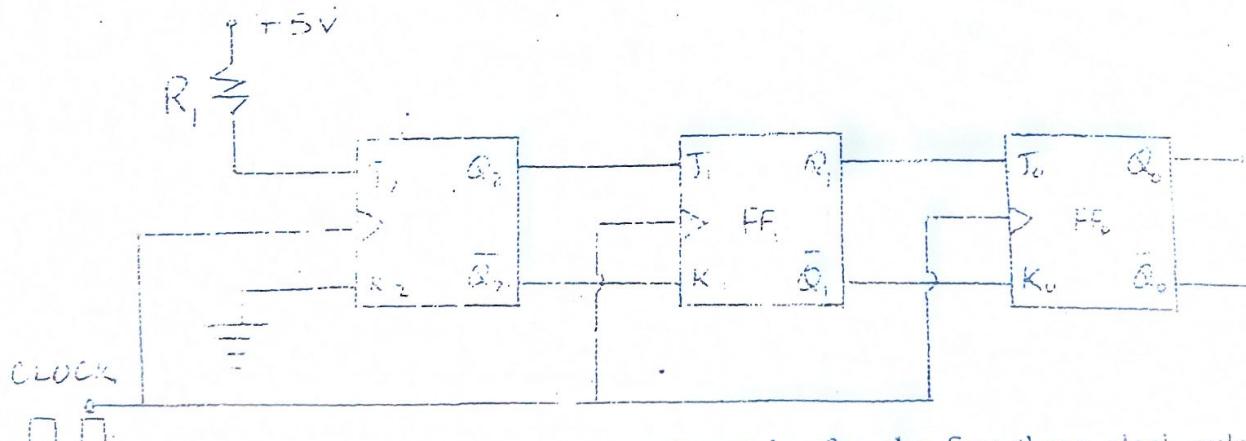


#### QUESTION 4

- (a) Given the input waveforms for the S-R Flip-flop below, determine the Q and  $\bar{Q}$  output waveforms. Assume that the positive edge-triggered flip-flop is initially RESET.



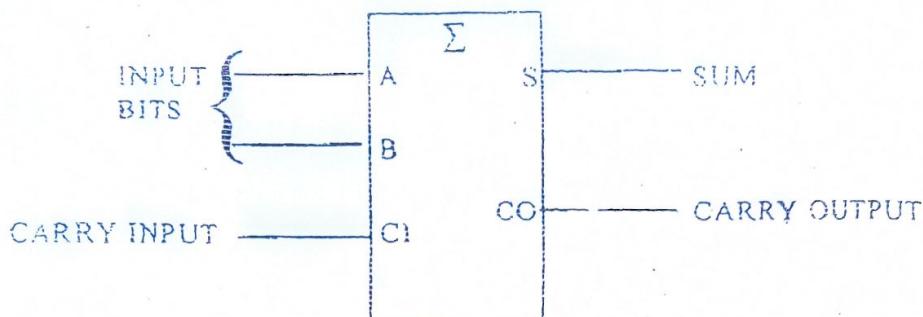
- (b) The diagram in the figure below is a 3-bit register. Explain the operation of the circuit and construct a truth table for 8 clock pulses. Assume that all Flip-flops are cleared to the LOW state before the arrival of the first clock pulse.



- (c) Suppose  $FF_0$  toggles continuously after the first three clock pulses, instead of giving the expected response, what possible circuit fault could produce this operation?

### QUESTION 2

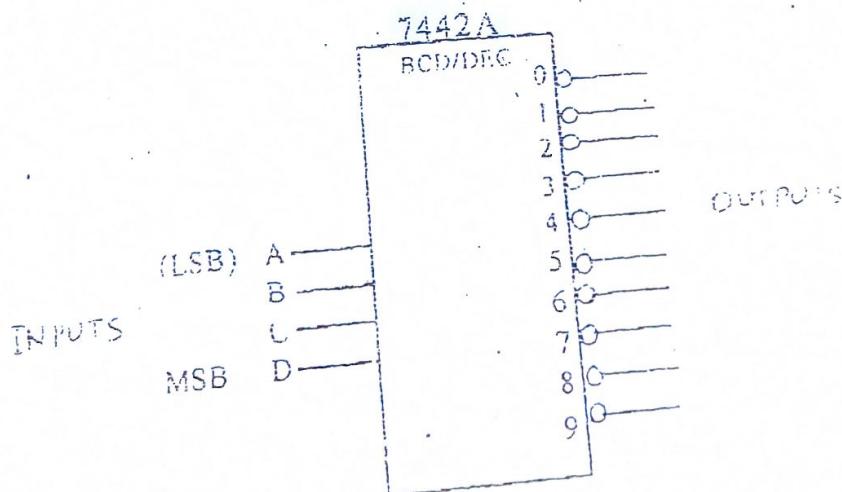
The block diagram below is a logic symbol for a full-adder.



- (a) Write a truth table of the full-adder.
- (b) Derive minimum Logic functions for :
  - (i) the sum (S)
  - (ii) the output carry ( CO )
- (c) Synthesize the full-adder logic circuit using two half-adders.

### QUESTION 3

- (a) Implement a logic circuit required to decode the binary number DCBA = 1011, by producing a LOGIC HIGH at the output.
- (b) The block diagram below is a logic symbol of the 7442A Integrated circuit BCD to decimal decoder producing active LOW outputs.



Write a truth table for the Decoder and synthesize a logic circuit for the 7442A Decoder IC.

DEPARTMENT OF ELECTRICAL ENGINEERING  
 B.Sc ELECTRICAL/TELECOMMUNICATIONS ENGINEERING  
 FIRST YEAR, SECOND SEMESTER 2009/2010

ELE1201: INTRODUCTION TO DIGITAL ELECTRONICS CAT 2

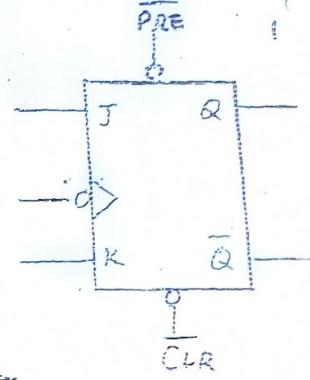
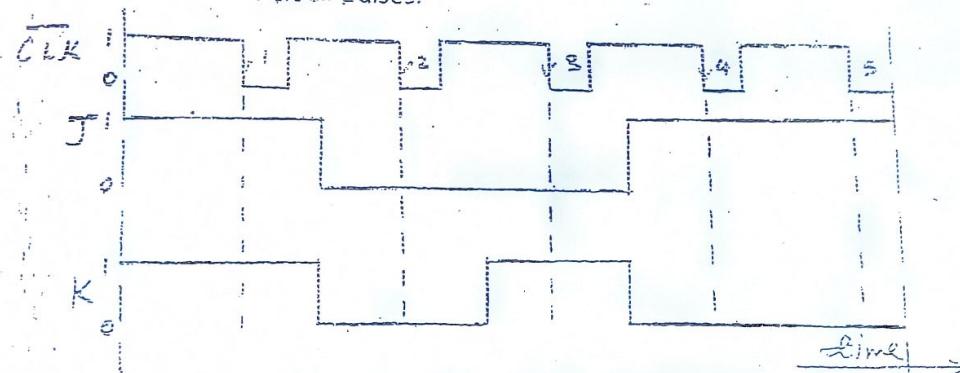
DATE: 29<sup>TH</sup> APRIL, 2010

TIME: 100-1200 NOON

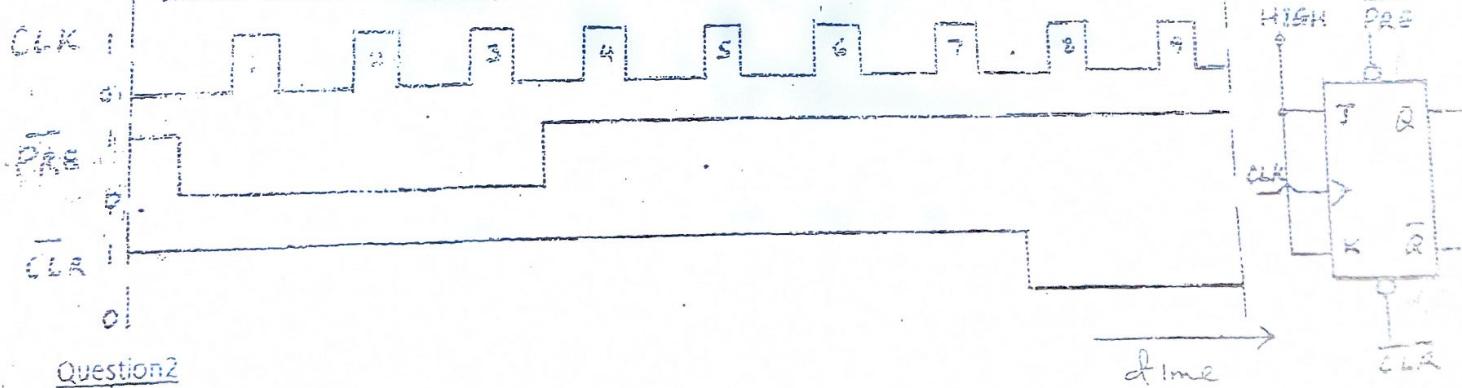
**INSTRUCTIONS: ANSWER ALL THE FOUR QUESTIONS**

**Question 1**

- (a) The voltage waveforms in the figure below are applied to the J-K and CLOCK inputs of a Flip-flop. Assuming the Flip-flop is initially RESET and  $\overline{PRE} = \overline{CLR} = 1$ , sketch the Q-output waveform for a duration of five clock pulses.

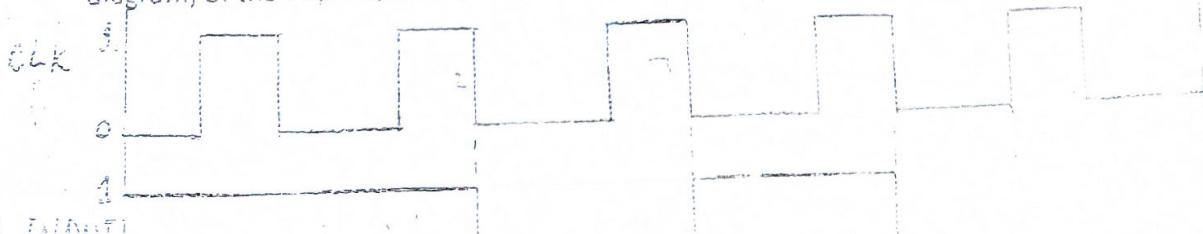


- (a) The following PRESET and CLEAR voltage waveforms are applied to a J-K Flip-flop connected as shown. Sketch the Q-output waveform, assuming Q is initially LOW.



**Question 2**

- (a) Draw a circuit diagram of a 5-bit SISO register using D-type Flip-flops and show the states (timing diagram) of the Flip-flops for the specified input and clock waveforms below:



DATA INPUT

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 DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING  
 SECOND YEAR, SECOND SEMESTER EXAMINATIONS 2015/2016  
 CMP 2203: DIGITAL LOGIC

DATE: 17<sup>TH</sup> MAY, 2016.

TIME: 9.00 – 12.00 NOON

**INSTRUCTIONS:**

This paper contains FIVE questions. Attempt FOUR questions only.  
 Each question carries a total of 25 marks.

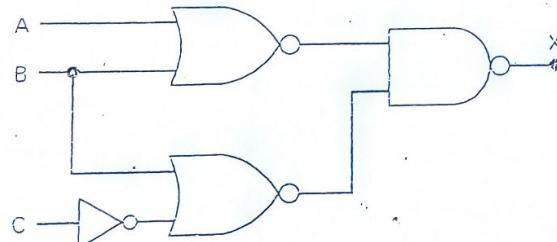
**QUESTION 1**

- a) Use a Karnaugh map to simplify the Logic function below and draw the simplified Logic circuit using NAND gates only.

$$Y = \bar{A} \bar{B} \bar{C} + \bar{B}C + \bar{A}B$$

(9 marks)

- b) Determine the truth table for the Logic circuit below:



(8 marks)

- c) The circuit in part (b) above operates with an active-LOW output and turns ON an indicator lamp under the following input conditions:

$$A = B = \text{LOW (LOGIC 0)}$$

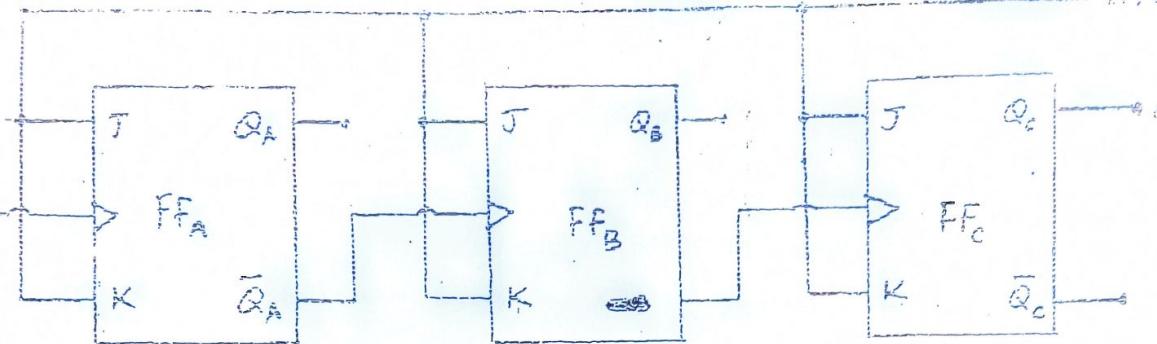
$$C = \text{HIGH (LOGIC 1)}$$

Draw a modified Logic circuit to represent this mode of operation.

(8 marks)

- (b) The circuit diagram below shows a 3-bit asynchronous binary counter.

SL167H

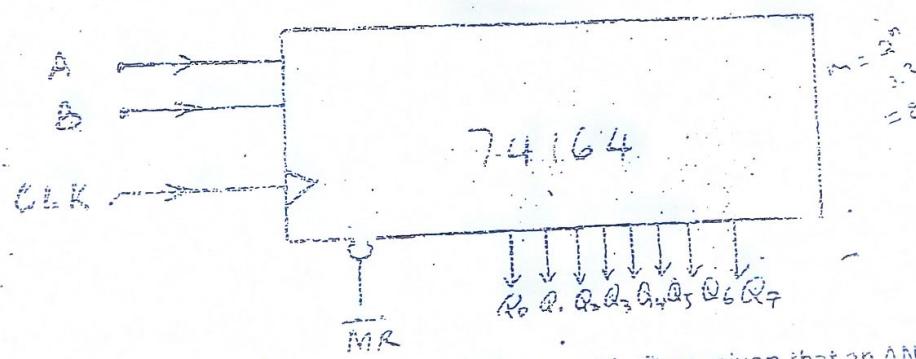


Sketch the timing diagram for one count cycle, assuming the counter is initially RESET.

(iii) Draw an upgraded circuit diagram capable of decoding decimal count 6 using ACTIVE HIGH decoding method.

### Question 3

- (a) The logic symbol for the IC 74164 SIPO Register is shown below:

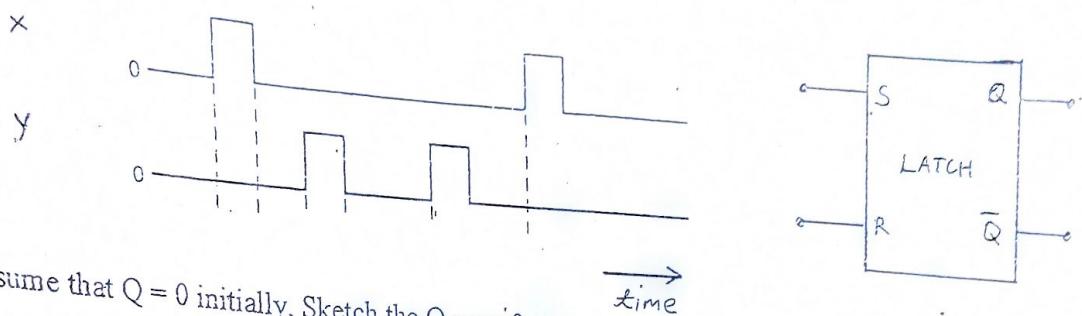


Draw the circuit diagram of the IC74164 using D-type Flip-flops, given that an AND gate combines inputs A, B and to produce the serial input to FF<sub>0</sub>.

QUESTION 2

- a) Using appropriate Logic circuits and Truth tables briefly explain how the following latches are conditioned to operate in a digital system design.
- SR-NOR Latch
  - SR-NAND Latch

- b) i) The x and y waveforms below are applied to the S and R inputs of a NOR latch. (8 marks)



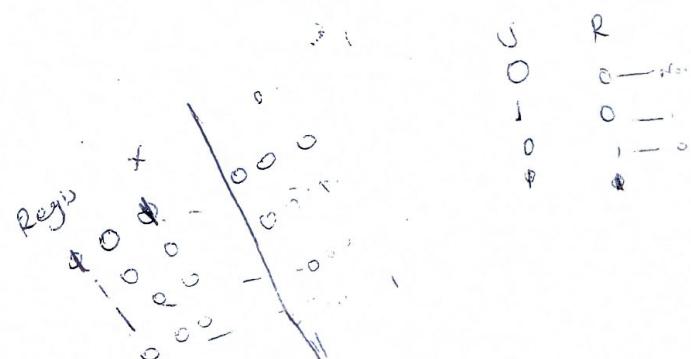
Assume that  $Q = 0$  initially, Sketch the  $Q$  waveform.

- ii) Invert the x and y waveforms and apply them to the SET and RESET inputs of a NAND Latch, determine the  $Q$  waveform. Assume  $Q = 0$  initially.

- c) i) Draw a Logic circuit used for serial transfer of a DATA word  $X_2 X_1 X_{0LSB} = 1 0 1$  from one register X to another register Y leaving register X with a DATA word  $X_2 X_1 X_0 = 0 0 0$  at the end of the transfer operation. Use D-type Flip-flops. (8 marks)

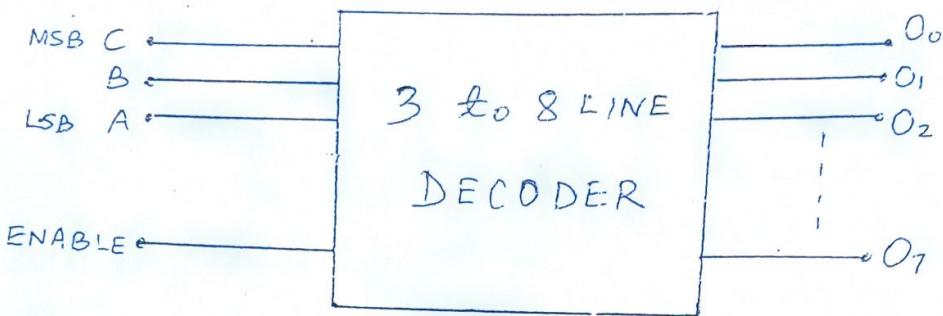
- iii) Modify the Logic circuit in part (i) above so that the original DATA word stored in register X is present in both registers at the end of the transfer operation.

(9 marks)

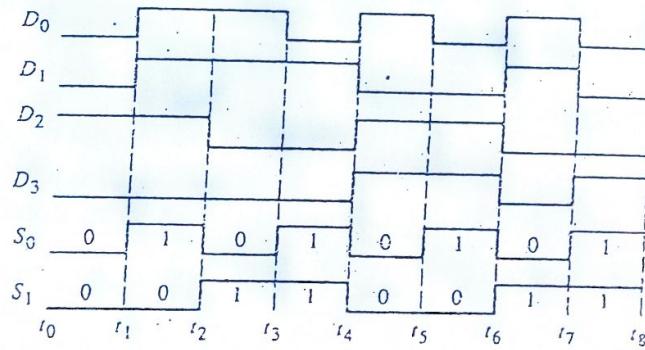


### QUESTION 3

The block symbol below represents a 3 to 8 line Decoder.



- a) Draw a Logic circuit of the Decoder and construct its truth table (12 marks)
- b) Show how a 1 to 8 line Demultiplexer can be implemented using the Decoder circuit in part (a) above
- c) The following Data and select waveforms are applied to 1 of 8 multiplexer. (7 marks)

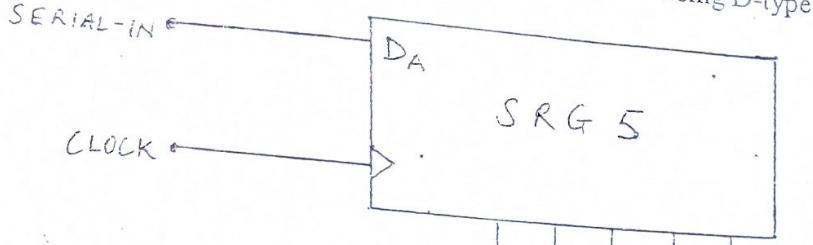


Determine the output waveform.

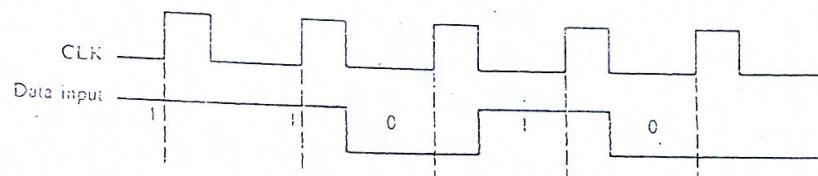
(6 marks)

QUESTION 4

- a) The block symbol of a 5-bit SISO type register using D-type Flip-flops is shown below:

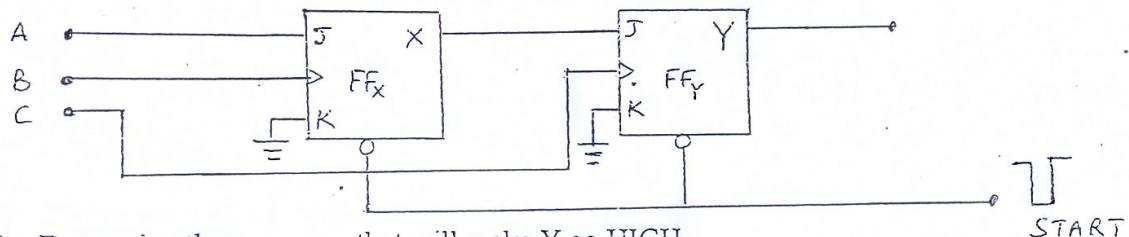


Draw the Logic circuit of the register and construct a waveform diagram showing the states of the register for the following specified Data input and Clock waveforms. Assume that the register is initially cleared.



(10 marks)

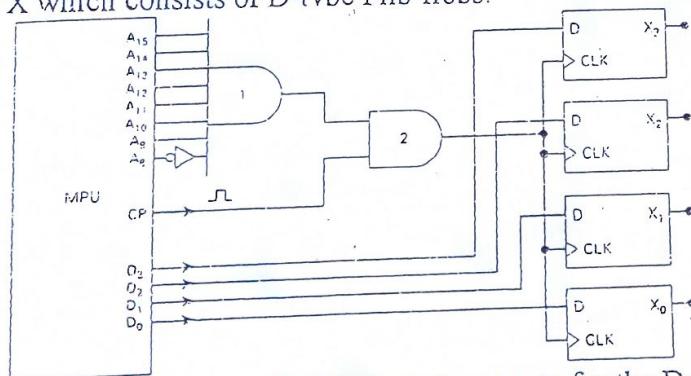
- b) In the Logic circuit below the inputs A, B and C are all initially LOW, output Y is supposed to go HIGH only when the inputs(HIGH or LOW) change in a certain sequence



- i) Determine the sequence that will make Y go HIGH.  
ii) Explain why a START pulse is needed.

(6 marks)

- c) The figure below shows a microprocessor unit (MPU) with its outputs used to transfer Binary data to register X which consists of D-type Flip-flops.

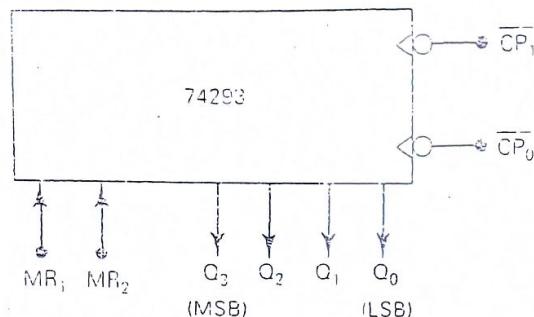


- i) Determine address code the MPU must generate for the Data to be transferred into register X.  
ii) Assume that  $X_3 - X_0 = 0110$ ,  $A_{15} - A_8 = 11111111$ ,  $D_3 - D_0 = 1011$ . Determine the contents in register X after the clock pulse occurs.  
iii) Modify the circuit above so that only the presence of address code 10110110 will allow Data to be transferred to register X.

(9 Marks)

## QUESTION 5

The Logic symbol of the 74293 IC asynchronous counter is shown below:



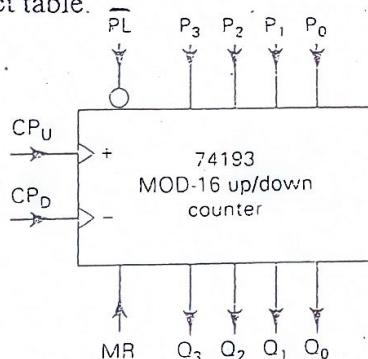
- a) Draw the Logic circuit of the 74293 IC asynchronous counter

(8 marks)

- b) Use the Logic symbol of the 74293 IC counter and show how it can be wired to produce 1.2kpps output from 18kpps clock input.

(8 marks)

- c) The figure below is a Logic symbol of the 74193 IC MOD -16 presetable UP/DOWN counter and its Mode select table.



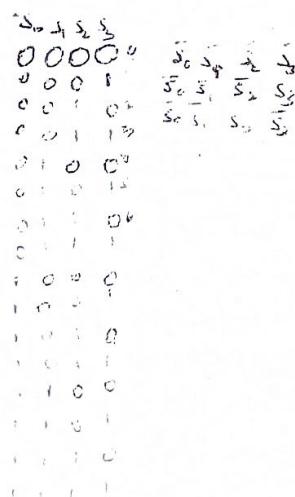
Mode Select				
MR	PL	CP <sub>U</sub>	CP <sub>D</sub>	Mode
H	X	X	X	Asynch. reset
L	L	X	X	Asynch. preset
L	H	H	H	No change
L	H	↑	H	Count up
L	H	H	↑	Count down

H = HIGH; L = LOW

X = Don't care; ↑ = PGT

With the clock wired at CP<sub>D</sub> terminal, MR at ground potential and CP<sub>U</sub> terminal maintained in the HIGH state, draw the state transition diagram of the counter

(9 marks)



# Makerere University

## Introduction to Digital Electronics

Continuous Assessment Test 1

Time: 1 hour and 30 minutes

Instructions: Answer all questions.

**Question 1:** The NAND gate output will be low if the two inputs are

- A. 00      B. 01      C. 10

D. 11

**Question 2:** What is the binary equivalent of the decimal number 368?

A. 101110000

B. 110110000

C. 111010000

D. 00011101

**Question 3:**  $734_8 = (?)_{16}$

- A. C 1 D      B. D C 1      C. 1 C D      D. 1 D C

**Question 4:** The number of control lines for a 16-to-1 multiplexer is

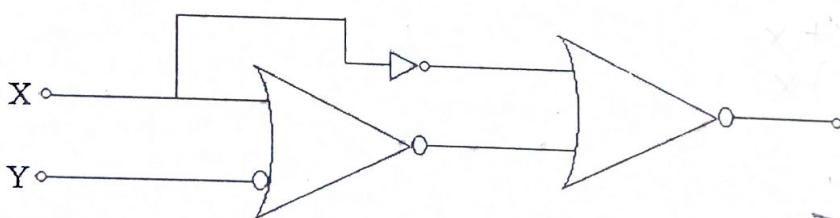
- A. 2      B. 4      C. 8      D. 16

**Question 5:** The Boolean expression  $\bar{A}B + \underline{\bar{A}\bar{B}} + AB$  is equivalent to

- A.  $A + B$       B.  $\bar{A}B$       C.  $B + A\bar{B}$       D.  $AB$

$$\begin{array}{l} \bar{A}B+A \\ \hline A+B \end{array}$$

**Question 6:** The logic circuit below can be minimized to



- A.  $\bar{X}$       B.  $\bar{X}Y$       C.  $X$       D.  $X\bar{Y}$

**Question 7:** The hexadecimal number for the decimal number  $\underline{95.5}$  is

- A. 5F.8      B. 9A.B      C. 2E.F      D. 5A.4

**Question 8:** Which of the following is a universal logic gate?

- A. OR      B. AND      C. XOR      D. NAND

**Question 9:**

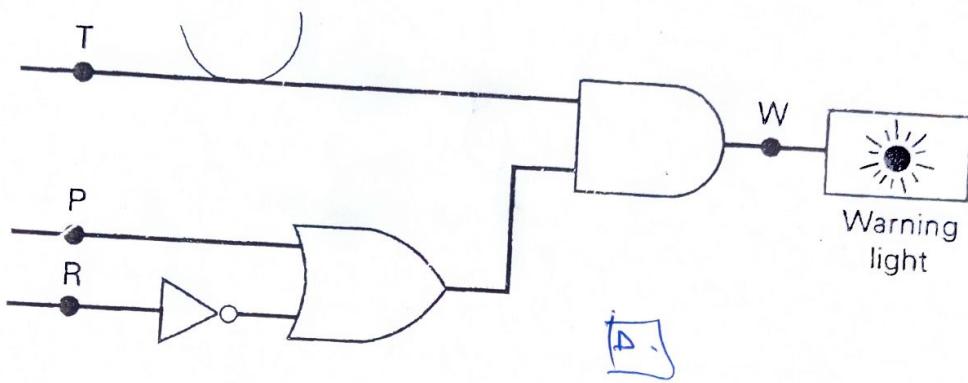
Simplify the expression of  $A$  using Boolean postulates:

$$A = \overline{XY} + XYZ + X(Y + XY).$$

**Question 10:**

The figure below shows a logic circuit that controls a cockpit warning light for certain combinations of engine conditions. Assume that a HIGH output activates the warning light.

- Determine the engine conditions that will give a warning to the pilot.
- Change this circuit to one using all NAND gates.



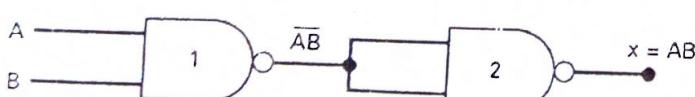
*Note: For this question, the following equivalent gates might be helpful.*



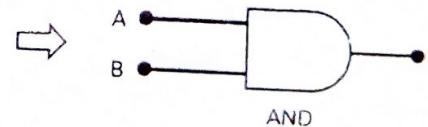
(a)



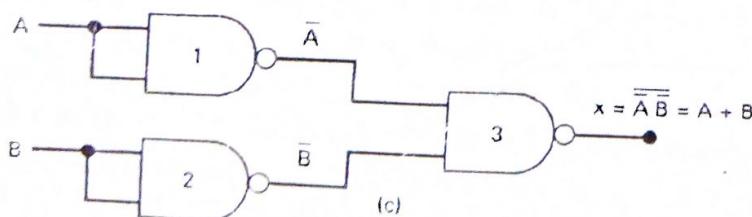
INVERTER



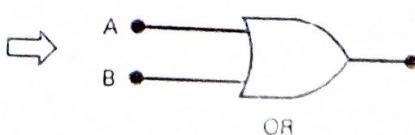
(b)



AND



(c)



OR

Time: 1hr: 15 min

Answer all questions

### Question One.

- a) Give four reasons to justify Boolean expression minimization in digital logic. Hence simplify the following expressions using Boolean algebra and compare the results using K-Map.
- $w = ABC + A\bar{B}C + \bar{A}$
  - $x = AB(\bar{C}\bar{D}) + \bar{A}BD + \bar{B}\bar{C}\bar{D}$
  - $k = AB + A'B'C'D + A'B'C'D + AB'C'D'$
- b) A sequential circuit has two JK flip-flops A and B, two inputs  $x$  and  $y$ , and one output  $z$  with A being the normal output of Flip-Flop A and B being the normal output of Flip-flop B. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y'$$

$$K_A = B'xy'$$

$$J_B = A'x$$

$$K_B = A + xy'$$

$$z = Ax'y' + Bx'y'$$

Give the logic diagram and the state diagram of the circuit.

### Question Two

- a) Distinguish between sequential and combinational Circuit. Hence consider a combinational majority circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority circuit by finding the circuit's using the minimum number of logic components.
- b) Design counter with state diagram below using T-Flipflops

