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ECE 558 – Intro to VLSI Design, Lab 2 Report

Step 1:

Input		Output	
C_{in}	**Q**	**S**	**C_{out}**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

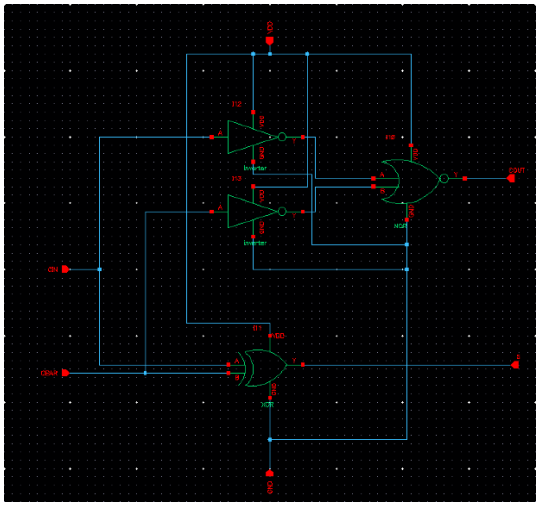
Input		Output
S	RST	D
0	0	1
0	1	1
1	0	1
1	1	0

Input		Output		
PHI	**D**	**Q**	**$\bar{Q}$**	**S_{out}**
0	0	Q	$\bar{Q}$	$\bar{Q}$
0	1	Q	$\bar{Q}$	$\bar{Q}$
1	0	0	1	1
1	1	1	0	0

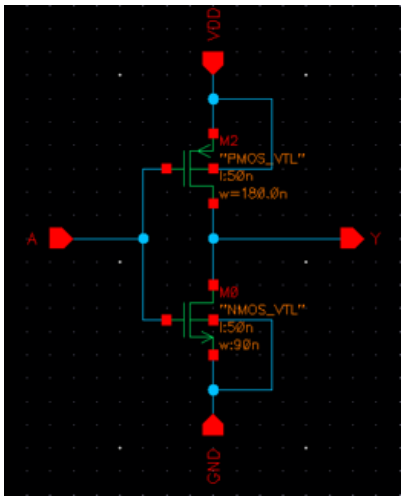
Input				Output		
C_{in}	Q	RST	PHI	S	C_{out}	D
0	0	0	0	0	0	1
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	0
1	0	0	0	1	0	1
1	0	0	1	1	0	1
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	0	1	1
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	0	1	1

Step 2:

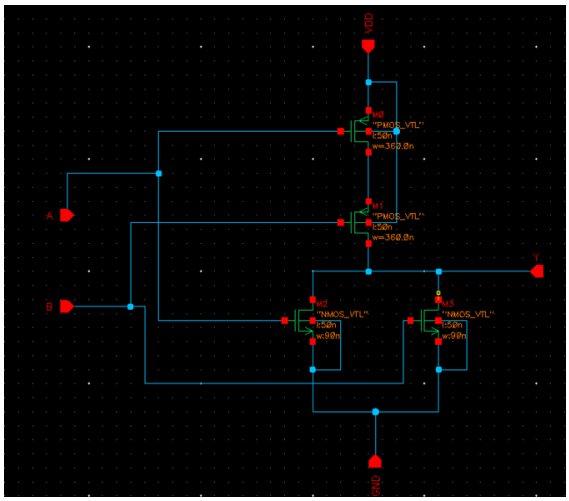
Half Adder:



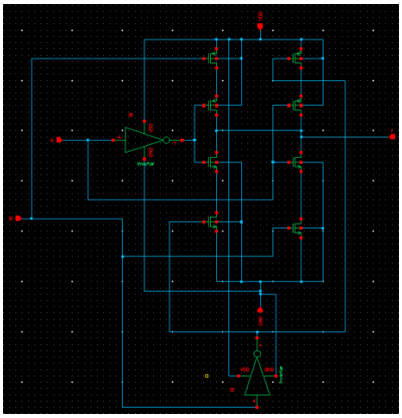
Inverter:



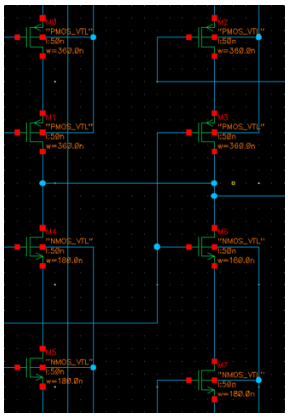
NOR Gate:



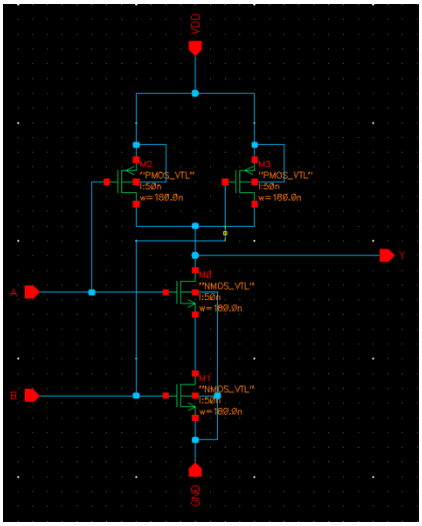
XOR Gate



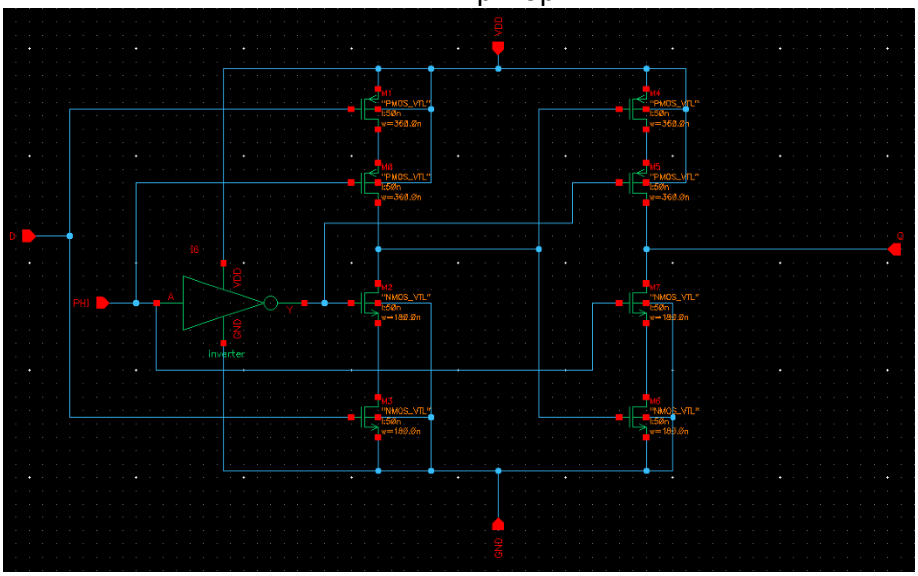
XOR Transistors Size



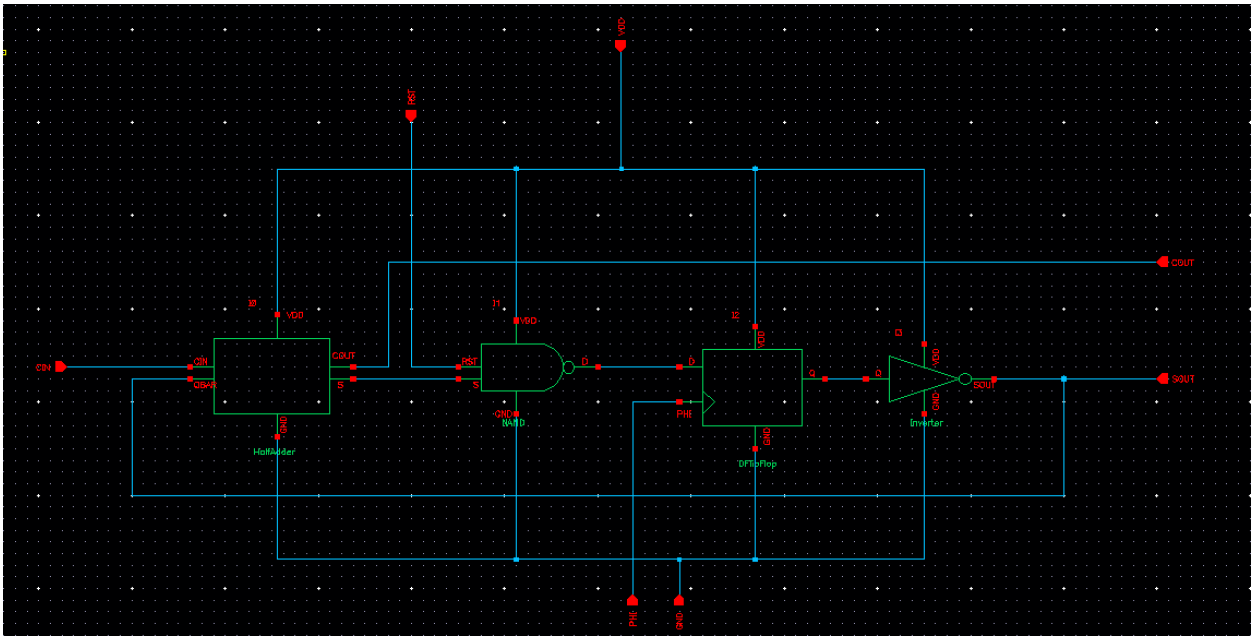
NAND Gate:



Flip Flop:

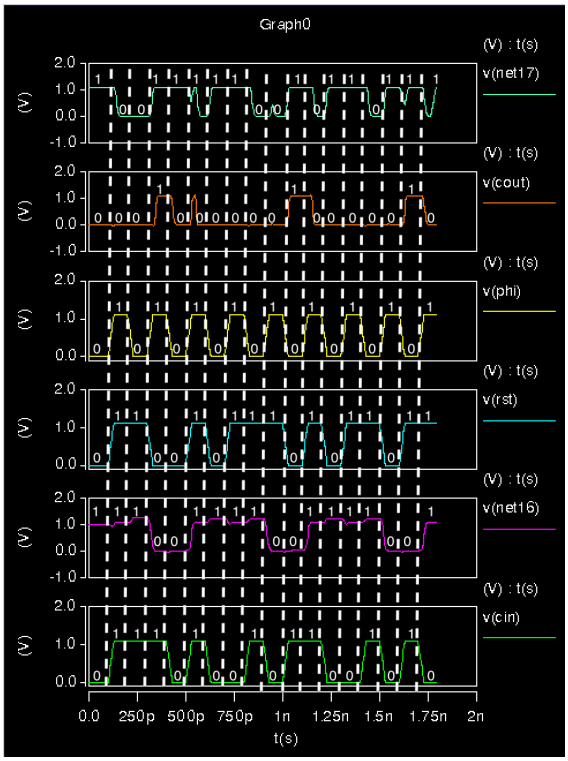


Accumulator:



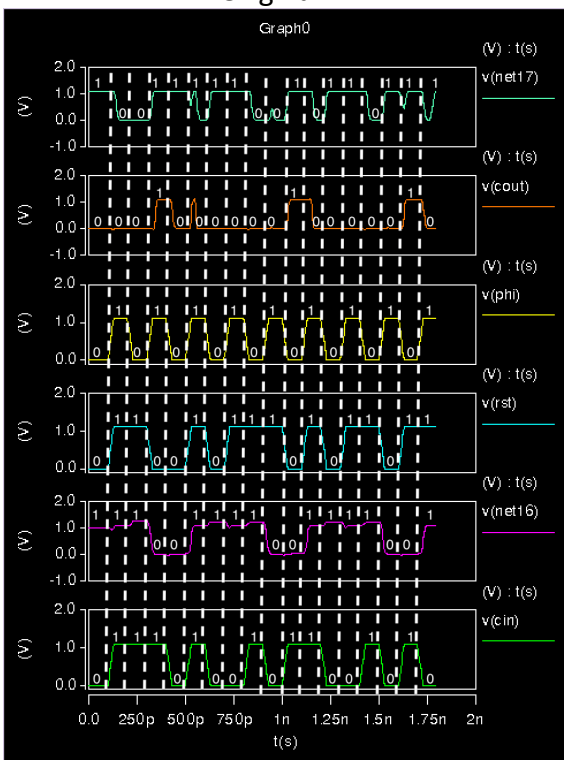
Step 3:

Input					Output	
C_{in}	Q	RST	PHI	S	Cout	D
0	1	0	0	0	0	1
1	1	1	1	1	0	0
1	1	1	0	1	0	0
1	0	0	1	0	1	1
0	0	0	0	1	0	1
1	1	1	1	1	0	1
0	1	0	0	0	0	1
0	1	1	1	0	0	1
1	1	1	0	1	0	0
0	0	1	1	1	0	0
1	0	0	0	0	1	1
1	1	1	1	1	0	0
0	1	0	0	0	0	1
0	1	1	1	0	0	1
1	1	1	0	1	0	0
0	0	0	1	1	0	1
1	0	0	0	0	1	1
0	1	1	1	0	0	1

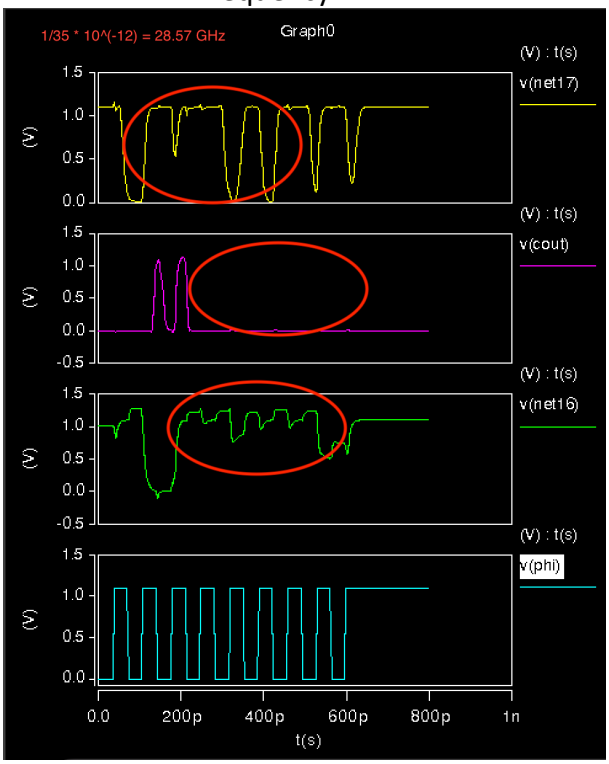


Step 4

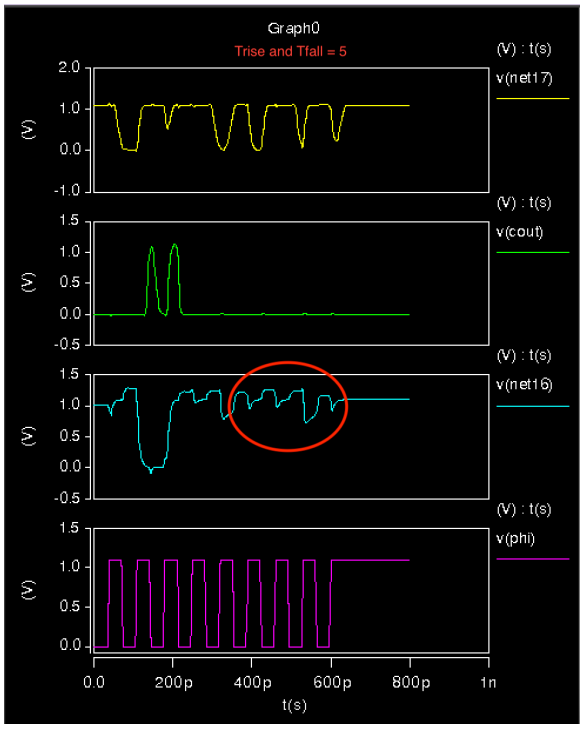
Original



Frequency



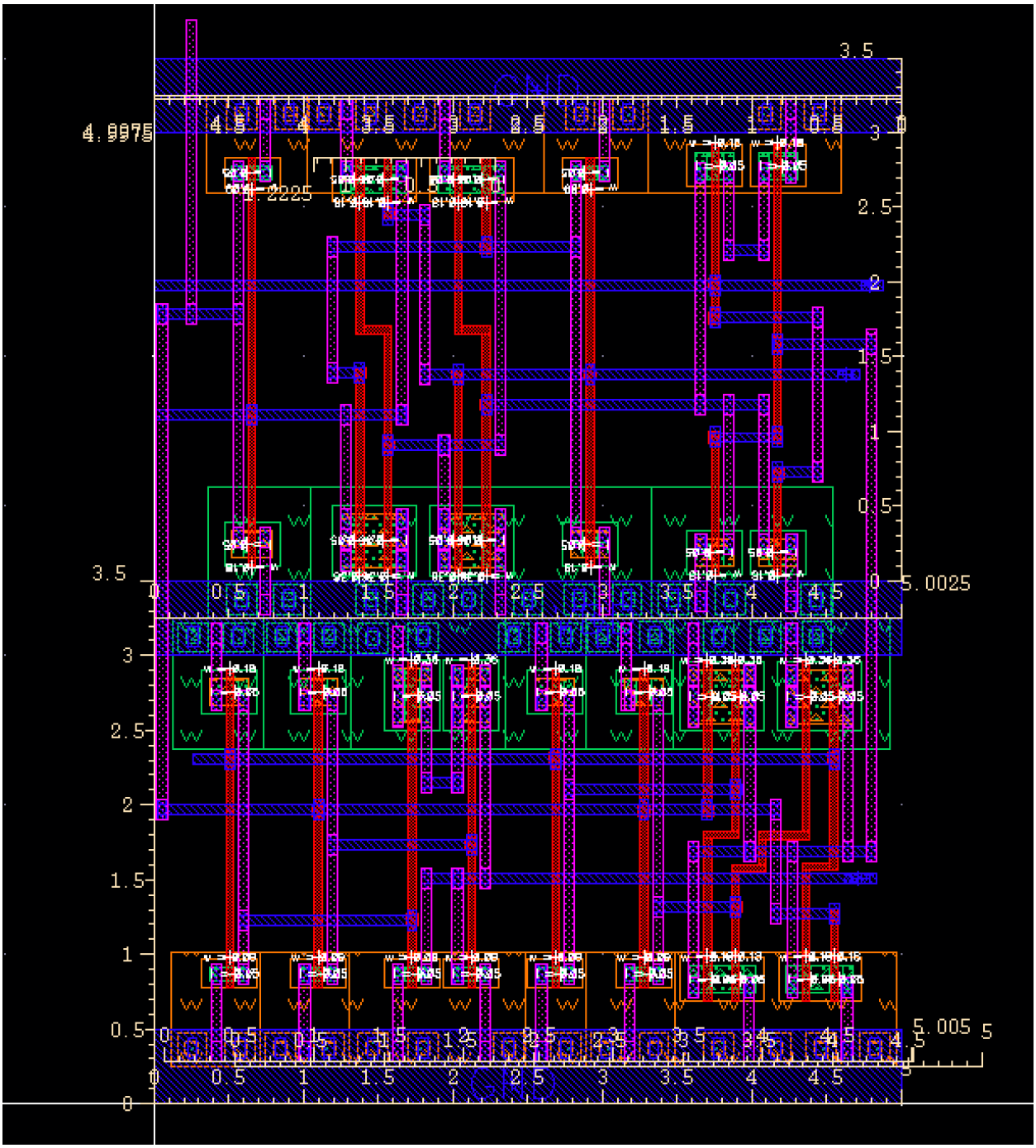
Rise and Fall time

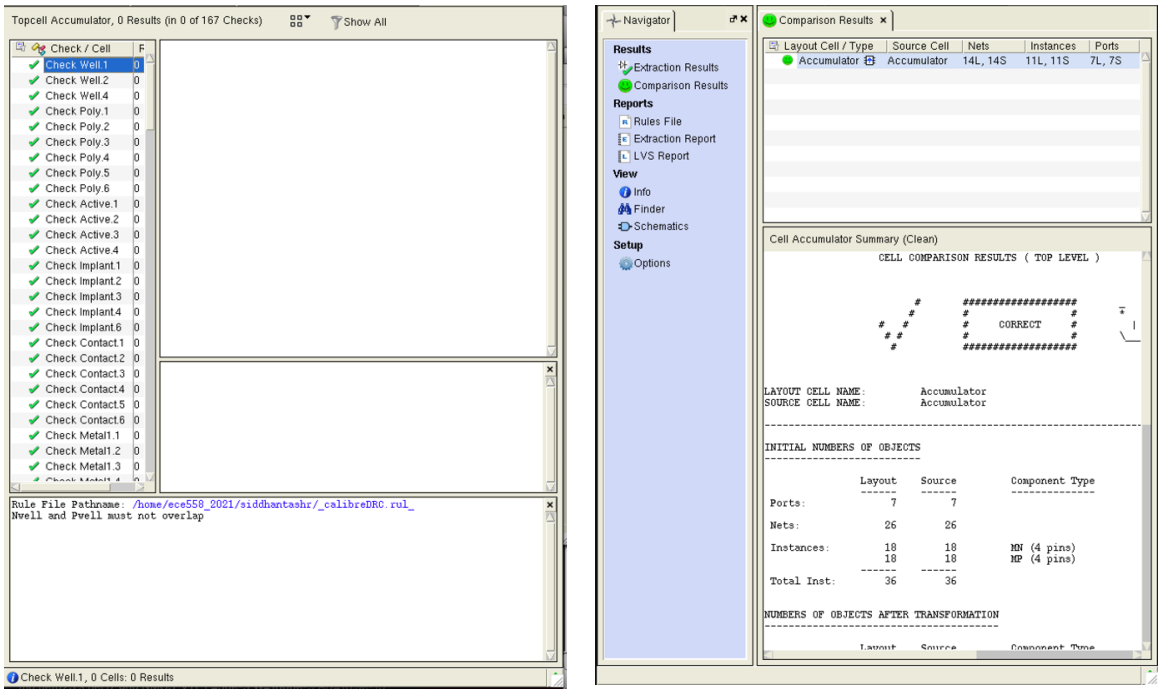


The maximum clock frequency is 28.57 GHz

Step 5

Step 6




Topcell Accumulator, 0 Results (in 0 of 167 Checks)
Show All
Check / Cell
Check Well.1
Check Well.2
Check Well.4
Check Poly.1
Check Poly.2
Check Poly.3
Check Poly.4
Check Poly.5
Check Poly.6
Check Active.1
Check Active.2
Check Active.3
Check Active.4
Check Implant.1
Check Implant.2
Check Implant.3
Check Implant.4
Check Implant.6
Check Contact.1
Check Contact.2
Check Contact.3
Check Contact.4
Check Contact.5
Check Contact.6
Check Metal1.1
Check Metal1.2
Check Metal1.3
Rule File Pathname: /home/ece558_2021/siddhantashr/_calibreDRC.rul_
Nwell and Pwell must not overlap
Check Well.1, 0 Cells: 0 Results
Navigator
Results
Extraction Results
Comparison Results
Reports
Rules File
Extraction Report
LVS Report
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
Accumulator
Accumulator
14L, 14S
11L, 11S
7L, 7S
Cell Accumulator Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: Accumulator
SOURCE CELL NAME: Accumulator
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 7 7
Nets: 26 26
Instances: 18 18 NN (4 pins)
18 18 MP (4 pins)
Total Inst: 36 36
NUMBERS OF OBJECTS AFTER TRANSFORMATION

Step 7