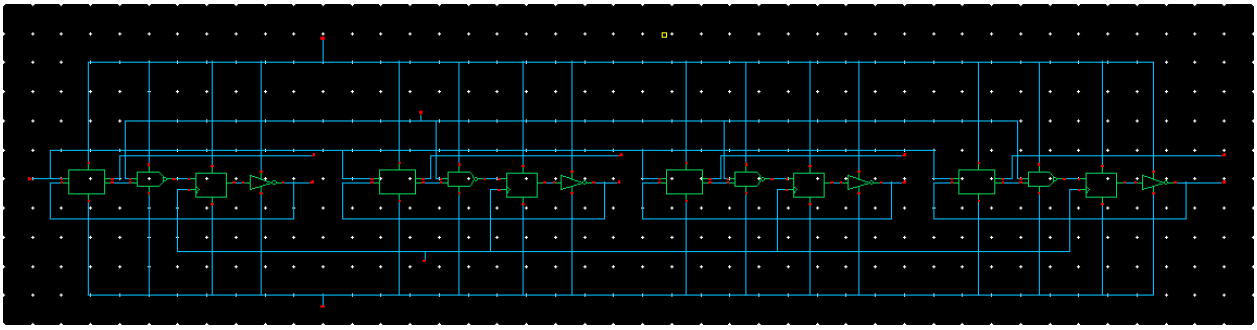
Siddhanta Shrestha

ECE 558 – Intro to VLSI Design, Lab 3 Report

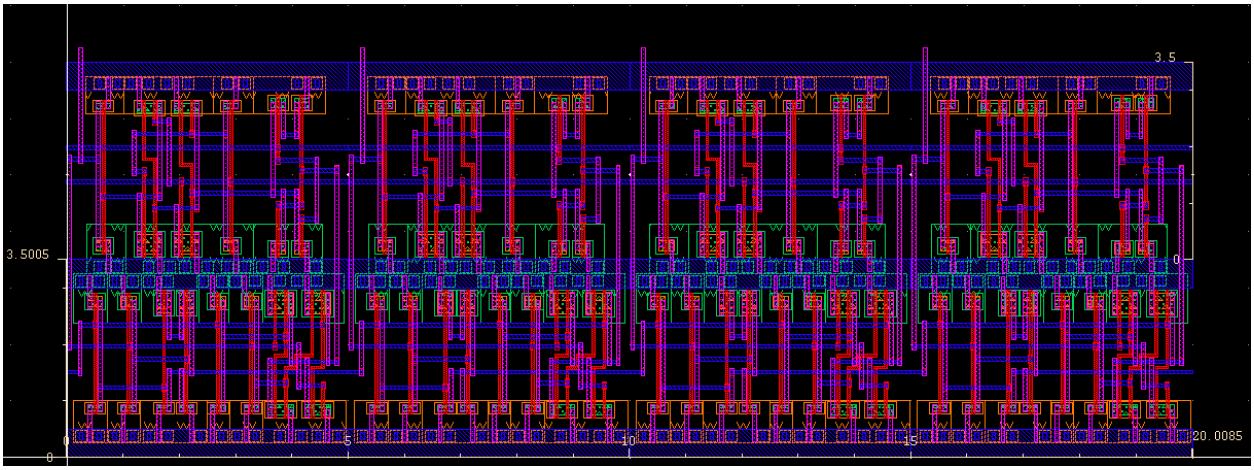
Step 1:



Step 2:

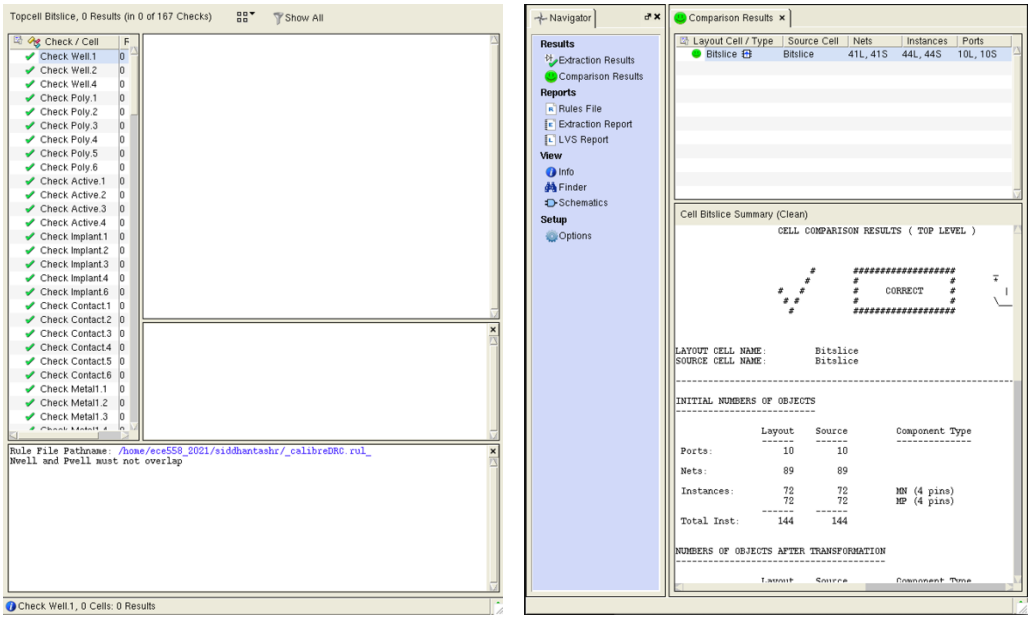
CLK	RST	CIN	D3	D2	D1	D0	SOUT3	SOUT2	SOUT1	SOUT0	Q3	Q2	Q1	Q0
0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	1	1	1	1	1	1	0	0	0	0	1	1	1	1
0	1	0	1	1	1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
1	1	0	0	0	0	0	1	1	1	1	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	0	0	0	0
1	1	0	0	0	0	0	1	1	1	1	0	0	0	0
0	1	0	0	0	0	0	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
1	1	0	0	0	0	0	1	1	1	1	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

Step 3:



There were several changes that needed to be made to the bitslice layout from Lab 2. The First being the adjustment of CIN. Because the COUT of the half adder was the CIN to the next accumulator, there needed to be an adjustment so that the layout reflected this. Thus metal 2 was used to bring down the input for CIN. In addition to this, the labels for the inputs/outputs also needed to be adjusted so that it reflected the labels from the bitslice schematic.

Step 4:



Step 5: