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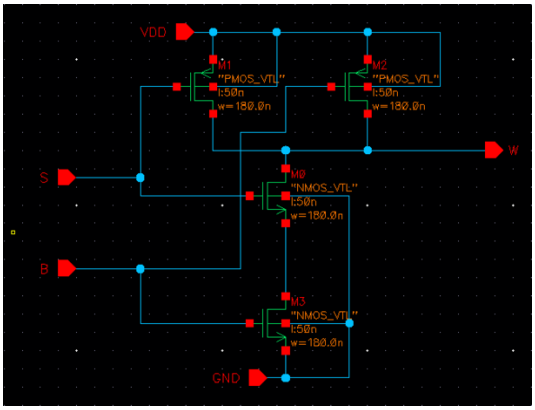
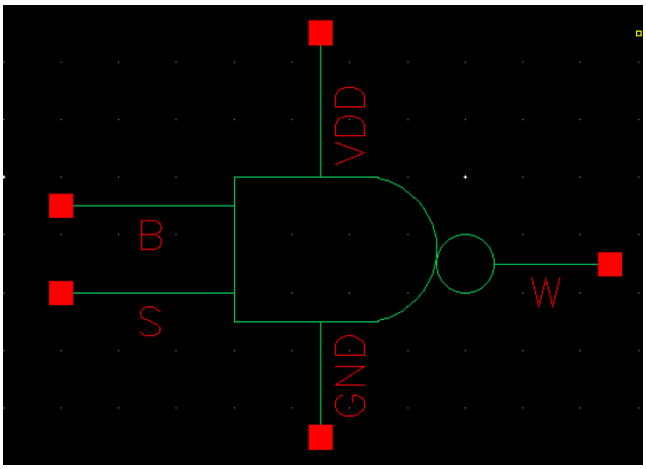
ECE 558 – Intro to VLSI Design, Lab 1 Report

Step 1. **Truth table for NAND gate**

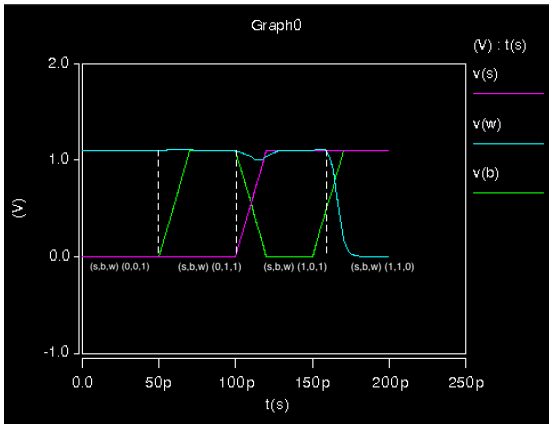
INPUT		OUTPUT
S	**B**	**W**
0	0	1
0	1	1
1	0	1
1	1	0

Step 2. **NAND Gate Transistor-Level Schematic and NAND Gate**





Step 3.



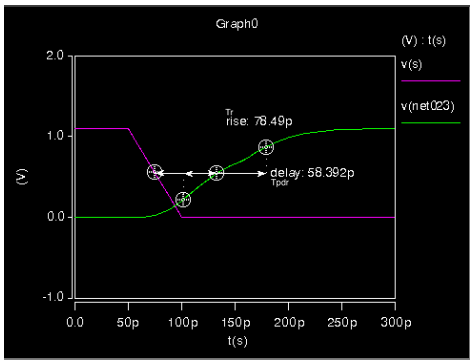
Looking at the graph of the two inputs (s,b) and the output (w), it matches up with the truth table from Step 1. When s and b are both 0s, or when one of them is a 0 then w is a 1. But when both s and b are 1 then w is a 0.

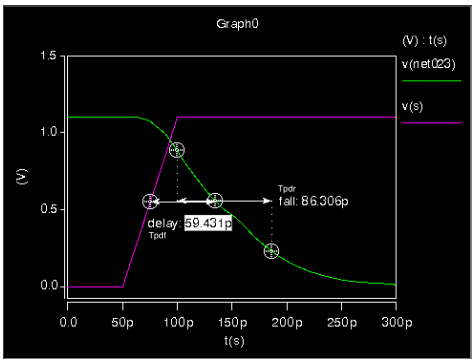
Step 4.

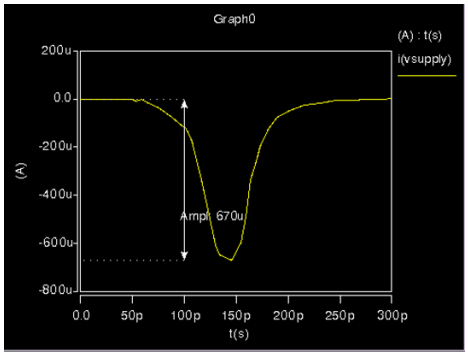
Input Combination	t_{pdf} or t_{pdr}	tf or tr	
11 -> 01; w -> 1 to 0	7.4966 ps	11.133 ps	rise
11 -> 10; w -> 1 to 0	10.798 ps	13.884 ps	Worst case for rise
01 -> 11; w -> 0 to 1	7.1958 ps	11.373 ps	Worst case for fall
10 -> 11 ; w -> 0 to 1	6.2960 ps	10.084 ps	F fall

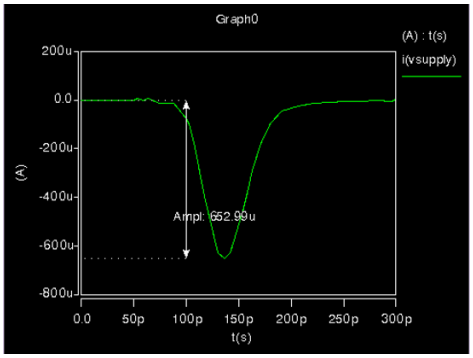
Step 5.

Input Combination	t_{pdr} or t_{pdf}	t_r or t_f	P_{stat} or P_{dyn}
11 -> 01; w -> 1 to 0	58.392 ps	78.49 ps	737 uWatts
01 -> 11; w -> 0 to 1	59.431 ps	86.306 ps	718.289 uWatts







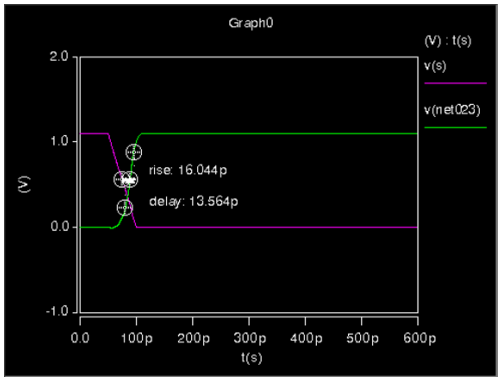


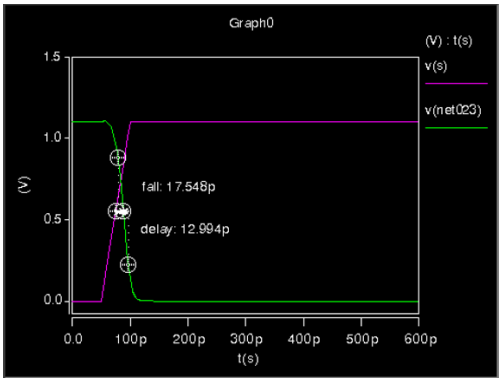
The time measurements in step 5 are much bigger thus the rise and fall occur over a longer period compared to the time measurements in step 4. This is because the inverter delays the output signal of the NAND gate. As a result, the rise fall delay occurs over a longer period of time.

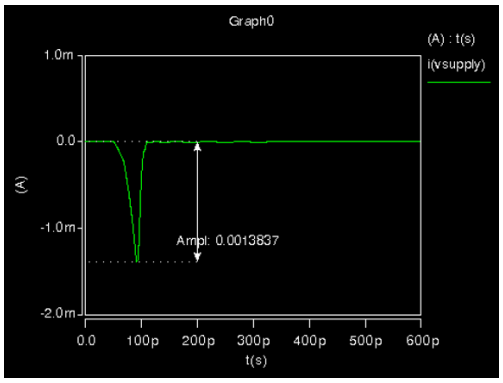
Peak power can be calculated by using the equation $P_{peak} = I_{peak} * V_{DD}$. Where I_{peak} is simply the max current from the v supply and can be found by the amplitude of the current. Dynamic power is being consumed in the inverters as they are charging and discharging at the output.

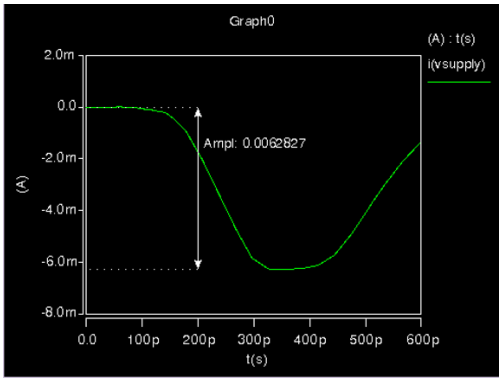
Step 6.

Input Combination	t_{pdr} or t_{pdf}	t_r or t_f	P_{stat} or P_{dyn}
11 -> 01; w -> 1 to 0	13.564 ps	16.044 ps	0.00152 Watts
01 -> 11; w -> 0 to 1	12.994 ps	17.548 ps	0.00691 Watts



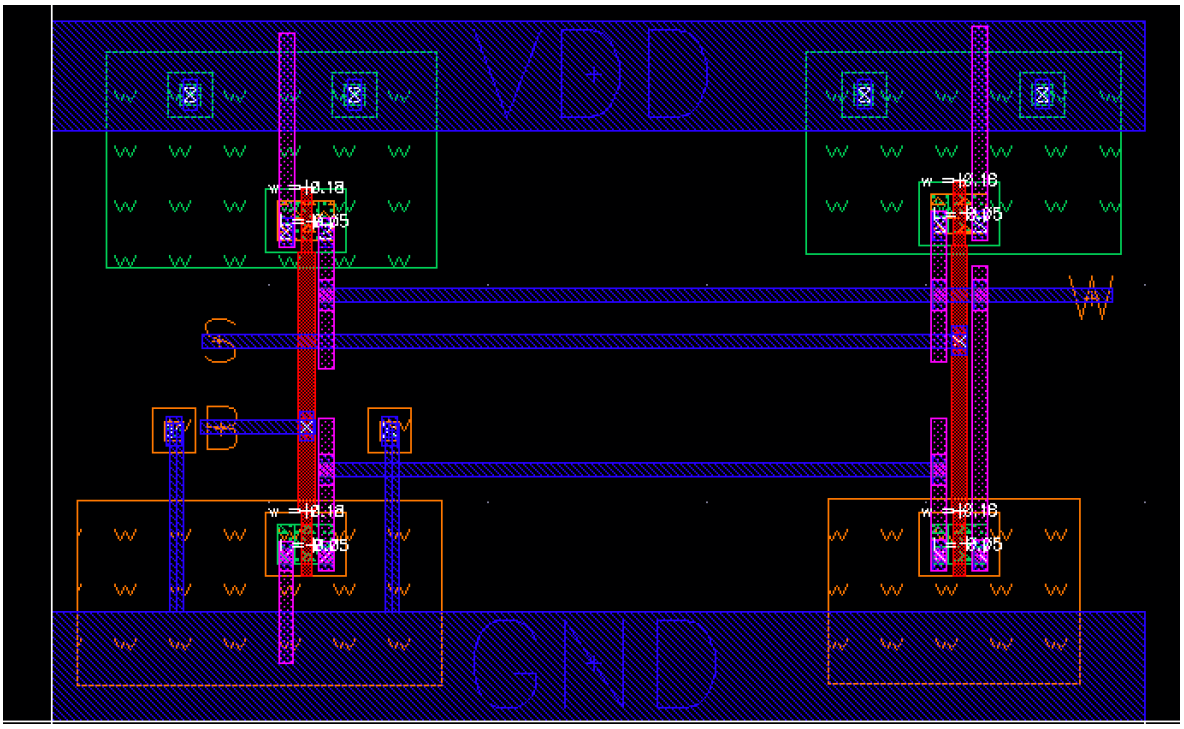




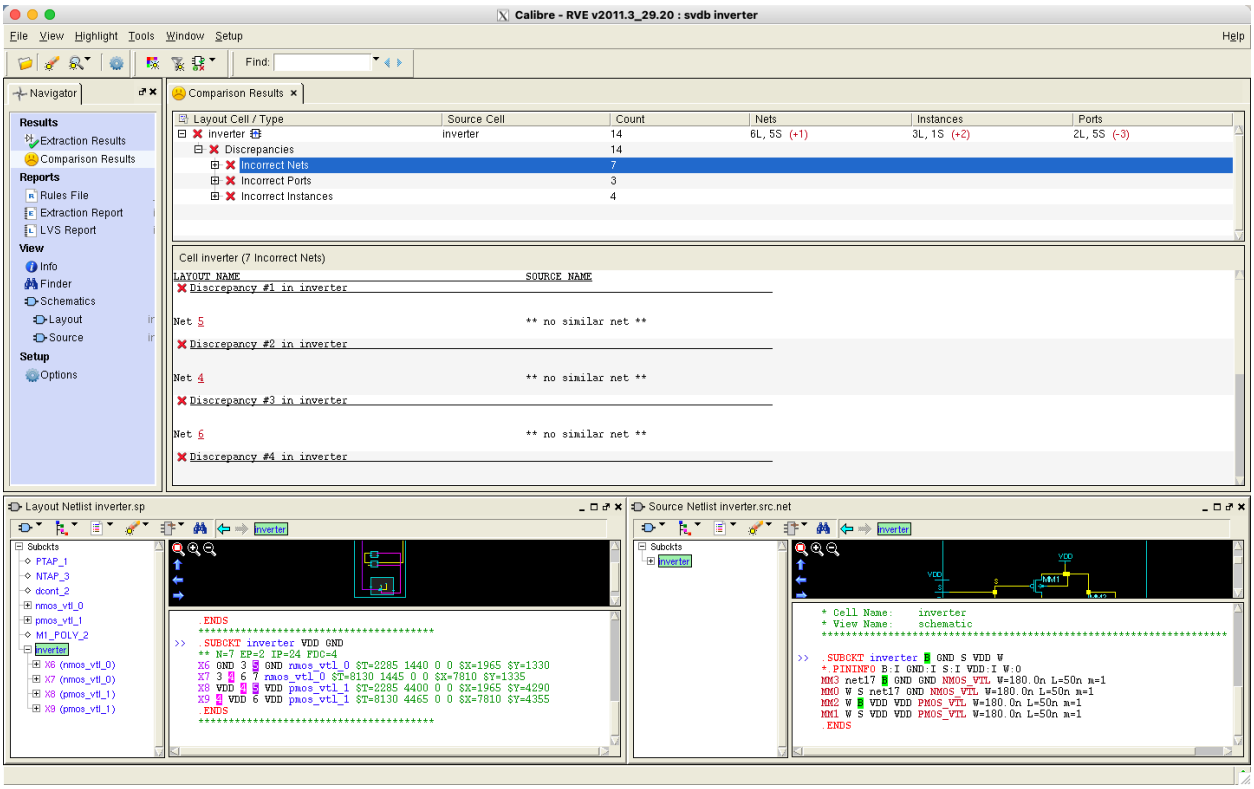


As the transistor increases in size, the delay it takes to charge and discharge increases. Additionally, it also consumes more power therefore the measured values for power in step 6 increased compared to the measured values in step 5 while the delays decreased.

Step 7.


VDD
S
D
GND


Topcell inverter, 0 Results (in 0 of 167 Checks)
Show All
Check / Cell
Check Well.1
Check Well.2
Check Well.4
Check Poly.1
Check Poly.2
Check Poly.3
Check Poly.4
Check Poly.5
Check Poly.6
Check Active.1
Check Active.2
Check Active.3
Check Active.4
Check Implant.1
Check Implant.2
Check Implant.3
Check Implant.4
Check Implant.6
Check Contact.1
Check Contact.2
Check Contact.3
Rule File Pathname: /home/ece558_2021/siddhantashr/_calibreDRC.rul_
Nwell and Pwell must not overlap



I realize I have errors that I still need to fix. I do not have time to fix them for this lab but I will fix it afterwards.