Siddhanta Shrestha

ECE 558 – Intro to VLSI Design, Lab 5 Report

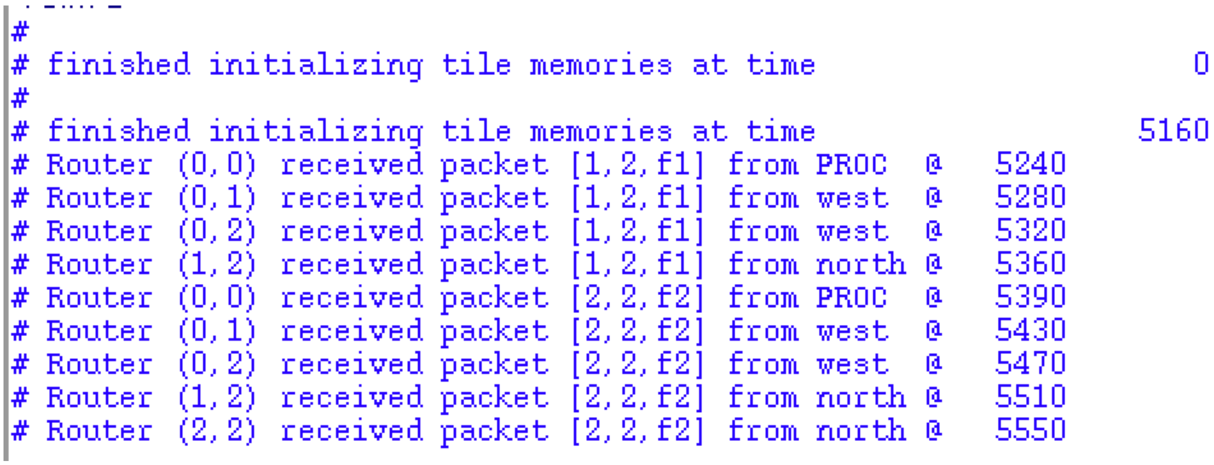
Part A. Analysis and Simulation

Step 1.

In mesh topology, packets hop from one tile to another only in X and Y directions. Therefore:

- A packet that would start at Tile [0,0] and hop right twice in the X direction to Tile [0,2]. It would then hop down twice in the Y direction to get to the destination Tile [2,2]
    - Tile [0,0] -> Tile [0,1] -> Tile [0,2] -> Tile [1,2] -> Tile [2,2]
- A packet that would start at Tile [2,2] would hop left once in the X direction to Tile [2,1]. Then it would hop up once in the Y direction to the destination Tile [1,1]

Step 2.



```
#
# finished initializing tile memories at time                        0
#
# finished initializing tile memories at time                     5160
# Router (0,0) received packet [1,2,f1] from PROC  @   5240
# Router (0,1) received packet [1,2,f1] from west  @   5280
# Router (0,2) received packet [1,2,f1] from west  @   5320
# Router (1,2) received packet [1,2,f1] from north @   5360
# Router (0,0) received packet [2,2,f2] from PROC  @   5390
# Router (0,1) received packet [2,2,f2] from west  @   5430
# Router (0,2) received packet [2,2,f2] from west  @   5470
# Router (1,2) received packet [2,2,f2] from north @   5510
# Router (2,2) received packet [2,2,f2] from north @   5550
```

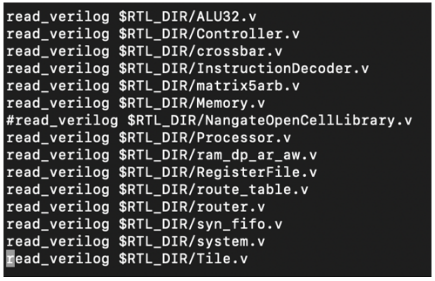
The Testbench.v file had a stop line that ended the program, thus by removing this line it allowed the simulation to be run

Part B. Synthesis

Step 3.

I imported the following files with the following edits:

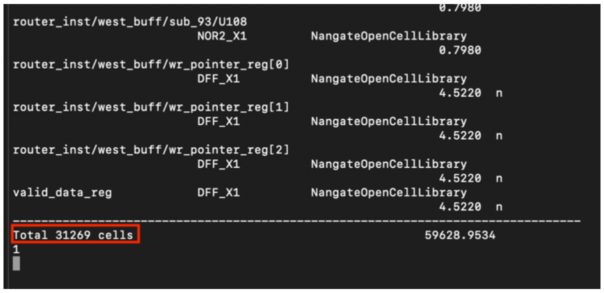
- ***setup.tcl***
    - In the *setup.tcl* file I set the clock name to *clk* because in the *system.v* file it references the clock as *clk*. I also set the modname to *Tile* because in this part we are only synthesizing a single tile.
- ***read.tcl***

  - In the *read.tcl* file, I added the following Verilog files from lab4 so that the synthesis could be conducted. The only Verilog file that was not added was the *Testbench.v* file since that is only for simulation thus not needed for synthesis.
    - 

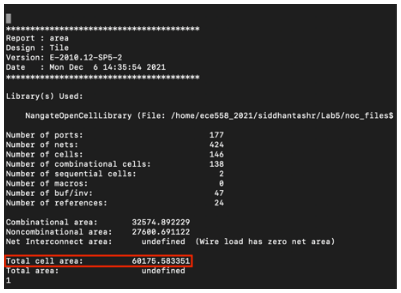
```
read_verilog $RTL_DIR/ALU32.v
read_verilog $RTL_DIR/Controller.v
read_verilog $RTL_DIR/crossbar.v
read_verilog $RTL_DIR/InstructionDecoder.v
read_verilog $RTL_DIR/matrix5arb.v
read_verilog $RTL_DIR/Memory.v
#read_verilog $RTL_DIR/NangateOpenCellLibrary.v
read_verilog $RTL_DIR/Processor.v
read_verilog $RTL_DIR/ram_dp_ar_aw.v
read_verilog $RTL_DIR/RegisterFile.v
read_verilog $RTL_DIR/route_table.v
read_verilog $RTL_DIR/router.v
read_verilog $RTL_DIR/syn_fifo.v
read_verilog $RTL_DIR/system.v
read_verilog $RTL_DIR/Tile.v
```

- ***Constraints.tcl***
  - In the *Constraints.*tcl file I set the *CLK_PER* to 10ns as directed in the lab. Although not a necessary step, it did speed up the synthesis process
- ***CompileAnalyze.tcl***
  - In the CompileAnalyze.tcl I added the line *ungroup -all -flatten* beneath the line *compile -only_design_rule -incremental* so that it would ungroup everything into individual parts (removing hierarchy) and flattened out the tile.

Within the synthesized design there are 31269 cell instances, and the total cell area is 60175.583351 nm^2. These numbers were observed by looking through the *cell_report_final.rpt* and area.rpt files respectively.

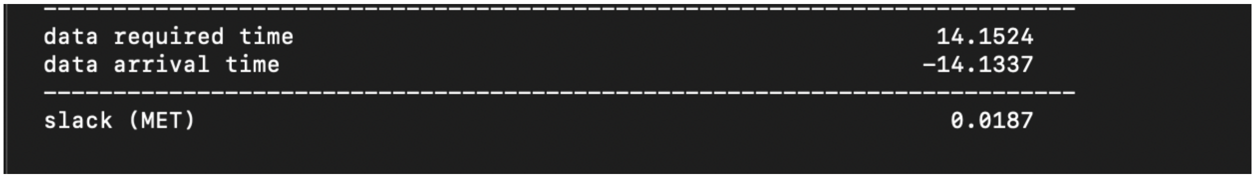


```
                                                  0.7980
router_inst/west_buff/sub_93/U108
                         NOR2_X1         NangateOpenCellLibrary
                                                  0.7980
router_inst/west_buff/wr_pointer_reg[0]
                         DFF_X1          NangateOpenCellLibrary
                                                  4.5220  n
router_inst/west_buff/wr_pointer_reg[1]
                         DFF_X1          NangateOpenCellLibrary
                                                  4.5220  n
router_inst/west_buff/wr_pointer_reg[2]
                         DFF_X1          NangateOpenCellLibrary
                                                  4.5220  n
valid_data_reg           DFF_X1          NangateOpenCellLibrary
                                                  4.5220  n
--------------------------------------------------------------------------------
Total 31269 cells                                59628.9534
1
```



```
****************************************
Report : area
Design : Tile
Version: E-2010.12-SP5-2
Date   : Mon Dec  6 14:35:54 2021
****************************************

Library(s) Used:

    NangateOpenCellLibrary (File: /home/ece558_2021/siddhantashr/Lab5/noc_files$

Number of ports:                          177
Number of nets:                           424
Number of cells:                          146
Number of combinational cells:            138
Number of sequential cells:                 2
Number of macros:                           0
Number of buf/inv:                         47
Number of references:                      24

Combinational area:       32574.892229
Noncombinational area:    27600.691122
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:          60175.583351
Total area:                 undefined
1
```

The maximum clock frequency is calculated by taking 1/minimum period. 1/(14.4 ns * 10^{-9}) = 69.44 Mhz

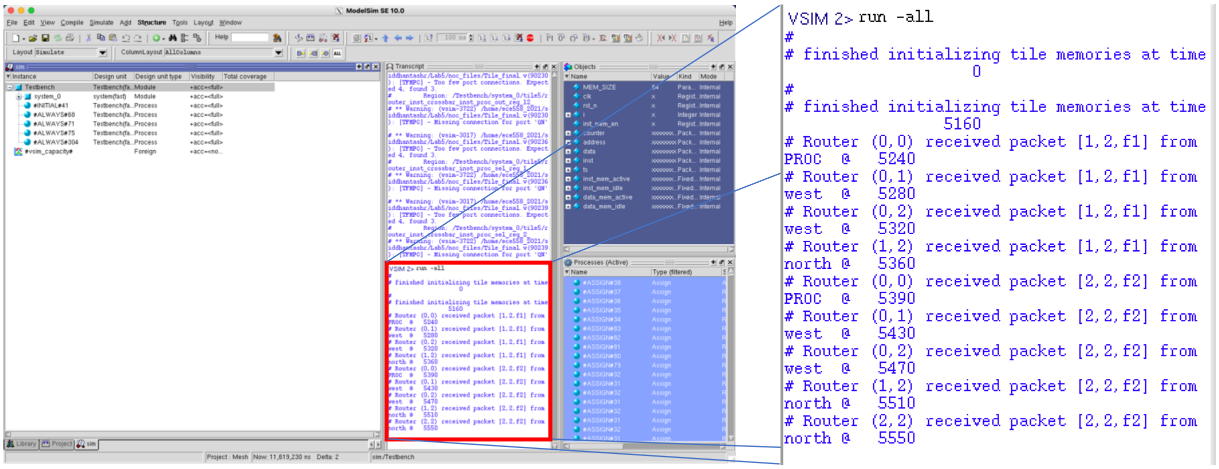


```
-----------------------------------------------------------------------------
data required time                                               14.1524
data arrival time                                               -14.1337
-----------------------------------------------------------------------------
slack (MET)                                                        0.0187
```

The critical path (in terms of the number of logic gates) is the path with the largest number of gates and hence the longest time delay.

Step 4: Post-Synthesis Simulation

In the *System.v* file (which I duplicated and renamed *modsystem.v*) I changed the type for tile5 from **Tile** to the module name from *Tile_final.v* (which I had changed to **Tilefinal)**


ModelSim SE 10.0
File Edit View Compile Simulate Add Structure Tools Layout Window Help
Transcript
Objects
Processes (Active)

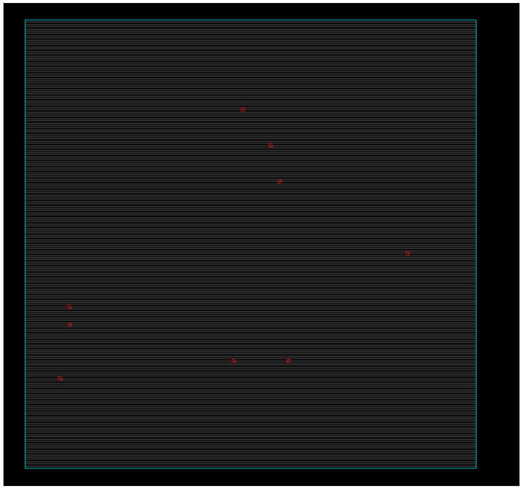
```
iddhantashr/Lab5/noc_files/Tile_final.v(90230
): [TFMPC] - Too few port connections. Expect
ed 4, found 3.
#         Region: /Testbench/system_0/tile5/r
outer_inst_crossbar_inst_proc_out_reg_12
# ** Warning: (vsim-3722) /home/ece558_2021/s
iddhantashr/Lab5/noc_files/Tile_final.v(90230
): [TFMPC] - Missing connection for port 'QN'
.
# ** Warning: (vsim-3017) /home/ece558_2021/s
iddhantashr/Lab5/noc_files/Tile_final.v(90236
): [TFMPC] - Too few port connections. Expect
ed 4, found 3.
#         Region: /Testbench/system_0/tile5/r
outer_inst_crossbar_inst_proc_sel_reg_1
# ** Warning: (vsim-3722) /home/ece558_2021/s
iddhantashr/Lab5/noc_files/Tile_final.v(90236
): [TFMPC] - Missing connection for port 'QN'
.
# ** Warning: (vsim-3017) /home/ece558_2021/s
iddhantashr/Lab5/noc_files/Tile_final.v(90239
): [TFMPC] - Too few port connections. Expect
ed 4, found 3.
#         Region: /Testbench/system_0/tile5/r
outer_inst_crossbar_inst_proc_sel_reg_2
# ** Warning: (vsim-3722) /home/ece558_2021/s
iddhantashr/Lab5/noc_files/Tile_final.v(90239
): [TFMPC] - Missing connection for port 'QN'
```

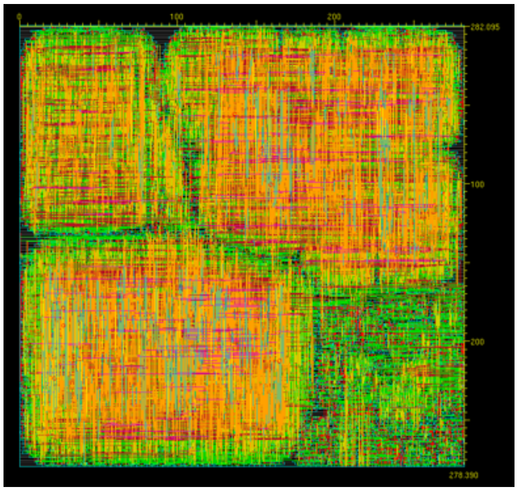
```
VSIM 2> run -all
#
# finished initializing tile memories at time
                         0
#
# finished initializing tile memories at time
                     5160
# Router (0,0) received packet [1,2,f1] from
PROC @   5240
# Router (0,1) received packet [1,2,f1] from
west  @   5280
# Router (0,2) received packet [1,2,f1] from
west  @   5320
# Router (1,2) received packet [1,2,f1] from
north @   5360
# Router (0,0) received packet [2,2,f2] from
PROC  @   5390
# Router (0,1) received packet [2,2,f2] from
west  @   5430
# Router (0,2) received packet [2,2,f2] from
west  @   5470
# Router (1,2) received packet [2,2,f2] from
north @   5510
# Router (2,2) received packet [2,2,f2] from
north @   5550
```

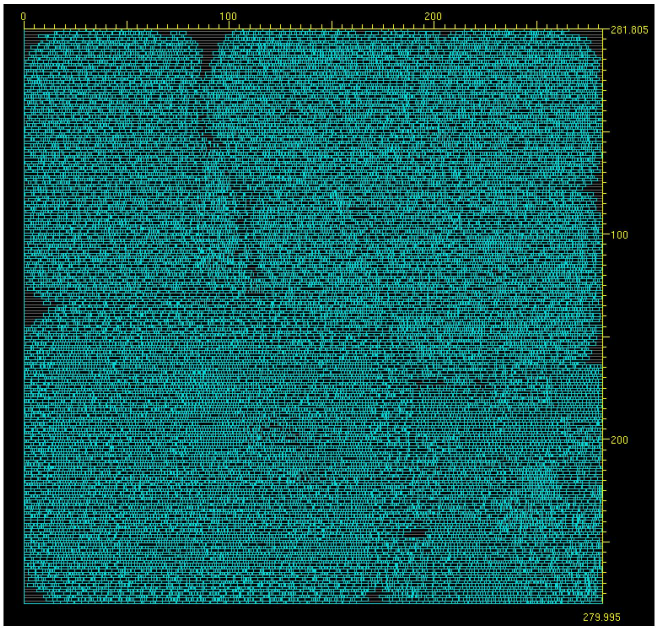
The output for step 4 (post-synthesis) is the same as the output from step 2 (pre-synthesis) meaning the path from post matches the path from the pre. This indicates that the post synthesis was conducted correctly. The packet goes *(Y,X):* east twice from *(0,0)* to *(0,1)* to *(0,2)* and then south *(1,2)*. The packet also goes *(Y,X):* east twice from *(0,0)* to *(0,1)* to *(0,2)* and then south twice from *(0,2)* to *(1,2) to (2,2)*.

Part C: Place and Route

Step 5: Placement

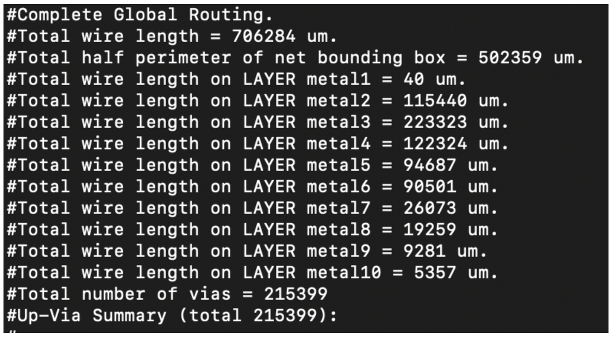






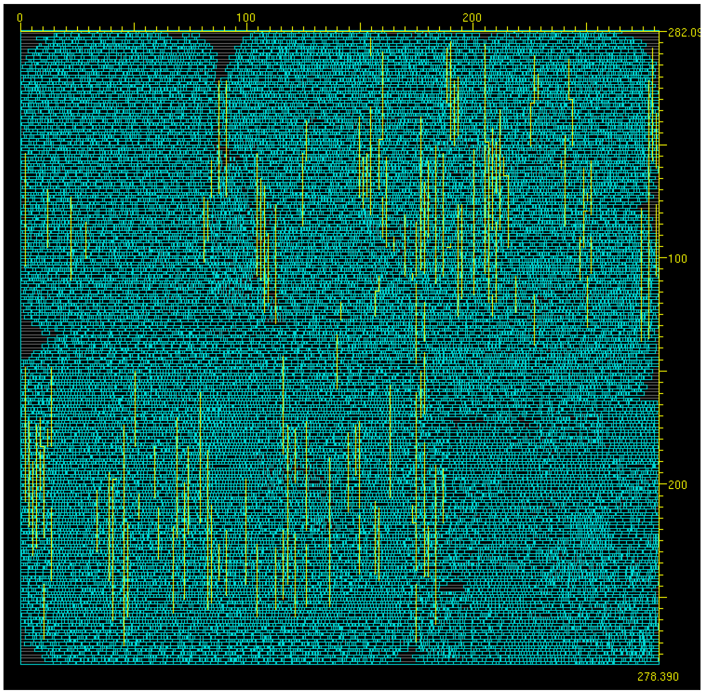
The dimension of the design is 281.805 x 279.995 or 78,903.990975 nm^2. This is larger than the total cell area found than 60,175.583351 nm^2. This is because the synthesized tile was large thus would explain the difference between the two dimensions.

Step 6: Detailed Routing

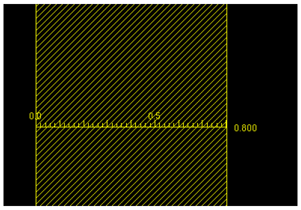


```
#Complete Global Routing.
#Total wire length = 706284 um.
#Total half perimeter of net bounding box = 502359 um.
#Total wire length on LAYER metal1 = 40 um.
#Total wire length on LAYER metal2 = 115440 um.
#Total wire length on LAYER metal3 = 223323 um.
#Total wire length on LAYER metal4 = 122324 um.
#Total wire length on LAYER metal5 = 94687 um.
#Total wire length on LAYER metal6 = 90501 um.
#Total wire length on LAYER metal7 = 26073 um.
#Total wire length on LAYER metal8 = 19259 um.
#Total wire length on LAYER metal9 = 9281 um.
#Total wire length on LAYER metal10 = 5357 um.
#Total number of vias = 215399
#Up-Via Summary (total 215399):
```

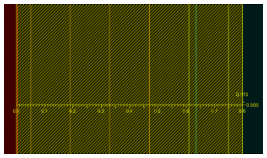
There are a total of 10 metals, where metal 3 has the most amount of wire length followed by metal 4 then metal 2. This is reasonable because M1 would be the thinnest due to it being used within-cell routing and thus the length wouldn't be long. Metal 2, 3 and 4 are all longer because although they are thicker compared to M1, they are not as thick as the top layers and because of the length needed to route between cells it would make sense that the lengths are longer for these metals compared to the metals in the upper level



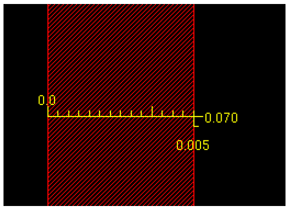
Here is the uppermost metal *(metal 10)* with all other wirings turned off



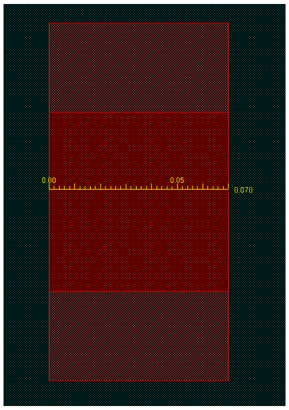
Metal 10: 0.8



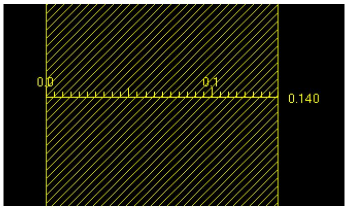
Via Metal 10: 0.8



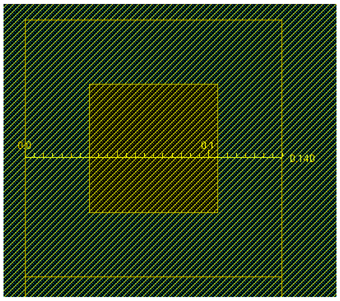
Metal 2: 0.07



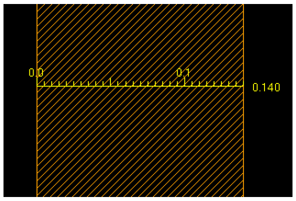
Via Metal 2: 0.07



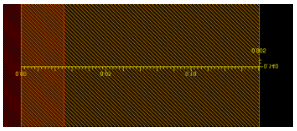
Metal 4: 0.140



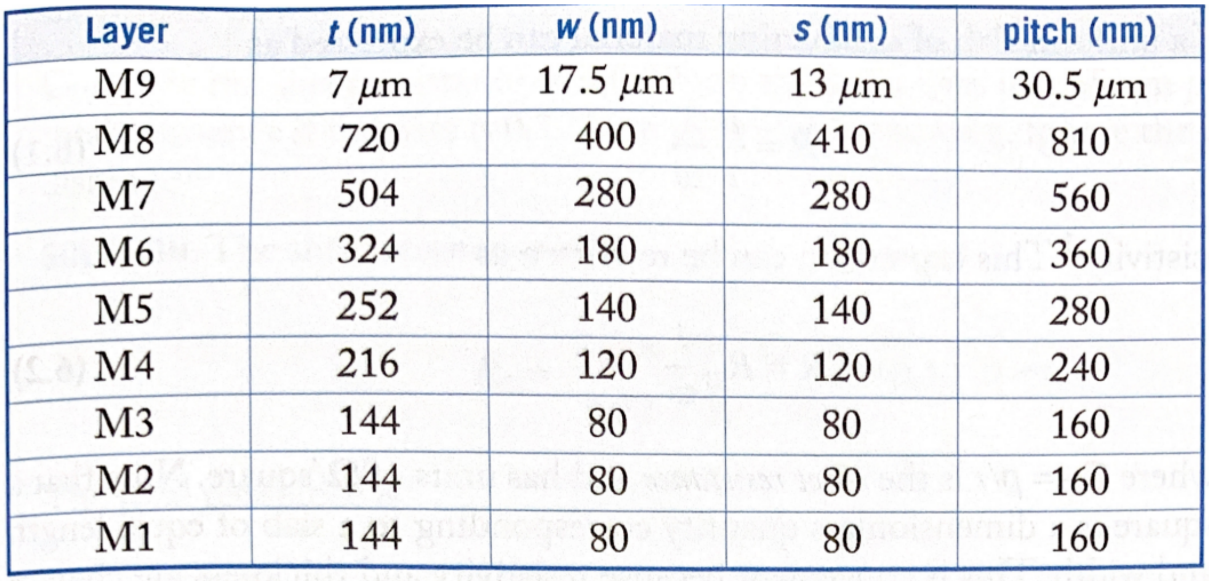
Via Metal 4: 0.140



Metal 6: 0.140



Via Metal 6: 0.140



Layer	*t* (nm)	*w* (nm)	*s* (nm)	pitch (nm)
M9	7 μm	17.5 μm	13 μm	30.5 μm
M8	720	400	410	810
M7	504	280	280	560
M6	324	180	180	360
M5	252	140	140	280
M4	216	120	120	240
M3	144	80	80	160
M2	144	80	80	160
M1	144	80	80	160

The widths do match my expectations from the lectures since in lecture we covered Intel's 45 nm metal stack *(from the table above)* where the widths of the metals are close to those observed in this lab. Thus, it makes sense that the difference is due to the different technologies.

The width of the 1mm chip/0.281805μm would fit 3.571 tiles or 3 tiles. Therefore, the chip would fit a total of 9.