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ECE 558 – Intro to VLSI Design, Lab 4 Report

Step A1.

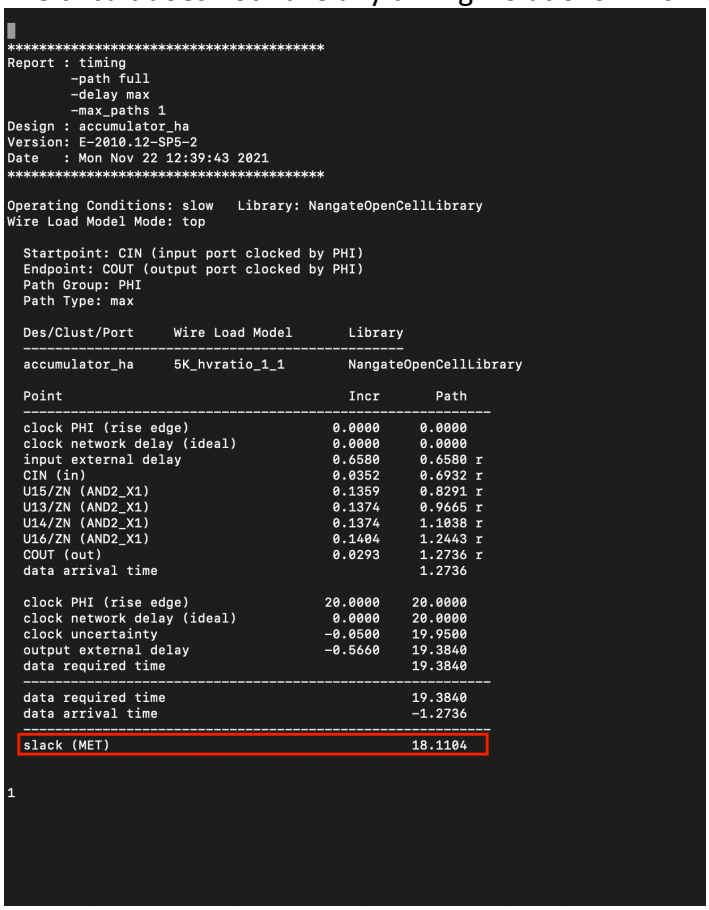
3a. The statement “set modname” is used to set a value for the variable *modname* (or module name) which is used within the file. This file provides the standard-cell netlist which is placed and routed.

3b. The specification of the clock name is necessary because the half adder requires the same specific clock as the one from lab 3. Additionally, *Constraints.tcl* references the clocks name

5a. To achieve the optimal area, the area is constrained to the minimum area. As a result, the max area is set to 0

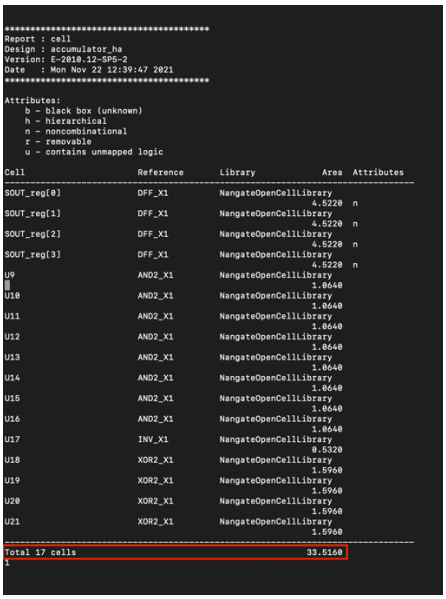
5b. In the Constraints, the period of the clock is set to 20 ns with a 50% duty cycle. It also includes a skew of 50 ps

7a. The circuit does not have any timing violations which is indicated by the positive slack value.

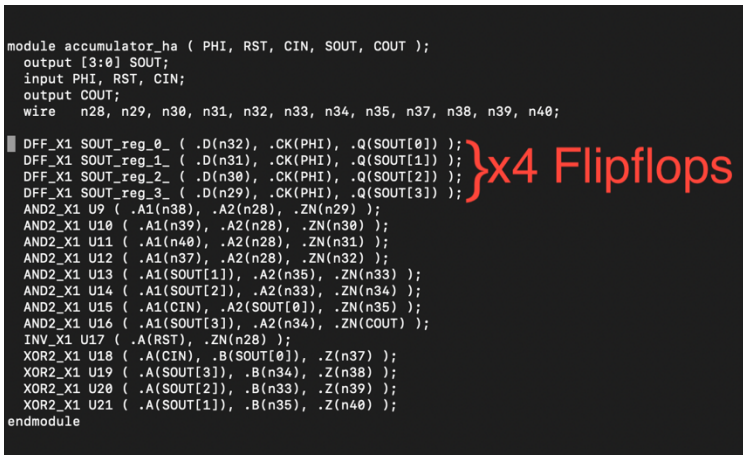


```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : accumulator_ha
Version: E-2010.12-SP5-2
Date   : Mon Nov 22 12:39:43 2021
****************************************

Operating Conditions: slow   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: CIN (input port clocked by PHI)
  Endpoint: COUT (output port clocked by PHI)
  Path Group: PHI
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  accumulator_ha     5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock PHI (rise edge)                   0.0000     0.0000
  clock network delay (ideal)             0.0000     0.0000
  input external delay                    0.6580     0.6580 r
  CIN (in)                                0.0352     0.6932 r
  U15/ZN (AND2_X1)                        0.1359     0.8291 r
  U13/ZN (AND2_X1)                        0.1374     0.9665 r
  U14/ZN (AND2_X1)                        0.1374     1.1038 r
  U16/ZN (AND2_X1)                        0.1404     1.2443 r
  COUT (out)                              0.0293     1.2736 r
  data arrival time                                  1.2736

  clock PHI (rise edge)                  20.0000    20.0000
  clock network delay (ideal)             0.0000    20.0000
  clock uncertainty                      -0.0500    19.9500
  output external delay                  -0.5660    19.3840
  data required time                                19.3840
  -----------------------------------------------------------
  data required time                                19.3840
  data arrival time                                 -1.2736
  -----------------------------------------------------------
  slack (MET)                                       18.1104


1
```

7b. The estimated area is 33.516 nm and utilizes 4 flip flops



```
****************************************
Report : cell
Design : accumulator_ha
Version: E-2010.12-SP5-2
Date   : Mon Nov 22 12:39:47 2021
****************************************

Attributes:
    b - black box (unknown)
    h - hierarchical
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library             Area  Attributes
--------------------------------------------------------------------------------
SOUT_reg[0]             DFF_X1          NangateOpenCellLibrary
                                                            4.5220  n
SOUT_reg[1]             DFF_X1          NangateOpenCellLibrary
                                                            4.5220  n
SOUT_reg[2]             DFF_X1          NangateOpenCellLibrary
                                                            4.5220  n
SOUT_reg[3]             DFF_X1          NangateOpenCellLibrary
                                                            4.5220  n
U9                      AND2_X1         NangateOpenCellLibrary
                                                            1.0640
U10                     AND2_X1         NangateOpenCellLibrary
                                                            1.0640
U11                     AND2_X1         NangateOpenCellLibrary
                                                            1.0640
U12                     AND2_X1         NangateOpenCellLibrary
                                                            1.0640
U13                     AND2_X1         NangateOpenCellLibrary
                                                            1.0640
U14                     AND2_X1         NangateOpenCellLibrary
                                                            1.0640
U15                     AND2_X1         NangateOpenCellLibrary
                                                            1.0640
U16                     AND2_X1         NangateOpenCellLibrary
                                                            1.0640
U17                     INV_X1          NangateOpenCellLibrary
                                                            0.5320
U18                     XOR2_X1         NangateOpenCellLibrary
                                                            1.5960
U19                     XOR2_X1         NangateOpenCellLibrary
                                                            1.5960
U20                     XOR2_X1         NangateOpenCellLibrary
                                                            1.5960
U21                     XOR2_X1         NangateOpenCellLibrary
                                                            1.5960
--------------------------------------------------------------------------------
Total 17 cells                                             33.6160
1
```



```
module accumulator_ha ( PHI, RST, CIN, SOUT, COUT );
  output [3:0] SOUT;
  input PHI, RST, CIN;
  output COUT;
  wire   n28, n29, n30, n31, n32, n33, n34, n35, n37, n38, n39, n40;

  DFF_X1 SOUT_reg_0_ ( .D(n32), .CK(PHI), .Q(SOUT[0]) );
  DFF_X1 SOUT_reg_1_ ( .D(n31), .CK(PHI), .Q(SOUT[1]) );
  DFF_X1 SOUT_reg_2_ ( .D(n30), .CK(PHI), .Q(SOUT[2]) );
  DFF_X1 SOUT_reg_3_ ( .D(n29), .CK(PHI), .Q(SOUT[3]) );
  AND2_X1 U9 ( .A1(n38), .A2(n28), .ZN(n29) );
  AND2_X1 U10 ( .A1(n39), .A2(n28), .ZN(n30) );
  AND2_X1 U11 ( .A1(n40), .A2(n28), .ZN(n31) );
  AND2_X1 U12 ( .A1(n37), .A2(n28), .ZN(n32) );
  AND2_X1 U13 ( .A1(SOUT[1]), .A2(n35), .ZN(n33) );
  AND2_X1 U14 ( .A1(SOUT[2]), .A2(n33), .ZN(n34) );
  AND2_X1 U15 ( .A1(CIN), .A2(SOUT[0]), .ZN(n35) );
  AND2_X1 U16 ( .A1(SOUT[3]), .A2(n34), .ZN(COUT) );
  INV_X1 U17 ( .A(RST), .ZN(n28) );
  XOR2_X1 U18 ( .A(CIN), .B(SOUT[0]), .Z(n37) );
  XOR2_X1 U19 ( .A(SOUT[3]), .B(n34), .Z(n38) );
  XOR2_X1 U20 ( .A(SOUT[2]), .B(n33), .Z(n39) );
  XOR2_X1 U21 ( .A(SOUT[1]), .B(n35), .Z(n40) );
endmodule
```


7c. The netlist includes:

- 4 DFlip Flops with
  - inputs
    - D (Wires n29-n32), Clock (Phi)
  - outputs
    - Q (Sout for each accumulator)
- 8 And gates with
  - inputs
    - A1(Wires n37-n40, SOUT, CIN, SOUT[1-3]), A2(Wire n28, n33, n35, SOUT[0] , n34)
  - outputs
    - ZN(Wires n29-n35, COUT)
- Inverter with
  - input
    - A(RST)
  - output
    - ZN(Wires n28)
- XOR with
  - input
    - A(CIN, SOUT[1-3]), B(SOUT[0], n33-n35)
  - output
    - Z(n37-n40)

These primitives are part of the accumulator_ha library

8a. Max Frequency = 1/Max Period = 1/ 1.4497 = 0.68979788921

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : accumulator_ha
Version: E-2010.12-SP5-2
Date   : Mon Nov 22 17:02:50 2021
****************************************

Operating Conditions: slow   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: CIN (input port clocked by PHI)
  Endpoint: COUT (output port clocked by PHI)
  Path Group: PHI
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  accumulator_ha     5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock PHI (rise edge)                    0.0000     0.0000
  clock network delay (ideal)              0.0000     0.0000
  input external delay                     0.6580     0.6580 r
  CIN (in)                                 0.0288     0.6868 r
  U19/ZN (AND2_X2)                         0.1174     0.8042 r
  COUT (out)                               0.0293     0.8336 r
  data arrival time                                   0.8336

  clock PHI (rise edge)                    1.4497     1.4497
  clock network delay (ideal)              0.0000     1.4497
  clock uncertainty                       -0.0500     1.3997
  output external delay                   -0.5660     0.8337
  data required time                                  0.8337
  -----------------------------------------------------------
  data required time                                  0.8337
  data arrival time                                  -0.8336
  -----------------------------------------------------------
  slack (MET)                                         0.0001


1
```

8b. Lower frequency = 1/20 = 0.05

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : accumulator_ha
Version: E-2010.12-SP5-2
Date   : Mon Nov 22 17:45:21 2021
****************************************

Operating Conditions: slow   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: CIN (input port clocked by PHI)
  Endpoint: COUT (output port clocked by PHI)
  Path Group: PHI
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  accumulator_ha     5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock PHI (rise edge)                   0.0000     0.0000
  clock network delay (ideal)             0.0000     0.0000
  input external delay                    0.6580     0.6580 r
  CIN (in)                                0.0352     0.6932 r
  U15/ZN (AND2_X1)                        0.1359     0.8291 r
  U13/ZN (AND2_X1)                        0.1374     0.9665 r
  U14/ZN (AND2_X1)                        0.1374     1.1038 r
  U16/ZN (AND2_X1)                        0.1404     1.2443 r
  COUT (out)                              0.0293     1.2736 r
  data arrival time                                  1.2736

  clock PHI (rise edge)                  20.0000    20.0000
  clock network delay (ideal)             0.0000    20.0000
  clock uncertainty                      -0.0500    19.9500
  output external delay                  -0.5660    19.3840
  data required time                                19.3840
  -----------------------------------------------------------
  data required time                                19.3840
  data arrival time                                 -1.2736
  -----------------------------------------------------------
  slack (MET)                                       18.1104


1
```

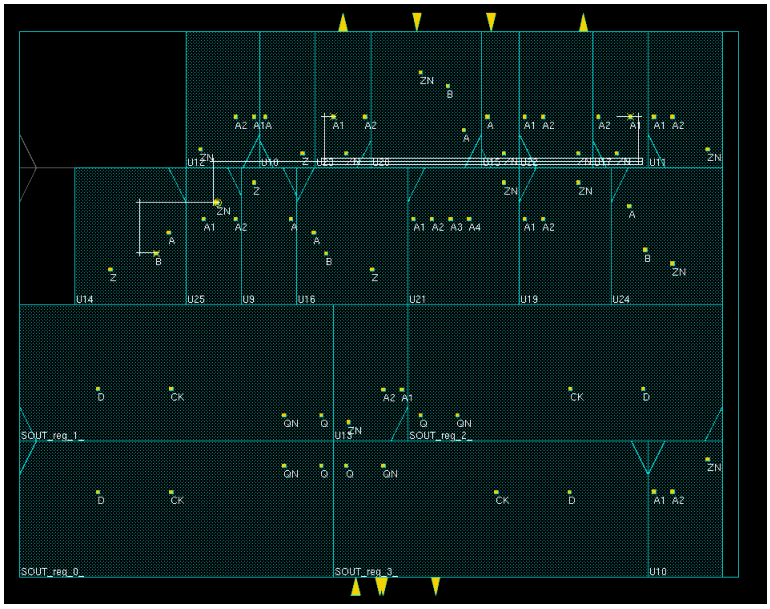
8c. The area of the Max frequency is 37.24 nm with 21 total cells while the area of the Lower frequency is 33.516 nm with 17 total cells. The lower frequency area includes 4 D Flipflops, 8 And gates, 1 Inverter, 4 XOR gates. The Max frequency also includes 4 D-Flipflops, 6 AND Gate, 1 Inverter but also includes XNOR, CLKBuffer

```
                                                    1.0640
U11                  AND2_X1        NangateOpenCellLibrary
                                                    1.0640
U12                  AND2_X1        NangateOpenCellLibrary
                                                    1.0640
U13                  AND2_X1        NangateOpenCellLibrary
                                                    1.0640
U14                  XOR2_X1        NangateOpenCellLibrary
                                                    1.5960
U15                  INV_X1         NangateOpenCellLibrary
                                                    0.5320
U16                  XOR2_X1        NangateOpenCellLibrary
                                                    1.5960
U17                  NOR2_X1        NangateOpenCellLibrary
                                                    0.7980
U18                  CLKBUF_X1      NangateOpenCellLibrary
                                                    0.7980
U19                  AND2_X2        NangateOpenCellLibrary
                                                    1.3300
U20                  XNOR2_X1       NangateOpenCellLibrary
                                                    1.5960
U21                  AND4_X1        NangateOpenCellLibrary
                                                    1.5960
U22                  OR2_X1         NangateOpenCellLibrary
                                                    1.0640
U23                  NOR2_X1        NangateOpenCellLibrary
                                                    0.7980
U24                  XNOR2_X1       NangateOpenCellLibrary
                                                    1.5960
U25                  NAND2_X1       NangateOpenCellLibrary
                                                    0.7980
-------------------------------------------------------------------------------
Total 21 cells                                     37.2400
1
```

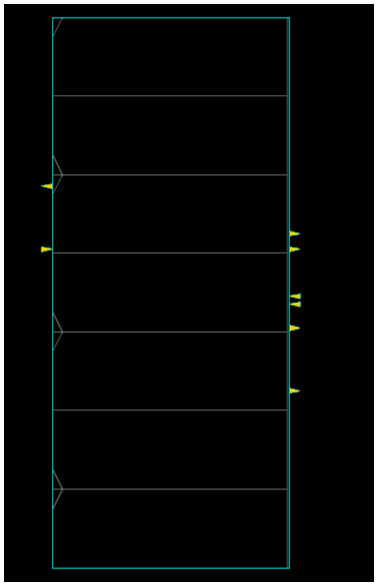
```
****************************************
Report : cell
Design : accumulator_ha
Version: E-2010.12-SP5-2
Date   : Mon Nov 22 17:45:25 2021
****************************************

Attributes:
    b - black box (unknown)
    h - hierarchical
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                 Reference      Library              Area  Attributes
-------------------------------------------------------------------------------
DOUT_reg[0]          DFF_X1         NangateOpenCellLibrary
                                                        4.5320  n
DOUT_reg[1]          DFF_X1         NangateOpenCellLibrary
                                                        4.5320  n
DOUT_reg[2]          DFF_X1         NangateOpenCellLibrary
                                                        4.5320  n
DOUT_reg[3]          DFF_X1         NangateOpenCellLibrary
                                                        4.5320  n
U9                   AND2_X1        NangateOpenCellLibrary
                                                        1.0640
U10                  AND2_X1        NangateOpenCellLibrary
                                                        1.0640
U11                  AND2_X1        NangateOpenCellLibrary
                                                        1.0640
U12                  AND2_X1        NangateOpenCellLibrary
                                                        1.0640
U13                  AND2_X1        NangateOpenCellLibrary
                                                        1.0640
U14                  AND2_X1        NangateOpenCellLibrary
                                                        1.0640
U15                  AND2_X1        NangateOpenCellLibrary
                                                        1.0640
U16                  AND2_X1        NangateOpenCellLibrary
                                                        1.0640
U17                  INV_X1         NangateOpenCellLibrary
                                                        0.5320
U18                  XOR2_X1        NangateOpenCellLibrary
                                                        1.5960
U19                  XOR2_X1        NangateOpenCellLibrary
                                                        1.5960
U20                  XOR2_X1        NangateOpenCellLibrary
                                                        1.5960
U21                  XOR2_X1        NangateOpenCellLibrary
                                                        1.5960
-------------------------------------------------------------------------------
Total 17 cells                                         33.5160
```

Step A2.

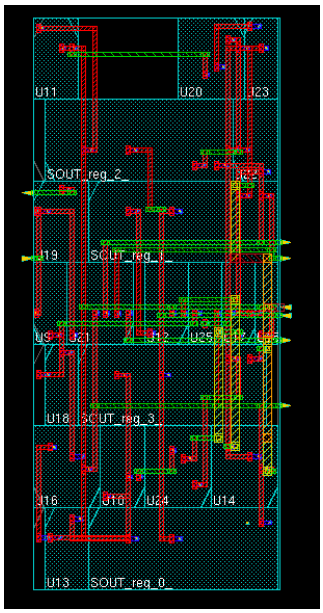
12a.



13a.



13b.



13.c

Std. Cell

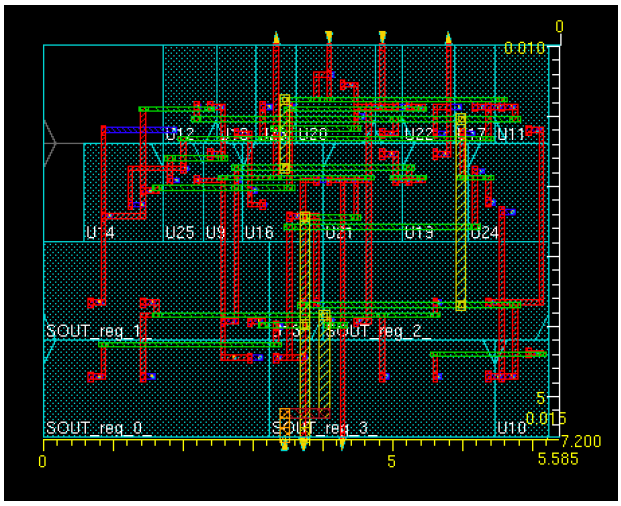
Step B1.

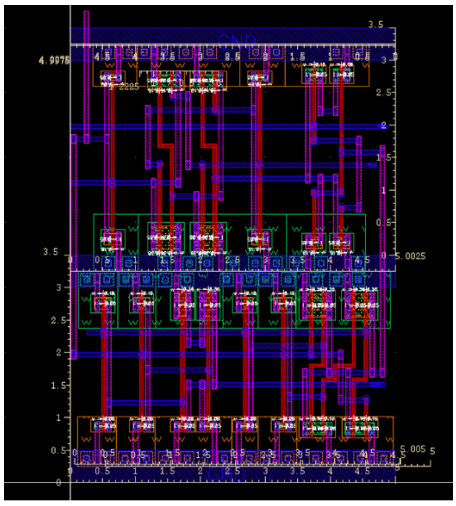
B1a.

	Lab 3	Lab 4
Frequency	0.68979788921	
Power		
Area	140	140
Metal Layer	Metal 1, Metal 2	Metal 1, Metal 2, Metal 3, Metal 4, Metal 5, Metal 6,
Height	Cell Height is 3.5	Cell Height is 1.4

B1b.

B2a.



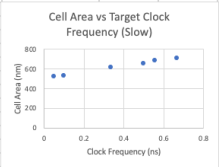


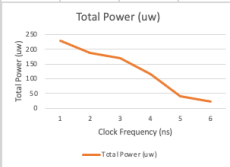
Step C1.

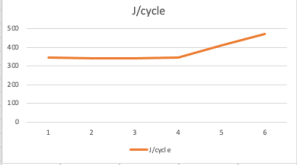
C1a. Within the *constraints.tcl* file the CLK_PER value was changed to each of the target clock periods. Within the *CompileAnalyze.tcl* file "*report_timing > timing_max_slow.rpt*" "*report_area > area_max_slow.rpt*" "*report_power > power_max_slow.rpt*" "*report_timing > timing_max_slow.rpt*" "*report_timing > timing_max_fast.rpt*" "*report_area > area_max_fast.rpt*" "*report_power > power_max_fast.rpt*" "*report_timing > timing_max_fast.rpt*" were added to both the slowest path and fast path respectively.

Slow

Clock Frequency (ns)	0.6666667	0.5555556	0.5	0.3333333	0.1	0.05
Cell Area (nm)	712.34799	687.60999	652.498	616.322	536.25599	528.27599
Dynamic Power (uw)	221.4529	180.8933	161.8619	107.7809	34.6825	17.3205
Static Power (uw)	9.0073	7.5447	7.5893	6.8511	6.2057	6.1669







Fast

Clock Frequency (ns)	0.666667	0.555556	0.5	0.333333	0.1	0.05
Cell Area (nm)	704.102	687.61	652.498	616.588	536.522	528.542
Dynamic Power (uw)	385.8888	315.4605	282.3184	187.7519	60.2967	30.1062
Static Power (uw)	49.6437	40.9933	40.7808	35.3688	33.4455	33.0757