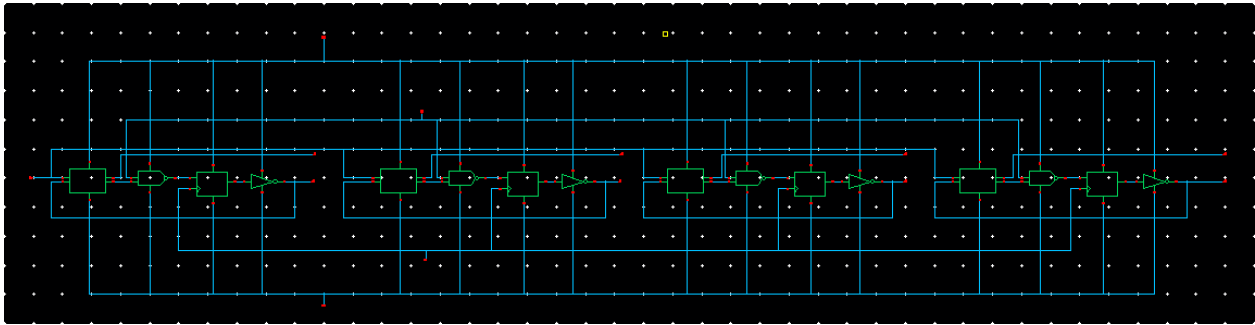


Siddhanta Shrestha

ECE 558 – Intro to VLSI Design, Lab 3 Report

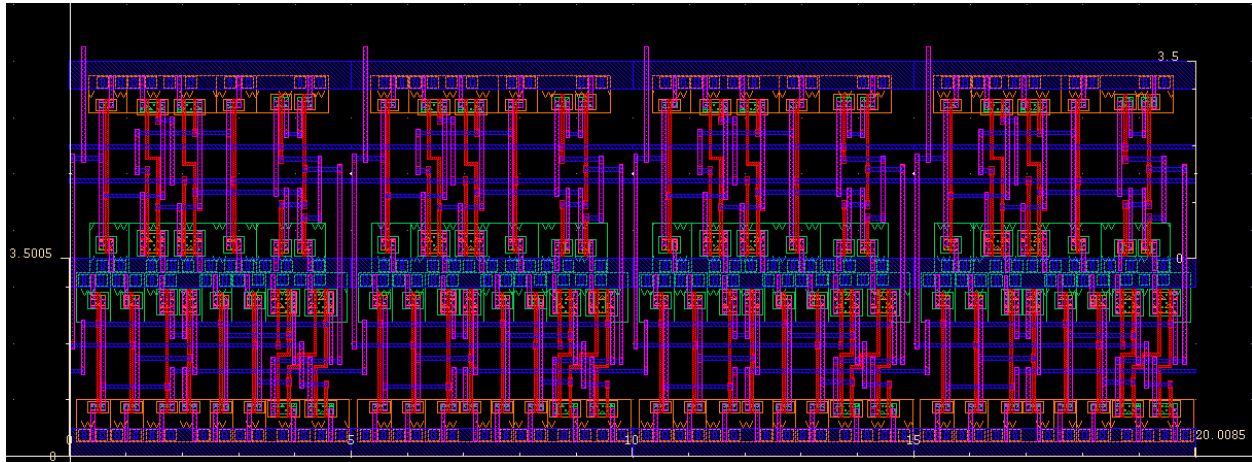
Step 1:



Step 2:

CLK	RST	CIN	D3	D2	D1	D0	SOUT3	SOUT2	SOUT1	SOUT0	Q3	Q2	Q1	Q0
0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	1	1	1	1	1	1	0	0	0	0	1	1	1	1
0	1	0	1	1	1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
1	1	0	0	0	0	0	1	1	1	1	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	0	0	0	0
1	1	0	0	0	0	0	1	1	1	1	0	0	0	0
0	1	0	0	0	0	0	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
1	1	0	0	0	0	0	1	1	1	1	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

Step 3:



There were several changes that needed to be made to the bitslice layout from Lab 2. The First being the adjustment of CIN. Because the COUT of the half adder was the CIN to the next accumulator, there needed to be an adjustment so that the layout reflected this. Thus metal 2 was used to bring down the input for CIN. In addition to this, the labels for the inputs/outputs also needed to be adjusted so that it reflected the labels from the bitslice schematic.

Step 4:

Topcell Bitslice, 0 Results (in 0 of 167 Checks) Show All

Check / Cell	F
Check Well.1	0
Check Well.2	0
Check Well.4	0
Check Poly.1	0
Check Poly.2	0
Check Poly.3	0
Check Poly.4	0
Check Poly.5	0
Check Poly.6	0
Check Active.1	0
Check Active.2	0
Check Active.3	0
Check Active.4	0
Check Implant.1	0
Check Implant.2	0
Check Implant.3	0
Check Implant.4	0
Check Implant.6	0
Check Contact.1	0
Check Contact.2	0
Check Contact.3	0
Check Contact.4	0
Check Contact.5	0
Check Contact.6	0
Check Metal.1	0
Check Metal.2	0
Check Metal.3	0
Check Metal.4	0

Rule File Pathname: /home/ee558_0201/siddhantashr/calibreDRG_rul_

Well and Pwell must not overlap

1 Check Well.1, 0 Cells: 0 Results

Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
Bitslice	Bitslice	41L, 41S	44L, 44S	10L, 10S

Cell Bitslice Summary (Clean)

CELL COMPARISON RESULTS (TOP LEVEL)

LAYOUT CELL NAME: Bitslice
SOURCE CELL NAME: Bitslice

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	10	10	
Nets:	89	89	
Instances:	72	72	MN (4 pins)
	72	72	MP (4 pins)
Total Inst:	144	144	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

Layout	Source	Component Type

Step 5:

