HEART2017 Program

DAY-1 : June 7

8:30 - 9:00 **Registration**

9:00 - 9:10 **Opening**

9:10 - 10:10 **Invited Keynote Lecture 1** (Chair: Hiroki Nakahara)

Unlocking Latent Performance

Ephrem Wu
Xilinx

10:10 - 10:40 **Coffee Break**

10:40 - 12:20 **Session 1 : Architecture & system I** (Chair: Kentaro Sano)

An FPGA NIC Based Hardware Caching for Blockchain

Yuma Sakakibara, Kohei Nakamura and Hiroki Matsutani.

High Speed Performance Estimation of Embedded Hardcore Processors in FPGA-based SoCs

Deshya Wijesundera, Achintha Ihalage, Alok Prakash and Thambipillai Srikanthan

A Time-Division Multiplexing Ising Machine on FPGAs

Kasho Yamamoto, Huang Weiqiang, Shinya Takamaeda-Yamazaki, Masayuki Ikebe, Tetsuya Asai and Masato Motomura

An Adaptive Demotion Policy for High-Associativity Caches

Jubee Tada, Masayuki Sato and Ryusuke Egawa.

12:20 - 14:00 **Lunch**

14:00 - 16:05 **Session 2 : Design methodology & tools I** (Chair: Diana Göhringer)

Towards Flexible Automatic Generation of Graph Processing Gateware

Nina Engelhardt and Hayden Kwok-Hay So

Dataflow based Near Data Computing Achieves Excellent Energy Efficiency

Charles Shelor and Dr. Krishna Kavi Kavi

DTP: Enabling Exhaustive Exploration of FPGA Temporal Partitions for Streaming HPC Applications

Mostafa Koraei, Magnus Jahre and S.Omid Fatemi

Hardware Acceleration with Multi-Threading of Java-Based High Level Synthesis Tool

Hironori Nakajo, Yuto Ishikawa, Keisuke Koike and Keitaro Yanai

Application Performance using Tightly Coupled Accelerators

Takahiro Kaneda, Ryotaro Sakai, Naoki Nishikawa, Chiharu Tsuruta, Toshihiro Hanawa and Hideharu Amano

16:05 - 17:00 **Poster Session I** (Chair: Shinya Takamaeda-Yamazaki)

A Case for Remote GPUs over 10GbE Network for VR Applications

Shin Morishima, Masahiro Okazaki and Hiroki Matsutani

Acceleration of the aggregation process in a Hall-thruster simulation using Altera SDK for OpenCL

Hiroyuki Noda, Ryotaro Sakai, Takaaki Miyajima, Naoyuki Fujita and Hideharu Amano

FPGA Accelerated NoC-Simulation – A Case Study on the Intel Xeon Phi Ringbus Topology

Oliver Jakob Arndt, Christian Spindeldreier, Kevin Wohnrade, Daniel Pfefferkorn, Martin Neuenhahn and Holger Blume

Performance Evaluation of a CPU-FPGA Hybrid Cluster Platform Prototype

Yasunori Osana and Yohei Sakamoto

High-level Synthesis based on Parallel Design Patterns using a Functional Language

Morihiro Kuga, Kansuke Fukuda, Motoki Amagasaki, Masahiro Iida and Toshinori Sueyoshi

DAY-2 : June 8

9:00 - 9:10 **Opening**

9:00 - 10:00 **Invited Keynote Lecture 2** (Chair: Holger Blume)

New developments in point-of-care ultrasound functional imaging

Peter Brands
Esaote, NL

10:00 - 10:30	**Coffee Break**
10:30 - 12:10	**Session 3 : Application I** (Chair: Michael Hubner)

Accelerated Embedded AKAZE Feature Detection Algorithm on FPGA

Lester Kalms, Khaled Mohamed and Diana Göhringer

Reducing the cost of artefact free Fourier transforms

Donald Bailey, Faisal Mahmood and Ulf Skoglund

A porting and optimization of search for neighbour-particle in MPS method for GPU by using OpenACC

Takaaki Miyajima, Kenichi Kubota and Naoyuki Fujita

Acceleration of Publish/Subscribe Messaging in ROS-compliant FPGA Component

Yuhei Sugata, Takeshi Ohkawa, Kanemitsu Ootsu and Takashi Yokota

12:20 - 14:00	**Lunch**
14:0 - 16:00	**Poster Session II** (Chair: Yuichiro Shibata)

High-Performance Hardware Accelerators for Solving Ordinary Differential Equations

Ioannis Stamoulias, Matthias Moller, Rene Miedema, Christos Strydis, Christoforos Kachris and Dimitrios Soudris.

Access Network Generation for Efficient Debugging of FPGAs

Habib Ul Hasan Khan, Tomas Grimm, Michael Hubner and Diana Göhringer

Probabilistic Strategies Based on Staged LSH for Speedup of Audio Fingerprint Searching with Ten Million Scale Database

Masahiro Fukuda and Yasushi Inoguchi

RANSAC Acceleration on FPGA Multi-Processor with Overlay extension

Danielle Tchuinkou Kwadjo, Joel Mandebi Mbongue and Christophe Bobda

HLS Compilation for CPU Interlays

Jose Raul Garcia Ordaz and Dirk Koch

17:00	**Bus departure for evening event**
19:00 - 21:00	**Banquet**

DAY-3 : June 9

8:40 - 9:00	**Registration**
9:00 - 10:00	**Invited Keynote Lecture 3** (Chair: Martin Herbordt)

FPGA Acceleration in the Era of High Level Design

John Freeman
Intel, CA

10:00 - 10:30	**Coffee Break**
10:30 - 12:35	**Session 4 : Architecture & Applications** (Chair: Hideharu Amano)

FPGA Implementation of a Graph Cut Algorithm for Stereo Vision

Ryo Kamasaka, Yuichiro Shibata and Kiyoshi Oguri

HW/SW Co-design of an IEEE 802.11a/g Receiver on Xilinx Zynq SoC using High-Level Synthesis

Sajjad Nouri, Jens Rettkowski, Diana Göhringer and Jari Nurmi

FPGA-based Stream Computing for High-Performance N-Body Simulation using Floating-Point DSP Blocks

Kentaro Sano, Shin Abiko and Tomohiro Ueno

Neural Network Training Acceleration with PSO Algorithm on a GPU Using OpenCL

Jiajun Li and Qiang Liu

FPGA based ASIC Emulator with High Speed Optical Serial Link

Motoki Amagasaki, Futoshi Murase, Morihiro Kuga, Masahiro Iida and Toshinori Sueyoshi

Closing of the Conference

12:35 - 14:00	**Lunch**