HeteroSim: A Heterogeneous CPU-FPGA Simulator

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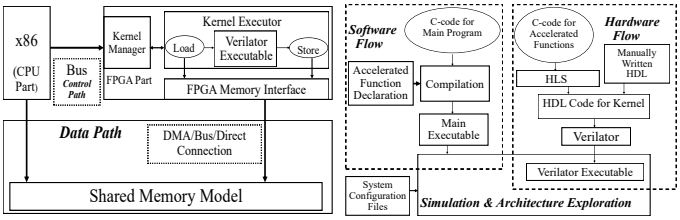
***Abstract*—Heterogeneous computing is rapidly gaining increased attention due to the promise it holds in overcoming power and performance walls in traditional computing systems. With its focus on customized processing nodes dedicated to the different tasks in an application, it is hoped that these walls will be overcome. Therefore, CPU-FPGA co-architectures are also gaining ground in application areas like recognition, mining, search, datacenter etc. However, research in CPU-FPGA co-architecture is constrained by the available synthesis and simulation tools which do not provide an integrated system level simulation and architectural exploration environment. This becomes critical when we incorporate novel memory hierarchies, multi-processor chip architectures, hardware level cache coherence etc. In this paper, we describe our open source and integrated system level simulator and architecture exploration tool called *HeteroSim*. It supports x86 based multi-core processor combined with a FPGA via bus-based architecture. It allows integrated system level simulation and returns performance metrics to understand application performance with respect to the simulated architectural configuration.**

I. Introduction

In heterogeneous computing widely different architectures like processors, graphics processing units (GPUs), digital signal processors (DSPs), Field Programmable Gate Arrays (FPGAs) are combined as a coupled system to address the requirements of different tasks in application in a power and performance efficient manner. Architecture simulators play a crucial role in evaluating these new designs. Examples of such simulators include gem-5-GPU [2] for CPU-GPU architecture simulation and performance modeling. An open-source system level simulator and architecture exploration tool for heterogeneous CPU-FPGA designs is an interesting and challenging area especially with the increased focus on CPU-FPGA co-architectures as demonstrated by works Intel's HARP[1] platform which combined server class Xeon multi-processor with an Altera FPGA.

Our proposed integrated system level simulator and architecture exploration tool *HeteroSim* allows cycle accurate simulation and generates various performance metrics for an application partitioned for execution on FPGA and CPU in a CPU-FPGA system. Additionally, users can configure parameters like number of processor cores, different kinds of acceleration kernels on FPGA and others to perform rapid architecture exploration using the in-built compilation and synthesis support. *HeteroSim* provides the following major features: (1) flexible memory sub-system hierarchy, (2) detailed hardware level cache coherence model for cache coherent



(a) HeteroSim Simulator Architecture (b) HeteroSim Flow

Fig. 1. HeteroSim Simulation and Architecture Exploration

communication between CPU and FPGA, (3) smart FPGA kernel management for invocation of different acceleration kernels by an application, (4) support for direct memory access (DMA) based data transfer and (5) different kinds of interface connections between the CPU and the FPGA.

II. HeteroSim Architecture

HeteroSim is built by heavily modifying *Multi2Sim* which is a heterogeneous simulator for CPU-GPU designs and combining it with open source Verilog simulator *Verilator*.

The architecture of the simulator part is shown in Fig. 1(a) while Fig. 1(b) shows the *HeteroSim* flow including the in-built compilation flow to enable application performance modeling and architecture exploration beginning from C or C++ code of an application. It is freely available at http://www.ece.ust.hk/~eeweiz/projects.html.

III. Experiments and Results

Results from a subset of the performed experiments on a number of benchmarks to evaluate *HeteroSim* by exploring different levels of cache access (L1, L2) granted to FPGA, direct memory access (Mem) and software only execution (SW) are shown in Fig. 2.

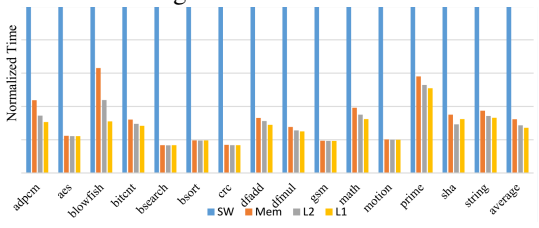


Fig. 2. Normalized Execution Time under Different Modes

References

[1] S. Anthony. (2014). *Intel unveils new xeon chip with integrated fpga, touts 20x performance boost* [Online]. Available: http://www.extremetech.com

[2] J. Power *et al.*, "gem5-gpu: A heterogeneous cpu-gpu simulator," in *Computer Architecture Letters*, 2015, vol. 14(1), pp. 34-36.