

# 【OS】 Day28(2)

▼ Class	Operating System: Three Easy Pieces
📅 Date	@January 27, 2022

## 【Ch22】 Beyond Physical Memory: Policies Homework

### Question 1

1. Generate random addresses with the following arguments: `-s 0 -n 10`, `-s 1 -n 10`, and `-s 2 -n 10`. Change the policy from FIFO, to LRU, to OPT. Compute whether each access in said address traces are hits or misses.

```
-s 0 -n 10 -p FIFO
```

Assuming a replacement policy of FIFO, and a cache of size 3 pages, figure out whether each of the following page references hit or miss in the page cache.

```
Access: 8 Hit/Miss? State of Memory?
Access: 7 Hit/Miss? State of Memory?
Access: 4 Hit/Miss? State of Memory?
Access: 2 Hit/Miss? State of Memory?
Access: 5 Hit/Miss? State of Memory?
Access: 4 Hit/Miss? State of Memory?
Access: 7 Hit/Miss? State of Memory?
Access: 3 Hit/Miss? State of Memory?
Access: 4 Hit/Miss? State of Memory?
Access: 5 Hit/Miss? State of Memory?
```

Access	Hit/Miss?	Evict	Resulting Cache Size
8	M		8
7	M		8, 7
4	M		8, 7, 4
2	M	8	7, 4, 2
5	M	7	4, 2, 5

4	H		4, 2, 5
7	M	4	2, 5, 7
3	M	2	5, 7, 3
4	M	5	7, 3, 4
5	M	7	3, 4, 5

Hit: 1 Hitrate: 10.00

```
-s 0 -n 10 -p LRU
```

Access	Hit/Miss?	Evict	Resulting Cache Size
8	M		8
7	M		8, 7
4	M		8, 7, 4
2	M	8	7, 4, 2
5	M	7	4, 2, 5
4	H		2, 5, 4
7	M	2	5, 4, 7
3	M	5	4, 7, 3
4	H		7, 3, 4
5	M	7	3, 4, 5

Hit: 2 Hitrate: 20.00

```
-s 0 -n 10 -p LRU
```

Access	Hit/Miss?	Evict	Resulting Cache Size
8	M		8
7	M		8, 7
4	M		8, 7, 4
2	M	4	8, 7, 2
5	M	2	8, 7, 5

4	M	5	8, 7, 4
7	H		8, 4, 7
3	M	7	8, 4, 3
4	M	3	8, 3, 4
5	M	4	8, 3, 5

Hit: 2 Hitrate: 20.00

## Question 2

- For a cache of size 5, generate worst-case address reference streams for each of the following policies: FIFO, LRU, and MRU (worst-case reference streams cause the most misses possible). For the worst case reference streams, how much bigger of a cache is needed to improve performance dramatically and approach OPT?

FIFO: -a 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5 //need size 6

```
Access: 0 MISS FirstIn -> [0] <- Lastin Replaced:- [Hits:0 Misses:1]
Access: 1 MISS FirstIn -> [0, 1] <- Lastin Replaced:- [Hits:0 Misses:2]
Access: 2 MISS FirstIn -> [0, 1, 2] <- Lastin Replaced:- [Hits:0 Misses:3]
Access: 3 MISS FirstIn -> [0, 1, 2, 3] <- Lastin Replaced:- [Hits:0 Misses:4]
Access: 4 MISS FirstIn -> [0, 1, 2, 3, 4] <- Lastin Replaced:- [Hits:0 Misses:5]
Access: 5 MISS FirstIn -> [1, 2, 3, 4, 5] <- Lastin Replaced:0 [Hits:0 Misses:6]
Access: 0 MISS FirstIn -> [2, 3, 4, 5, 0] <- Lastin Replaced:1 [Hits:0 Misses:7]
Access: 1 MISS FirstIn -> [3, 4, 5, 0, 1] <- Lastin Replaced:2 [Hits:0 Misses:8]
Access: 2 MISS FirstIn -> [4, 5, 0, 1, 2] <- Lastin Replaced:3 [Hits:0 Misses:9]
Access: 3 MISS FirstIn -> [5, 0, 1, 2, 3] <- Lastin Replaced:4 [Hits:0 Misses:10]
Access: 4 MISS FirstIn -> [0, 1, 2, 3, 4] <- Lastin Replaced:5 [Hits:0 Misses:11]
Access: 5 MISS FirstIn -> [1, 2, 3, 4, 5] <- Lastin Replaced:0 [Hits:0 Misses:12]

FINALSTATS hits 0 misses 12 hitrate 0.00
```

LRU: -a 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5 //need size 6

```

Access: 0 MISS LRU ->      [0] <- MRU Replaced:- [Hits:0 Misses:1]
Access: 1 MISS LRU ->      [0, 1] <- MRU Replaced:- [Hits:0 Misses:2]
Access: 2 MISS LRU ->      [0, 1, 2] <- MRU Replaced:- [Hits:0 Misses:3]
Access: 3 MISS LRU -> [0, 1, 2, 3] <- MRU Replaced:- [Hits:0 Misses:4]
Access: 4 MISS LRU -> [0, 1, 2, 3, 4] <- MRU Replaced:- [Hits:0 Misses:5]
Access: 5 MISS LRU -> [1, 2, 3, 4, 5] <- MRU Replaced:0 [Hits:0 Misses:6]
Access: 0 MISS LRU -> [2, 3, 4, 5, 0] <- MRU Replaced:1 [Hits:0 Misses:7]
Access: 1 MISS LRU -> [3, 4, 5, 0, 1] <- MRU Replaced:2 [Hits:0 Misses:8]
Access: 2 MISS LRU -> [4, 5, 0, 1, 2] <- MRU Replaced:3 [Hits:0 Misses:9]
Access: 3 MISS LRU -> [5, 0, 1, 2, 3] <- MRU Replaced:4 [Hits:0 Misses:10]
Access: 4 MISS LRU -> [0, 1, 2, 3, 4] <- MRU Replaced:5 [Hits:0 Misses:11]
Access: 5 MISS LRU -> [1, 2, 3, 4, 5] <- MRU Replaced:0 [Hits:0 Misses:12]

FINALSTATS hits 0   misses 12   hitrate 0.00

```

MRU: -a 0, 1, 2, 3, 4, 5, 4, 5, 4, 5

```

Access: 0 MISS LRU ->      [0] <- MRU Replaced:- [Hits:0 Misses:1]
Access: 1 MISS LRU ->      [0, 1] <- MRU Replaced:- [Hits:0 Misses:2]
Access: 2 MISS LRU ->      [0, 1, 2] <- MRU Replaced:- [Hits:0 Misses:3]
Access: 3 MISS LRU -> [0, 1, 2, 3] <- MRU Replaced:- [Hits:0 Misses:4]
Access: 4 MISS LRU -> [0, 1, 2, 3, 4] <- MRU Replaced:- [Hits:0 Misses:5]
Access: 5 MISS LRU -> [0, 1, 2, 3, 5] <- MRU Replaced:4 [Hits:0 Misses:6]
Access: 4 MISS LRU -> [0, 1, 2, 3, 4] <- MRU Replaced:5 [Hits:0 Misses:7]
Access: 5 MISS LRU -> [0, 1, 2, 3, 5] <- MRU Replaced:4 [Hits:0 Misses:8]
Access: 4 MISS LRU -> [0, 1, 2, 3, 4] <- MRU Replaced:5 [Hits:0 Misses:9]
Access: 5 MISS LRU -> [0, 1, 2, 3, 5] <- MRU Replaced:4 [Hits:0 Misses:10]

FINALSTATS hits 0   misses 10   hitrate 0.00

```