【OS】Day25

Class	Operating System: Three Easy Pieces
Date	@January 24, 2022

【Ch20】Paging: Smaller Tables

Question 1

1. With a linear page table, you need a single register to locate the page table, assuming that hardware does the lookup upon a TLB miss. How many registers do you need to locate a two-level page table? A three-level table?

A two-level page table needs two registers.

A three-level table needs three registers.

Question 2

2. Use the simulator to perform translations given random seeds 0, 1, and 2, and check your answers using the `-c` flag. How many memory references are needed to perform each lookup?

Page Directory Number: 5 digits(holding 32 pages directory entries)

Page Table Entry Number: 5 digits(holding 32 pages entry)

Offset: 5 digits

Virtual Address: 611c(11000 01000 11100)

The page directory base register is 108, thus to find the directory entry, we find 108[24] = a1.

0xa1= 1(valid) 0100001(Decimal 33)

Then, we find 33[8] = 0xb5.

0xb5 = 1(valid) 0110101(Decimal 53)

The physical address is 53[28] = 08

Virtual Address: 3DAB = 01111 01101 01000

PDE: 15 = 108[15] = d6

d6 = 1(valid) 1010110(86)

PTE: 13 = 86[13] = 7f

7f = 0(invalid) 111111

Question 3

3. Given your understanding of how cache memory works, how do you think memory references to the page table will behave in the cache? Will they lead to lots of cache hits (and thus fast accesses?) Or lots of misses (and thus slow accesses)?

The page table references doesn’t have good temporal and spatial locality and thus will cause lots of misses and thus slow accesses.