【CA】Day6

Course	Nand to Tetris
Study Date	@February 8, 2022

【Ch2】Boolean Arithmetic

2.3 Implementations

Half-Adder

The function `sum(a, b)` and `carry(a, b)` happen to be identical to the standard `Xor(a, b)` and `And(a, b)` Boolean functions. Thus, the implementation of this adder is straightforward using previously built gates.

Full-Adder

A full adder chip can be implemented from two half adder chips and one additional simple gate.

Adder

The addition of two signed numbers represented by the 2's complement method as two n-bit buses can be done bit-wise, from right to left, in n steps.

In step 0, the least significant pair of bits is added, and the carry bit is fed into the addition of the next significant pair bits.

The process continues until in step n-1 the most significant pair of bits is added. Note that each step involves the addition of three bits. Hence, an n-bit adder can be implemented by creating an array of n full-adder chips and propagating the carry bits up the significance ladder.

Incrementer

An n-bit incrementer can be implemented trivially from an n-bit adder.

Our ALU is carefully planned to effect all the desired ALU operations logically, using simple Boolean operations. Therefore, the physical implementation of the ALU is reduced to implementing these simple Boolean operations.