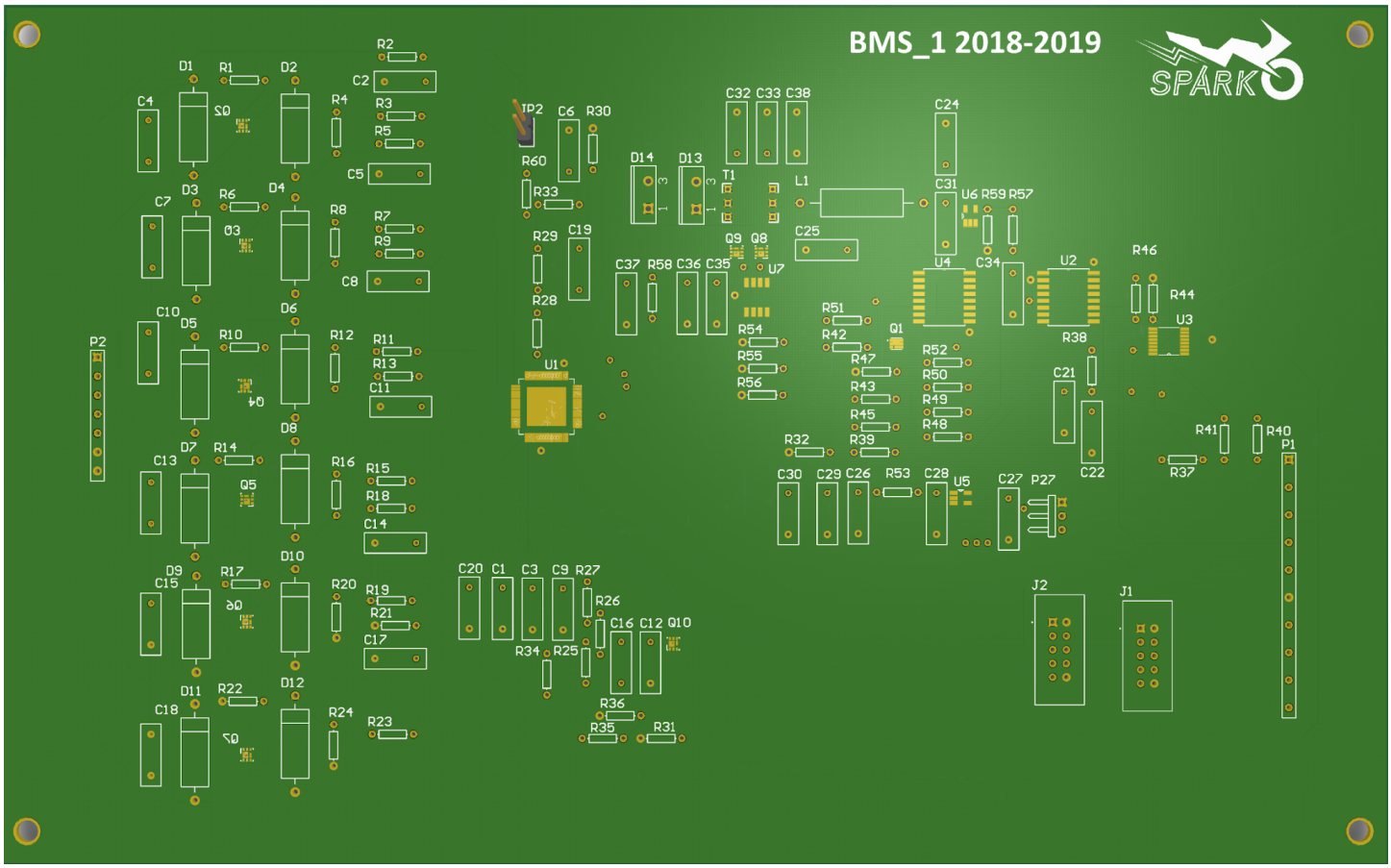
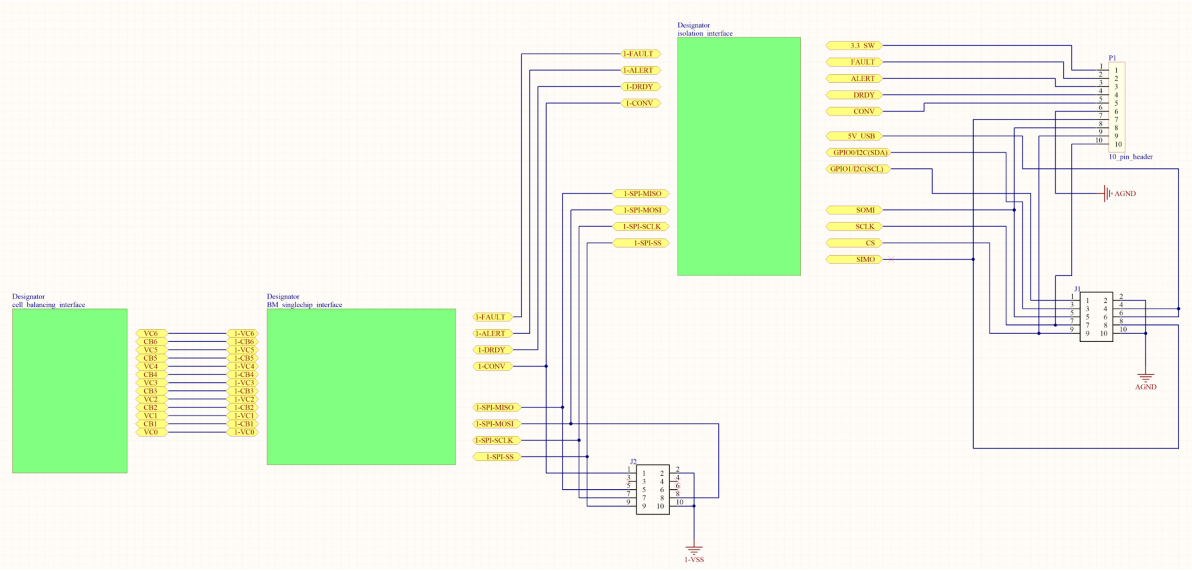
Battery Management System V1



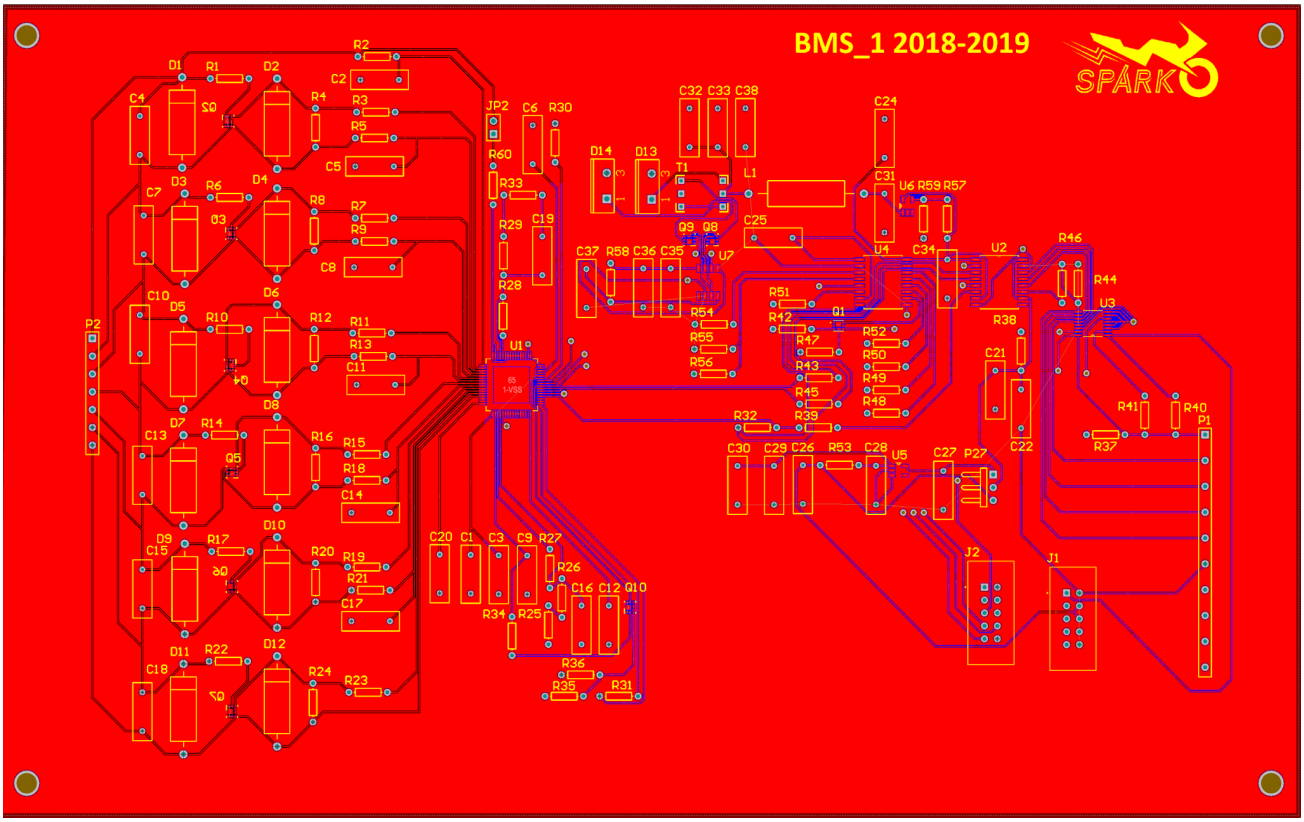
3D CAD Render of the Finished Battery Management Cell Protector

During the spring 2019 school semester, I worked with my student project design team (SPARK) to design a custom battery management pcb for the electric motorcycle. This prototype battery management system features passive balancing, works with up to six cells, and uses SPI communications written in C for fast communications. Because our team plans on building custom lithium ion cell packs for the bike next season, we felt it was necessary to also design a battery management system to maintain these cells. One of the primary objectives in designing this pcb was to ensure that it was modular. By designing it in this way, we would be able to daisy chain several bms pcbs together to accurately monitor each of the cell packs on the bike. Another consideration that factored into the design, was the battery management chip we chose. We chose to use a TI BQ76PL536A chip because it is well documented and supports cell stacks of up to 192 cells at once. Further details about the rest of the PCB and Schematic Design Process can found below.



Top Level Schematic Document with Abstracted Cell Balancing, Battery Management Chip, and Communications

This was the first relatively complex pcb I had worked on, which gave me the opportunity to expand my knowledge of Altium, the pcb design software I used. Working with my team, we split up the pcb design into four distinct submodules: the cell balancing interface, battery management chip interface, and isolation interface. The cell balancing interface primarily plugs in directly to the battery cells and handles analog digital converters to the bms chip. One aspect of the design uses zener diodes to provide overvoltage protection for ADC inputs and a path for inrush currents during hot plug-in. The battery management chip module and isolation interface handle the spi communications with other devices and monitors cell voltages for under and over voltage. The isolation interface also includes a 10 pin header that will be connected to a separate microcontroller and power supply.



Top Layer View of Signal Traces, with Internal, Ground, and Bottom Trace Layers below

After connecting all of the nets on the schematics, I systematically laid out each submodule's nets before integrating them together on the pcb. The most difficult aspect of the layout came from the isolation interface. I needed to cut down the length of the signal traces to reduce noise in the system. Because I needed to group the components more tightly, I opted to use the top and bottom layers for signal routing to reduce route lengths. Additionally, I decided to create internal power and ground planes for the respective through hole and surface mount components to reduce the layout complexity. We plan on programming and testing this board over the course of the summer and fall semesters to further iterate on this base design, with the intent of integrating an on board microcontroller to the pcb and potentially three additional battery management chips to monitor up to 18 battery cells with one pcb.